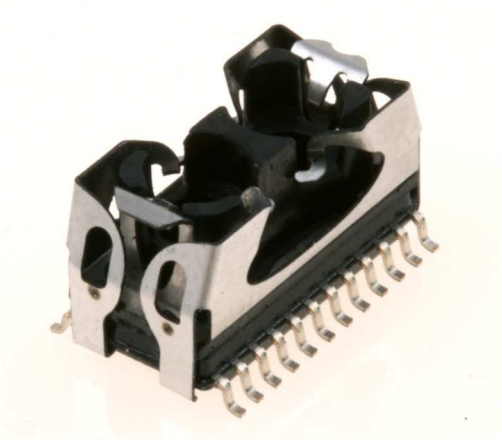
MLX75605

150Mbps Transmitter and Receiver for POF fiber

Features and Benefits

- Suitable for 1mm automotive PMMA Plastic Optical Fiber (POF).
- Includes 650nm LED and a PIN photodiode.
- Optical package combines transmitter and receiver, allows qualification according to AEC-Q100.
- Product is qualified according to Automotive Application Recommendation for optical MOST® interfaces
- Ambient operating Temperature Range [-40°C to 95°C]
- Data Communication rate up to 75 Mbps (biphase) and 150 Mbps (non return to zero).
- Robust to electromagnetic radiative disturbances due to full integration of the photodetector within the receiver IC
- Emitted Optical output power 50% cut mode.
- Compliant with Laser Class 1 Product standard
- LVDS Input and output compliant with:
  - 1596.3 SCI-LVDS Standard, IEEE Std
  - TIA/EIA-644, National Semiconductor Corp., ANSI/TIA/EIA, 2001



Ordering Information

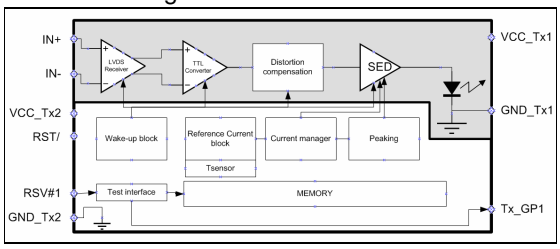
Part No.	Temperature Code	Package Code	Option code	Packing form
MLX75605	P (-40°C to 95°C)	XV (SOIC24 for MOST)	AAA-000	TU (tube)
MLX75605	P (-40°C to 95°C)	XV (SOIC24 for MOST)	AAA-000	RE (reel)

Example: MLX75605PXV-AAA-000-RE

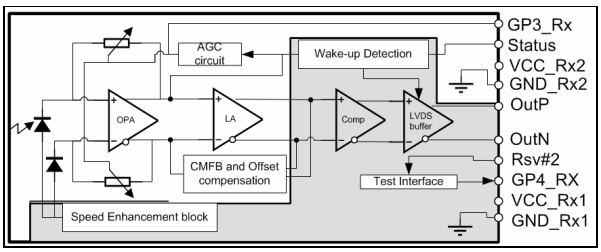
Application Examples

Automotive infotainment networks: e.g. rear seat entertainment, navigation system, car radio…
Vision enhancement systems.
Audio/Video Data transmission.
Multimedia / telematic systems.
…

Functional Diagram



150 Mbps Transmitter



150 Mbps Receiver

General Description

The MLX75605 fiber optic transceiver (FOT) is a surface mountable device (SMD). This single package solution (with 24 pin SOIC footprint) contains a photo transmitter IC and a photo receiver IC developed for communication on PMMA Plastic Fiber (POF) at a speed up to 75 Mbps (bi-phase) or 150 Mbps (non return to zero).

The optical transmitter houses a LED driver and a 650 nm light source die. The light source drive current is optimized so that a maximum extinction ratio between the 1 and 0 light levels is obtained. The light source modulation current is fully programmable in absolute value over the full temperature range. This feature allows trimming of the optical emitted power within a narrow range at any temperature, hence giving rise to an enhanced optical budget. In addition the trimming capability over temperature allows full compensation of the temperature dependence of the Light Source optical efficiency.
Driver circuitry embeds full data signal monitoring and control, allowing increase of the robustness at the application level:
- An input frequency monitoring allows input signal check. Only a signal within MOST frequency domain can activate the optical signal.
- A dedicated pin (/RST) controls direct activation or disabling of the optical signal.
This prohibits unwanted light emission during startup or hard shutdown of the transmitter part.

The optical receiver is implemented as one monolithic Integrated Circuit and consists of a PIN photo detector with a trans-impedance amplifier (TIA), a limiting amplifier and finally an LVDS buffer output stage. This receiver circuit operates at 150 Mbps speed and automatically controls its gain over a wide range of optical power.
As for the transmitter, the optical receiver embeds a full wake-up procedure. When the optical input signal is outside the frequency range specified or when the received average optical power is below the specified threshold, the circuit puts itself into sleep mode. As soon as any optical power is detected, the sleep mode controller enters into an input frequency check mode. In this mode, as soon as a valid average optical power and valid input frequency are detected, the receiver resumes full power operation.
The circuit flags its sleeping mode activation via the STATUS pin, which is set at HIGH state. During valid operation, STATUS pin is set at LOW state.
The wake-up procedure guarantees robustness against unwanted wakeup. When fully woken-up, a high quality communication line is obtained.

Table of Content

Glossary of Terms

MOST	Media Oriented Systems Transport
EOC	Electrical to Optical Converter
LVDS	Low Voltage Differential Signal
dBm	Decibel referred to 1 milli-watt
A_{PWD}	Average Pulse Width Distortion
P_{av}	Average Optical Power
ESD	Electro Static Discharge
RoHs	Restriction Of the use of certain Hazardous Substances

Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	100	ºC
Junction Temperature	T_J	-40	105	ºC
Power Dissipation	P_{TOT}	-	380	mW
Power Supply Voltage	VCC_{Max}	-0.5	7	V
ESD Level (Human Body Model)	ESD	2		kV

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Supply Voltage	VCC	3.135	3.3	3.465	V
Operating Ambient Temperature Range	T_{AMB}	-40	-	95	ºC

Recommended Networks Conditions

Parameter	Symbol	Min	Typ	Max	Units
Maximum bit rate (Not Return Zero)	BR	135.4	-	147.52	Mbps
Unit Interval	UI	3.391	-	3.691	ns
Minimum bit length	B_{length}	2	-	-	UI
DC Adaptive coding period	t_{DCA}	4	-	10	UI
Digital Sum Value	DSV	-5	-	5	UI

Transmitter part DC Characteristics

DC Operating Parameters T_A = -40°C to 95 °C, V_{cc} =3.135V to 3.465V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Differential input voltage	V_{IND}		100	-	636	mV
Input Current	I_{IN}		-	-	20	µA
Input voltage range	V_{CM}		0	-	2.4	V
Supply current (electrical power on mode)	I_{DDO}		-	30	50	mA
Supply Current (electrical power down mode)	I_{DDS}	@3.3V and 25 °C.	-	-	1	mA
/RST pin Threshold	V_{Th3dB}	LVTTL compliant	0.4	-	2.5	V
M3dB pin impedance	Z_{Ctrl}		0.5		2	MΩ

Transmitter part AC Characteristics

AC Operating Parameters T_A = -40°C to 95°C, V_{cc} =3.135V to 3.465V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Optical Power Up Delay	Ton2		-	-	100	µs
Optical Power Down Delay	Toff2		-	-	2	µs
Bit rate	BR	Without return to zero	10	-	150	Mbps
Unit Interval	UI	For MOST fastest sampling frequency=48Khz	3.39	-	3.391	ns
Rise Time	Tr	Measured between 20%-80% of signal	-	-	0.5	UI
Fall Time	Tf	Measured between 20%-80% of signal	-	-	0.5	UI
Pulse-width-variation	tpwv	Measured at 50% of signal amplitude And SP1 PWV within 0.925UI~1.075UI	0.7	-	1.3	UI
Transferred Jitter	Jtr_2	After jitter filter (Low pass, f_{3dB}=200Khz, Att=-20dB/dec), with 50ps RMS input jitter	-	-	100	ps RMS
Positive overshoot	Over_p1 Over_p2	Within 0 ~ 1.37UI Within 1.37 ~ 2UI	-20 -15	-	40 15	% %
Negative Overshoot	Over_n		-20	-	20	%

Transmitter part Optical Specifications

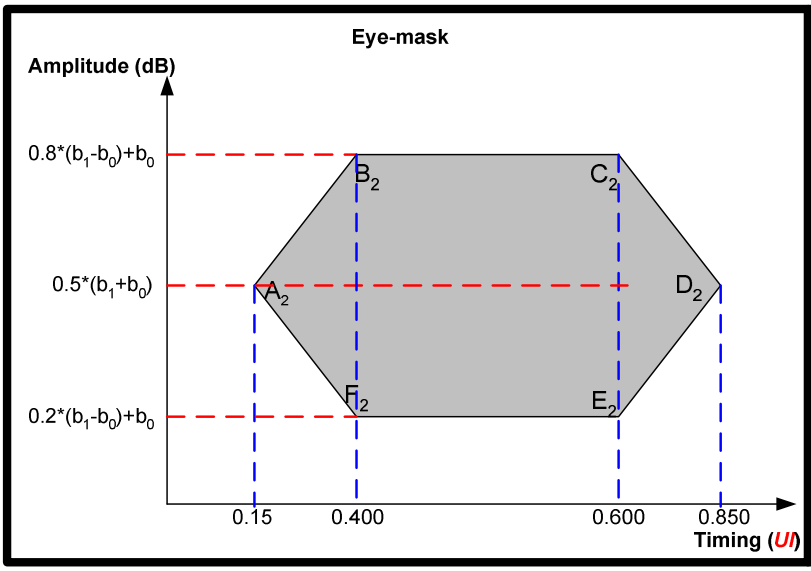
DC Operating Parameters T_A = -40°C to 95 °C, V_{cc} =3.135V to 3.465V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Center Wavelength	λ_{c2}		635	650	675	nm
Spectral Width (RMS)	$\sigma_{\lambda 2}$		-	-	17	nm
Average optical power emitted by the Transmitter component	P_{av}	1) Power within a far field angle of 30° (NA=0.5) 2) within a diameter of 1.0mm 3) at FOT level, assuming 1.5dB in a fiber pigtail	-6.5	-	-1.5	dBm

Extinction ratio	E_r	Measured with 5UI pulse width	10	-	-	dB
Target variation of the optical output power over temperature	ΔP_{temp}		-	-	3	dB
Optical output power “Light off”	P_{off}		-	-	-50	dBm
Misalignment between light source center and the center of the Ferrule coupling hole.	Δ_{xy}	.	0	-	35	µm
Distance between top of light source and Ferrule stopper top plate of package in the ferrule coupling hole	Δ_z		-	-	150	µm

Transmitter part Eye Characteristics

DC Operating Parameters T_A = -40°C to 95 °C, V_{dd} = 3.135V to 3.465V, made with MOST network worst case pattern (2UI minimum pulse width) generated at SP1, including pulse width variation (0.075UI~0.925UI) Eye mask should be generated using golden PLL transfer function, which consists into low pass filter from 10Hz to F3dB=125kHz and attenuation of -20dB/ decade.

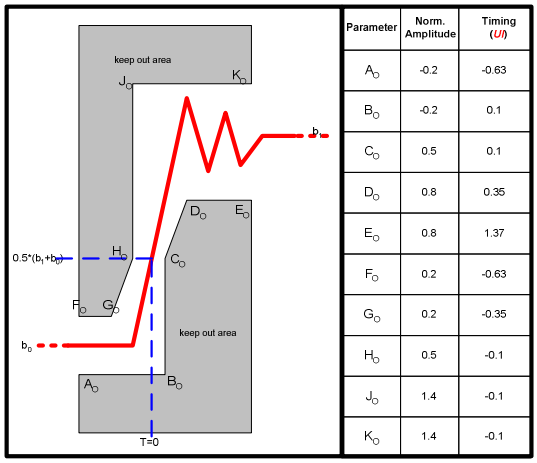


Parameter	Timing (*UI*)	Amplitude (dB)
A_2	0.150	$0.5*(b_1+b_0)$
B_2	0.400	$0.8*(b_1-b_0)+b_0$
C_2	0.600	$0.8*(b_1-b_0)+b_0$
D_2	0.850	$0.5*(b_1+b_0)$
E_2	0.600	$0.2*(b_1-b_0)+b_0$
F_2	0.400	$0.2*(b_1-b_0)+b_0$

b1 and b0 level refers to light power for a ‘1’ and respectively a ‘0’ Measured between 2.5UI and 4UI with input signal equal to 5UI or 6UI

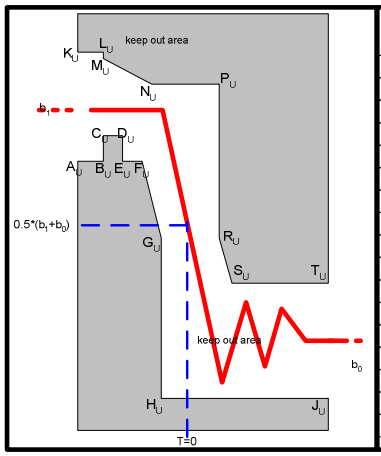
Transmitter pulse transition Characteristics

Operating Parameters T_A = -40°C to 95 °C, V_{dd} =3.135V to 3.465V, made with MOST network worst case pattern (2UI minimum pulse width).



Parameter	Norm. Amplitude	Timing (UI)
A_O	-0.2	-0.63
B_O	-0.2	0.1
C_O	0.5	0.1
D_O	0.8	0.35
E_O	0.8	1.37
F_O	0.2	-0.63
G_O	0.2	-0.35
H_O	0.5	-0.1
J_O	1.4	-0.1
K_O	1.4	-0.1

Rise time mask (measured with PW=2UI)



Parameter	Norm. Amplitude	Timing (UI)
A_U	0.8	-0.63
B_U	0.8	-0.53
C_U	0.85	-0.53
D_U	0.85	-0.43
E_U	0.8	-0.43
F_U	0.8	-0.35
G_U	0.5	-0.1
H_U	-0.2	-0.1
J_U	-0.2	1.37
K_U	1.4	-0.63
L_U	1.4	-0.53
M_U	1.34	-0.53
N_U	1.15	-0.22
P_U	0.5	0.1
R_U	0.2	0.1
S_U	0.2	0.35
T_U	0.2	1.37

Fall time mask (measured with PW=2UI)

Receiver part DC Characteristics

DC Operating Parameters T_A = -40°C to 95 °C, V_{cc} =3.135V to 3.465V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Differential Signal Output	V_{OL}	R_L=100Ω	247	-	454	mV
Offset Voltage	V_{OFF}	R_L=100Ω	1.125	-	1.375	V
Low Level Output Voltage for Status pin (JESD8C LVTTL)	V_{OSL}	I_{OL}=1.6 mA	-	-	0.4	V
High Level Output Voltage for Status pin (JESD8C LVTTL)	V_{OSH}	I_{OH}=1.6 mA	2.5	-	-	V
Supply current (Operating Mode)	I_{CCO}	Light on	-	22	30	mA
Supply Current (Sleeping Mode)	I_{CCS}	Light off With 100Ω output load	-	-	45	µA

Receiver part AC Characteristics

DC Operating Parameters T_A = -40°C to 95 °C, V_{cc} =3.135V to 3.465V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Supply Rejection Ratio	PSSR		-	30	-	dB
Output Rise Time	t_R	R_L=100Ω	-	-	1.01	ns
Output Fall Time	t_F	R_L=100Ω	-	-	1.01	ns

Transferred Jitter	Jtr_4	After jitter filter (Low pass, f_{3dB}=200Khz, Att=-20dB/dec), after 15m POF and 112ps RMS generated filter	-	-	200	ps RMS
Average Pulse width Distortion	A_{PWD}		-0.1	-	0.2	UI

Receiver part Optical Specifications

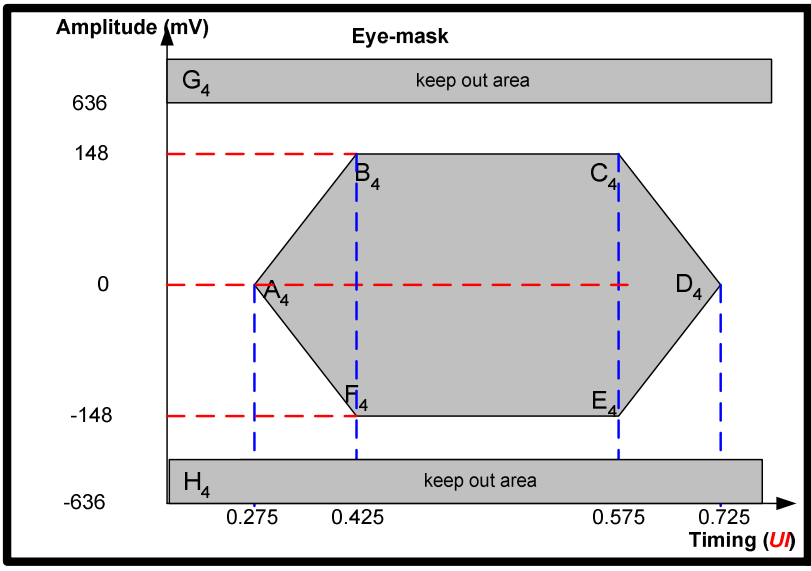
DC Operating Parameters T_A = -40°C to 95 °C, V_{CC} = 3.135V to 3.465V, Data rate = 150 Mbps (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Photosensitivity Spectral Range	λ		630	650	685	nm
Acceptable Extinction ratios of optical input signal	E_r		10	-	-	dB
Receivable average optical power for data recovery when in operational mode	S_{AVG}	According to Eye mask specification	-22*	-	-2	dBm
Maximum Polymer Optical Step Index fiber length	L_{pof}	Launch condition NA=0.5	-	-	15	m

*-22dBm is the optical power at SP3. 1.5dB additional loss from the optical pigtail can be tolerated, so the receiver is still fully functional with -22dBm-1.5dB=-23.5dBm optical power falling on the photodiode.

Receiver part Eye Characteristics

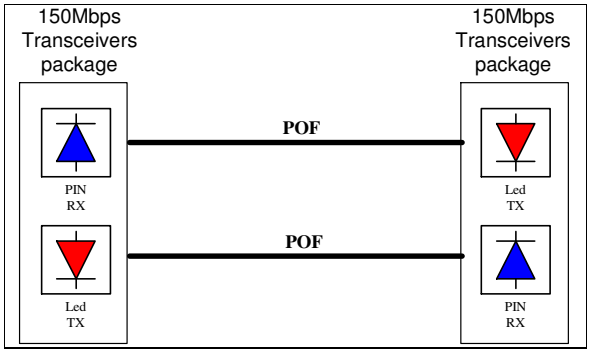
DC Operating Parameters T_A = -40°C to 95 °C, V_{cc} =3.135V to 3.465V, made with MOST network worst case pattern out of 1mm Step Index POF launched with NA=0.5, using golden PLL transfer function, which consists into low pass filter from 10Hz to F3dB=125kHz and attenuation of -20dB decade.



Parameter	Timing (UI)	Amplitude (mV)
A_4	0.275	0
B_4	0.425	148
C_4	0.575	148
D_4	0.725	0
E_4	0.575	-148
F_4	0.425	-148
G_4	-	636
H_4	-	-636

General Description

Optical part

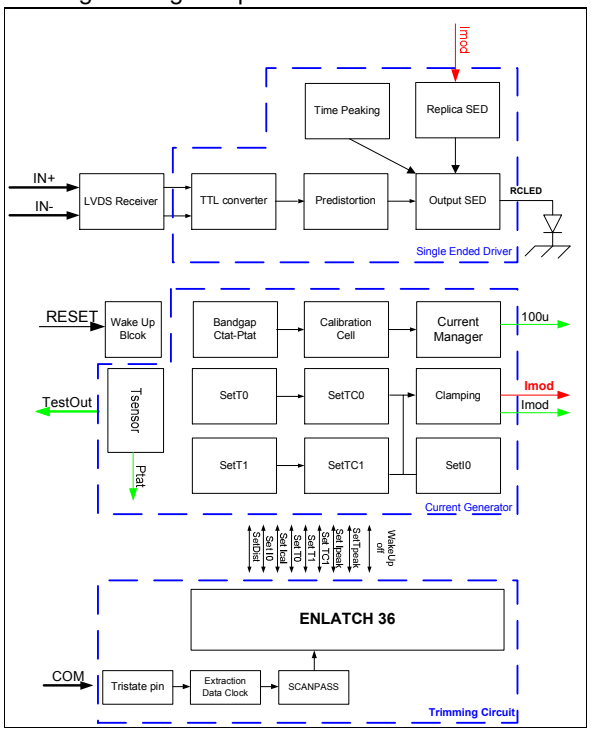


Optical specification is based on:

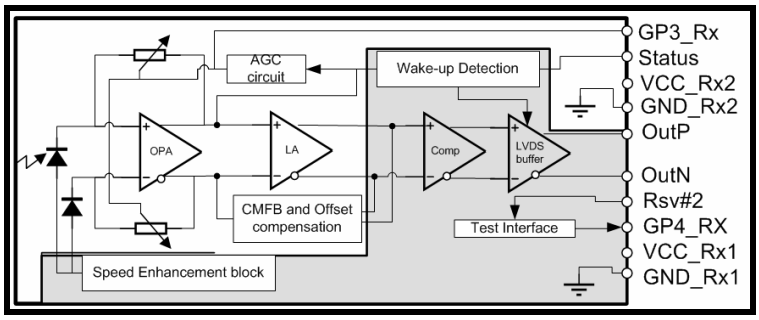
- Receiver: Silicon Embedded PIN photodiode type with 1.1mm^2 active area.
- Transmitter: 650 nm LED with 83µm aperture.

Block Diagram

Light source driver consists of three main blocks: Input buffer, Output driver, and Current source. The current source can be trimmed over process variations of LED and the LED driver IC and also compensates the variation of optical output of the light source with temperature. A 50% power control allows sending only half modulation current to the LED. The test register and memory blocks are used for Melexis to obtain high test coverage during component test and in order to be able to trim the component.



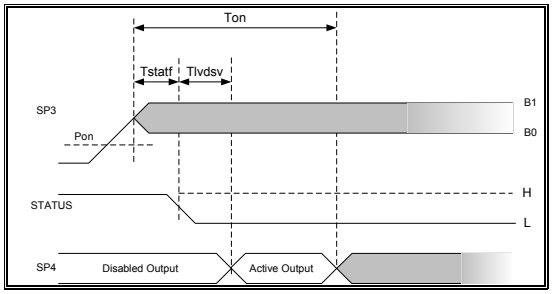
The receiver is based on front-end block (TIA) with a large illuminated photodiode and the second blind photodiode. Both photodiodes have the same shape and size. This front end is controlled by automatic gain control circuitry to gain same performance over light full range. A second stage is responsible for detecting light variations and is able to remove common mode and DC offset. Last stage is used as an output buffer. In addition a block is available to detect light for status pin and a second one is used for fault detection.
High test coverage is guaranteed by test modes which can be activated at die or package level based on dedicated patterns on Melexis production lines.

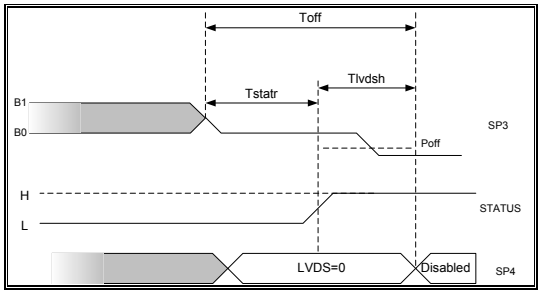


Power up and Power down Sequence

Receiver power up and power down

Receiver part is always powered in application. A dedicated “wakeup LAN function” allows the optical signal to initiate the wake up of the sleeping portions of the IC. Power up scenario consists of receiving light power above Pon threshold. Receiver then checks the signal frequency. As soon as the signal is within MOST frequency range, Status pin is put to low state and LVDS is released to transmit data.
As soon as frequency goes under valid frequency minimum value, chip puts Status pin to high and sets output to LVDS “0’ state. As soon as light is going under Poff threshold, the chip goes in sleep mode.
Receiver has no internal control of transmitter. The wake up and sleeping of the transmitter should be made externally.

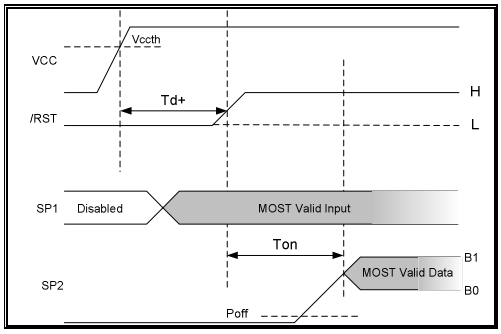


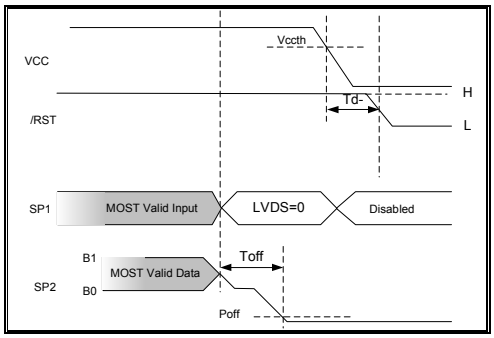


Parameter	Sym-bol	Test Condi-tions	Min	Typ	Max	Units
Delay between optical signal and Status pin falling edge	Tstatf		200	-	500	µs
Delay from status pin falling to activation of LVDS output	Tlvdsv				1	µs
Delay between valid optical signal and valid LVDS output	Ton		-	-	2	ms
Optical power for transition from Sleep to Operate Mode	Pon	average power	-27	-	-24	dBm

Parameter	Sym-bol	Test Condi-tions	Min	Typ	Max	Units
Delay between removal valid optical signal and Status pin rising edge	Tstatr		-	-	1	µs
Delay be-tween rising edge Status pin and disabling of LVDS output	Tlvdsh		2		4	µs
Delay be-tween remo-val valid opti-cal signal and disabling of LVDS output	Toff		3	-	5	µs
Optical power for transition from Operate to Sleep Mode	Poff	average power	-35	-	-24	dBm

Transmitter power up and power down



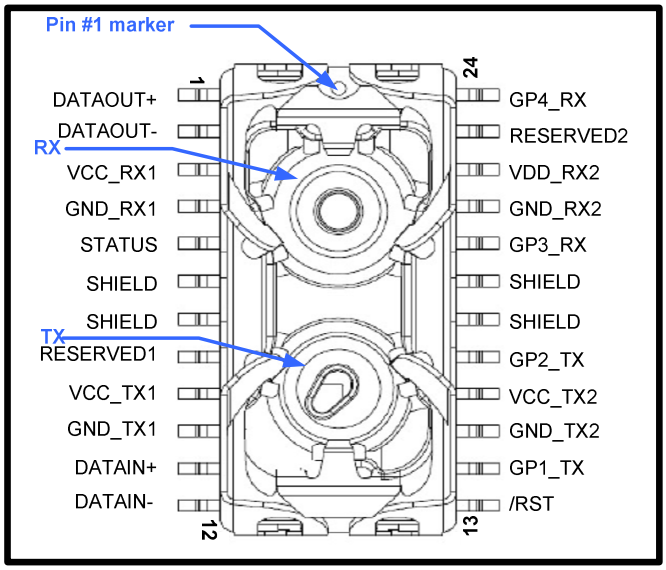


Parameter	Symb	Test Conditions	Min	Typ	Max	Units
Delay between supply rise and Reset line release	Td+		1	-	-	ms
Supply threshold for valid logic levels	Vccth		2.97	-	-	V
Power-On Delay from /Rst signal	Ton		-	-	100	µs
Optical power for transmitter Off-state	Poff	average power	-	-	-50	dBm

Parameter	Symb	Test Conditions	Min	Typ	Max	Units
Delay between supply fall and Reset pin falling edge	Td-		0	-	100	µs
Power-Off Delay	Toff		0	-	2	µs

Pin Definitions and Descriptions

All pins related to primary functions are placed on left side of the package, to allow more flexibility for PCB floor plan. All dedicated and options pins are placed on the right side of the package.
Pin 1 is located on the left side of the orientation dot as shown in diagram.



Pin Number	Pin name	Description
1	DataOUT Plus	LVDS Positive Output
2	DataOUT Minus	LVDS Negative Output
3	VCC_Rx1	Supply voltage for Receiver
4	GND_Rx1	Ground for Receiver
5	STATUS	This pin is only put on “LOW” when the following two conditions are met: modulated light is received **and** the received data rate is within the operation frequency range. The status pin is used in the application to switch on or off the power supply of the application, where the MOST transceiver is part of.
6	Shield	Shield pin connected to die pad of package
7	Shield	Shield pin connected to die pad of package
8	Reserved1	M3dB function. Should be Connected to GND through 0-Ω resistor if M3dB function isn’t used. Used for factory test purpose.
9	VCC_Tx1	Supply voltage for Transmitter
10	GND_Tx1	Ground for Transmitter
11	DataIN Plus	LVDS Negative Input
12	DataIN Minus	LVDS Positive Input
13	/RST	Optical Output power disabling. Active-low logic signal disables the optical output

14	Tx_GP1	Currently used for Test output pin. Should be left unconnected
15	GND_Tx2	Ground for Transmitter
16	VCC_TX2	Supply voltage for Transmitter
17	Tx_GP2	Unconnected pin
18	Shield	Shield pin connected to die pad of package
19	Shield	Shield pin connected to die pad of package
20	GP3_RX	Automatic Gain Control analog output and Factory test output Should be left unconnected
21	GND_Rx2	Ground for Receiver
22	VCC_Rx2	Supply voltage for Receiver
23	Reserved2	Connect to VCC_RX2 through 0-Ω resistor. Used for factory test purpose.
24	GP4_RX	Should be left unconnected.

Package Outline

Package solution gains advantage by fully encapsulating the receiver and transmitter die. The available 2 optical openings allow the light to enter and leave both die. Openings are designed with a conical shape to receive POF ferrule.

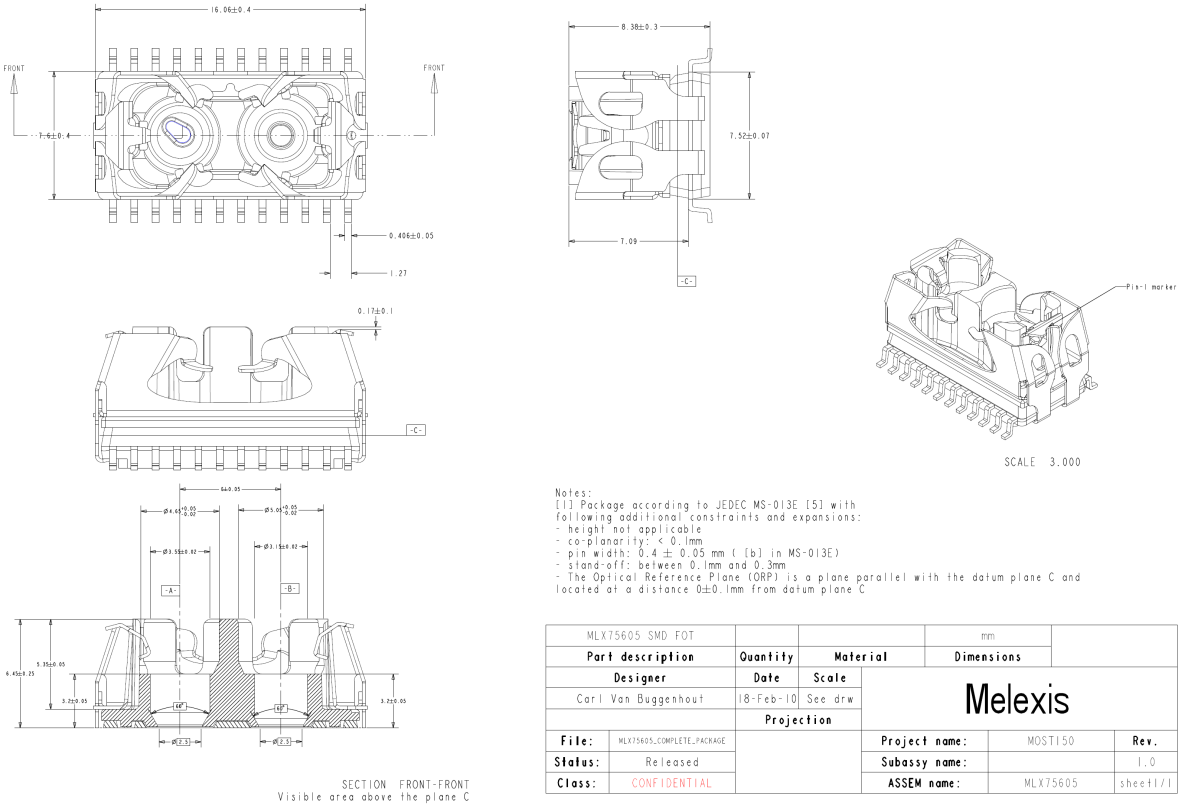
The top part is used as guiding structure, allowing improvement versus misalignment and tilt. An additional metal structure is placed on the top part to ensure ferrule clamping.
This ferrule clamping system allows blocking and maintaining ferrule against the bottom part by a spring effect. Moreover, it allows rework by easy removal of the ferrule out of the guiding structure.
The cavity depth is currently at 3.2 mm, allowing low fiber tilt and accurate alignment.
The hole diameters are different: one is 3.55mm for the transmitter side and the other is 3.15mm for receiver side with dedicated ferrule receptacle shape, allowing mistake proofing (Poka-Yoke). The cavity pitch is fixed at 6mm.

Package Parameters

Parameter	Comment	Min	Typ	Max	Units
Package length		15.7	16.1	16.5	mm
Package width		7.2	7.6	7.8	mm
Pin pitch		1.145	1.27	1.395	mm
Co-planarity		-	-	0.1	mm
Stand-off		0.1	0.2	0.3	mm
Total package height		-	-	12.7	mm
Pin width		0.356	0.406	0.456	mm

Ferrule cavity depth		3.15	3.2	3.25	mm
Receiver ferrule diameter hole		3.13	3.15	3.17	mm
Transmitter ferrule diameter hole		3.53	3.55	3.57	mm
Hole pitch		5.95	6.0	6.05	mm
Package weight	Including clamping system		1.3	2	g
Ferrule Pressing force of each interface hole		1.5	-	8.5	N
Ferrule pull out force of each interface hole		4	-	15	N

Package Drawing

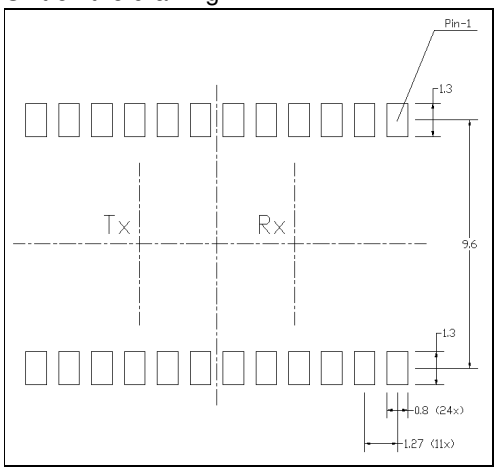


Notes:
[1] Package according to JEDEC MS-013E [5] with following additional constraints and expansions:
- height not applicable
- co-planarity: < 0.1mm
- pin width: 0.4 ± 0.05 mm ([b] in MS-013E)
- stand-off: between 0.1mm and 0.3mm
- The Optical Reference Plane (ORP) is a plane parallel with the datum plane C and located at a distance 0±0.1mm from datum plane C

MLX75605 SMD FOT				mm		
Part description		Quantity	Material	Dimensions		
Designer		Date	Scale	Melexis		
Carl Van Buggenhout		18-Feb-10	See drw			
		Projection				
File:	MLX75605_COMPLETE_PACKAGE		Project name:	MOST150	Rev.	
Status:	Released		Subassy name:		1.0	
Class:	CONFIDENTIAL		ASSEM name:	MLX75605	sheet1/1	

Footprint

Foot print is based on standard SOIC 300 mil package with 24 pins.
Unit on the drawing: mm



Lead frame

A dedicated leadframe has been designed taking into account EMI considerations. Additionally to this, some die pad/fused pins are put in the middle allowing direct shielding inside component, enabling noise reduction and increased robustness against mechanical stress.

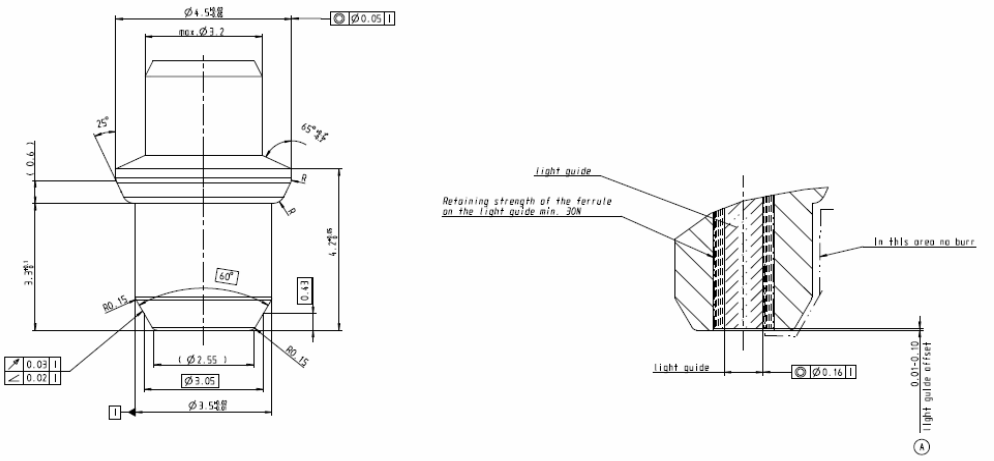
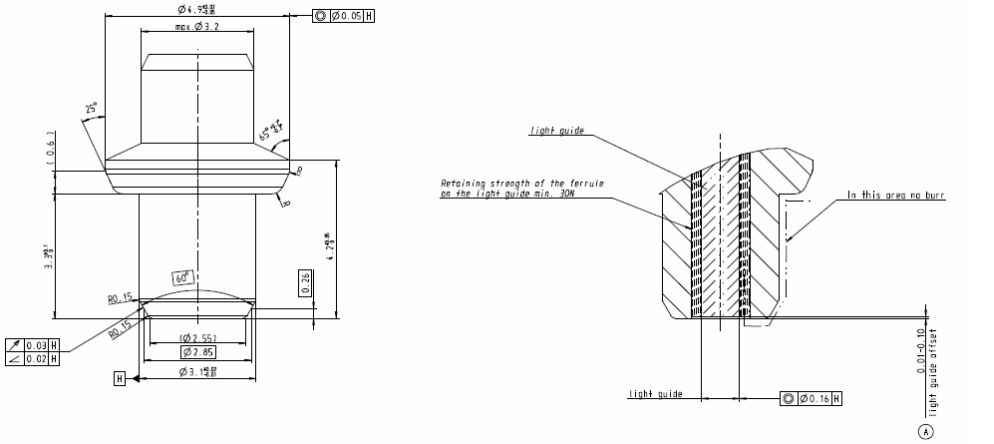
Unique Features

- Temperature range: -40°C up to 95°C.
- Full automotive qualified package.
- Surface Mounting Device
- LED is trimmed during Melexis process to guarantee a maximum and stable optical output power.

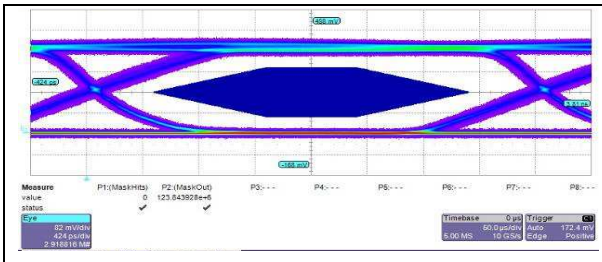
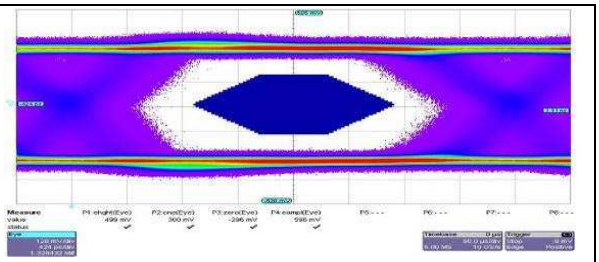
PCB integration recommendation

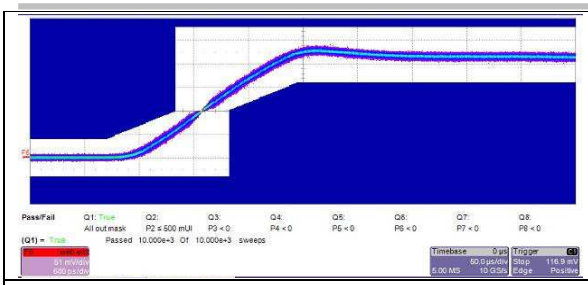
See separate application note “MLX75605 PCB recommendations”.

Recommended fiber ferrules

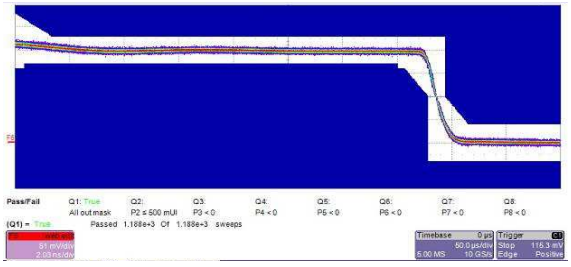
Transmitter Ferrule	
Receiver Ferrule	

Performance Graphs

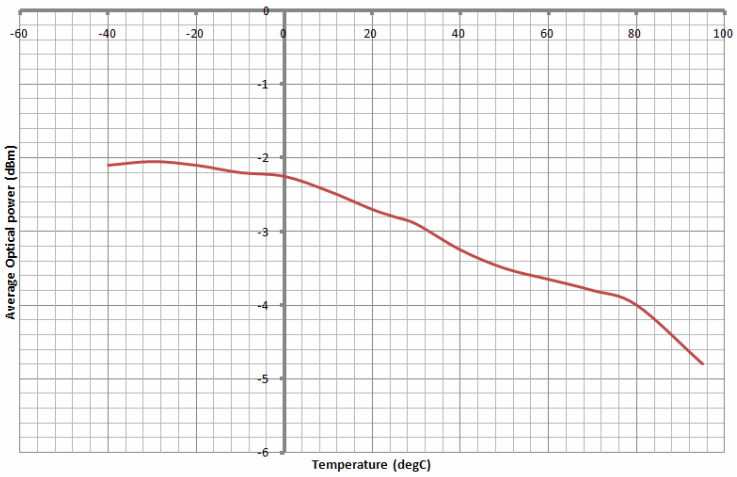
	
Transmitter eye mask at 3.3V power supply, 95°C ambient temperature	Receiver eye mask at -24dBm average optical power, 3.3V power supply, 95°C ambient temperature



Transmitter overshoot at 3.3V power supply, 95°C ambient temperature



Transmitter undershoot at 3.3V power supply, 95°C ambient temperature



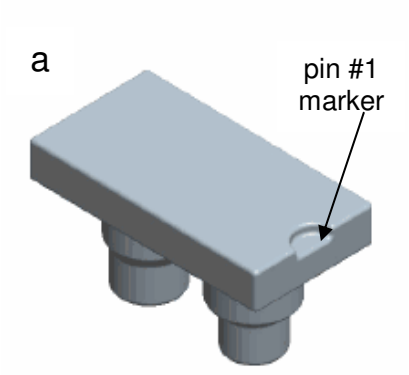
Transmitter average optical power over temperature range (typical)

Protection cap

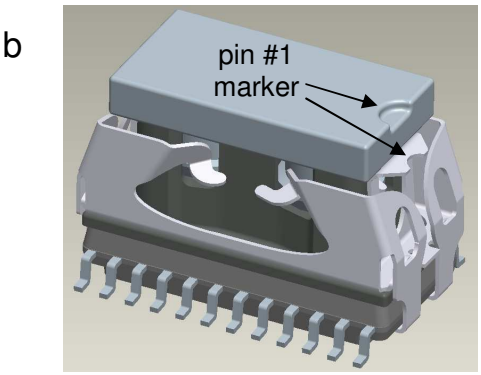
A protection cap is placed before placing the device into the carrier tape. The cap allows better pick and place capability with a standard pick-up head. In addition, it increases immunity against possible contamination from the reflow oven. The material of the protection cap is able to withstand soldering reflow process. The protection cap can be removed easily, either manually or with a vacuum head. The protection cap can be plugged into the device in only one manner (poka yoke principle). A pin #1 marker can be found on top of the cap. In addition the metal clamp of the FOT also has a pin #1 marker. In following figure some drawings of the protection cap and the device in which it is plugged are shown with indication of both (cap and FOT) pin #1 markers.

The protection cap specifications are summarized in following table:

Parameter	Min	Typ	Max	Units
Pull-out force to remove protection cap.	0.8	1	1.5	N
Cap Length	12.9	13	13.1	mm
Cap Width	6.7	6.8	6.9	mm
Cap pin #1 marker radius	0.9	1	1.1	mm



a) protection cap with "pin #1 marker" indicated



b) device with protection cap plugged in

Reliability Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's
IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices
(classification reflow profiles according to table 5-2)
EIA/JEDEC JESD22-A113
Preconditioning of Non-hermetic Surface Mount Devices Prior to Reliability Testing
(reflow profiles according to table 2)

IMPORTANT Note: Wave Soldering for this type of SMD component isn't allowed, due to optical package opening.

EN60749-20
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
EIA/JEDEC JESD22-B106 and EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Solderability
EIA/JEDEC JESD22-B102 and EN60749-21

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.asp

IMPORTANT: In alignment with automotive standards, prior to production deliveries for automotive applications, a Part Submission Warrant need to be signed by the customer, in order to make sure that the is compatible with the applications. As the MLX75605 was developed for infotainment applications, use in safety-critical applications is at full responsibility of the customer.

Manufacturing Information

Soldering Process

Product withstands Moisture Sensitivity Level #2a.
Product survives 260°C according IPC/JEDEC J-STD-020.
Besides to the JEDEC standard, the chip is able to withstand 245°C during 5 sec and 217°C during 60sec.

In order to protect device during soldering process, sample is delivered by Melexis with a protection on the top of the lid. This one can be easily removed before ferrule insertion. See also separate application note “MLX75605/MLX75608 Description of Packing”.

Packing information

See application note “MLX75605/MLX75608 Description of Packing” for details concerning packing (tube vs. reel), labeling, minimum order of quantity, etc.

Precaution

Optical Eye precautions

Only insertion of optical fiber terminated with a ferrule with dimensions as specified in the 150 Mbps MOST standard is allowed. Inserting anything else, e.g. an optical fiber not terminated with a standard 150 Mbps MOST ferrule, can damage the part and will automatically lead to the loss of the Melexis Warranty.

ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
The product is qualified to reach 2kV Human Body Model.
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

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