AAT2605

SystemPower™

Five Channel 300mA LDO Regulator

General Description

The AAT2605 is a member of AnalogicTech's Total Power Management IC™ (TPMIC™) product family. It contains five fully integrated 300mA low dropout (LDO) regulators in a small Pb-free 14-pin 3mm x 3mm TDFN package, making it ideal for space-constrained systems.

The AAT2605 features low power consumption, low dropout, and high noise immunity from the input power supply. Each channel consumes a mere 30µA of current when enabled, features 250mV of dropout at 250mA and 68dB of power supply rejection at 10kHz. Each channel has its own enable pin and uses a small 1µF output capacitor. Output voltages are factory One Time Programmable (OTP) between 0.6V and 3.7V with 100mV increment and typical regulation accuracy is ±1%. LDO1 and LDO2 share the same input voltage, as do LDO3 and LDO4 while LDO5 has its own independent input.

The AAT2605 is a safe solution that integrates an over-current limit for each channel and an over-thermal protection. The device is rated over a temperature range of -40°C to 85°C.

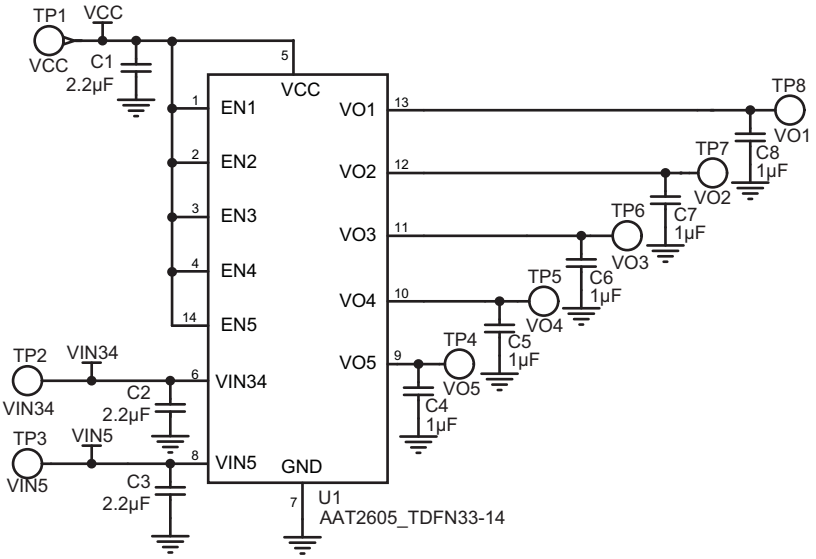
Features

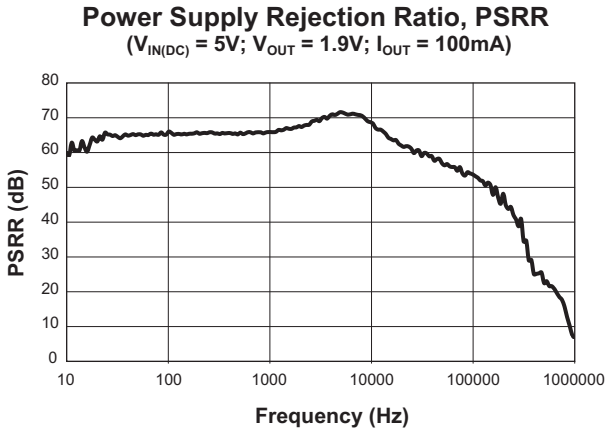
- 2.7V to 5.5V Operating Input Voltage Range
- 5 Outputs with Factory Programmable Voltages from 0.6V to 3.7V
- 300mA Output Current Per Channel
- 3mmx3mm, 14-Pin TDFN Package
- ±1% Typical Accuracy
- Low 30µA Quiescent Current
- High PSRR (68dB @10KHZ)
- 250mV Dropout Voltage at 250mA
- Independent Enable
- Over-Current Protection
- Over-Thermal Protection

Applications

- Cellular Applications
- Handheld Products
- Media Players (MP4 Players)
- Portable Navigation Devices (PND)

Typical Application



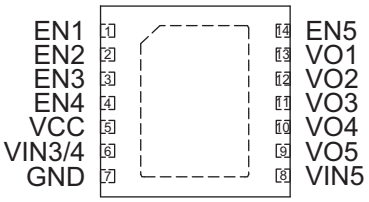


Pin Descriptions

Pin #	Symbol	Function
1	EN1	LDO1 enable; active high.
2	EN2	LDO2 enable; active high.
3	EN3	LDO3 enable; active high.
4	EN4	LDO4 enable; active high.
5	VCC	Input to power control circuit, LDO1, and LDO2.
6	VIN3/4	Input to LDO3 and LDO4.
7	GND	Analog ground.
8	VIN5	Input to LDO5.
9	VO5	LDO5 output voltage.
10	VO4	LDO4 output voltage.
11	VO3	LDO3 output voltage.
12	VO2	LDO2 output voltage.
13	VO1	LDO1 output voltage.
14	EN5	LDO5 enable; active high.

Pin Configuration

TDFN33-14
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VCC, VIN3/4, VIN5, EN1, EN2, EN3, EN4, EN5 to GND	-0.3 to 6.5	V

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation	2	W
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

V_{CC} = $V_{IN3/4}$ = V_{IN5} = 5.0V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

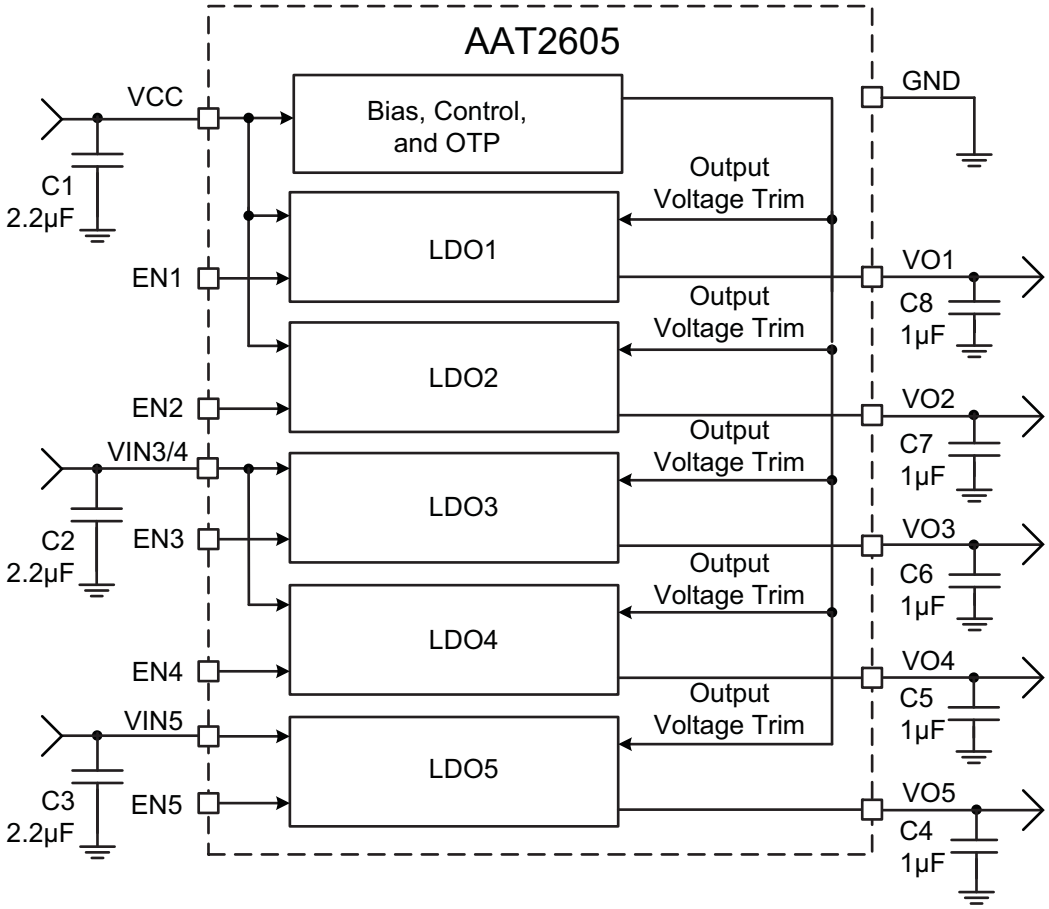
Symbol	Description	Conditions	Min	Typ	Max	Units
Logic Control / Protection						
V_{ENx}	Input High Threshold		1.4			V
	Input Low Threshold				0.3	V
Input Supply						
V_{CC}, $V_{IN3/4}$, V_{IN5}	Input Voltage Range		2.7		5.5	V
UVLO	Under-Voltage Lockout Threshold	VCC Falling		2		V
		VCC Rising		2.2		
Low-Dropout Regulator (LDO1:LDO5)						
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 250mA, OTP per requirement	0.6V		V_{INLDO} - V_{DO}	V
	LDO Accuracy	I_{LDO} = 10mA	-3		+3	%
I_Q	LDO Quiescent Current	V_{INx} = 5.0V, added quiescent current when LDO is enabled		30	55	µA
I_{SHDN}	Shutdown Current	V_{INx} = 5.0V, EN = GND		1		µA
	Line Regulation	I_{LDO} = 10mA		0.1		%/V
V_{DO}	Dropout Voltage	I_{LDO} = 250mA		250	500	mV
PSRR	Power Supply Rejection Ratio	V_{INx} = 5.0V, EN = High, I_{LDO} = 100mA, f = 10KHz, V_{Ox} = 1.8V		68		dB
$I_{LDO(LIM)}$	LDO Current Limit		300			mA
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold	Rising		145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			25		°C

1. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

Programming Output Voltages via OTP

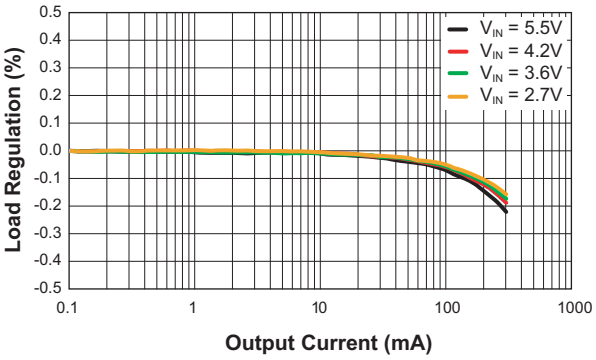
Regulator	Output Voltage Range		Resolution
LDO1	0.6V	3.7V	100mV
LDO2	0.6V	3.7V	100mV
LDO3	0.6V	3.7V	100mV
LDO4	0.6V	3.7V	100mV
LDO5	0.6V	3.7V	100mV

Block Diagram

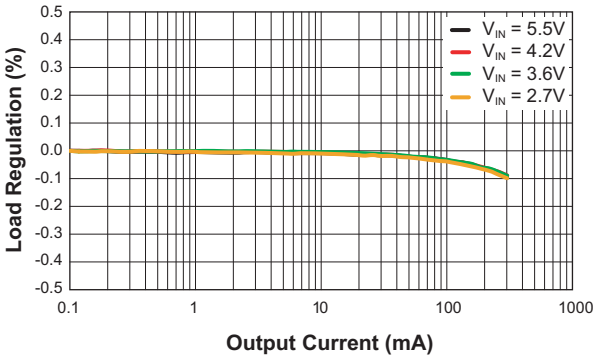


Typical Characteristics

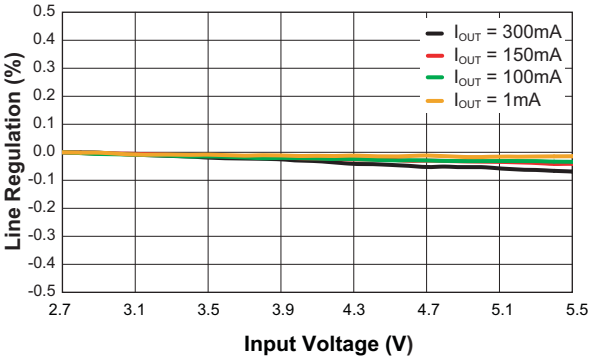
Load Regulation
(V_{OUT} = 1V)



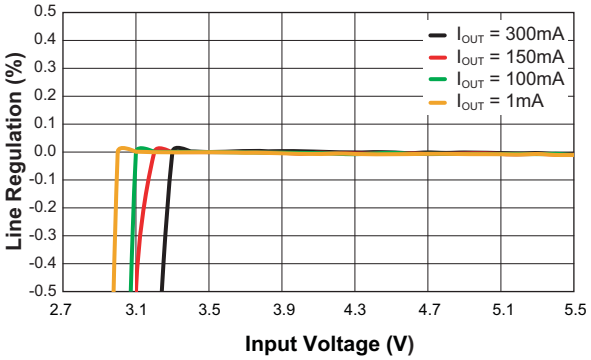
Load Regulation
(V_{OUT} = 3V)



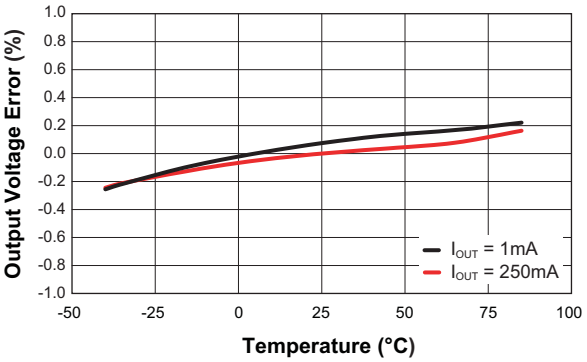
Line Regulation
(V_{OUT} = 1V)



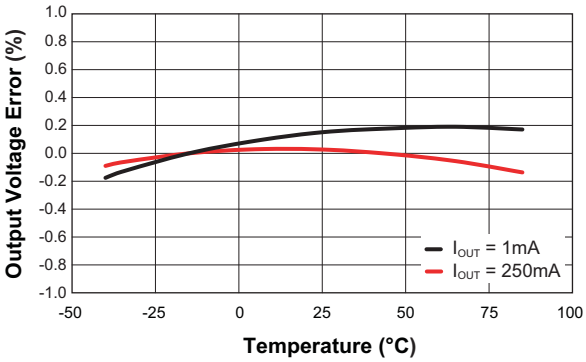
Line Regulation
(V_{OUT} = 3V)



Output Voltage Error vs. Temperature
(LDO V_{OUT} = 1V)

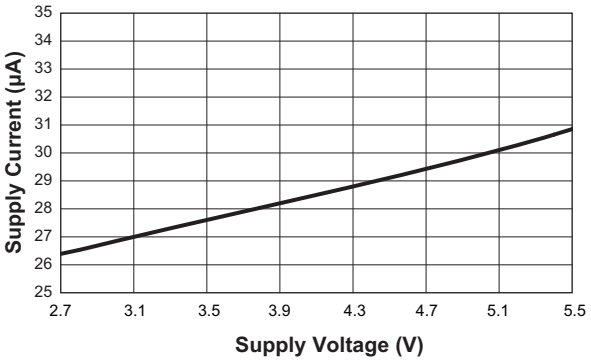


Output Voltage Error vs. Temperature
(LDO V_{OUT} = 3V)

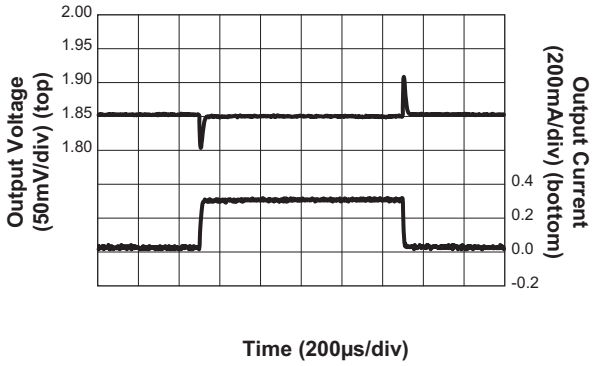


Typical Characteristics

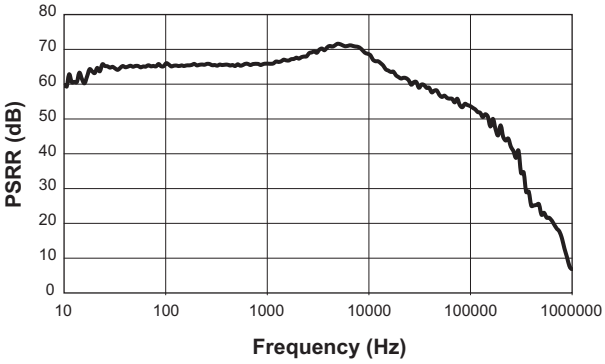
Supply Current vs. Supply Voltage
(Contributed By Each LDO)



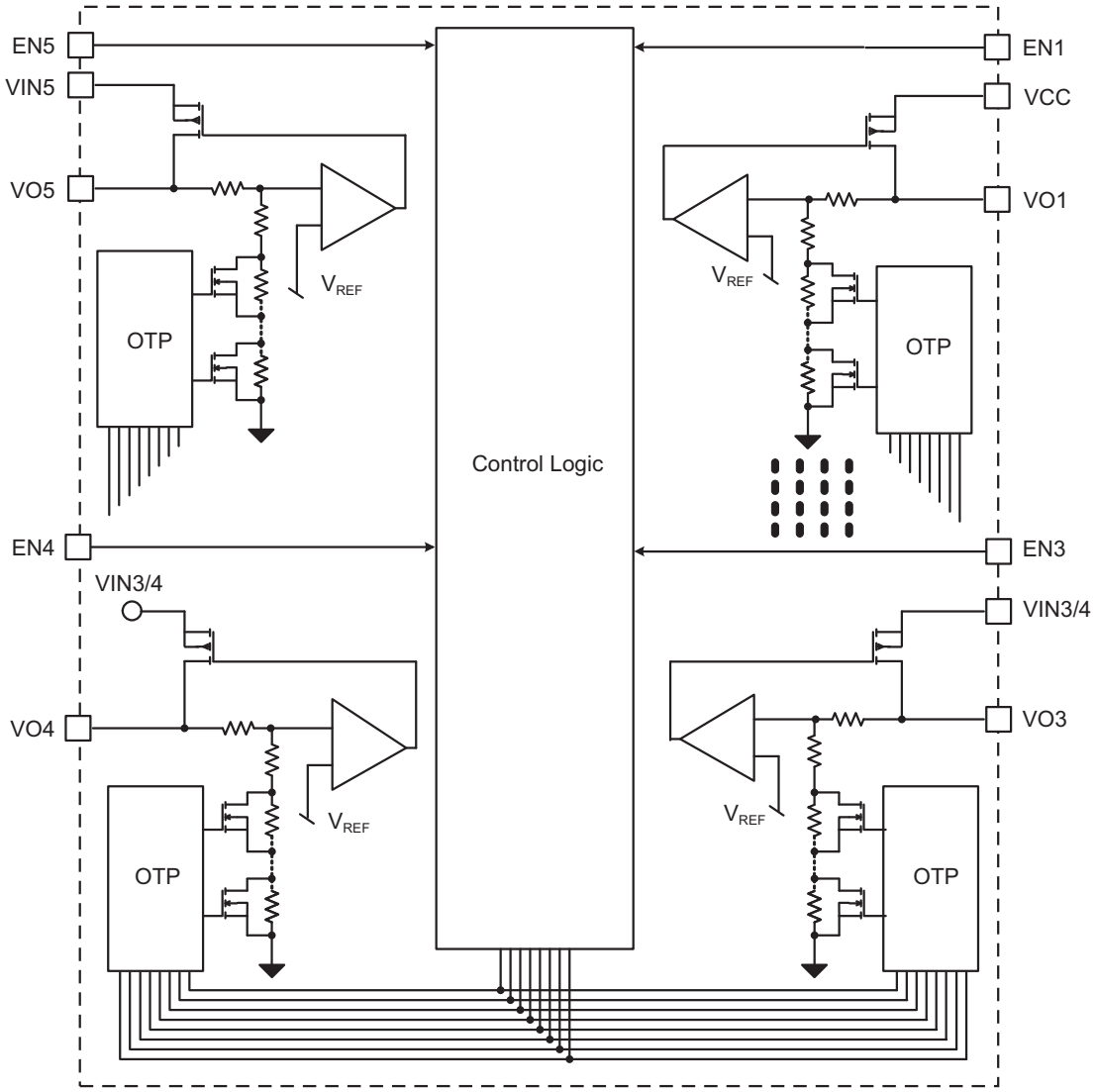
Load Transient
(V_{OUT} = 1.85V; V_{IN} = 3.6V; I_{OUT} = 30mA to 300mA)



Power Supply Rejection Ratio, PSRR
($V_{IN(DC)}$ = 5V; V_{OUT} = 1.9V; I_{OUT} = 100mA)



Functional Block Diagram



Functional Description

The AAT2605 includes five LDO regulators. The regulators operate from the 2.7V to 5.5V input voltage to a regulated output voltage. Each LDO regulator has its own independent enable pin. The LDO regulators have a fixed output programmed during manufacturing. Each LDO consumes 30µA of quiescent current and is stable with a small 1.0µF ceramic output capacitor. These LDOs offer high power supply rejection, over-current protection and over-temperature protection.

Application Information

Input Capacitor

Typically, a 2.2µF or larger ceramic capacitor is recommended for C_{VCC}, $C_{VIN3/4}$, and C_{VIN5} in most applications. The input capacitor should be located as close to the input (V_{IN}) of the device as practically possible. C_{VIN} values greater than 2.2µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins VOUT and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT2605's LDO regulators have been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF.

Thermal Calculations

There are two types of losses associated with the AAT2605 total power management solution (five LDO regulators): conduction losses and quiescent current losses. Conduction losses are associated with the power loss of the voltage difference across the pass switch/FET of the five LDO regulators. At full load, a simplified form of the losses is given by the following (quiescent losses are ignored, since conduction losses are so dominant):

$$P_{LDO1} = I_{LDO1} \cdot (V_{CC} - V_{O1})$$

$$P_{LDO2} = I_{LDO2} \cdot (V_{CC} - V_{O2})$$

$$P_{LDO3} = I_{LDO3} \cdot (V_{IN3/4} - V_{O3})$$

$$P_{LDO4} = I_{LDO4} \cdot (V_{IN3/4} - V_{O4})$$

$$P_{LDO5} = I_{LDO5} \cdot (V_{IN5} - V_{O5})$$

$$P_{TOTAL} = P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4} + P_{LDO5}$$

Layout

The suggested PCB layout for the AAT2605 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitors (C1, C2 and C3 should connect as closely as possible to VCC, VIN3/4 and VIN5 (Pins 5, 6 and 8) and GND (Pin 7).
2. The resistance of the trace from the load return to GND (Pin 7) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
3. For good thermal coupling, PCB vias are required from the pad for the TDFN33-14's exposed paddle to the ground plane.

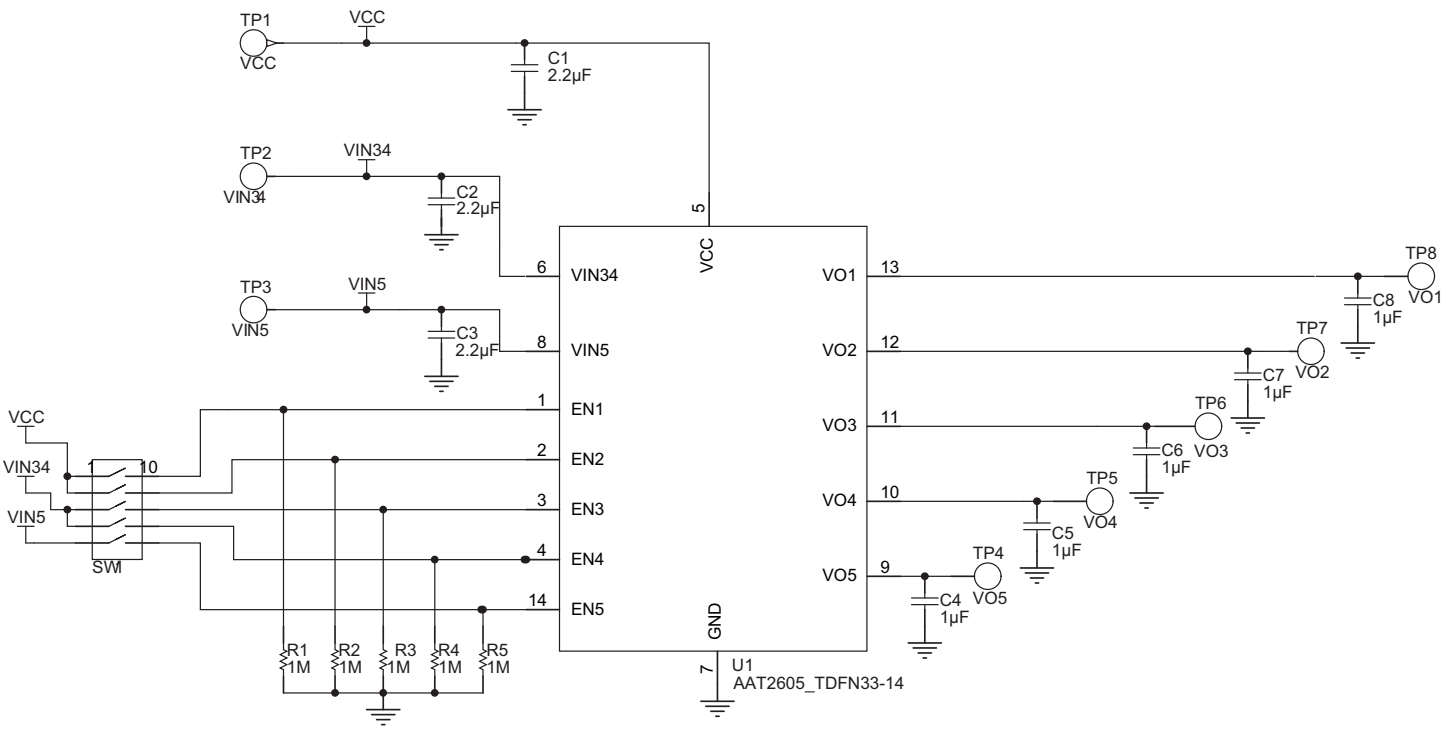


Figure 1: AAT2605 Evaluation Board Schematic.

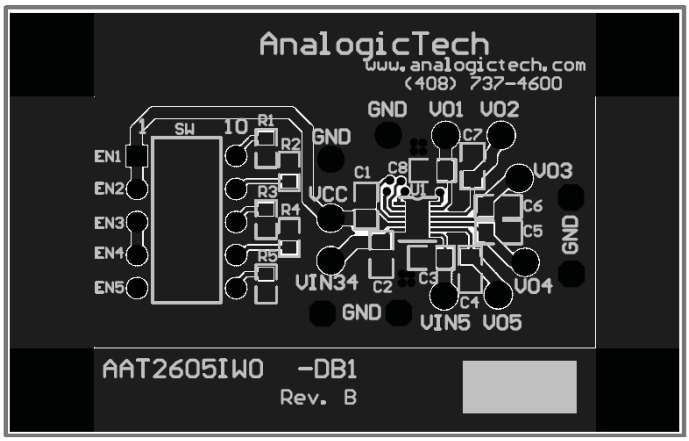


Figure 2: AAT2605 Evaluation Board Top Side Layout.

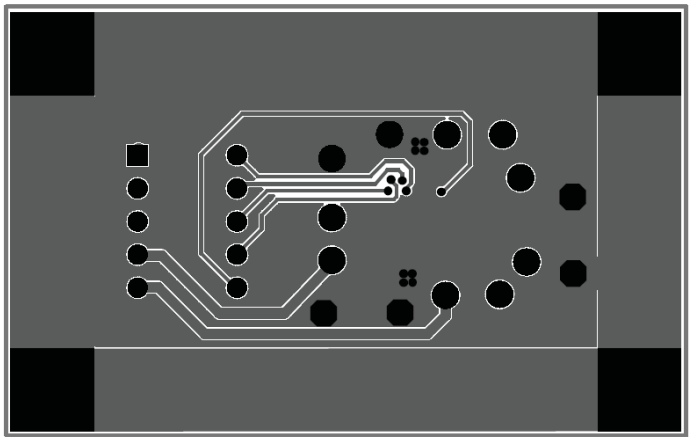


Figure 3: AAT2605 Evaluation Board Bottom Side Layout.

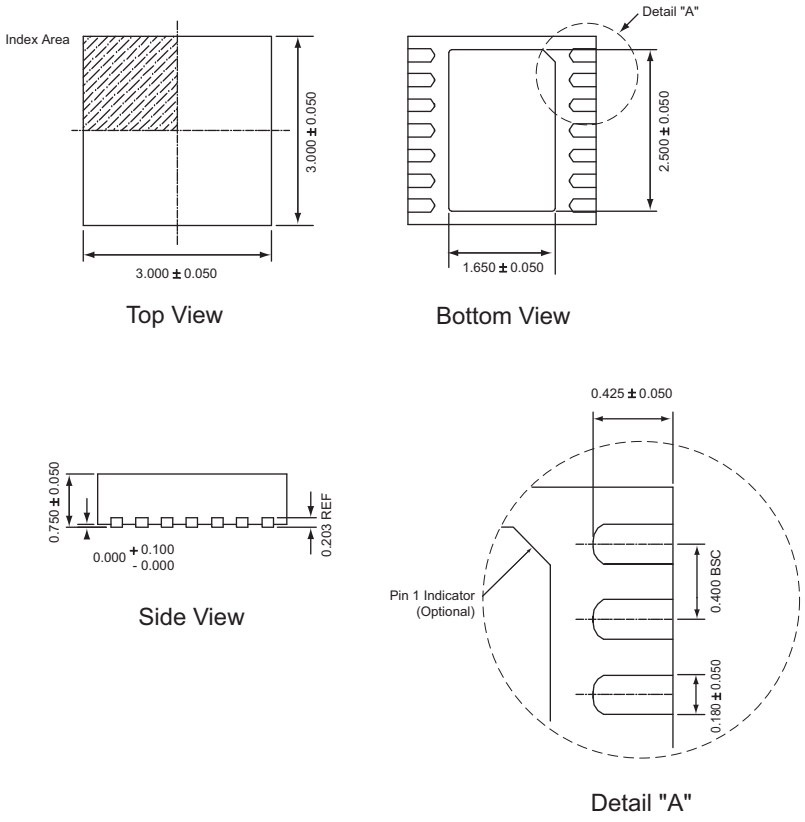
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TDFN33-14	9VXYY	**AAT2605IWO-1-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/aboutus/quality.php.

Package Information

TDFN33-14[3]



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
3230 Scott Boulevard, Santa Clara, CA 95054
Phone (408) 737-4600
Fax (408) 737-4611