LX1695

Switched Royer CCFL Inverter Monitor IC

PRODUCTION DATA SHEET

DESCRIPTION

The LX1695 is a general purpose DC to PWM generator with supervisory functions for switched Royer CCFL inverter modules used in single or multiple lamp desktop monitors and LCD TV sets. It integrates a PWM that generates digital (burst mode) dimming from a DC brightness control input, and a protection circuit that shuts off the Royer oscillator if lamp ignition does not occur in a timely manner, or in the event of one or more open lamps. Strike and initial open lamp timeout is user programmable with an external RC, and PWM frequency is programmable with a single external resistor.

The DIM_FREQ pin can also accept an external clock signal to program and/or synchronize the Royer output frequency.

This low cost eight pin IC includes under-voltage lockout and a logical ENABLE input that permits shutting down the Royer inverter(s) remotely without removing their power. A single output pin can be expanded with external transistors to drive any number of Royer circuits, giving a single device the ability to control very large displays for LCD TV applications or single lamp panels in notebooks and web tablets. The device is available in either an 8 pin plastic DIP or SOIC package.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website:

KEY FEATURES

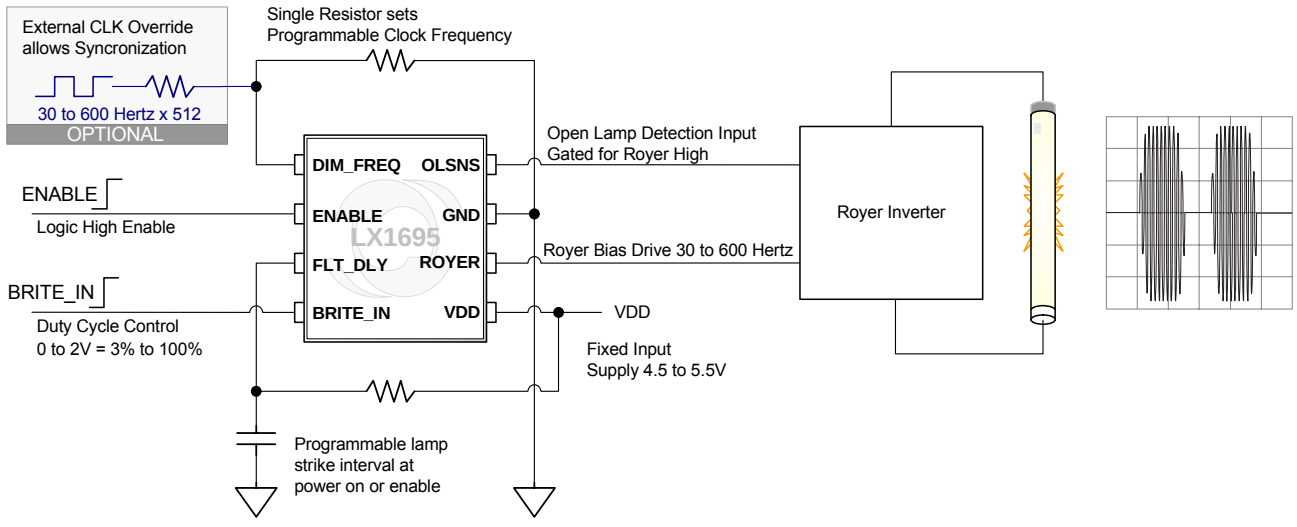
- Single Resistor Programs Output Frequency
- Allows External Synchronized PWM
- Open Lamp Sense Protection
- Programmable Fault Delay
- Enable and UV Lockout
- Preset 3.125% Minimum Output Duty Cycle

APPLICATIONS/BENEFITS

- DC to PWM Generator
- Single or Multi Lamp Designs
- Desktop Monitors
- LCD TV
- Industrial Displays

PRODUCT HIGHLIGHT

Wide Range Dimming For a Fixed Royer Inverter



PACKAGE ORDER INFO

T_J (°C)	M Plastic DIP 8-Pin RoHS / Pb-free	DM Plastic SOIC 8-Pin RoHS / Pb-free
-40 to 85	LX1695IM	LX1695IDM

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1695IDM-TR)
RoHS compliant.

Rev. 1.0a, 2006-01-06

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}) 6V
Inputs (BRITE_IN, OLSNS, FLT_DLY, ENABLE, DIM_FREQ) ..... V_{DD}
Output Current (ROYER) 150mA
RoHS / Pb-free Peak Package Solder Reflow Temperature
(40 seconds Maximum Exposure) ..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

THERMAL DATA

M Plastic 8-Pin DIP

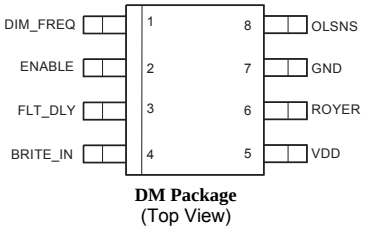
THERMAL RESISTANCE-JUNCTION AMBIENT, θ_{JA}	85°C/W

DM Plastic 8-Pin SOIC

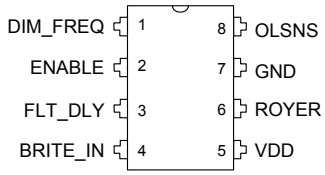
THERMAL RESISTANCE-JUNCTION AMBIENT, θ_{JA}	163°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



DM Package
(Top View)



M Package
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Description
VDD	Input Voltage. The IC will be functional and in specifications when this pin is between 4.5 and 5.5V_{DC}.
GND	Ground
BRITE_IN	Lamp Brightness Control. A DC input of 0 to 2V controls the duty cycle of the Royer output. Zero volts corresponds to minimum duty cycle (3.125%), maximum input voltage must yield 100% duty cycle. BRITE_IN has a high input impedance.
OL_SNS	Open Lamp Sense Input. This input receives rectified and filtered voltages from each Royer transformer secondary winding that are proportional to lamp current amplitude. These signals are diode OR'ed and compared to 3VDC at the OL_SNS input. If an under limit condition is detected, a fault is declared and the output is turned off. This condition is latched and can only be cleared by cycling the main power input or the ENABLE input signal off and on.
ROYER	Royer Bias Drive Output. This output signal drives external transistors that feed bias currents to one or more oscillators to turn them on. Output drive is totem pole and must be capable of ±50mA at 0.4 and 4.0V output when the supply voltage is 4.5 to 5.5 volts.
FLT_DLY	Fault Delay. An external resistor and capacitor at this pin program the time that open lamp fault detection is disabled following power on or an ENABLE low to high transition. By choosing the appropriate resistor and capacitor combination, delay time may be as high as 5 seconds
DIM_FREQ	A resistor to ground determines the frequency of the dual slope ramp generator for the digital dimming PWM. This pin may be overdriven through a resistor with totem pole output logic gates to force an external clock to over ride the internal clock, allowing the ROYER output to be synchronized to an external frequency without using another package pin. Input voltage levels of the external pulse are as follows: High state is; 2.9 to 5.5V minus 0.4 volts noise margin for minimum of 2.5 volts. Low state is; 0 to 0.36V plus 0.44 volts for noise margin for total of 0.8 volts.
ENABLE	A positive logic level enables the ROYER output pin. A low level turns it off, resets the fault latch and discharges the FLT_DLY capacitor. Logic threshold is about 1.6V. Upon ENABLE going high (True), the fault delay capacitor is allowed to charge, initiating the delay.

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RECOMMENDED OPERATING CONDITIONS

Parameter	LX1695			Units
	Min	Typ	Max	
Supply Voltage (V_{DD})	4.5		5.5	V
BRITE Linear DC Voltage Range	0		1.95	V
DIM_FREQ, ENABLE, FLT_DLY	0		V_{DD}	V
Royer Output Frequency Range	30	250	600	Hz

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, specifications apply over the range: T_A=-40 to 85°C, V_{DD} = 4.5 to 5.5V, R_{DIM_FREQ} =25.2K ohms, Royer = 1000pF ENABLE = V_{DD}, BRITE_IN = 1.0V, FLT_DLY = 3V

Parameter	Symbol	Test Conditions	LX1695			Units
			Min	Typ	Max	
POWER						
V_{VDD} Dynamic Current	I_{DD}	V_{DD}=5.5V		4.0		mA
Output Off Mode Current	$I_{\_OUT\ OFF}$	V_{DD}=5.5V; Enable ≤ 0.4V		3.5		mA
Enable Threshold	V_{IH}		2			V
	$V_{IL\_}$				0.8	V
ENABLE Input High Current	I_{IH_ENABLE}	V_{DD}=5V; ENABLE = 5V	-1	0.01	1	µA
ENABLE Input Low Current	I_{IL_ENABLE}	V_{DD}=5V; ENABLE = 0V	-1	-0.01	1	µA
UV Threshold	UV_{TH}	V_{DD} Rising	3.7	4	4.3	V
UV Hysteresis				350		mV
ROYER						
ROYER Output Sink Current	I_{SK_ROYER}	BRITE_IN = 2V ROYER = 0.4V	40	75		mA
ROYER Output Source Current	I_{SRC_ROYER}	BRITE_IN = 2V ROYER = VDD-0.5V		100		mA
ROYER Output Rise Time	T_R	C_{OUT} = 1000pF		20	100	nS
ROYER Output Fall Time	T_F	C_{OUT} = 1000pF		20	100	nS
DIM FREQ						
DIM_FREQ Voltage	V_{DIM_FREQ}			1		V
DIM_FREQ ISC	ISC_{DIM_FREQ}	DIM_FREQ = 0V; self limiting		-600		µA
LOW ROYER Output Frequency	$F_{ROYER\ LOW}$	R_{DIM_FREQ} = 215K	27	30	33	Hz
NOMINAL ROYER Output Frequency	$F_{ROYER\ NOM}$	R_{DIM_FREQ} = 25.2K	237	250	263	Hz
HIGH ROYER Output Frequency	$F_{ROYER\ HIGH}$	R_{DIM_FREQ} = 10K	555	600	645	Hz
DIM_FREQ IIH	IIH_{DIM_FREQ}	DIM_FREQ = 3V; No R_{DIM_FREQ}		120		µA
DIM_FREQ IIL	IIL_{DIM_FREQ}	DIM_FREQ = 0.4V; No R_{DIM_FREQ}		-475		µA
EXT CLK ROYER Output Frequency	$F_{ROYER\ EXT\_CLK}$	DIM_FREQ = 15KHz to 300KHz Square Wave		$\frac{DIM\_FREQ}{512}$		Hz
BRITE_IN / DUTY CYCLE CONTROL						
BRITE_IN Input High Current	$I_{IH\_BRITE\_IN}$	V_{DD}=5V; BRITE_IN = 2V	-1	0.01	1	µA
BRITE_IN Input Low Current	$I_{IL\_BRITE\_IN}$	V_{DD}=5V; BRITE_IN = 0V	-1	-0.01	1	µA
Duty Cycle 0	DC_0	BRITE_IN = 0V;	2.5	3.125	5	%
Duty Cycle 1	DC_1	BRITE_IN = 1V		52		%
Duty Cycle 2	DC_1	BRITE_IN = 1.95	95	100		%
VDAC Ramp Valley Voltage	$VDAC_{RP}$	For reference only		40		mV
VDAC Ramp Peak Voltage	$VDAC_{RV}$	For reference only		1.9		V
OLSNS / FAULT DELAY THRESHOLD						
OLSNS Threshold Voltage	V_{TH_OLSNS}		2.92	3	3.05	V
OLSNS Clock Cycle Delay	$OLSNS_{DY}$	Note 1		48		cycles
FLT_DLY Threshold	FLT_DLY_{TH}			2.1		V

Note 1 : If duty cycle is set to less than 10% open lamp sensing is internally disabled

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SIMPLIFIED BLOCK DIAGRAM

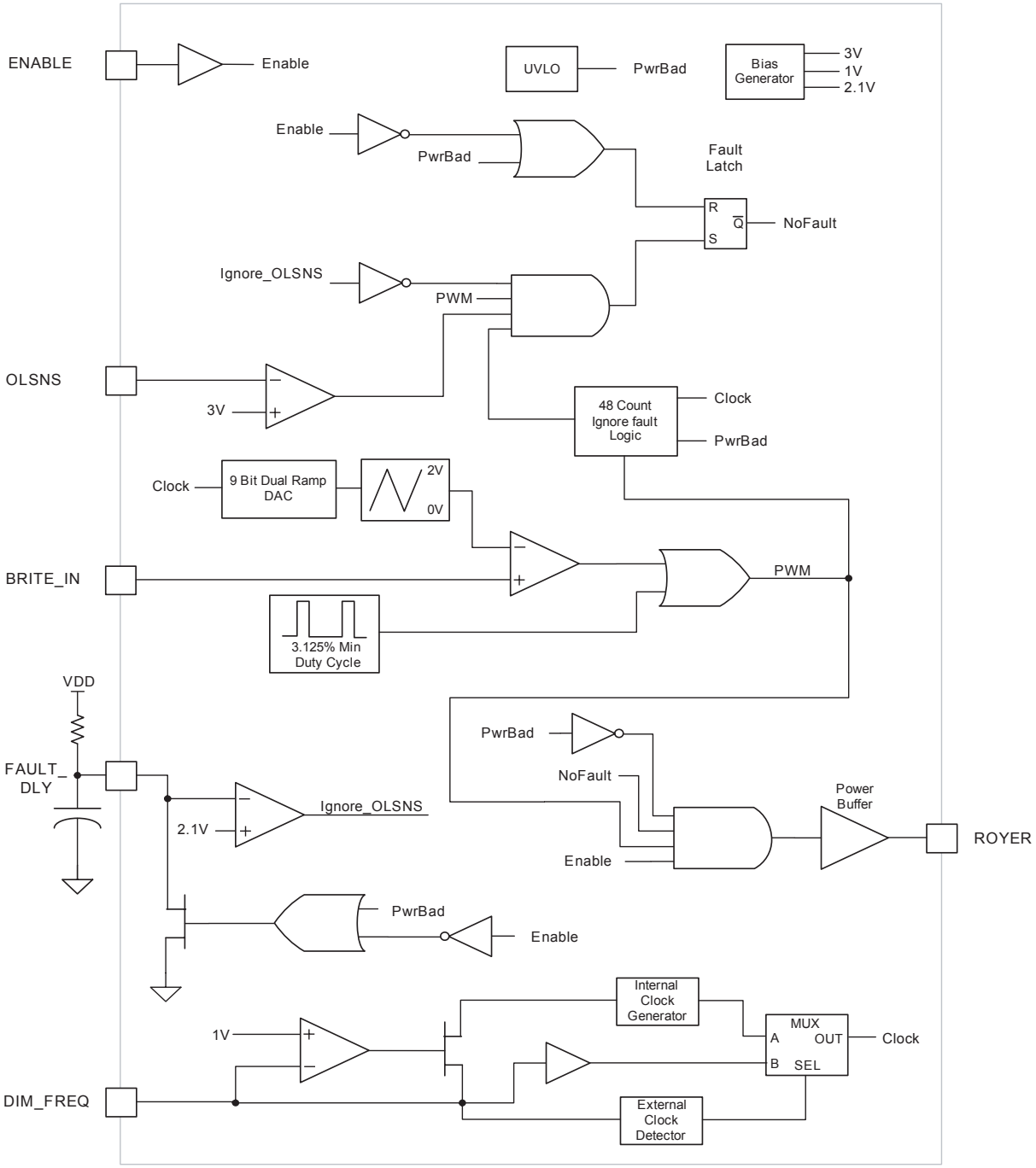

Figure 1 – Simplified Block Diagram

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APPLICATION CIRCUIT

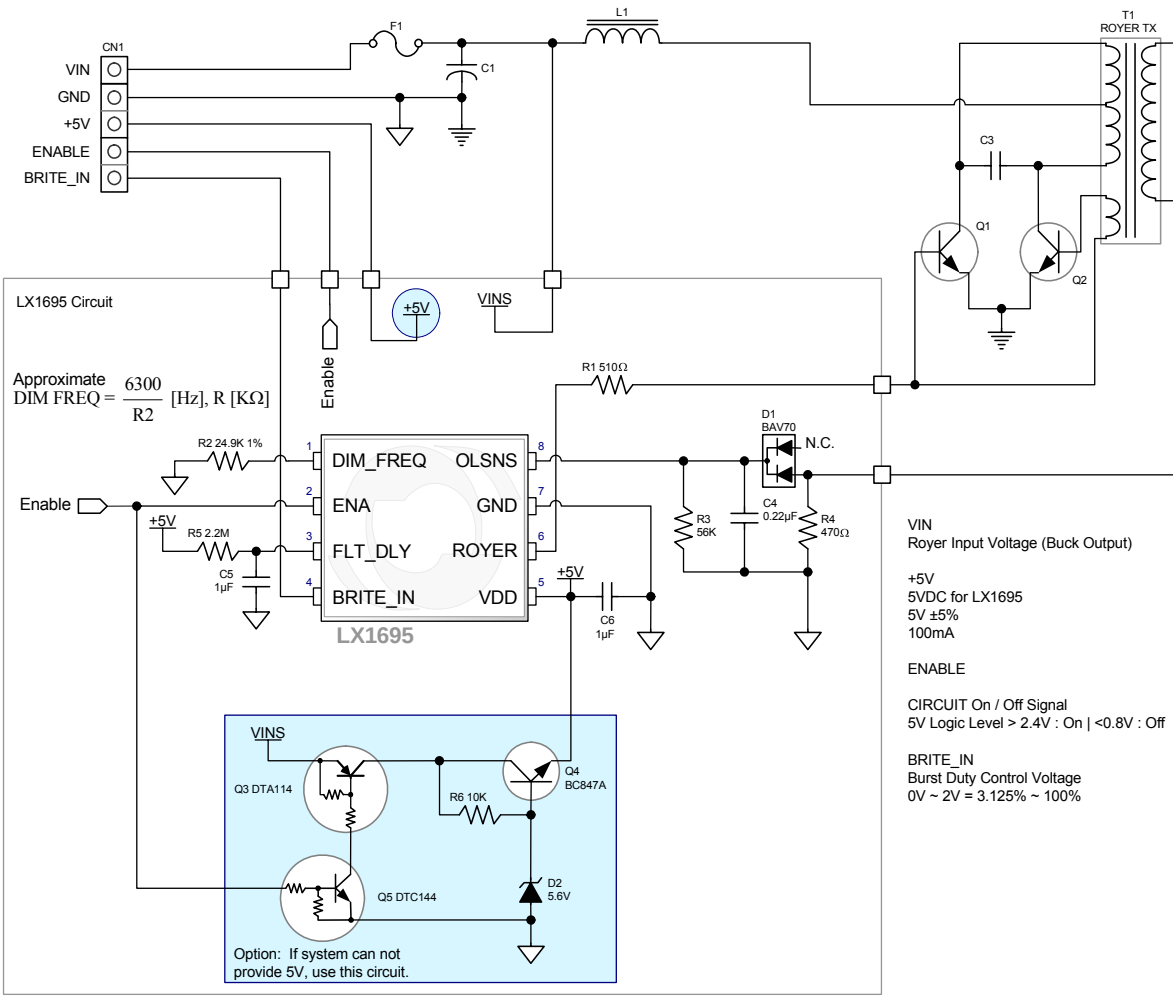

Figure 2 – Typical Application

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THEORY OF OPERATION

DIGITAL DIMMING PWM

A DC voltage to PWM converter provides an accurate digital dimming brightness control by varying Royer on time from 100% to as low as 3.125%. Minimum duty cycle is implemented by causing the Royer output signal to be high any time the DAC clock count is less than 8. Since the DAC is dual slope, this insures duty will be at least 16 out of the full 512 counts per cycle (See figure 3).

The PWM includes an on chip oscillator that provides dimming burst rates between 30 and 600Hz. The oscillator frequency is trimmed to ±3% accuracy (+20 to +65°C) to prevent unwanted display artifacts that can be caused by the lamp dimming frequency beating with the displays video.

Burst frequency can be controlled in two ways: An external resistor from DIM_FREQ to ground sets the frequency of the on chip oscillator. The formula for calculating a given ROYER output frequency based on the DIM_FREQ resistor to ground is as follows:

$$R_{DIM\_FREQ} = \frac{\left(1/\text{ROYER Output Frequency} - 184.32E\text{-}6\right)}{151.23E\text{-}9}$$

As an example, if a ROYER output frequency of 120Hz is desired then:

$$R_{DIM\_FREQ} = \frac{\left(1/120 - 184.32E\text{-}6\right)}{151.23E\text{-}9} = 53885$$

The closed nominal 1% resistor value would be 53.6K, nominally yielding a just slightly higher than 120Hz output.

Dimming frequency becomes the oscillator frequency divided by 512 or a logic level pulse supplied through a 10K resistor to the DIM_FREQ pin overrides the internal timing circuits causing the dimming frequency to be input frequency divided by 512. The 10K external series resistor limits current into the ESD structure at the DIM_FREQ pin.

The duty cycle at the Royer output is directly and linearly proportional to the DC level of signal BRITE_IN. Two (2.0) volts corresponds to 100% duty and zero volts corresponds to minimum duty. Minimum duty is internally limited to 3.125% even if BRITE_IN is zero volts

High input impedance (>10 MΩ) at the BRITE_IN pin makes it easy to set up minimum and maximum duty cycle outputs using only a few external resistors. The input pin is also directly compatible with Microsemi's LX1970 and 1971 ambient light sensors that provide automatic brightness control.

START-UP FAULT DELAY

Open lamp detection is disabled for a programmable period after power turn-on, giving the Royer oscillators sufficient time to ignite all lamps. An external resistor and capacitor at pin FLT_DLY controls this time. The capacitor begins to charge at power on, and its exponential voltage rise is compared to a 2.1 volt reference to signal the end of fault delay interval. This condition is latched and then the external capacitor is discharged by an on chip NMOS transistor. Discharge time is about 10% of charge time, and the capacitor value can be up to 10uF. The resistor will typically be less than 1 megohm.

OPEN LAMP DETECTION

The open lamp detection circuit can sense if any lamp in the entire array is not conducting and shut the system off to prevent possible catastrophic system failure. Lamp current sensing is gated only during Royer on time and is delayed from its leading edge so that reliable detection is provided, even while dimming with very low duty cycles. Delay is 48 counts of the DAC clock beginning when Royer goes high. This gives the actual Royer oscillators time to come up to full power before testing for a broken lamp. At low dimming levels when the output duty cycle less than 12.5% open lamp sensing is internally disabled. This corresponds to about 0.25V on the BRITE_IN pin.

An external R/C time out at pin FLT_DLY programs a delay after power-on to mask fault detection while the lamps are igniting. Typically this time-out is in the one to two second range, but can be as long as 5 seconds. Maximum recommended value of the resistor is 1 megohm to prevent error due to leakage current on the PCB, and low leakage ceramic capacitors are recommended.

Typically this time-out is in the one to two second range, but can be as long as 5 seconds.

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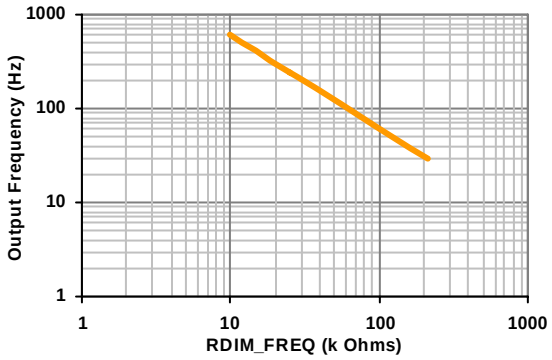
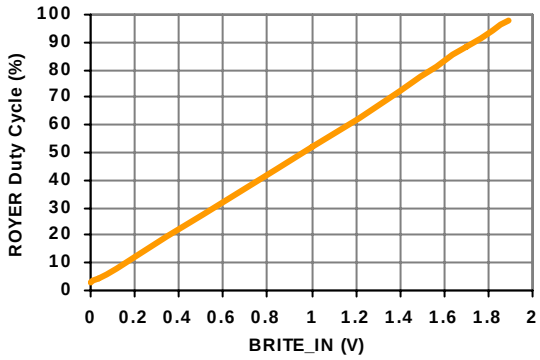
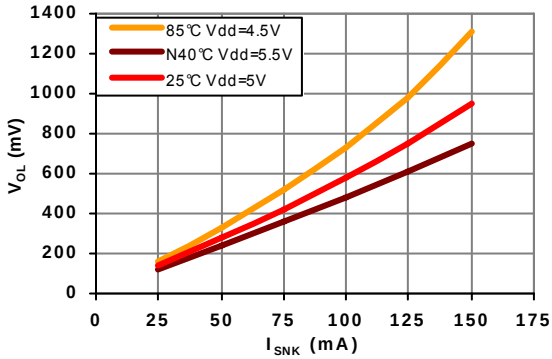
OUTPUT FREQ VS RDIM FREQ



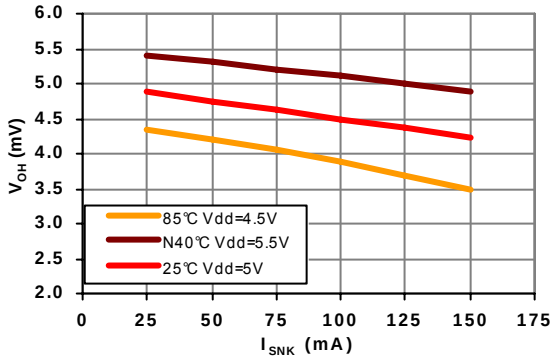
ROYER DUTY CYCLE



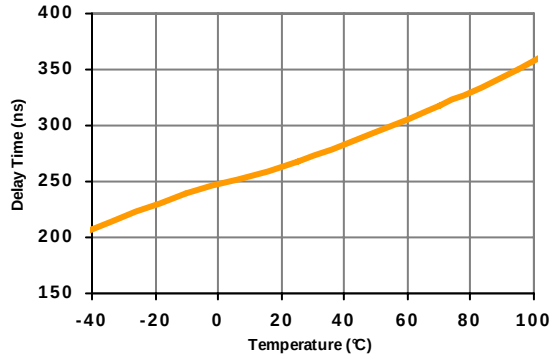
ROYER VOL VS ISNK



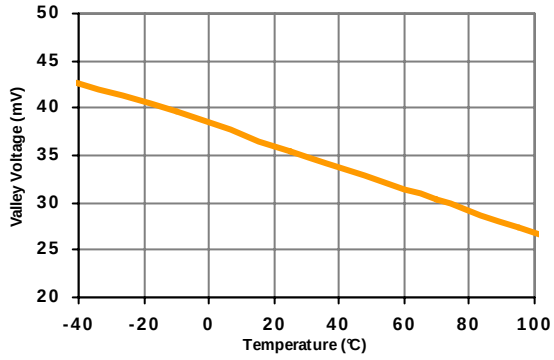
ROYER VOH VS ISNK



DELAY TIME ENABLE



VALLEY VOLTAGE @ MIN DUTY +1%



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TIMING DIAGRAM

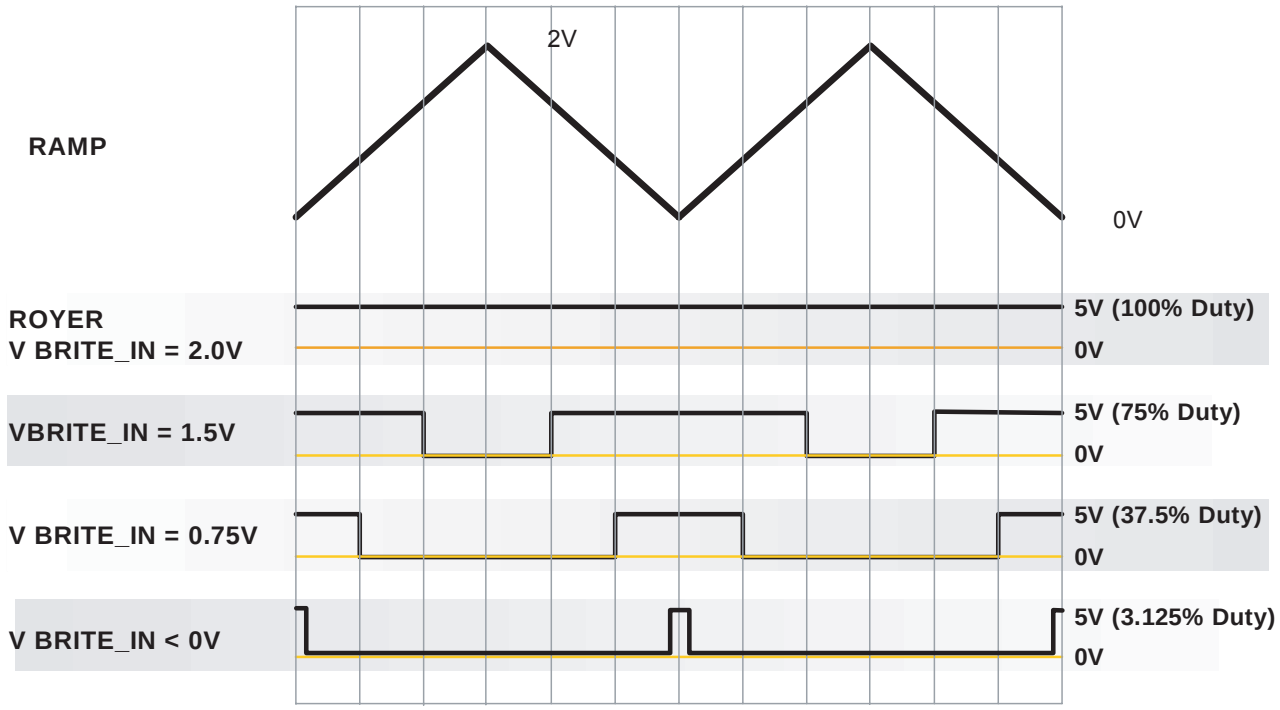

Figure 3 – Timing Diagram

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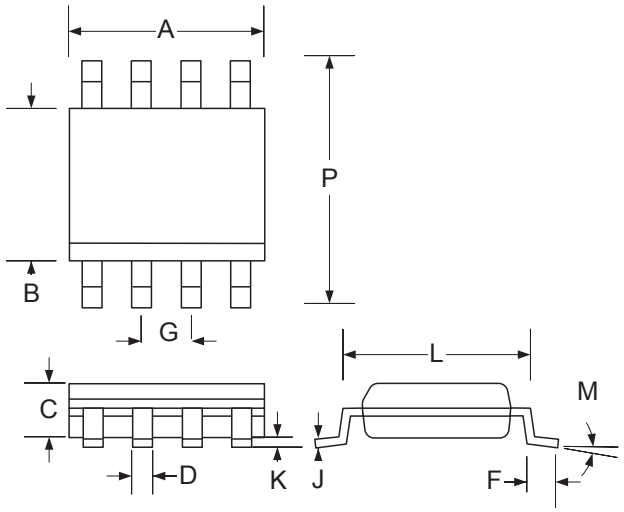
PACKAGE DIMENSIONS

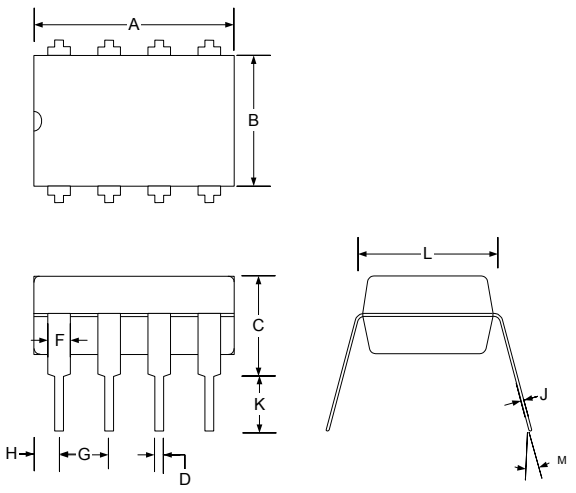
DM 8-Pin Plastic SOIC



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.00	0.190	0.197
B	3.81	3.94	0.150	0.155
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
F	-	0.77	-	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.13	0.25	0.005	0.010
L	4.80	5.21	0.189	0.205
M	-	8°	-	8°
P	5.79	6.20	0.228	0.244
*LC	-	0.10	-	0.004

*Lead Coplanarity

M 8-Pin Plastic Mini Dip



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	10.16	-	0.400
B	6.10	6.60	0.240	0.260
C	-	5.08	-	0.200
D	0.38	0.51	0.0145	0.020
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.38	0.008	0.015
K	3.18	-	0.125	-
L	7.62 BSC		0.300 BSC	
M	-	15°	-	15°

*Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES

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