Microsemi

2N682, 2N683, 2N685 – 2N692 and 2N5206

RoHS

Available on commercial versions

PNPN SILICON, REVERSE-BLOCKING, POWER TRIODE THYRISTORS

Qualified per MIL-PRF-19500/108

DESCRIPTION

This silicon controlled rectifier device is military qualified up to a JANTX level for high-reliability applications. Microsemi also offers numerous other products to meet higher and lower power voltage regulation applications.

Important: For the latest information, visit our website http://www.microsemi.com.

FEATURES

- JEDEC registered 2N682, 2N683, 2N685, 2N687 – 2N692 and 2N5206.
- JAN and JANTX qualifications are available per MIL-PRF-19500/108.
- RoHS compliant versions available (commercial grade only).

APPLICATIONS / BENEFITS

- A general purpose, reverse-blocking thyristor.

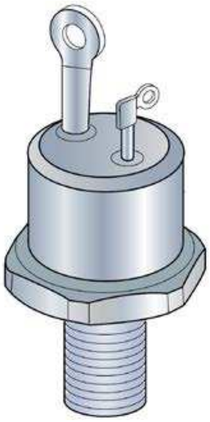
MAXIMUM RATINGS

Parameters/Test Conditions	Symbol	Value	Unit
Junction Temperature	T_J	-65 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Gate Voltage	V_{GM}	5	V(pk)
Maximum Average DC Output Current (1)	I_O	16	A
Non-repetitive Peak On-State Current (2) @ t = 7 ms	I_{TSM}	150	A

Notes:

1. This average forward current is for a maximum case temperature of +65 °C, and 180 electrical degrees of conduction.
2. Surge rating is non-recurrent and applies only with device in the conducting state. The peak rate of surge current must not exceed 100 amperes during the first 10 μs after switching from the off (blocking) state to the on (conducting) state. This time is measured from the point where the thyristor voltage has decayed to 90 percent of its initial blocking value.

Qualified Levels:
JAN and JANTX



TO-208 / TO-48 Package

MSC – Lawrence
6 Lake Street,
Lawrence, MA 01841
Tel: 1-800-446-1158 or
(978) 620-2600
Fax: (978) 689-0803

MSC – Ireland
Gort Road Business Park,
Ennis, Co. Clare, Ireland
Tel: +353 (0) 65 6840044
Fax: +353 (0) 65 6822298

Website:
www.microsemi.com

MECHANICAL and PACKAGING

- CASE: Nickel plated copper.
- TERMINALS: Nickel plated steel, solder dipped.
- MARKING: Manufacturer's ID, part number, date code, polarity.
- POLARITY: Terminal 1: gate, terminal 2: cathode, terminal 3 (stud): anode.
- WEIGHT: 12.36 grams.
- See Package Dimensions on last page.

PART NOMENCLATURE

JAN 2N682 (e3)

Reliability Level
JAN = Jan level
JANTX = JANTX level
CDS (reference JANS)
Blank = Commercial

JEDEC type number
(See Electrical Characteristics
table)

RoHS Compliance
e3 = RoHS compliant (available on commercial grade only)
Blank = non-RoHS compliant

SYMBOLS & DEFINITIONS

Symbol	Definition
V_{AA}	Anode power supply voltage (dc).

ELECTRICAL CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Repetitive Peak Reverse Voltage And Repetitive Peak Off-State Voltage	2N682	V_{RRM} (1) and V_{DRM}		50	V (pk)
	2N683			100	
	2N685			200	
	2N686			250	
	2N687			300	
	2N688			400	
	2N689			500	
	2N690			600	
	2N691			700	
	2N692			800	
	2N5206			1,000	

(1) Values applicable to zero or negative gate voltage (V_{GM}).

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Holding current: Bias condition D; V_{AA} = 24 V maximum; $I_{TM} = I_{F1}$ = 1 A $I_T = I_{F2}$ = 100 mA trigger voltage source = 10 V trigger PW = 100 μs (minimum) R_2 = 20 Ω	I_H		50	mA
Reverse blocking current AC method, bias condition D; f = 60 Hz, V_{RRM} = rated	I_{RRM1}		2	mA (pk)
Forward blocking current AC method, bias condition D; f = 60 Hz; V_{DRM} = rated	I_{DRM1}		2	mA (pk)
Gate trigger voltage and current $V_2 = V_D$ = 6 V; R_L = 50 Ω; R_e = 20 Ω maximum	V_{GT1} I_{GT1}		3 35	V mA
Forward on voltage I_{TM} = 50 A(pk) (pulse); pulse width = 8.5 ms; maximum; duty cycle = 2 percent maximum	V_{TM}		2	V (pk)
Reverse gate current V_G = 5 V	I_G		250	mA

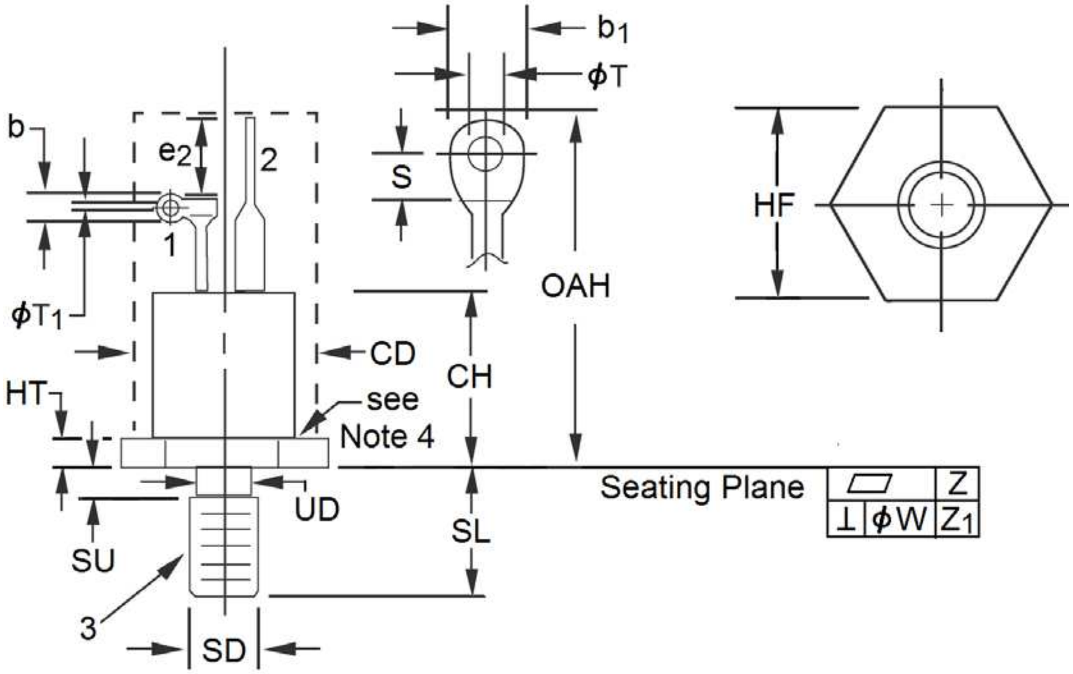
ELECTRICAL CHARACTERISTICS (continued)

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Reverse blocking current (T_C = +120 ºC) AC method, bias condition D; f = 60 Hz; V_{RRM} = rated		I_{RRM2}		5	mA (pk)
Forward blocking current (T_C = +120 ºC) AC method, bias condition D; f = 60 Hz; V_{DRM} = rated		I_{DRM2}		5	mA (pk)
Gate trigger voltage (T_C = +120 ºC; R_e = 20 Ω max)		V_{GT2}	.25		V
$V_2 = V_{DM}$ = 50 V; R_L = 140 Ω	2N682				
$V_2 = V_{DM}$ = 100 V; R_L = 140 Ω	2N683				
$V_2 = V_{DM}$ = 200 V; R_L = 140 Ω	2N685				
$V_2 = V_{DM}$ = 250 V; R_L = 650 Ω	2N686				
$V_2 = V_{DM}$ = 300 V; R_L = 650 Ω	2N687				
$V_2 = V_{DM}$ = 400 V; R_L = 3 k Ω	2N688				
$V_2 = V_{DM}$ = 500 V; R_L = 3 k Ω	2N689				
$V_2 = V_{DM}$ = 600 V; R_L = 3 k Ω	2N690				
$V_2 = V_{DM}$ = 700 V; R_L = 3 k Ω	2N691				
$V_2 = V_{DM}$ = 800 V; R_L = 3 k Ω	2N692				
$V_2 = V_{DM}$ = 1,000 V; R_L = 3 k Ω	2N5206				
Reverse blocking current (T_C = -65 ºC) AC method, bias condition D; f = 60 Hz; V_{RRM} = rated		I_{RRM3}		2	mA (pk)
Forward blocking current (T_C = -65 ºC) AC method, bias condition D; f = 60 Hz; V_{DRM} = rated		I_{DRM3}		2	mA (pk)
Gate trigger voltage and current (T_C = -65 ºC) $V_2 = V_D$ = 6 V; R_L = 50 Ω; R_e = 20 Ω maximum		V_{GT3} I_{GT2}		3 80	V mA
Exponential rate of voltage rise Bias condition D; T_C = +120℃ minimum, dv/dt = 25 v/µs; repetition rate = 60 pps; test duration = 15 s; C = 1.0 µF; R_L = 50 Ω					
V_{AA} = 50 V	2N682	V_D	47		V
V_{AA} = 100 V	2N683		95		
V_{AA} = 200 V	2N685		190		
V_{AA} = 250 V	2N686		240		
V_{AA} = 300 V	2N687		285		
V_{AA} = 400 V	2N688		380		
V_{AA} = 500 V	2N689		475		
V_{AA} = 600 V	2N690		570		
V_{AA} = 700 V	2N691		665		
V_{AA} = 800 V	2N692		760		
V_{AA} = 1,000 V	2N5206		950		

ELECTRICAL CHARACTERISTICS (continued)

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Circuit-commutated turn-off time T_C = +120℃ minimum; I_{TM} = 10 A; t_{on} = 100 ±50 µs; di/dt = 5 A/µs minimum; di/dt = 8 A/µs maximum; reverse voltage at t_1 = 15 V minimum; repetition rate = 60 pps maximum; di/dt = 20 V/µs; gate bias conditions; gate source voltage = 0 V; gate source resistance = 100 Ω					
V_{DM} = V_{DRM} = 50 V (pk); V_{RRM} = 50 V maximum	2N682	t_{off}		30	µs
V_{DM} = V_{DRM} = 100 V (pk); V_{RRM} = 100 V maximum	2N683			30	
V_{DM} = V_{DRM} = 200 V (pk); V_{RRM} = 200 V maximum	2N685			30	
V_{DM} = V_{DRM} = 250 V (pk); V_{RRM} = 250 V maximum	2N686			30	
V_{DM} = V_{DRM} = 300 V (pk); V_{RRM} = 300 V maximum	2N687			30	
V_{DM} = V_{DRM} = 400 V (pk); V_{RRM} = 400 V maximum	2N688			30	
V_{DM} = V_{DRM} = 500 V (pk); V_{RRM} = 500 V maximum	2N689			40	
V_{DM} = V_{DRM} = 600 V (pk); V_{RRM} = 600 V maximum	2N690			40	
V_{DM} = V_{DRM} = 700 V (pk); V_{RRM} = 700 V maximum	2N691			60	
V_{DM} = V_{DRM} = 800 V (pk); V_{RRM} = 800 V maximum	2N692			60	
V_{DM} = V_{DRM} = 1,000 V (pk); V_{RRM} = 1,000 V max.	2N5206			60	
Gate controlled turn-on time V_{AA} = 50 V for 2N682 V_{AA} = 100 V for 2N683, 2N685 through 2N692 and 2N5206 I_{TM} = 10 A; V_{GG} = 10 V; R_e = 25 Ω t_{p1} = 15 ±5 µs; 4 A/µs ≤ di/dt ≤ 200 A/µs.	2N682, 2N683, 2N685 through 2N692 & 2N5206	t_{on}		5	µs

PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Device contour, except on hex head and noted terminal dimensions, is optional within zone defined by CD and OAH, CD not to exceed actual HF.
3. Contour and angular orientation of terminals 1 and 2 with respect to hex portion and to each other are optional.
4. Chamfer or undercut on one or both ends of the hexagonal portion are optional.
5. Square or radius on end of terminal is optional.
6. Minimum difference in terminal lengths to establish datum line for numbering terminals.
7. Dimension SD is pitch diameter of coated threads.
8. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
b	.115	.139	2.92	3.53	3
b1	.210	.300	5.33	7.62	3
CD		.543		13.8	2
CH		.550		14.00	
e2	.125		3.17		6
HF	.544	.563	13.8	14.3	
HT	.075	.200	1.9	5.08	4
OAH		1.193		30.3	2
S	.120		3.05		3
SD	¼ - 28 UNF 2A				
SL	.422	.453	10.7	11.5	
SU		.090		2.29	
ΦT	.125	.165	3.17	4.19	
ΦT1	.060	.075	1.52	1.9	
UD	.220	.249	5.59	6.32	

Terminal 1	Gate	
Terminal 2	Cathode	5
Terminal 3	Anode (Stud)	7