AAT3242

PowerLinear™

300mA/150mA Dual CMOS LDO Linear Regulator

General Description

The AAT3242 is a dual low dropout linear regulator with Power OK (POK) outputs. Two integrated regulators provide a high power 300mA output and a lower power 150mA output, making this device ideal for use with microprocessors and DSP cores in portable products. Two POK pins provide open drain output signals when their respective regulator output is within regulation. The AAT3242 has independent input voltage and enable pins for increased design flexibility. This device features a very low quiescent current (140µA typical) and low dropout voltages (typically 200mV and 400mV at the full output current level), making it ideal for portable applications where extended battery life is critical. The AAT3242 has complete over-current/short-circuit and over-temperature protection circuits to guard against extreme operating conditions.

The AAT3242 is available in the space-saving, Pb-free, 12-pin TSOPJW and TDFN33 packages. This device is capable of operation over the -40°C to +85°C temperature range.

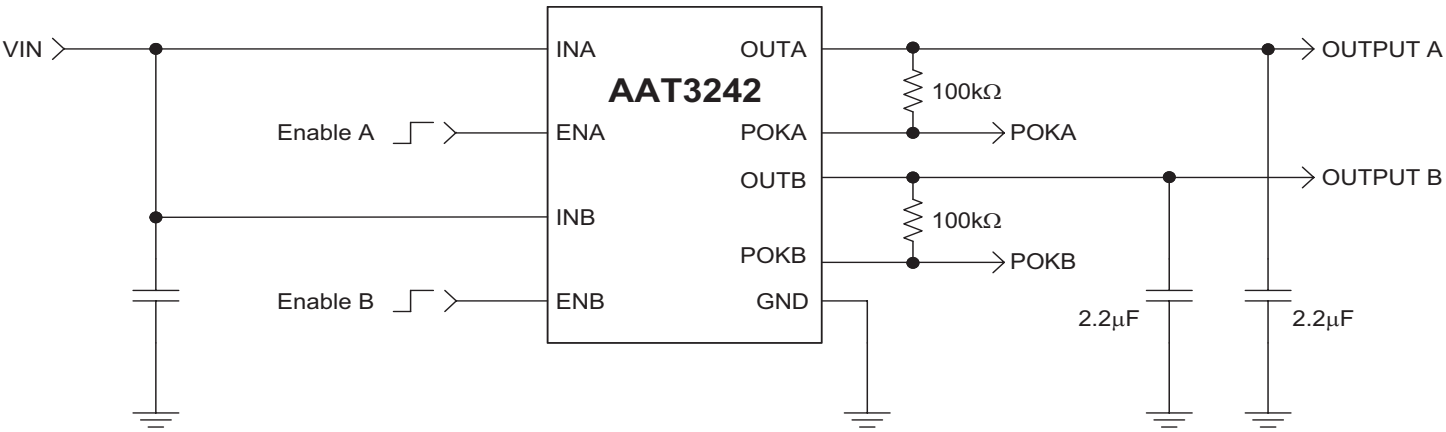
Features

- High/Low Current Outputs, 300mA/150mA
- Low Dropout:
  - LDO A: 400mV at 300mA
  - LDO B: 200mV at 150mA
- High Output Voltage Accuracy: ±1.5%
- High PSRR: 65dB at 1kHz
- 70µA Quiescent Current for Each LDO
- Over-Current/Short-Circuit Protection
- Over-Temperature Protection
- Two POK Outputs
- Independent Power and Enable Inputs
- Uses Low Equivalent Series Resistance (ESR) Ceramic Capacitors
- 12-Pin TSOPJW and TDFN33 Packages
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor / DSP Core / I/O Power
- Notebook Computers
- PDAs and Handheld Computers
- Portable Communication Devices

Typical Application

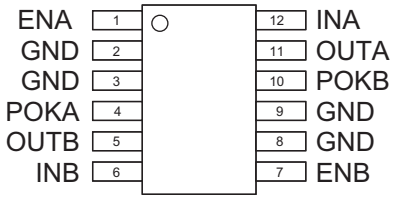


Pin Descriptions

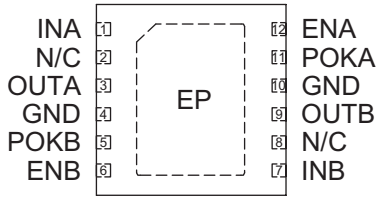
Pin #		Symbol	Function
TSOPJW-12	TDFN33-12		
1	12	ENA	Enable Regulator A pin; this pin should not be left floating. When pulled low, the PMOS pass transistor turns off and the device enters shutdown mode, consuming less than 1µA.
2, 3, 8, 9	4, 10	GND	Ground connection pins. For the TDFN33 package, The exposed thermal pad (EP) should be connected to the board ground plane and Pins 4 and 10. The ground plane should include a large exposed copper pad under the package with vias to the bottom layer ground plane for thermal dissipation (see package outline).
4	11	POKA	Power OK pin with open drain output. It is pulled low when the OUTA pin is below the 10% regulation window.
5	9	OUTB	Low current (150mA) regulator output pin; should be decoupled with a 2.2µF or greater output low-ESR ceramic capacitor.
6	7	INB	Input voltage pin for Regulator B; should be decoupled with 1µF or greater capacitor.
7	6	ENB	Enable Regulator B; this pin should not be left floating. When pulled low, the PMOS pass transistor turns off and the device enters shutdown mode, consuming less than 1µA.
10	5	POKB	Power OK pin with open drain output. It is pulled low when the OUTB pin is below the 10% regulation window.
11	3	OUTA	High-current (300mA) regulator output pin; should be decoupled with a 2.2µF or greater output low-ESR ceramic capacitor.
12	1	INA	Input voltage pin for Regulator A; should be decoupled with 1µF or greater capacitor.
n/a	2, 8	N/C	Not connected.

Pin Configuration

TSOPJW-12
(Top View)



TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Voltage	6.0	V
$V_{ENIN(MAX)}$	Maximum EN to Input Voltage	0.3	
I_{OUT}[2]	DC Output Current	$P_D/(V_{IN} - V_O)$	mA
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

Thermal Information

Symbol	Description		Value	Units
Θ_{JA}	Thermal Resistance[3]	TSOPJW-12	110	°C/W
		TDFN33-12	50	
P_D	Maximum Power Dissipation (T_A = 25°C)	TSOPJW-12[4]	909	mW
		TDFN33-12[5]	2	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
2. Based on long-term current density limitation.
3. Mounted on an FR4 board.
4. Derate 9.1mW/°C above 25°C.
5. Derate 6.25mW/°C above 25°C.

Electrical Characteristics[1]

V_{IN} = $V_{OUT(NOM)}$ + 1.0V for V_{OUT} options greater than 1.5V. V_{IN} = 2.5V for V_{OUT} ≤ 1.5V. I_{OUT} = 1.0mA, C_{OUT} = 2.2µF, C_{IN} = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
LDO A; I_{OUT} = 300mA							
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 300mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40 to 85°C	-2.5		2.5	
V_{IN}	Input Voltage			V_{OUT} + V_{DO}[5]		5.5	V
V_{DO}	Dropout Voltage[2, 3]	I_{OUT} = 300mA			400	600	mV
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation[4]	V_{IN} = V_{OUT} + 1V to 5.0 V				0.09	%/V
$\Delta V_{OUT(Line)}$	Dynamic Line Regulation	I_{OUT} = 300mA, V_{IN} = V_{OUT} + 1 to V_{OUT} + 2, T_R/T_F = 2µs			5.0		mV
$\Delta V_{OUT(Load)}$	Dynamic Load Regulation	I_{OUT} = 1mA to 300mA, T_R < 5µs			60		
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.5			
V_{POK}	Power OK Trip Threshold	V_{OUT} Rising, T_A = 25°C		90	94	98	% of V_{OUT}
V_{POKHYS}	Power OK Hysteresis				1.0		
$V_{POK(LO)}$	Power OK Output Voltage Low	I_{SINK} = 1mA				0.4	V
I_{POK}	POK Output Leakage Current	V_{POK} < 5.5V, V_{OUT} in Regulation				1.0	µA
I_{OUT}	Output Current	V_{OUT} > 1.2V		300			mA
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V			600		
I_Q	Ground Current	V_{IN} = 5V, No Load; EN A = V_{IN}			70	125	µA
I_{SD}	Shutdown Current	V_{IN} = 5V, EN A = 0V				1.0	
PSRR	Power Supply Rejection Ratio	I_{OUT} =10mA	1kHz		65		dB
			10kHz		45		
			1MHz		42		
T_{SD}	Over-Temperature Shutdown Threshold				145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				12		
e_N	Output Noise	e_{NBW} = 300Hz to 50kHz			250		µVRMS
T_C	Output Voltage Temperature Coefficient				22		ppm/°C

1. The AAT3242 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.
3. For V_{OUT} < 2.1V, V_{DO} = 2.5 - V_{OUT}.
4. C_{IN} = 10µF.
5. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)}$ = $V_{OUT(MAX)}$ + $V_{DO(MAX)}$ as long as V_{IN} ≥ 2.5V.

Electrical Characteristics[1] (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1.0V for V_{OUT} options greater than 1.5V. V_{IN} = 2.5V for V_{OUT} ≥ 1.5V. I_{OUT} = 1.0mA, C_{OUT} = 2.2µF, C_{IN} = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

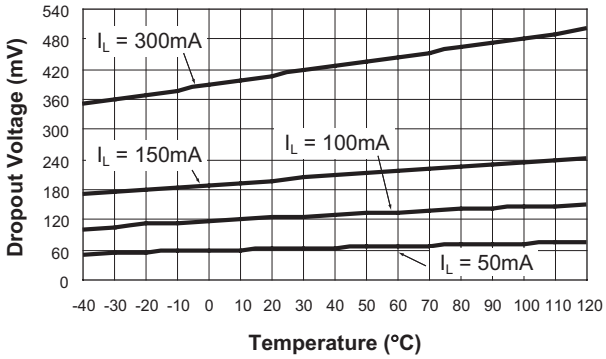
Symbol	Description	Conditions		Min	Typ	Max	Units
LDO B; I_{OUT} = 150mA							
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 150mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40 to 85°C	-2.5		2.5	
V_{IN}	Input Voltage			V_{OUT} + V_{DO}[5]		5.5	V
V_{DO}	Dropout Voltage[2, 3]	I_{OUT} = 150mA			200	300	mV
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation[4]	V_{IN} = V_{OUT} + 1V to 5.0V				0.09	%/V
$\Delta V_{OUT(Line)}$	Dynamic Line Regulation	I_{OUT} = 150mA, V_{IN} = V_{OUT} + 1 to V_{OUT} + 2, T_R/T_F = 2µs			5.0		mV
$\Delta V_{OUT(Load)}$	Dynamic Load Regulation	I_{OUT} = 1mA to 150mA, T_R <5µs			60		
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.5			
V_{POK}	Power OK Trip Threshold	V_{OUT} Rising, T_A = 25°C		90	94	98	% of V_{OUT}
V_{POKHYS}	Power OK Hysteresis				1.0		
$V_{POK(LO)}$	Power OK Output Voltage Low	I_{SINK} = 1mA				0.4	V
I_{POK}	POK Output Leakage Current	V_{POK} < 5.5V, V_{OUT} in Regulation				1.0	µA
I_{OUT}	Output Current	V_{OUT} > 1.2V		150			mA
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V			600		
I_Q	Ground Current	V_{IN} = 5V, No Load; EN B = V_{IN}			70	125	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA	1kHz		65		dB
			10kHz		45		
			1MHz		42		
T_{SD}	Over-Temperature Shutdown Threshold				145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				12		
e_N	Output Noise	e_{NBW} = 300Hz to 50kHz			250		µVRMS
T_C	Output Voltage Temperature Coefficient				22		ppm/°C

1. The AAT3242 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.
3. For V_{OUT} < 2.3V, V_{DO} = 2.5 - V_{OUT}.
4. C_{IN} = 10µF.
5. To calculate minimum input voltage, use the following equation: $V_{IN(MIN)}$ = $V_{OUT(MAX)}$ + $V_{DO(MAX)}$ as long as V_{IN} ≥ 2.5V.

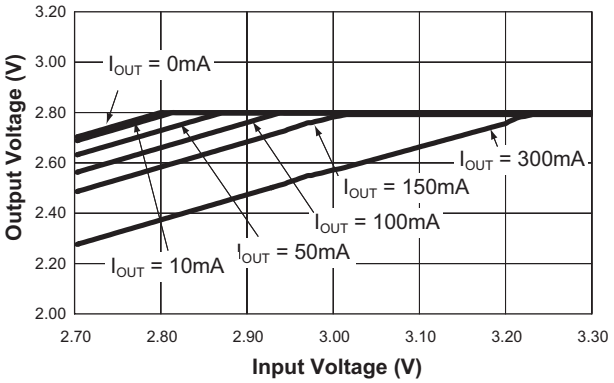
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

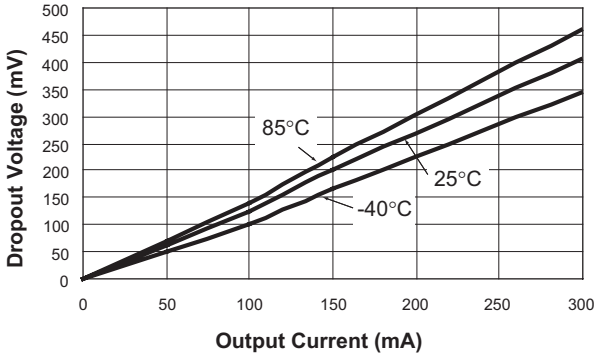
Dropout Voltage vs. Temperature



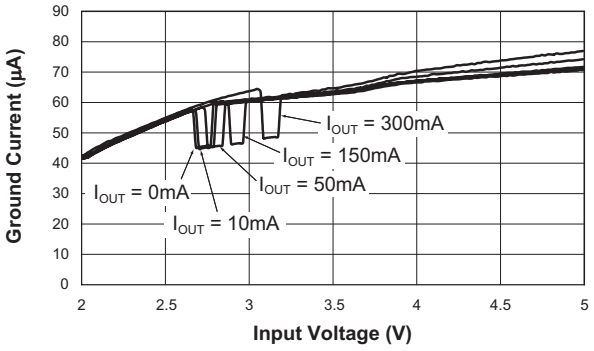
Dropout Characteristics



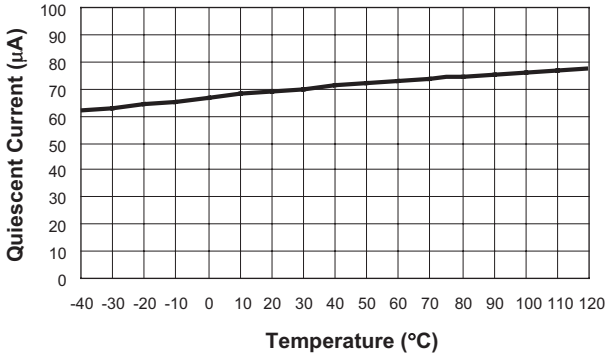
Dropout Voltage vs. Output Current



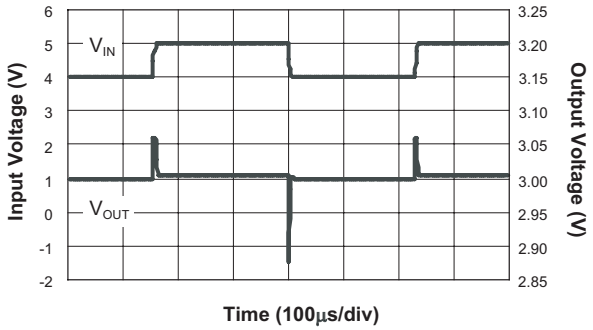
Ground Current vs. Input Voltage



Quiescent Current vs. Temperature



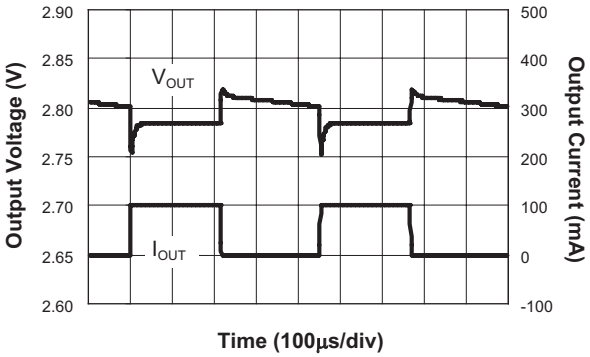
Line Transient Response



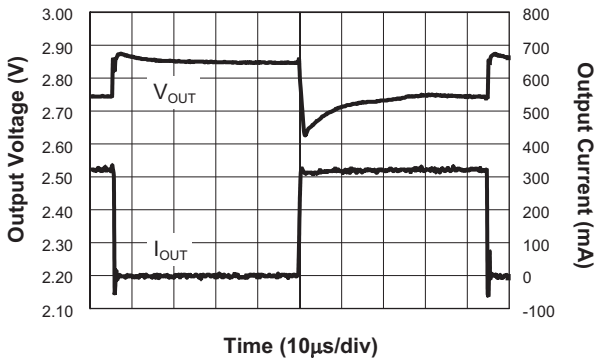
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

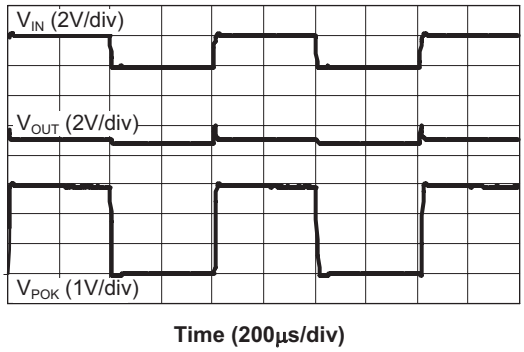
Load Transient Response



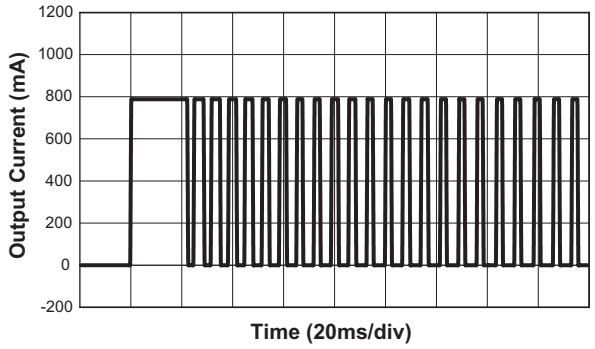
Load Transient Response 300mA



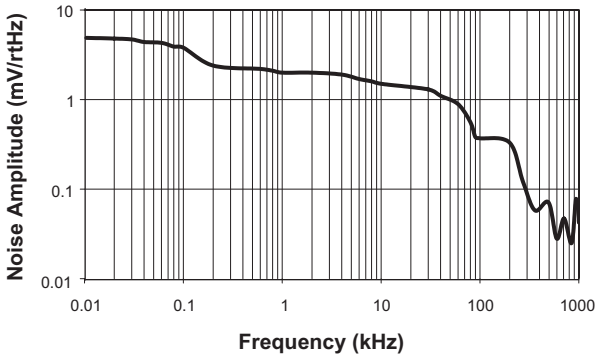
POK Output Response



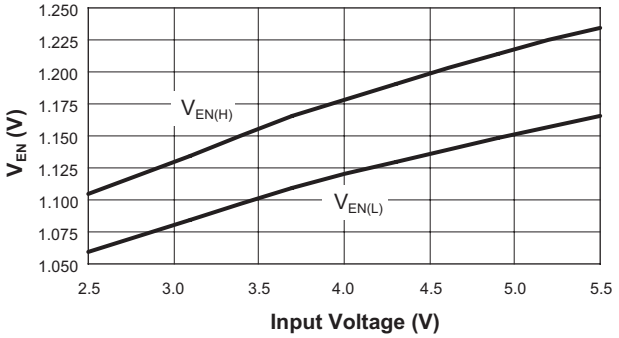
Over-Current Protection



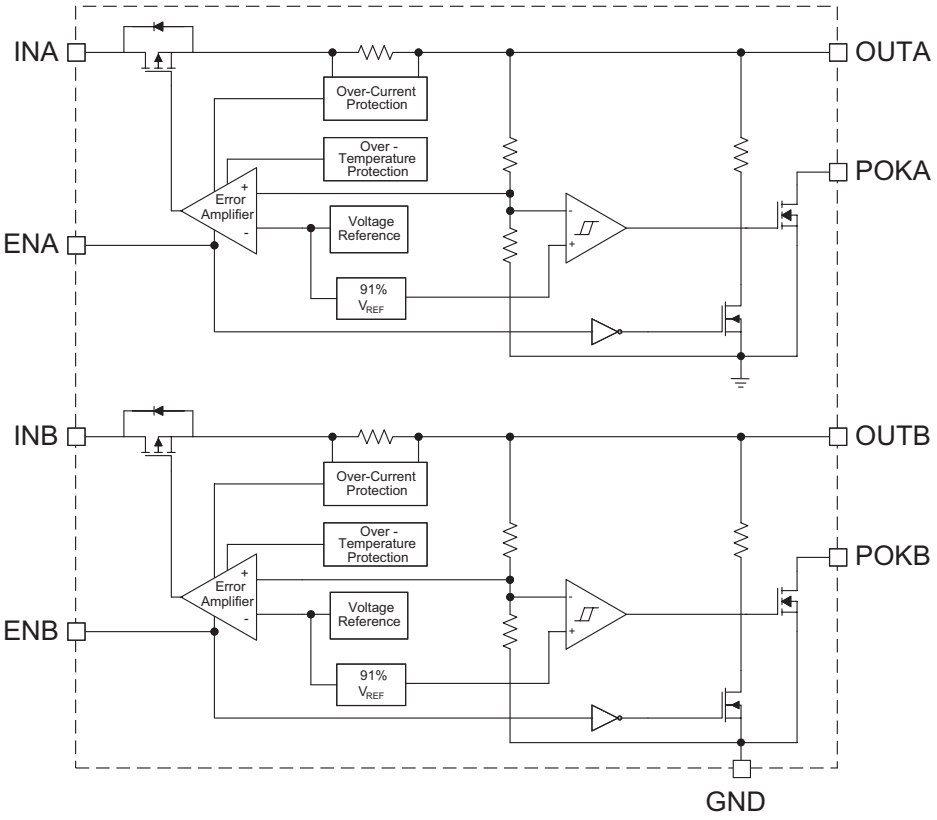
Self Noise



$V_{EN(H)}$ and $V_{EN(L)}$ vs. V_{IN}



Functional Block Diagram



Functional Description

The AAT3242 is a high performance dual LDO regulator with two Power OK pins. The first regulator (A) sources 300mA of current, while the second (B) regulator can deliver 150mA. Each regulator has an integrated Power OK comparator which indicates when the respective output is out of regulation. The POK pins are open drain outputs, and they are held low when the respective regulator is in shutdown mode.

The device has independent enable pins to shut down each LDO regulator for power conservation in portable products. Forcing EN A/B low (<0.6V) powers down the regulators and draws a maximum of 1.0µA. The AAT3242 has short-circuit and thermal protection in case of adverse operating conditions. Device power dissipation is limited to the package type and thermal dissipation properties. Refer to the Thermal Considerations section of this datasheet for details on device operation at maximum output current loads.

Applications Information

To assure the maximum possible performance is obtained from the AAT3242, please refer to the following application recommendations.

Input Capacitor

A 1µF or larger capacitor is typically recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation; however, if the AAT3242 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device V_{IN} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}; however, for 300mA LDO regu-

lator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance. The AAT3242 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF.

Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT3242 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT3242. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance

ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials

Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%. Capacitor area is another contributor to ESR. Capacitors which are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size. Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

POK Output

The AAT3242 features integrated Power OK comparators which can be used as an error flag. The POK open drain output goes low when output voltage is 6% (typ) below its nominal regulation voltage. Additionally, any time one of the regulators is in shutdown, the respective POK output is pulled low. Connect a pull-up resistor from POKA to OUTA, and POKB to OUTB.

Enable Function

The AAT3242 features an LDO regulator enable/disable function. Each LDO has its own dedicated enable pin. These pins (EN) are active high and are compatible with CMOS logic. To assure the LDO regulators will switch on, ENA/B must be greater than 1.6V. The LDO regulators will shut down when the voltage on the ENA/B pins falls below 0.6V. In shutdown, the AAT3242 will consume less than 1.0µA of current. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulators are in shutdown mode, an internal 20Ω resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulators are disabled. The internal 20Ω has no adverse effects on device turn-on time.

Short-Circuit Protection

The AAT3242 contains internal short-circuit protection that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

Thermal Protection

The AAT3242 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 145°C. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 145°C trip point. The combination and interaction between the short-circuit and thermal protection systems allows the LDO regulators to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT3242 is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator. In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

Thermal Considerations and High Output Current Applications

The AAT3242 is designed to deliver continuous output load currents of 300mA and 150mA under normal operations, and can supply up to 500mA during circuit start-up conditions. This is desirable for circuit applications where there might be a brief high in-rush current during a power-on event.

The limiting characteristic for the maximum output load current safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account.

The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the layout considerations section of this document. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}}$$

Constants for the AAT3242 are $T_{J(MAX)}$ (the maximum junction temperature for the device, which is 125°C) and Θ_{JA} = 110°C/W (the package thermal resistance). Typically, maximum conditions are calculated at the maximum operating temperature of T_A = 85°C and under normal ambient conditions where T_A = 25°C. Given T_A = 85°C, the maximum package power dissipation is 364mW. At T_A = 25°C, the maximum package power dissipation is 909mW.

The maximum continuous output current for the AAT3242 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator. To determine the maximum output current for a given output voltage, refer to the following equation. This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{D(MAX)} = [(V_{IN} - V_{OUTA}) \cdot I_{OUTA} + V_{IN} \cdot I_{GND}] + [(V_{IN} - V_{OUTB}) \cdot I_{OUTB} + V_{IN} \cdot I_{GND}]$$

This formula can be solved for I_{OUTA} to determine the

maximum output current for LDOA:

$$I_{OUTA(MAX)} = \frac{P_{D(MAX)} - 2V_{IN} \cdot I_{GND} - (V_{IN} - V_{OUTB}) \cdot I_{OUTB}}{V_{IN} - V_{OUTA}}$$

The following is an example for a 2.5V output in the TSOPJW package:

V_{OUTA} = 2.5V

V_{OUTB} = 1.5V

I_{OUTB} = 150mA

V_{IN} = 4.2V

I_{GND} = 125µA

$$I_{OUTA(MAX)} = \frac{909mW - (2 \cdot 4.2V \cdot 125\mu A) - (4.2 - 1.5) \cdot 150mA}{4.2 - 2.5}$$

$I_{OUTA(MAX)}$ = 296mA

From the discussion above, $P_{D(MAX)}$ was determined to equal 909mW at T_A = 25°C.

Therefore, with Regulator B delivering 150mA at 1.5V, Regulator A can sustain a constant 2.5V output at a 296mA load current at an ambient temperature of 25°C. Higher input-to-output voltage differentials can be obtained with the AAT3242, while maintaining device functions within the thermal safe operating area. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the LDO regulator in a duty-cycled mode.

For example, an application requires V_{IN} = 4.2V while V_{OUT} = 1.5V at a 500mA load and T_A = 25°C. To maintain this high input voltage and output current level, the LDO regulator must be operated in a duty-cycled mode. Refer to the following calculation for duty-cycle operation:

I_{GND} = 125µA

I_{OUT} = 500mA

V_{IN} = 4.2V

V_{OUT} = 1.5V

$$\%DC = \frac{P_{D(MAX)}}{[(V_{IN} - V_{OUTA}) \cdot I_{OUTA} + V_{IN} \cdot I_{GND}] + [(V_{IN} - V_{OUTB}) \cdot I_{OUTB} + V_{IN} \cdot I_{GND}]}$$

$$\%DC = \frac{909mW}{[(4.2V - 1.5V) \cdot 500mA + 4.2V \cdot 125\mu A] + [(4.2V - 1.5V) \cdot 200mA + 4.2V \cdot 125\mu A]}$$

%DC = 48.10%

$P_{D(MAX)}$ is assumed to be 909mW.

For a 500mA output current and a 2.7V drop across the AAT3242 at an ambient temperature of 25°C, the maximum on-time duty cycle for the device would be 48.10%.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	LDO A	LDO B		
TSOPJW-12	3.3V	2.5V	LSXYY	AAT3242ITP-WN-T1
	3.3V	1.8V	PAXYY	**AAT3242ITP-WI-T1**
	3.0V	2.85V	LPXYY	**AAT3242ITP-TR-T1**
	3.0V	2.5V	LJXYY	**AAT3242ITP-TN-T1**
	3.0V	1.8V	LHXYY	**AAT3242ITP-TI-T1**
	3.0V	1.5V	NTXYY	**AAT3242ITP-TG-T1**
	2.9V	1.5V	MOXYY	**AAT3242ITP-SG-T1**
	2.8V	3.0V	LVXYY	**AAT3242ITP-QT-T1**
	2.8V	2.8V	LDXYY	**AAT3242ITP-QQ-T1**
	2.8V	2.6V	LQXYY	**AAT3242ITP-QO-T1**
	2.8V	2.5V	LLXYY	**AAT3242ITP-QN-T1**
	2.8V	1.9V	LRXYY	**AAT3242ITP-QY-T1**
	2.8V	1.5V	MCXYY	**AAT3242ITP-QG-T1**
	1.8V	2.5V	SGXYY	**AAT3242ITP-IN-T1**
	1.8V	2.7V	PZXYY	**AAT3242ITP-IP-T1**
TDFN33-12	1.8V	2.8V	5ZXYY	**AAT3242IWP-IQ-T1**

Pb-free

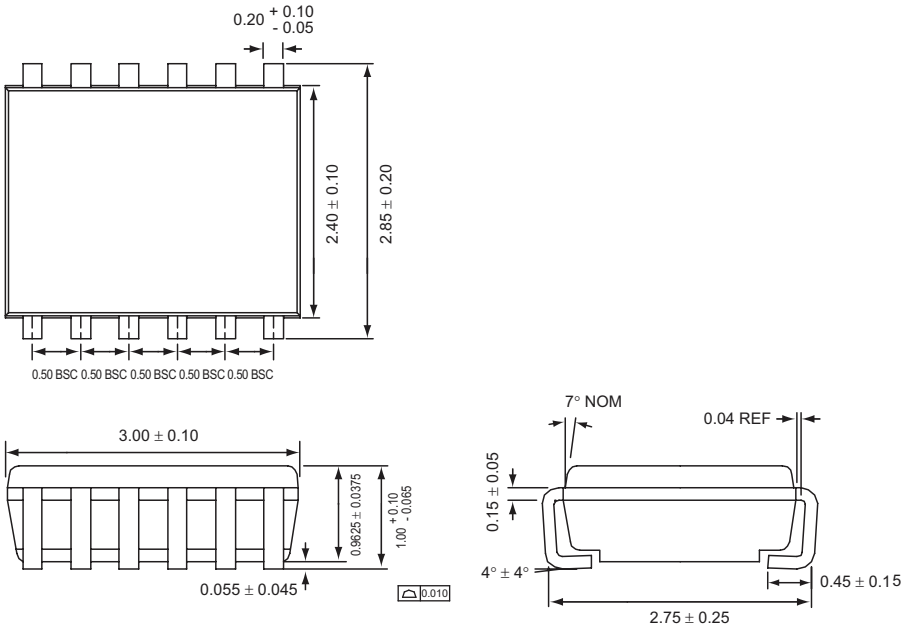
All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/aboutus/quality.php.

Legend	
Voltage	Code
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

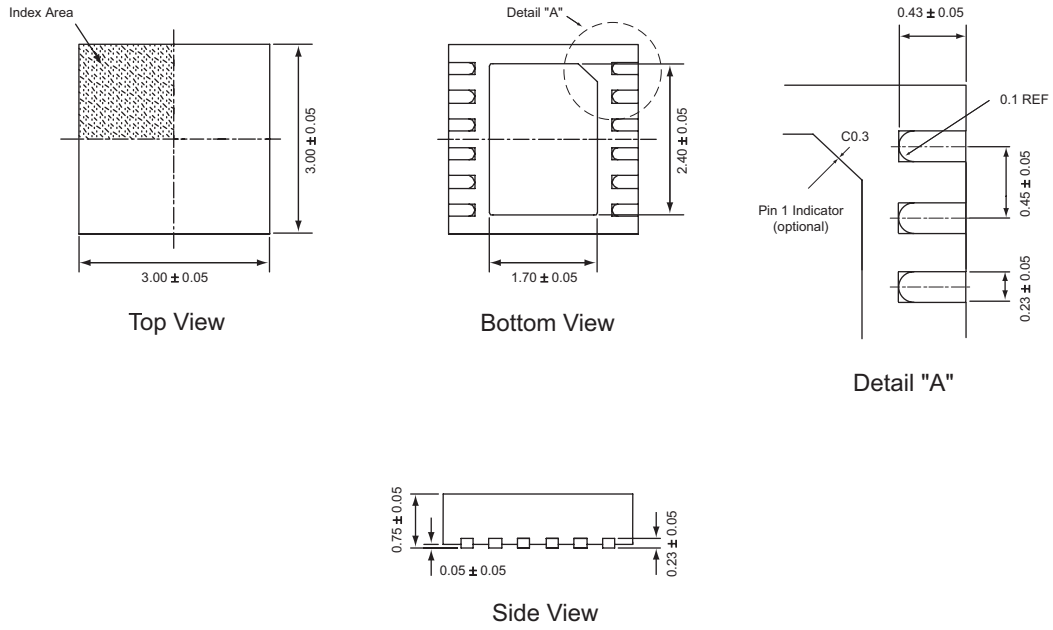
Package Information

TSOPJW-12



All dimensions in millimeters.

TDFN33-12



1. The leadless package family, which includes QFN, TQFN, DFN, TDFN, and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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