

**DESCRIPTION**

The PD70100AA and PD70200 devices are part of Microsemi's™ series of Power over Ethernet (PoE) Powered Devices chips (PD). The PD70100AA and PD70200 devices transmit integrated power and analog data in a single 12-pin package. They are used in Powered Devices (PD), thus enabling next generation network devices to share power and data over the same cable.

Microsemi's new PD family offers a solution to any PD application compliant with IEEE802.3af and IEEE802.3at standards and 4-pairs extra power applications. The IC family's components can be used in both indoor and outdoor applications.

The device family meets all PD-side-standards such as:

- Detection
- Classification

- Integrated isolation switch with inrush current limiter, and over-current protection.
- Two-events classification recognition and AT flag generation (PD70200 only).

In addition, the devices have a discharge mechanism for a DC/DC input capacitor, ensuring quick redetection capability in case the RJ-45 plug is disconnected and reconnected within a short time span.

PD70200 IC design specifically supports IEEE802.3at standard, including two-events classification detection that enables the PD to distinguish whether the connected power source equipment (PSE) is IEEE802.3at or IEEE802.3af based.

The PD70100AA/PD70200 ICs are designed to support 4-pair applications for PDs that require higher power.

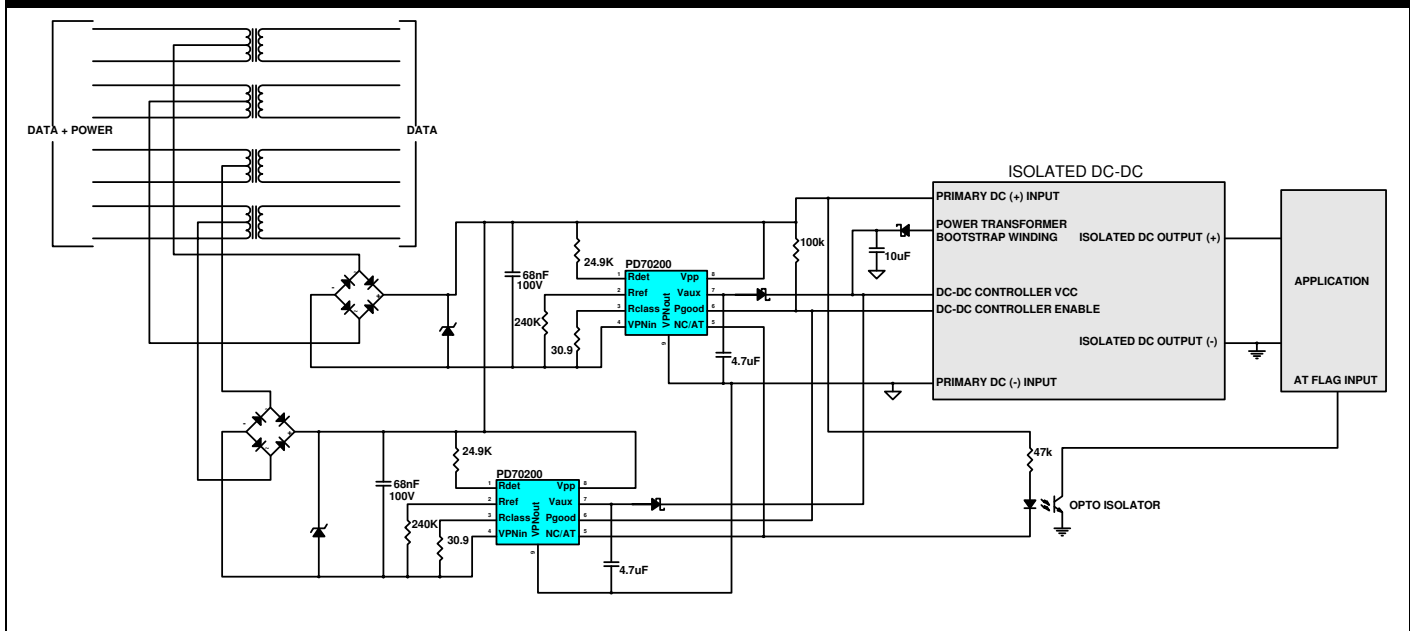
**KEY FEATURES**

- Designed to Support IEEE802.3af and IEEE802.3at standards
- PD Detection & Programmable Classification Signature
- Two-events Classification Flag
- Signature Resistor Disconnection after Detection
- Integrated 0.6Ω Isolating Switch and Inrush Current Limiter.
- 4-pairs support with a single IC for up to 48W
- 4-pairs support with two ICs for up to 96W
- Less than 10μA Offset Current during Detection
- Single DC Voltage Input (37V-57V)
- Wide Operating Temperature Range: -40° to +85°C
- On-chip Thermal Protection
- 12-pin 3x4mm Package
- RoHS Compliant

**APPLICATIONS**

- Power over Ethernet Powered Devices
- IEEE802.3af & at 10/100/1000 BASE-T
- 4-pair Extra Power Applications
- Indoor as Well as Outdoor Applications

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

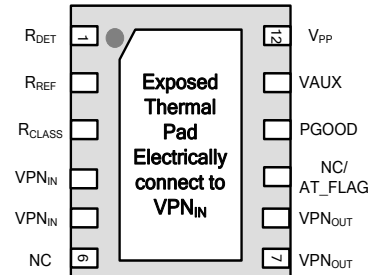
**TYPICAL APPLICATION**


**ABSOLUTE MAXIMUM RATINGS**

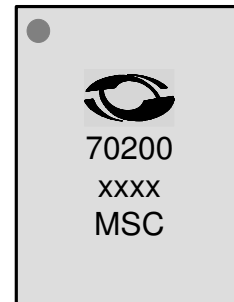
Supply Input Voltage ( $V_{PP}$ ) .....	-0.3V to 74 V <sub>DC</sub>
Port Negative Out Voltage ( $VPN_{OUT}$ ) .....	-0.3V to 74 V <sub>DC</sub>
$R_{DET}$ .....	-0.3V to 74 V <sub>DC</sub>
$R_{CLASS}$ , $R_{REF}$ .....	-0.3V to 5 V <sub>DC</sub>
VAUX .....	-0.3V to 30 V <sub>DC</sub>
PGOOD, AT_FLAG (with respect to $VPN_{OUT}$ ) .....	-0.3V to 74 V <sub>DC</sub>
ESD Protection* .....	±1.5kV HBM
Maximum Operating Junction Temperature .....	150°C
Operating Ambient Temperature .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 150°C
Peak Package Solder Reflow Temp (40 seconds max exposure) .....	260°C

\*All pins except pin 11 (VAUX). Pin 11 ESD Protection ±150V HBM.

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to  $VPN_{IN}$ . Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

**PACKAGE PIN OUT**


**DFN PACKAGE**  
(Top View)



**DFN PACKAGE MARKINGS**

"xxxx" Denote Date Code and Lot Identification

RoHS / Pb-free 100% matte Tin Pin Finish

**PACKAGE ORDER INFO**
**THERMAL DATA**

$T_A$ (°C)	12 Pins DFN 4x3	40 °C/W THERMAL RESISTANCE-JUNCTION TO AMBIENT
	RoHS Compliant / Pb-free	4 °C/W THERMAL RESISTANCE-JUNCTION TO CASE
-40 to 85	<b>PD70100AAILD (IEEE802.3af)</b>	Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$ . The $\theta_{JA}$ numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.
	<b>PD70200ILD (IEEE802.3at)</b>	
Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. PD70200ILD-TR)		

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, the following specifications apply over the operating ambient temperature  $-40^{\circ}\text{C} \leq T_{\text{AMB}} \leq 85^{\circ}\text{C}$ . Production tests are done at  $25^{\circ}\text{C} T_{\text{A}}$ .

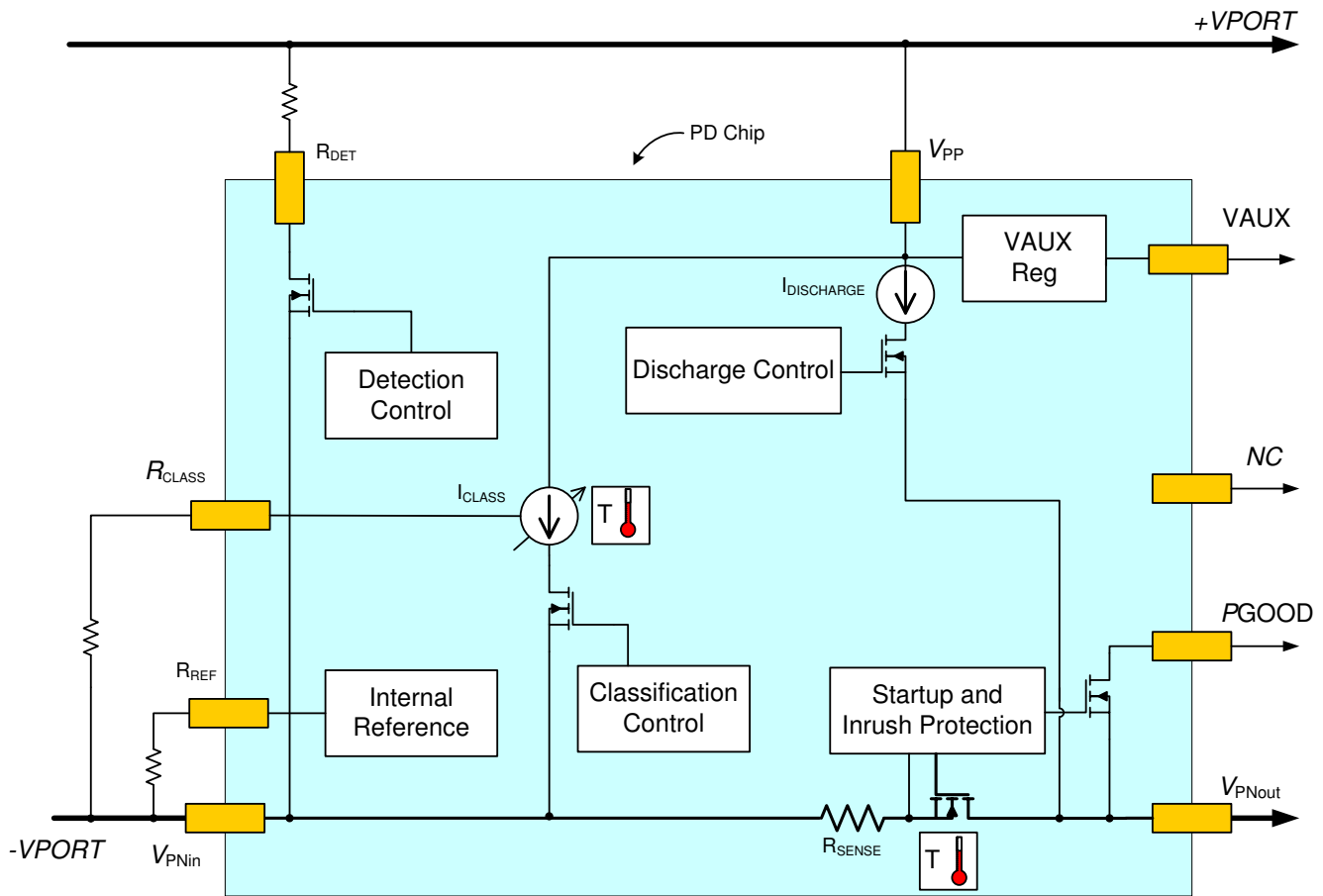
Parameter	Symbol	Test Conditions / Comment	PD70100A/PD70200			Units
			Min	Typ	Max	
<b>Power Supply</b>						
Input Voltage	$V_{\text{PP}}$	Supports Full IEEE802.3 af/at functionality	0	55	57	V
Power Supply Current at Operating Mode		$V_{\text{PP}} = 55\text{V}$		1	3	mA
<b>DETECTION MODE</b>						
Detection is connected. At this voltage range $R_{\text{DET}}$ must be on.	$\text{DET}_{\text{RANGE}}$	Measured between $V_{\text{PP}}$ and $\text{VPN}_{\text{IN}}$	1.3		10.1	V
Detection Switch ON Resistance PD-detection	$R_{\text{DET-on}}$	$2.5\text{V} \leq (\Delta V_{\text{PP}} \text{ to } \text{VPN}_{\text{IN}}) \leq 10.1\text{V}$ Measured between $R_{\text{DET}}$ and $\text{VPN}_{\text{IN}}$			50	$\Omega$
Detection is Disconnected	$R_{\text{DET-off}}$	Measured between $V_{\text{PP}}$ and $\text{VPN}_{\text{IN}}$	10.1		12.8	V
Detection Switch OFF Resistance	$R_{\text{DET-off}}$	$12.8\text{V} \leq (\Delta V_{\text{PP}} \text{ to } \text{VPN}_{\text{IN}}) \leq 57.0\text{V}$ Measured between $R_{\text{DET}}$ and $\text{VPN}_{\text{IN}}$	2.0			$\text{M}\Omega$
Input Offset Current	$I_{\text{OFFSET}}$	1.1V to 10.1V $-40^{\circ}\text{C} \leq T_{\text{J}} \leq 85^{\circ}\text{C}$			16	$\mu\text{A}$
	$I_{\text{OFFSET}}$	1.1V to 10.1V $-40^{\circ}\text{C} \leq T_{\text{J}} \leq 55^{\circ}\text{C}$			10	$\mu\text{A}$
$R_{\text{DET}}$ Reconnection Level, $V_{\text{PP}}$ Falling	$V_{\text{RDET-on}}$	Measured between $V_{\text{PP}}$ and $\text{VPN}_{\text{IN}}$	1.95	3.0	4.85	V
<b>CLASSIFICATION MODE</b>						
Classification Current Source, Turn ON Threshold Range Measured at $V_{\text{PP}}$	$V_{\text{TH-low-on}}$	Turn on for any $I_{\text{CLASS}}$ while $V_{\text{PP}}$ increases	11.4		13.7	V
Classification Disconnection Minimum Hysteresis Voltage.	$V_{\text{HST}}$	Hysteresis between $V_{\text{TH-low-on}}$ and $V_{\text{TH-low-off}}$		1		V
Classification Current Source, Turn OFF Threshold Range Measured at $V_{\text{PP}}$	$V_{\text{TH-high-off}}$	Turn off while $V_{\text{PP}}$ increases	20.9		23.9	V
Current Limit Threshold	$I_{\text{CLASS-LIM}}$		50.0	68	80.0	mA
Input Current $I_{\text{PP}}$ When Classification Function is Disabled	$I_{\text{CLASS-DIS}}$	Class 0 $R_{\text{CLASS}} = \text{Disconnect}$			3.0	mA
Input Current $I_{\text{PP}}$ When Classification Function is Enabled	$I_{\text{CLASS-EN}}$	Class 1 $R_{\text{CLASS}} = 133\Omega \pm 1\%$	9.50	10.5	11.5	mA
		Class 2 $R_{\text{CLASS}} = 69.8\Omega \pm 1\%$	17.5	18.5	19.5	mA
		Class 3 $R_{\text{CLASS}} = 45.3\Omega \pm 1\%$	26.5	28.0	29.5	mA
		Class 4 $R_{\text{CLASS}} = 30.9\Omega \pm 1\%$	38.0	40.0	42.0	mA



MARK						
Mark, Working Voltage Range	$V_{MARK}$	When voltage decreases Measured between $V_{PP}$ to $VPN_{IN}$	4.9		10.1	V
Mark Current	$I_{MARK}$	Chip current	0.25		4	mA
ISOLATION SWITCH						
Isolation Switch MOSFET Switches from Off to $I_{LIM-LOW}$	$V_{SW-START}$		36			V
Isolation Switch MOSFET Switched Off	$V_{SW-OFF}$		30.5		34.5	V
Startup Current Limit, $I_{LIM}$	$I_{LIM-LOW}$		105	240	325	mA
$VPN_{IN}$ to $VPN_{OUT}$ Threshold Voltage for $I_{LIM-LOW}$ to $I_{LIM-HIGH}$ Switchover	$V_{DIFF}$	When $VPN_{IN}$ to $VPN_{OUT} \leq V_{DIFF}$ , Isolating switch switches over from $I_{LIM-LOW}$ to $I_{LIM-HIGH}$ .			0.7	V
Over Current Protection Current Limit	OCP		1500	1800	2000	mA
Continuous Operation Load Current	$I_{LOAD}$	Isolating switch at $I_{LIM-HIGH}$ PD70100A PD70200		350 600	450 1123	mA mA
Continuous Operation Total $RDS_{ON}$	SW- $RDS_{ON}$	Total resistance between $VPN_{IN}$ and $VPN_{OUT}$ Isolating switch at $I_{LIM-HIGH}$			0.6	$\Omega$
DC/DC CAPACITOR DISCHARGER						
DC/DC Input Capacitance		For reference only Guaranteed by design (not tested on production)		220		$\mu F$
Discharge Current.		$7.0V \leq V_{PP}$ to $VPN_{OUT} \leq 30V$	22.8	32	50	mA
Full Discharge Time for Full Discharge of Input Capacitance	$T_{DSC}$	$V_{PP} < UVLO$ threshold Guaranteed by design (not tested in production)			500	ms
AT_FLAG						
Output Low Voltage		$I_{OL} = 0.75mA$			0.4	V
		$I_{OL} MAX = 5mA$			2.5	V
Leakage Current		$V_{ATFLAG} = 57V$			1	$\mu A$
PGOOD						
Output Low Voltage		$I_{OL} = 0.75mA$			0.4	V
		$I_{OL} MAX = 5mA$			2.5	V
Leakage Current		$V_{PGOOD} = 57V$			1	$\mu A$



THERMAL SHUTDOWN						
Thermal Shutdown Temperature			180	200	220	°C
<b>VAUX</b>						
		Reference to VP <sub>N</sub> OUT				
VAUX Output Voltage Off (leakage current)	VAUX-off	PGOOD = High impedance Load = 1MΩ			1	V
VAUX Output Voltage On	VAUX-on	Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low	9.5	10.5	11.8	V
Output Current Peak	I <sub>VAUXP</sub>	Capacitor = 30uF When T <sub>LOAD</sub> ≤ 5mS Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low	0		10	mA
Output Continuous Current	I <sub>VAUXC</sub>	When T <sub>LOAD</sub> ≤ 10mS Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low	0		2	mA
VAUX Output Current Limit	I <sub>VAUX</sub>	Isolating switch at I <sub>LIM-HIGH</sub> and PGOOD = Low	10		32	mA

**PD70100A Functional Block Diagram**

**Figure 1: PD70100A Functional Block Diagram**

## PD70200 Functional Block Diagram

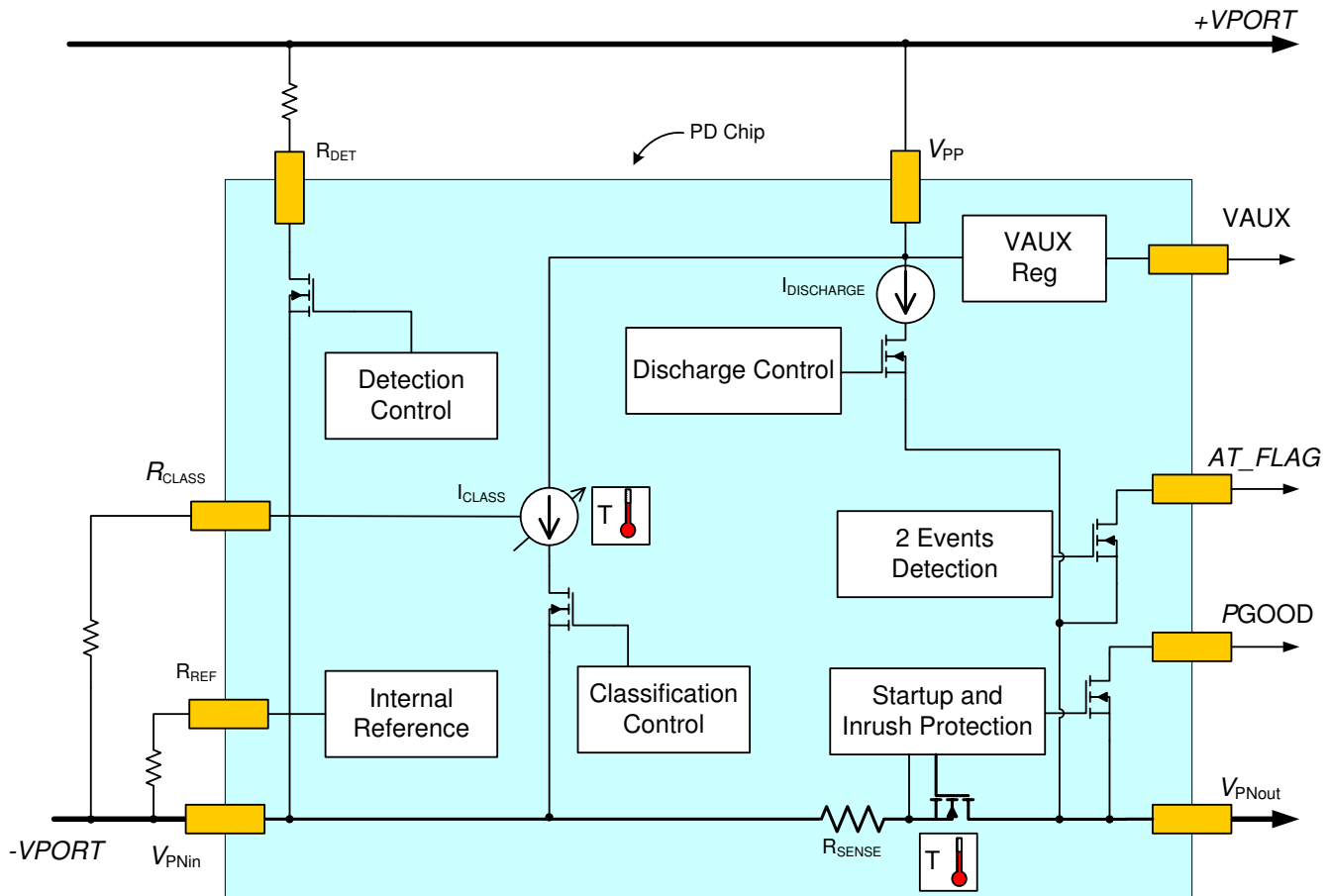


Figure 2: PD70200 Functional Block Diagram

**FUNCTIONAL PIN DESCRIPTION**

Pin	PD70100A Pin Name	PD70200 Pin Name	Type	Description
1	R <sub>DET</sub>	R <sub>DET</sub>		Valid Detection resistor. Connect external 24.9KΩ detection resistor between RDET and VPP
2	R <sub>REF</sub>	R <sub>REF</sub>		Bias current resistor
3	R <sub>CLASS</sub>	R <sub>CLASS</sub>		Power classification setting. Connect external class resistor between RCLASS and VPN <sub>IN</sub>
4	VPN <sub>IN</sub>	VPN <sub>IN</sub>	Power	VPort Negative input. Connected to the isolating SW input. N-channel MOSFET source. The exposed thermal PAD should be connect to these pins.
5				
6	N.C	N.C		
7	VPN <sub>OUT</sub>	VPN <sub>OUT</sub>	Power/Gnd	Vport Negative output. Connected to the isolating SW output. N-channel MOSFET Drain. Primary side Ground.
8				A decent ground plane should be deployed around this pin whenever is possible
9	N.C	AT_FLAG	Open drain	The two-event detector should discern between AF and AT classification waveforms and outputs the AT_FLAG
10	PGOOD	PGOOD	Open drain	After startup a PGOOD flag is generated in order to optionally inform the application DC/DC converter that the power rails are ready.
11	VAUX	VAUX	Power	Auxiliary output voltage to VPN <sub>OUT</sub> . Can be used for DC-DC startup for bootstrap initiation.
12	VPP	VPP	Power	High voltage positive input, Reference to VPN <sub>IN</sub> And High voltage positive out, Reference to VPN <sub>OUT</sub> (used for discharge as well)
EP	EPAD	EPAD		Connect to VPN <sub>IN</sub> . EPAD should be connected to a large copper area for improved thermal management.

**THEORY OF OPERATION****DETAIL DESCRIPTION**

PD70100A/PD70200 IC provides IEEE 802.3af/at compliant PD Front-End functions including Detection, Physical Layer Classification, Two-Events Classification (PD70200 only), Auxiliary Voltage Output, Power Good, Soft-Start Current Limiting, Over-Current Protection, and Bulk Capacitor Discharge.

**DETECTION**

IEEE 802.3af/at compliant detection is provided by means of a 24.9K $\Omega$  resistor connected between  $V_{PP}$  and  $R_{DET}$  pin.  $R_{DET}$  pin is connected to  $VPN_{IN}$  via an open drain MOSFET with a maximum specified  $R_{DS_{ON}}$  of 50 $\Omega$ . Internal logic monitors  $V_{PP}$  to  $VPN_{IN}$  and connects the  $R_{DET}$  pin to  $VPN_{IN}$  when the rising  $V_{PP}$  to  $VPN_{IN}$  voltage is between 2.5V and 10.1V. When rising  $V_{PP}$  to  $VPN_{IN}$  voltage exceeds 10.1V, the MOSFET is switched off. Once above 10.1V, falling  $V_{PP}$  to  $VPN_{IN}$  voltage between 2.45V and 4.85V will reconnect  $R_{DET}$  pin to  $VPN_{IN}$ .

**PHYSICAL LAYER CLASSIFICATION**

Physical Layer (hardware) Classification per IEEE 802.3af/at is generated via a regulated reference voltage of 1.2V, switched onto the  $R_{CLASS}$  pin. Internal logic monitors the  $V_{PP}$  to  $VPN_{IN}$  voltage and connects the 1.2V reference to  $R_{CLASS}$  pin at a rising  $V_{PP}$  to  $VPN_{IN}$  voltage threshold between 11.1V and 13.5V. Once  $V_{PP}$  to  $VPN_{IN}$  has exceeded the rising threshold, there is a 1V minimum hysteresis between the  $V_{PP}$  rising (turn-on) threshold and the  $V_{PP}$  falling (turn-off) threshold.

The 1.2V reference stays connected to the  $R_{CLASS}$  pin until the  $V_{PP}$  to  $VPN_{IN}$  rising voltage exceeds the upper turn-off threshold of 20.9V to 23.9V. The 1.2V reference voltage is disconnected from the  $R_{CLASS}$  pin at  $V_{PP}$  to  $VPN_{IN}$  voltages above the upper threshold.

Classification current signature is provided via a resistor connected between  $R_{CLASS}$  pin and  $VPN_{IN}$ . The classification current is therefore the current drawn by the PD70100A/PD70200 IC during the classification phase, and is simply the 1.2V reference voltage divided by the  $R_{CLASS}$  resistor value. The maximum current available at the  $R_{CLASS}$  pin is current limited to 55mA (typical).

**TWO-EVENTS DETECTION AND AT FLAG**

The PD70200 IC provides IEEE 802.3at Type 2 compliant detection of the “Two Events Classification Signature”, and generation of the AT flag. This feature is available on the PD70200 IC only.

Simply put, the “Two Events Classification Signature” is a means by which an IEEE 802.3at Type 2 Power Source can inform a compliant Power Device (PD) that it is AT Type 2 compliant, and as such is capable of providing AT Type 2 power levels.

The Power Source communicates with a Type 2 compliant signature by toggling the  $V_{PP}$  to  $VPN_{IN}$  voltage twice (2 “events”) during the Physical Layer Classification phase. The  $V_{PP}$  to  $VPN_{IN}$  voltage is toggled from the Physical Layer Classification’s voltage level (13.5V to 20.9V) down to a voltage “Mark” level. Voltage “Mark” level is specified as a  $V_{PP}$  to  $VPN_{IN}$  voltage of 4.9V to 10.1V.

PD70200 IC recognizes a  $V_{PP}$  to  $VPN_{IN}$  falling edge from Classification level to Mark level as being one event of the Two-Events Signature. If two such falling edges are detected, PD70200 will assert AT flag by means of an open drain MOSFET connected between  $AT\_FLAG$  pin and  $VPN_{OUT}$ .

$AT\_FLAG$  pin is active low; a low impedance state between  $AT\_FLAG$  and  $VPN_{OUT}$  indicates a valid Two-Events Classification Signature was received, and the Power Source is AT Type 2 compliant.

$AT\_FLAG$  MOSFET is capable of 5mA of current and can be pulled up to  $V_{PP}$ .

**SOFT START AND INRUSH CURRENT PROTECTION**

PD70100A/PD70200 IC contains an internal isolation switch, that provides ground isolation between Power Source and PD application during Detection and Classification phases. The isolation switch is a N-channel MOSFET, wired in a common source configuration where the MOSFET’s Source is connected to Power Source ground at  $VPN_{IN}$ , and the MOSFET’s Drain is connected to application’s primary ground at  $VPN_{OUT}$ .

### THEORY OF OPERATION

Internal logic monitors  $V_{PP}$  to  $VPN_{IN}$  voltage and keeps the MOSFET in a high impedance state until  $V_{PP}$  to  $VPN_{IN}$  voltage reaches turn-on threshold of 36V to 42V. Once  $V_{PP}$  to  $VPN_{IN}$  voltage exceeds this threshold, the MOSFET is switched into one of two modes.

The mode into which the MOSFET is switched is determined by the voltage developed across the MOSFET, or put another way, the  $VPN_{OUT}$  to  $VPN_{IN}$  differential voltage. Two modes are defined below:

Isolation Switch Modes		
$VPN_{OUT}$ to $VPN_{IN}$	Mode	Description
$> 0.7V$	Soft Start Mode	Limits $VPN_{OUT}$ current to 240mA (typical)
$\leq 0.7V$	Normal Operating Mode	Limits $VPN_{OUT}$ current to 1.8A (typical)

By controlling the MOSFET current based on  $VPN_{OUT}$  to  $VPN_{IN}$  voltage, inrush currents generated by fully discharged bulk capacitors can be limited. This method limits current to a maximum of 350mA, compliant with IEEE 802.3af/at specification.

Soft Start current limiting is required to reduce occurrences of voltage sag at the PD input during device power-up. A comparison is shown in Figure 3.

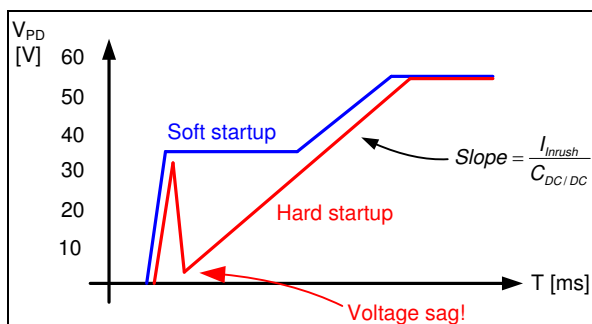


Figure 3. Comparison of input voltages without Soft Start (Hard startup), and with Soft Start (Soft startup).

Once bulk capacitance has charged up to a point where  $VPN_{OUT}$  to  $VPN_{IN}$  differential voltage is less than 0.7V, the isolation MOSFET is switched into normal operating mode with MOSFET current limit set at 1.8A (typical), to provide over-current protection.

PD70100A and PD70200 ICs are different in their respective isolation MOSFET's continuous current handling capability:

PD70100A: 450mA (max.)

PD70200: 1123mA (max.)

An adequate heat sink for the PD70100A/PD70200 IC's exposed pad must be provided to achieve these current levels without damaging the IC. A large, heavy copper fill area and/or a heavy ground plane with Thermal Vias is recommended. Electrically the exposed pad ground plane should be connected to  $VPN_{IN}$ .

Internal logic monitoring  $V_{PP}$  to  $VPN_{IN}$  will place the isolation switch MOSFET in a high impedance state if voltage between  $V_{PP}$  and  $VPN_{IN}$  drops below 31V to 34V.

#### OVER-CURRENT PROTECTION

Over-current protection is provided on the PD70100A/PD70200 IC using the Isolation MOSFET Switch, which limits the  $VPN_{OUT}$  current to 1.8A during normal operation. See previous description of Soft Start.

#### POWER GOOD

During Soft-Start mode, the PD70100A/PD70200 IC monitors  $VPN_{OUT}$  to  $VPN_{IN}$  differential voltage. When this voltage is less than 0.7V (max.), the IC enters normal operation mode and the isolation switch current limit is increased to 1.8A (typical). At this same 0.7V (max.) threshold the Power Good signal is asserted by means of an open drain MOSFET between PGOOD and  $VPN_{OUT}$ .

PGOOD pin is active low; a low impedance state between PGOOD and  $VPN_{OUT}$  indicates the Soft-start mode has finished and the isolation switch has transitioned into normal operating mode.

PGOOD MOSFET can handle current of 5mA and can be pulled up to  $V_{PP}$ .

**THEORY OF OPERATION****AUXILIARY VOLTAGE OUTPUT**

PD70100A/PD70200 IC provides a 10.5V (typical) regulated output to be used as a start-up supply for DC/DC controllers whose  $V_{CC}$  is provided via a bootstrap winding. This regulated supply is available at VAUX pin, and is referenced to  $VPN_{OUT}$  pin. VAUX supply is designed for low-duty operation, and should not be designed as a primary housekeeping supply. The current capability is continuous 2mA, with 10mA peak ( $\leq 10ms$ ). VAUX output is current-limited at 10mA (min.).

For stability, the VAUX regulator requires a minimum of 4.7 $\mu$ F ceramic capacitor connected directly between VAUX and  $VPN_{OUT}$  pins.

**THERMAL PROTECTION**

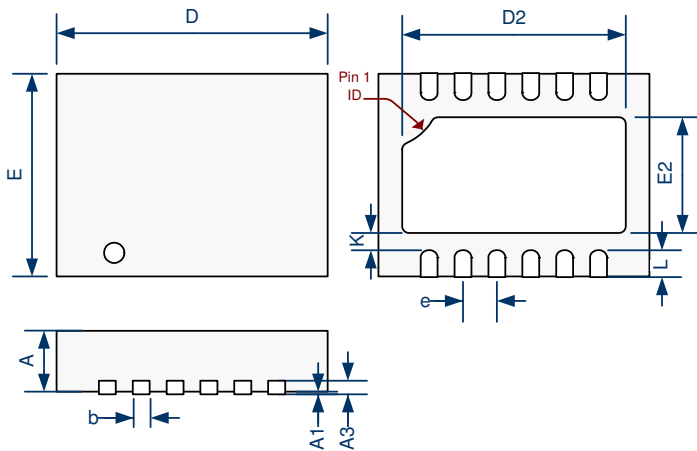
Both PD70100A and PD70200 IC include temperature sensors which individually monitor both the isolation MOSFET and the Classification Current Source for over temperature conditions. In case of an over temperature condition, the sensor will activate protection circuitry which will disconnect its respective monitored function.

**BULK CAPACITOR DISCHARGE**

The bulk capacitor discharge circuitry eliminates the need to place a diode in series with the  $V_{PP}$  line to prevent an application's bulk capacitance from discharging through the detection resistor and the isolation switch MOSFET's body diode. Discharge current through the detection resistor can cause failure of the detection signature in cases where a PD is connected and the bulk capacitance is not fully discharged.

During normal operation, PD70100A/PD70200 IC continuously monitors voltage at  $V_{PP}$  to  $VPN_{IN}$ . Should  $V_{PP}$  to  $VPN_{IN}$  voltage fall below isolation switch turn-off threshold (31V to 34V), isolation switch MOSFET is immediately placed in a high-impedance state. At this point the internal logic monitors the voltage at  $V_{PP}$  to  $VPN_{OUT}$ . If  $V_{PP}$  to  $VPN_{OUT}$  voltage is between 1.5V to 32V, a 23mA (min.) constant current source is connected across the  $V_{PP}$  and  $VPN_{OUT}$  pins. This constant current source provides bulk capacitor discharge.

A 220 $\mu$ F bulk capacitance can be discharged from 32V to 1.5V in a maximal period of 292ms.

**LD**
**12 Pin Plastic DFN 4x3 mm**


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
D	4.00 BSC		0.157 BSC	
E	3.00 BSC		0.118 BSC	
D2	3.00	3.70	0.118	0.146
E2	1.40	1.80	0.055	0.071
e	0.50 BSC		0.0197 BSC	
K	0.20 MIN		0.008 MIN	
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012

**Note:**

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / April 2010		Preliminary Release
0.3 / June 2010		Add Classification Pulse Diagrams
0.3 27 Jul 10		Changing catalog numbers metrology
0.3 12 Nov 10		Extensive changes to document format and Theory of Operation; corrected package drawing; added Product Highlight and Typical Characteristics
0.4 Dec 23 2010		Package update
0.5 Jan 05 2011		Package update
0.6 Jul 13 2011		Specification Update
1.1 Feb 2012		Updated Document Address Footer

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Cat. Num: DS\_PD70100A\_PD70200