

BASIC APPLICATION SCHEMATICS

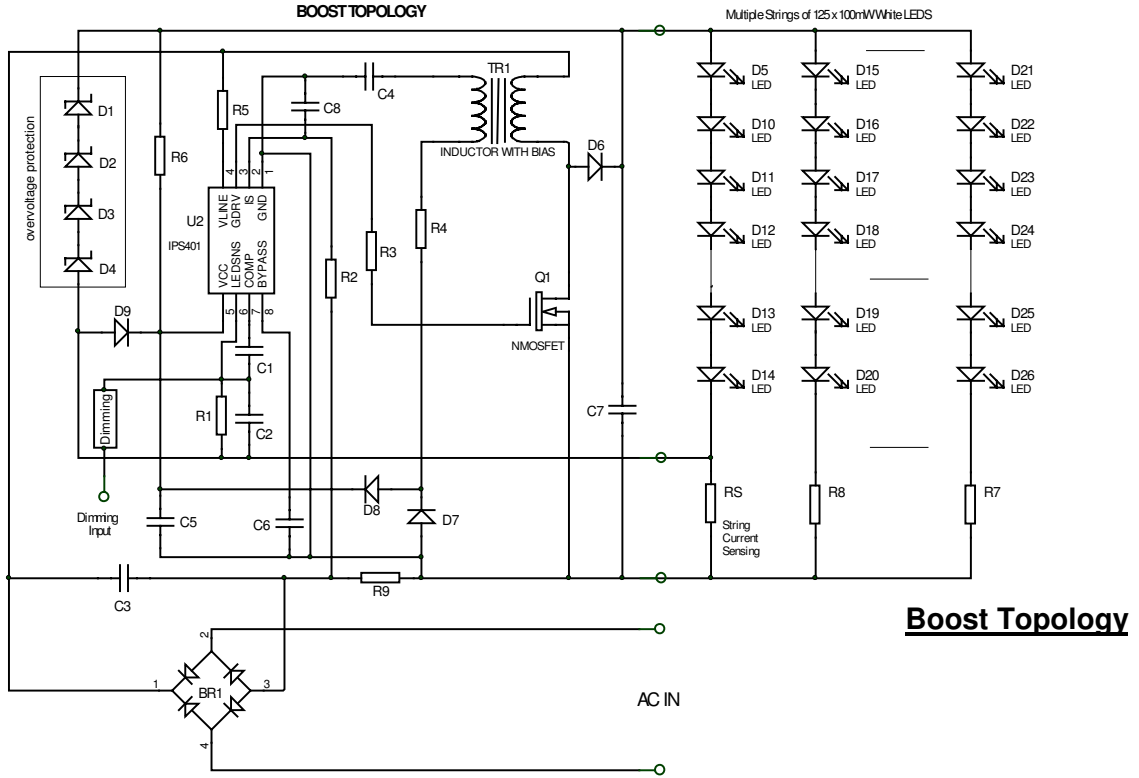


Figure 1

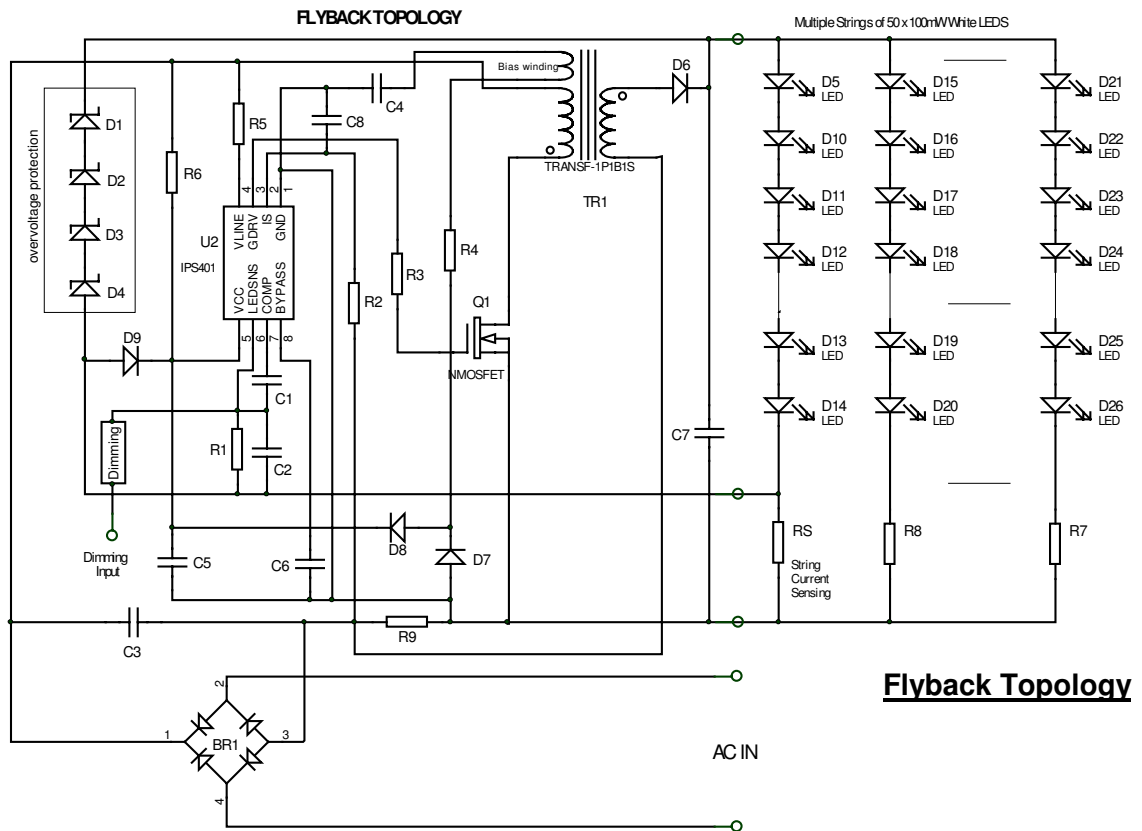


Figure 2

Note: see page 11 for topology selection

FUNCTIONAL BLOCK DIAGRAM

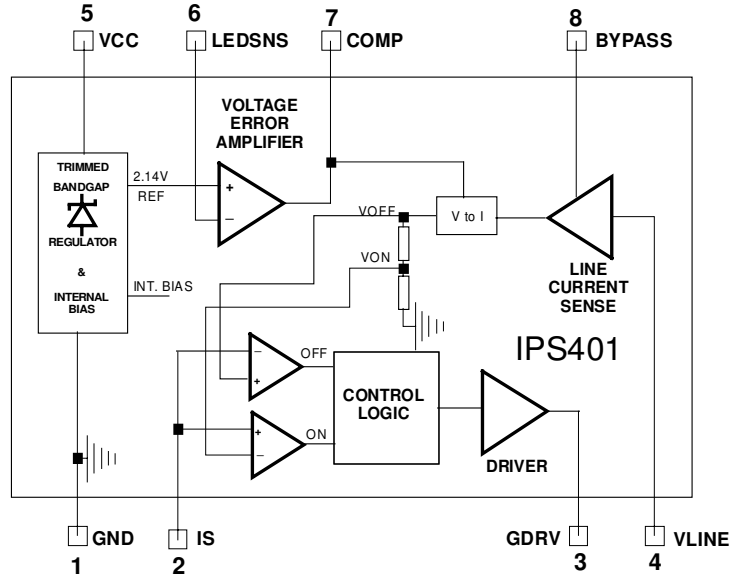


Figure 3

PIN DESCRIPTION

Number	Name	Description
1	GND	Ground pin. This pin must be connected to the general ground.
2	IS	Inductor current sensing pin. This pin is used to measure the current flowing through the inductor which is forced to be proportional to the instant AC line voltage. The power MOSFET is automatically driven in a self-oscillating mode to restart a new cycle when the current in the inductor has dropped below half of its peak value.
3	GDRIVE	MOSFET gate drive pin. The internal buffer connected to this pin can drive a broad variety of power MOSFETs and IGBTs. A series resistor is sometimes added to improve the EMI signature.
4	VLINE	AC voltage pin. This pin is used to sense the instantaneous AC line voltage through a series resistor that performs a voltage to current conversion. This forces the peak current in the inductor to be proportional to the instant AC line voltage.
5	VCC	IC supply pin. The circuit contains a shunt regulator that behaves like a 10V zener. During start-up the IC draws very little current. Operations start when the “zener” value is reached and stop should the VCC voltage becomes less than approximately 8V.
6	LEDSENSE	LED voltage feedback input pin. Negative feedback of the voltage error amplifier which positive input is internally connected to a 0.50V trimmed reference. It is used to regulate the voltage across the storage output capacitor to a value slightly above the maximum line peak voltage.
7	COMP	Voltage loop compensation pin. This output of the voltage error amplifier is used for loop feedback compensation purposes.
8	BYPASS	Constant loop gain capacitor pin. The bypass capacitor connected between this pin & GND helps maintain the loop gain constant at different line voltages thus preventing loop instabilities which could occur with other arrangements.

INTRODUCTION:

The IPS401 is based on the IPS101 core technology. It has all the qualities of AAI's PFC controller with low component count and a self-oscillating mode for low EMI and low switching losses, but it has been optimized for driving multi-LED strings or arrays, meeting high-brightness, high number of white LED control requirements. It offers the same key features of its predecessor but in most applications does not require input and output electrolytic capacitors.

OPERATING DESCRIPTION:

3-input current multiplier:

The IPS401 controller incorporates a 3-input current-mode multiplier that monitors a constant loop gain and ensures a good stability and response over a broad range of input AC voltages and output loads. It also forces the current drawn from the AC line to be proportional to the instant line voltage thus resulting in a power factor close to unity. This ensures to pass the AC line harmonic limits of the EN61000-3-2 standard for Class C equipment with all application requirements.

Voltage error amplifier:

The IPS401 includes a voltage error amplifier between pin 6 and pin 7. Its non-inverting input is connected to an internally trimmed 0.50V reference. Its output connected to pin 7, is internally connected to a V-to-I converter/multiplier. As indicated in the typical application schematic of figure 1, pin 6 and pin 7 are used for the following purposes:

- (a) DC output overvoltage protection:
 - The output DC voltage is set by the number and voltage characteristics of the output LED diodes in series.
 - The number of zener diodes involved in the overvoltage protection circuitry is determined by $\Sigma V_z \min > V_{out}$
- (b) Loop feedback, linear dimming, PWM dimming.
- (c) the loop feedback compensation network R1, C1, C2 (see Fig. 1) provides a suitable network for most applications. More complicated schemes are possible for demanding applications where transient response is paramount.

MOSFET current control:

The recommended use of the IPS401 is in a non-isolated boost converter operating from raw rectified AC voltage. The FET, diode, and boost inductor generate a regulated output voltage that exceeds the peak voltage of the AC input voltage.

The maximum current increases with increasing output power demand. Once V_{cc} is established, the control logic turns the MOSFET on. The current in the inductor and MOSFET is sensed by resistor R9. The output power of the circuit is determined by the value of this current.

When the current reaches the peak value set by the internal multiplier circuit, the MOSFET is switched off and the current in the inductor decreases as its energy is dumped into the output capacitor and load LEDs. In the recommended application circuit, the inductor current decreases to zero, at which time the control logic turns the MOSFET on again. The system is therefore self-oscillating and does not require a dedicated oscillator. Note that the frequency varies with input voltage and output load, but:

- the frequency variation is low (less than 2:1).
- the frequency variation helps to reduce conducted EMI.
- the frequency decreases with increasing load. Lower frequency implies higher efficiency.

MOSFET driver:

The MOSFET driver has been sized to be capable of driving power MOSFETs featuring a total gate charge up to 80nC.

Due to the continuous mode of operations of the inductor, the MOSFET must be driven with a reasonably (but not excessively) low impedance, to minimize switching losses at both turn-on and turn-off without generating too excessive EMI.

In term of R_{on} , the driver's output devices are as follow:

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- P-channel Ron: 30 Ω typical
- N-channel Ron: 20 Ω typical

A series resistor R3 on pin3 should be added to further reduce EMI and minimize the noise injection which could result from Miller-capacitance kick-back during transient conditions.

Examples of suitable MOSFETS:

- **IXYS PolarHT™ and Polar HV™** MOSFET series: IXTY1R4N60P, IXTY2N60P, IXTY3N60P
- **Fairchild** MOSFET series: FQPF1N60, FQPF 2N60, FQPF 3N60.
- **Infineon COOLMOS™** series: SPD01N60S5, SPD02N60S5, SPD03N60S5.
- **Motorola** MOSFET series: MTP1N60, MTP2N60, MTP3N60.
- **SGS-Thomson** MOSFET series: STD1NB60, STD2NB60, STD3NB60. **Etc...**

Note: Due to the rapid evolution of MOSFET technologies, please check for current models when designing a new SMPS.

PolarHT™ and Polar HV™ are trademarks of IXYS corporation. **COOLMOS™** is a trademark of Infineon.

Thermal shutdown:

An internal temperature sensing protection circuit disables the MOSFET gate drive when the temperature exceeds a typical value of 150°C. This circuit has sufficient hysteresis to prevent relaxation. Normal operations therefore only resume when the junction temperature has dropped below approximately 120°C.

Shunt bandgap regulator:

The IPS401 internal trimmed bandgap shunt regulator behaves like a 10V zener but also provides the 0.50V reference for the voltage error amplifier, and the various internal bias current and voltages required by the different blocks.

During start-up, the current consumption in the regulator is very low, typically 100 μ A, allowing many possible schemes to power the IPS401. Once the “zener” value is reached, the MOSFET gate drive is enabled and normal operation starts. When enabled, the typical chip consumption is 660 μ A plus the current necessary to drive the MOSFET which depends on the MOSFET’s total gate charge and the frequency of operation (linked to L1 inductance value).

The VCC voltage is allowed to drop below the “zener” value during normal operations but the circuit will reset itself and re-enter start-up mode should the VCC drop below approximately 8 volts.

The shunt regulator is sized to handle up to 50mA, which is especially useful to power the IPS401 with few components only. Be careful however not to exceed the package rated power dissipation (see table p7).

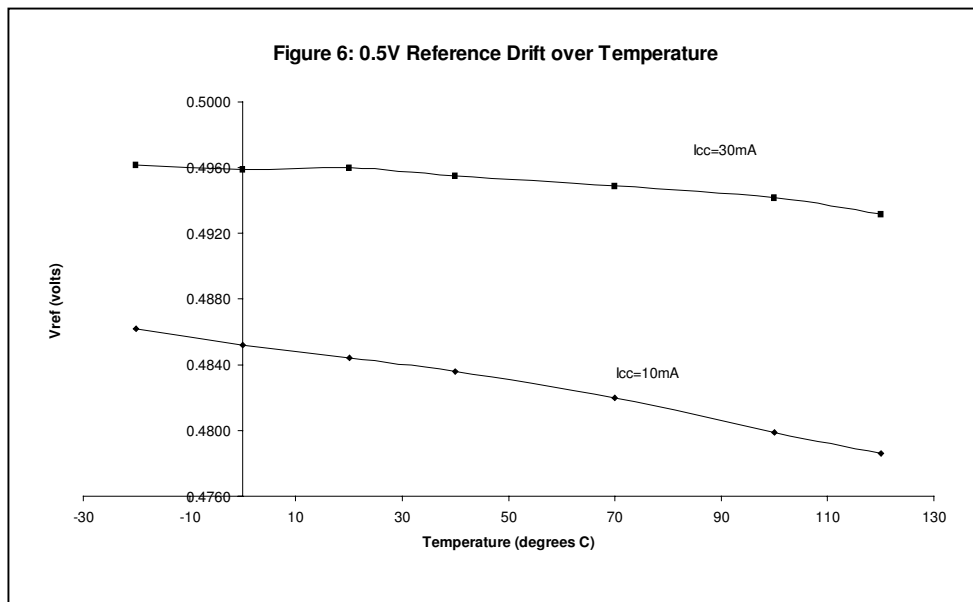
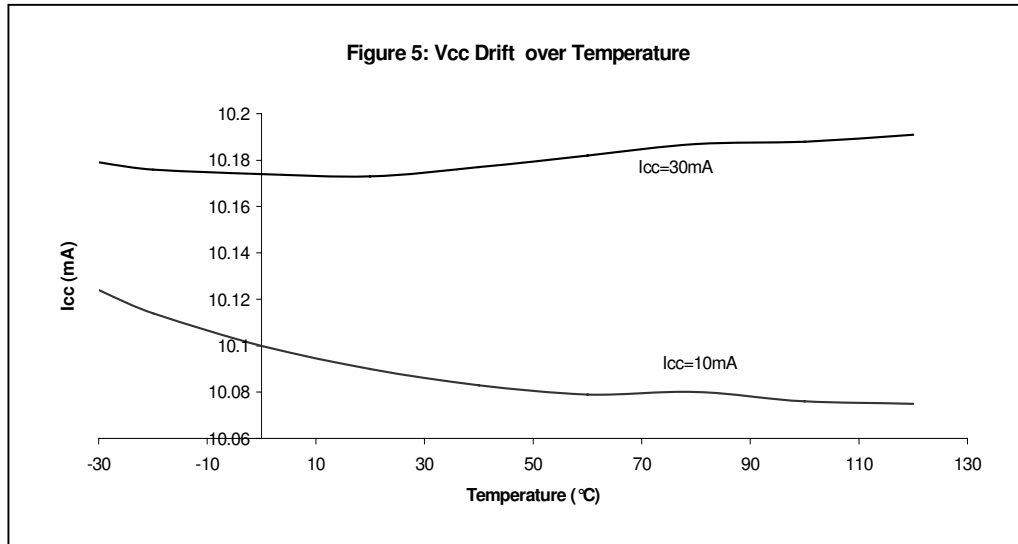
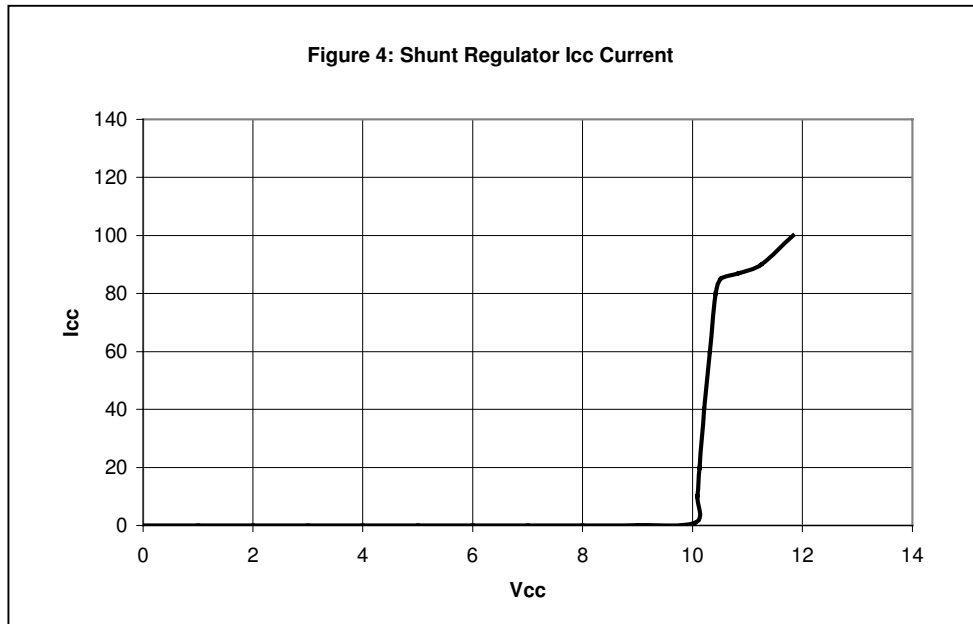
ELECTRICAL CHARACTERISTICS

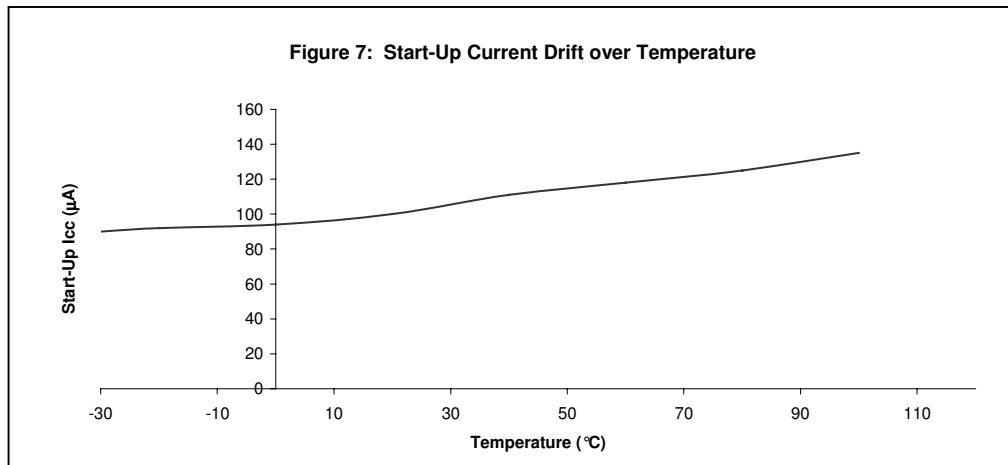
ABSOLUTE MAXIMUM RATING		
Characteristics	Value	UNITS
Shunt regulator max I_{CC} non-repetitive current (pin 5) - see fig 7-	60	mA
Peak drive output current (pin7)	Source=100, Sink=200	mA
Isense input voltage (pin 2)	0 / - 10	V
VLINE maximum input current (pin4)	700	μ A
Junction to case thermal resistance $R_{\theta J-C}$	PDIL = 42, SOIC = 45	°C / W
Junction to PCB thermal resistance $R_{\theta J-A}$	PDIL = 125, SOIC =155	
Power dissipation for $T_A \leq 70^\circ\text{C}$	PDIL = 640, SOIC = 500	mW
Operating junction temperature	- 40 to 150	°C
Storage temperature range	- 55 to 150	
Lead temperature (3 mm from case for 5 sec.)	260	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
		MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage (V_{CC})	ICC = 10 mA	9.7	10.0	10.3	V
Shunt regulator dynamic resistance	1 to 30 mA	2	4	6	Ω
Shunt regulator peak repetitive current (I_{CC})		-	-	50	mA
Start-up current (I_{CC})		-	100	150	μ A
Under voltage lock-out (V_{CC})		$V_{CC} - 2.1$	$V_{CC} - 1.8$	$V_{CC} - 1.4$	V
Min I_{CC} to ensure continuous operation	4A, 600V, 20 nC MOSFET, L = 7 mH	-	3	-	mA
Thermal shutdown trip temperature		-	150	-	$^{\circ}$ C
Multiplier					
Maximum operating voltage across IS resistor (R9)	See note2	-1.3	-1.2	-1.1	V
COMP voltage range		0	-	3	V
Vline input current operating range	$I_{CC} = 1$ to 10 mA Temp = 0 to 70 $^{\circ}$ C	20	-	600	μ A
Bypass capacitor (pin8)		-	1	-	μ F
Error amplifier					
Reference voltage	ICC = 10 mA	0.48	0.50	0.52	V
Open loop gain		-	85	-	dB
3 dB response		-	200	-	Hz
Output impedance		-	30	-	K Ω
P & N Outputs to MOSFET gate					
P gate driver saturation	10 mA (source)	-	0.3	0.5	V
N gate driver saturation	10 mA (sink)	-	0.2	0.35	V
Gate pull-down resistor	(internal)	30	45	65	K Ω
PDRIVE Rise time (10% to 90%)	390 pF load	-	100	200	ns
NDRIVE Fall time (10% to 90%)	390 pF load	-	50	100	ns
Max recommended total external MOSFET charge		-	-	50	nC

Note1: Electrical parameters, although guaranteed, are not all 100% tested in production.

Note2: To avoid damage to pin 2 by the in-rush current, size R2 to limit the input current into the IC to 30mA. 1Kohm to 33Kohm are suitable values for most applications.





Application Information

The IPS401 is intended for use as an LED controller in non-isolated applications directly connected to the AC line. It operates as a boost-converter that controls output current rather than voltage. Constant current ensures controlled brightness and consistent spectral output from the LEDs.

POWERING THE CHIP (Pin 5 – VCC, Pin 1 – GND)

The VCC pin acts like a 10V zener. The chip requires about 100µA to start and about 660 uA to operate. This does not include the current used to drive the gate of the FET. The recommended value of startup resistor R6 is 750k ohms. This will provide the 100µA of startup current when the input is above $750k \times 100\mu A = 75$ volts. Using a value of 47µF for Vcc capacitor C5 should give sufficient holdup time for the chip to begin operating before the bias winding on the boost inductor begins supplying power. Note that the frequency and duty-cycle on the bias winding will vary as the driver follows the input voltage. The polarity of the bias winding does not matter if connected as shown in the application schematic. The suggested values for the bias supply components are C4 = 4.7nF, D7/D8 = 1N4148, and R4 = 100 ohms. The current consumption during normal operation is 660 microamps maximum plus the gate drive current.

During debug, it can be helpful to do testing with power supplied to the chip from a lab power supply. It is suggested that PCB designs have a place to connect clips to the VCC and GND traces to facilitate this. It is important that an external supply connected in this way be set in “constant current” or “current limited” mode. Typical settings are 10 milliamps and 12 volts.

AC LINE SENSE (Pin 4 – VLINE)

The amplitude of the rectified AC input is sensed through dropping resistor R5. The suggested value for R5 is 820k for wide input range (85-265VAC) applications. The input impedance of the VLINE pin is about 20k ohms (plus two diode drops) to ground.

GATE DRIVE (Pin 3 – GDRV)

The GDRV pin switches between VCC and GND with about 30 ohms resistance to VCC and about 20 ohms resistance to GND. A series resistor between this pin and the gate of the FET of about 100 ohms is suggested to control the turn-on and turn-off speed of the FET and thereby reduce the conducted and radiated EMI. Generally, a higher resistor value means slower switching of the FET, lower efficiency, lower EMI, and higher FET losses (more FET cooling needed).

ROLLOFF (Pin 8 –BYPASS)

A capacitor connected between the BYPASS pin and GND is used to create a voltage which allows the chip to sense the peak/rms input voltage and adjust on and off times of the GDRV pin so as to maintain a constant current for the LEDs. The suggested value of this capacitor is 1uF, with a 16V or greater rating.

CURRENT SENSE (Pin 2 –IS)

A low-value resistor R9 is used in the application to sense the inductor current. The voltage across this resistor is sensed through resistor R2 from the IS pin to R9. Note that resistor R9 is NOT sensing just the FET current. Also note that in the voltage being generated is a NEGATIVE voltage, below GND level. The waveform will be a sawtooth, with an inductive ramp in both directions. The suggested series sense resistor R2 value is 1k ohms R9 should be sized to give a peak voltage of about -1.2 volts. As a conceptual guide, two simulation results showing the voltage across R9 are shown below. Vertical is the voltage and horizontal is time. The time scale is different between the two pictures. The first picture shows the “critical conduction” mode nature of the design, where the current goes between a peak value and zero (zero volts being the first major horizontal grid line from the top). The second picture shows that the peak current follows the rectified AC line. In an actual circuit, the waveform would have switching noise superimposed on it. A small capacitor from IS to GND (where $C \times R2 \ll T$) may be useful to improve the circuit behavior. Note that the IS pin is used to determine both when the peak current has been reached and the FET should be turned off, and, when the current has reached zero and the FET should be turned on.

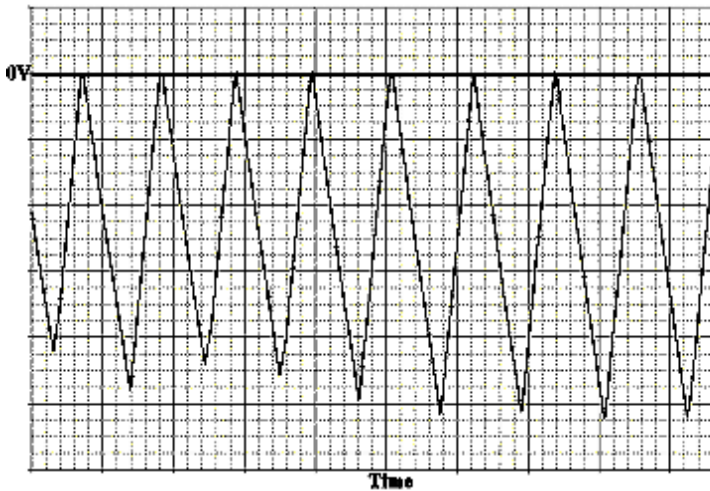


Fig. 8

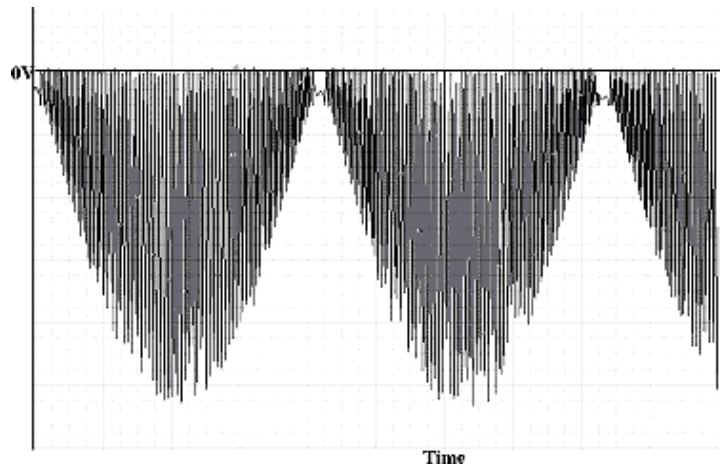


Fig. 9

LED CURRENT SENSE AND COMPENSATION (Pin 6 –LEDSNS, Pin 7 - COMP)

Two capacitors and a resistor (C1, C2, and R1 shown in Fig.10) provide a network around the feedback amplifier located inside the chip to stabilize the system performance. Recommended values are C1 = 100nF, C2 = 220nF, and R1 = 24k ohms.

The LED current is sensed through a sense resistor (RS in Fig. 1 and Fig. 2 page 2) and feedback to LEDSNS through resistor R1. The sense resistor RS should have a value of 0.50 volts divided by the desired peak string diode current.

The application circuit (Fig.10) also shows a suggested method for implementing output overvoltage protection by connecting a zener diode (or string of diodes) from the output to the LED current sense point. If the output voltage was to exceed the breakdown voltage of the zener, this will pull-up the LED current sense voltage and shut-off the gate drive.

Fig. 10

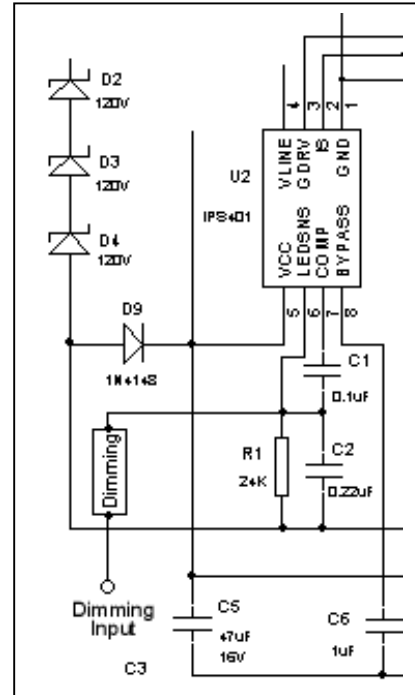
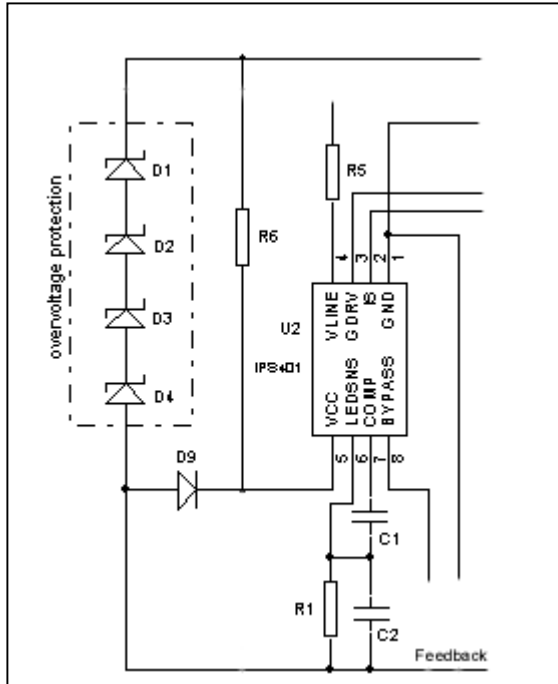


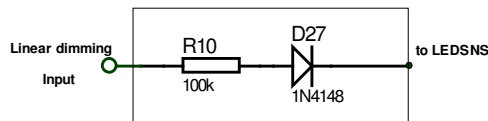
Fig. 11

DIMMING OPTIONS:

This section describes the dimming options and the components included in the associated ‘Dimming’ block as shown in Fig. 11.

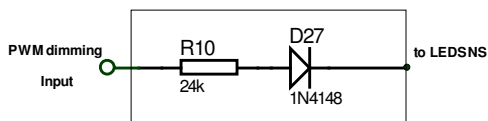
Linear dimming

A DC power supply connected through a 1N4148 diode and 100k resistor to the LEDSNS input (pin 5) and ramped from 0 to 10 volts will provide a fairly good dimming function. There is no effect until the voltage is above 0.50 volts, but it is gradual after that. An improvement would be to add a buffer operational amplifier with an offset, running off VCC. This would allow for a 0 to 5 volt linear control with low offset. The series resistor value needs to be chosen with more scrutiny to get full utilization of the voltage control range.



PWM dimming

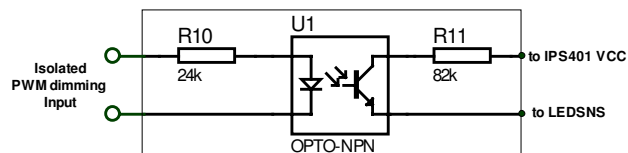
Changing the resistor to 24k ohms allows for fairly good PWM input control. The resistor is smaller since the PWM only goes to 5V. Tuning the series resistor value here would also be necessary for full range control.



Typical dimming frequency range 50Hz – 500Hz

Isolated PWM dimming

An optoisolator and two resistors connected as shown below would bring very good results. R10 resistor value must be selected, chosen to limit the input current to a reasonable value, 24Kohm seems very reasonable. R11 resistor value is selected to achieve 100% dimming. This resistor value would be in the range of 50K to 100K. Any application using this approach will need to test that there not an on-off blinking problem due to the chip power being too low when the LEDs are off.



Typical dimming frequency range 50Hz – 500Hz

Other Application Suggestions

SELECTION OF THE SUITABLE TOPOLOGY: BOOST vs FLYBACK

To make a decision, the user will have to consider the following requirements:

- Number of LEDs per string (Number of LEDs x threshold voltage of each LED)
- Input peak voltage (Peak rectified AC)
- Dimming requirement (Full dimming may require the output voltage to be below the peak input voltage)

The boost topology is the solution of choice for applications when the output DC voltage always remains above the peak input DC voltage and avoids the direct conduction of D6 (see Fig. 1 or Fig.13). It is the preferred solution for simplicity, efficiency and cost effectiveness.

The Flyback topology is the solution of choice when the DC output voltage needs to be below the peak input voltage. (See Fig. 2). For more details please refer to application note AN-IPS-07 “Flyback Topology IPS401 LED Controller Provides High Power Factor, Low In Rush Current and Good Efficiency”.

INPUT CAPACITANCE

In order to have a good power factor, the rectified input voltage needs to follow the line voltage closely. The C3 capacitor shown in the application circuit is a small value, present only for EMI reasons. A rule of 0.01uF/Watt is suggested to correctly size C3.

OUTPUT CAPACITANCE

The output capacitor C7 helps to maintain constant LED brightness. The suggested value is 0.1 uF per watt (i.e. for a 60 watt application, 6.8 uF would be a good starting point in the design). If good Power Factor Correction is required, up to 1uF/watt should be anticipated.

INDUCTOR SIZING

The rising and falling ramp of inductor current to a first approximation is given by the following equations, where V_{in} is the instantaneous input voltage, L is the boost inductor value, V_o is the output voltage, and I_{pk} is the peak inductor current:

$$I(t) = V_{in} \times t / L \quad \text{[FET on]}$$

$$I(t) = -(V_{out} - V_{in}) \times t / L \quad \text{[FET off]}$$

The on and off times for the switch are therefore:

$$T_{on} = L \times I_{pk} / V_{in}$$
$$T_{off} = L \times I_{pk} / (V_o - V_{in})$$
$$T \text{ (switching period)} = T_{on} + T_{off}$$

The peak inductor current occurs at minimum input AC voltage. If the output power is P, then the maximum I_{pk} is:

$$I_{pk,max} = 2.828 \times P / V_{ac,rms,min}$$

In most applications, it is desirable to keep the switching frequency above the audio range (for user comfort) but as low as possible (for efficiency). 25kHz gives a value for T of 40 usec. The above equations allow for computing the inductance and current rating for the boost inductor. The figure below shows the relationship between the inductor current and FET gate drive.

FET SWITCH AND DIODE

The above determination of I_{pk} gives a good sizing for the minimum current ratings for the FET and boost diode. The diode reverse voltage rating and the FET voltage rating need to be greater than the output voltage, which needs to be greater than the peak input voltage at maximum V_{ac} input.

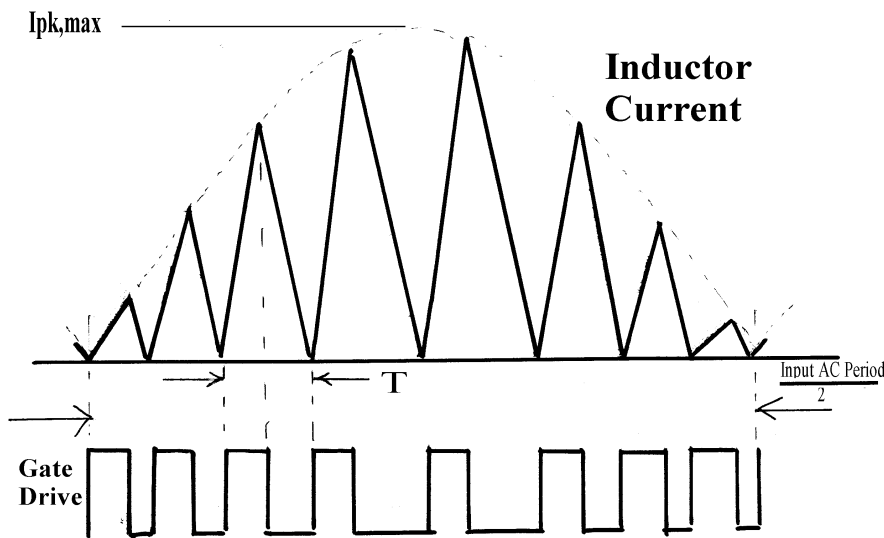


Fig. 12

40WATT APPLICATION SCHEMATIC: IPS401 White LED Driver Powering 3 rows of 125 x 100mW HB LEDs (Vin = 100V/220V AC)

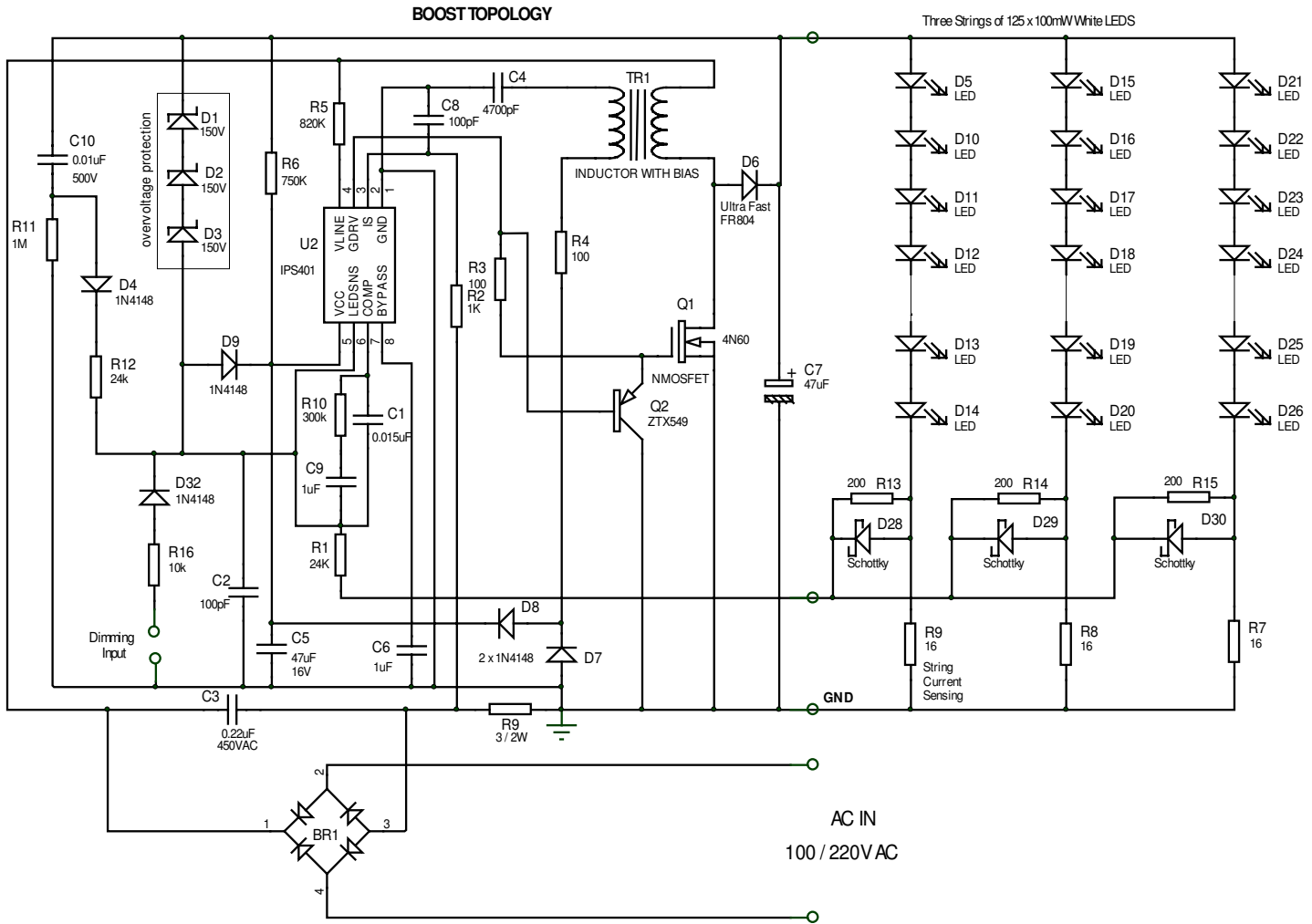
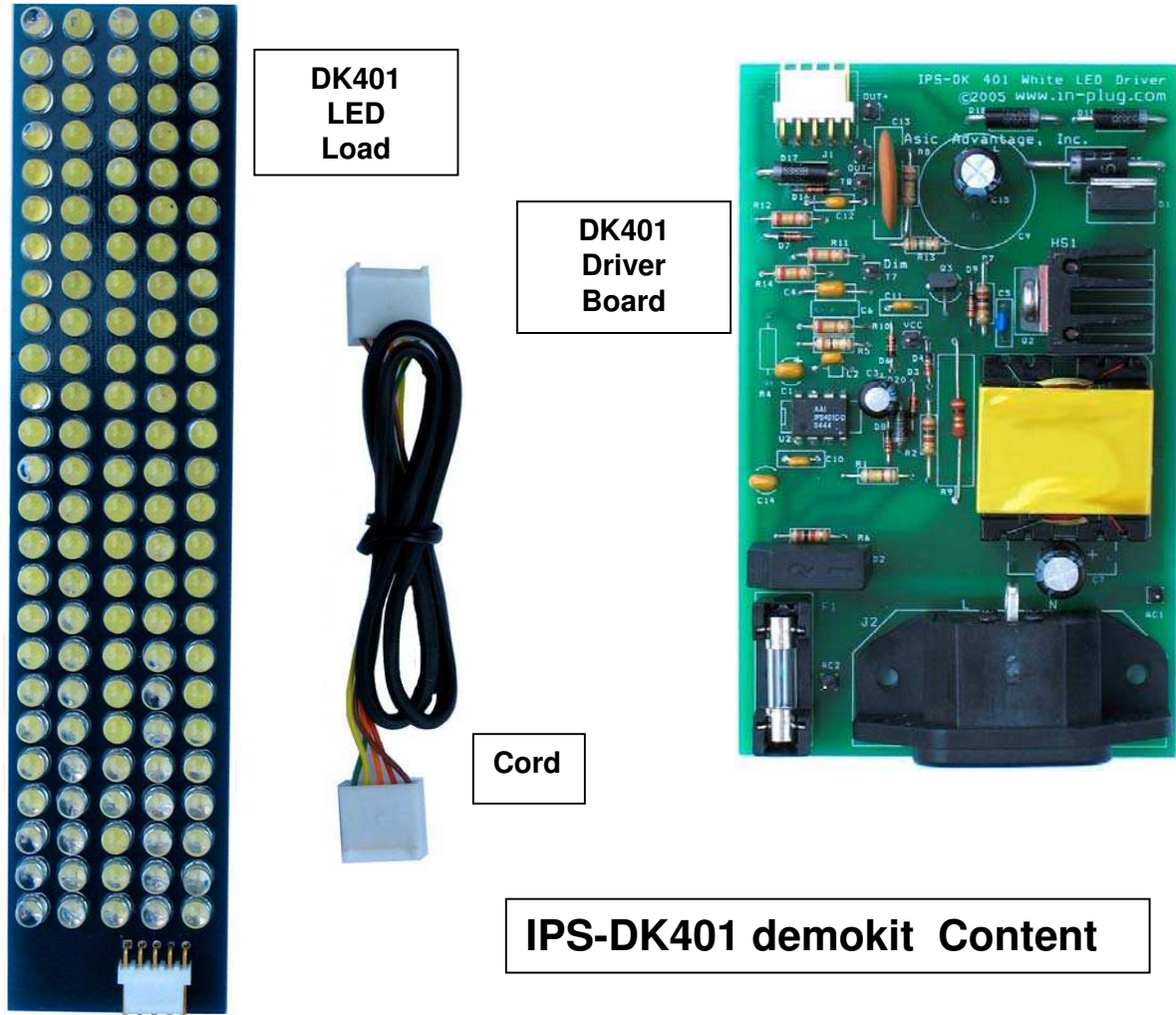


Fig. 13

The application shown in Fig. 13 is typical of large PDP or LCD panel backlighting control. The requirement is perfectly suited for a boost converter topology, where the IPS401 brings the simplest, highest-efficiency, highest power factor and cost-effective solution. The load, limited to 3 strings of 125 HB LEDs requires only to deliver 40W of continuous power on a typical 400V DC/current regulated rail from a wide range mains. But the number of strings could be easily extended by a factor of 10 as the IPS401 would efficiently deliver an output power up to 500W should some components such as TR1 (inductor), Q1 (MOSFET), D6 (Output Diode) be sized accordingly.

The above function is available for demonstration in AAI's IPS-DK401 demokit. Please contact sales (sales@asicadvantage.com) for availability and pricing.



Design Overview:

The basic operation of the driver section is a boost converter, taking the rectified input line voltage and converting it into a constant current into the LEDs. It has been sized to control up to Three LED boards involving 125 LEDs each. Each LED drops about 3.2 volts, for a total of 400 volts. The peak input voltage is 265VAC x 1.414 = 375 volts. This boost configuration can only provide an output voltage greater than the input peak voltage.

For applications which might want to run shorter strings of lamps, a different architecture suitable for lower output voltages must be anticipated :

- 1) Different transformer coupled arrangement. (The turns ratio inside the boost inductor should be decreased proportionately)
- 2) Reduction of the protection zener voltages presently sized for 450V.
- 3) Reduction of R6 according to target and to respect a start-up current of min.140uA.

Note : In places like the USA and Japan where the utility voltage is in the low range (100-120 VAC), it would be possible to operate with shorter strings of LEDs and retain the basic boost topology.

Design Options :

Auto-Isolating Soft Start

AAI has selected a soft start approach which isolates itself from the feedback once the driver is up and running, but requires some more parts than a simple soft start that can pose problems in case of partial loads. It consists of four parts (C10 , R11, D4, R12). The capacitor is used to sense how fast the output voltage is rising at startup, and its current passes through the diode and resistor into the feedback pin to reduce the ramp-up rate and thereby reduce the output overshoot. Note that the output is voltage sensed, not the input. There is a time delay when power is

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applied before the chip starts, while the VCC charges up. During this time delay, the output charges up to the input voltage through the bypass diode. The boost function is the one that needs overshoot control, and that occurs after the chip starts, after the delay, and requires sensing the output voltage.

Compensation Network

The compensation network has been modified and expanded from earlier versions to have a stable loop in all input/output/dimming conditions. A small capacitor to ground $C2=0.015\mu\text{F}$ is added after $R1=24\text{k}$ to get rid of noise spikes and limit the bandwidth of the feedback. This allows the previous $C1=0.1\mu\text{F}$ capacitor to be reduced to $C1=0.015\mu\text{F}$. There is a complementary RC ($C9=1\mu\text{F}$ and $R10=300\text{k}$) added in parallel to this, to add a-zero to the compensation.

Transformer/ Inductor Selection

The architecture of the IPS401 chip is variable frequency. At low loads, the operating frequency is higher. The design of the inductor used here was based on being above the audio range at a high load, specifically above 25kHz at 100 watts. Refer to AAI's Application Note AN-IPS-04 for more design methodology details.

Transformer Specification		
Item	Part	Type / Note
Core	PQ26/20	TDK PC44PQ26/20Z-12
Bobbin	BP26/20	TDK BP26/20-1112CP
Air gap	To be adjusted	Primary Inductance 3.5mH
Primary	1 Layer 155 +/-5 turns	AWG#26 (+/-5 turns to fill-up a complete layer)
Isolation	Not requested	OK to use 3M tape
Secondary	12 turns	AWG#30

Power Factor

Power factor highly depends on input and output capacitors ($C3=0.22\mu\text{F}$, $C7=47\mu\text{F}$) that have been sized to achieve the highest Power factor. When Power Factor is not a primary concern and because LEDs are tolerant to ripple, a lower output capacitor of $1\mu\text{F}$ can be used. It would possibly require as well to increase $C3$ to a larger value ($1\mu\text{F}$ is suggested). For some applications, which operate at high temperatures or need the highest reliability, using film capacitors in place of electrolytic caps should be considered.

Dimming

The application presents 2 pins available to connect external circuitry for controlling dimming. The component choices are suitable for PWM dimming (0 to 5 volts square wave). Linear dimming requires $R16$ to be increased to 100k. See page 10 for more details.

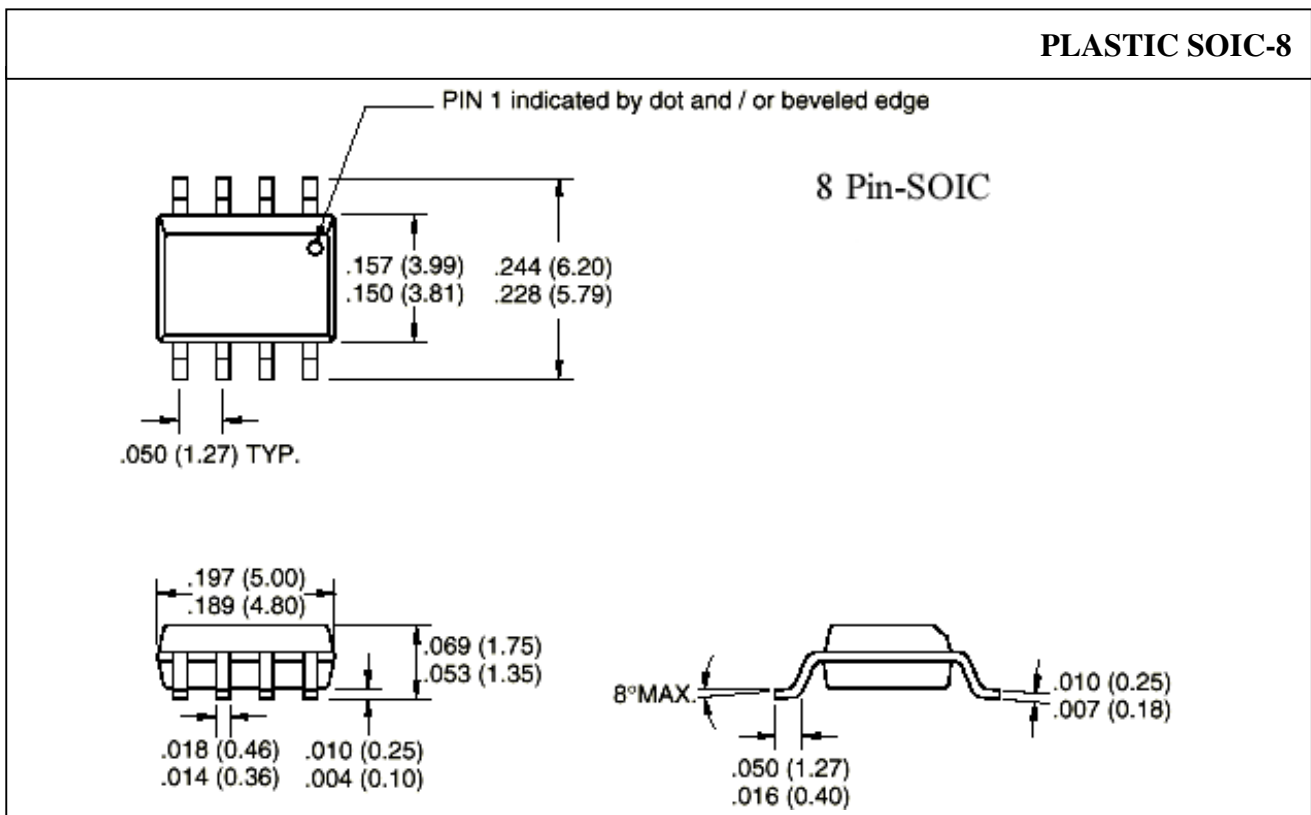
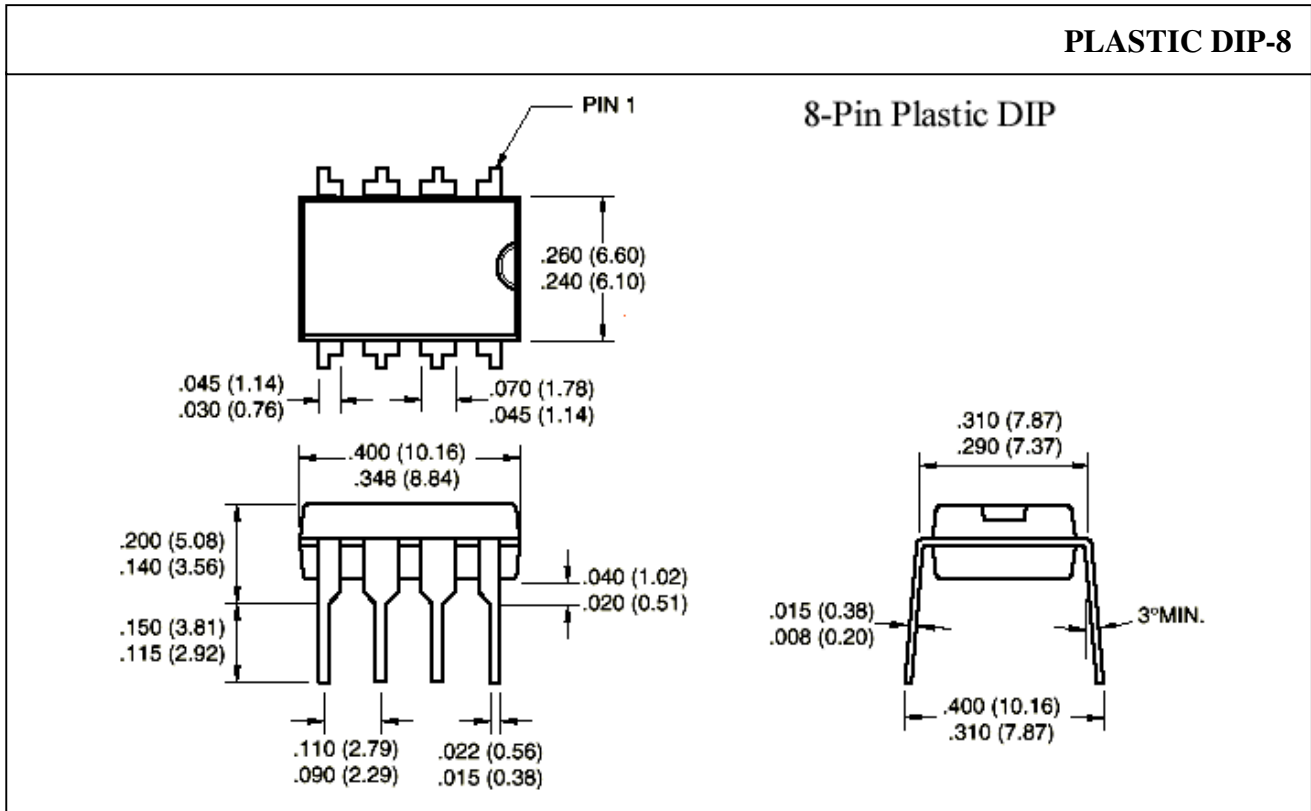
Load Options

The application can be sized for sourcing 100W but has been presented to only drive three strings of 125 LEDs in parallel. Each string of 125 LEDs was designed for full independence and parallelization without any impact on the driver section. Each LED string represents a load of about 12 watts (400 volts times 30 milliamps).

To ensure this autonomy, a 16 ohm ($R7,R8,R9$) resistor provides 0.50 volts to the driver section, representing the reference voltage inside the IPS401. A schottky diode ($D28,D29,D30$) and a 200 ohm resistor ($R13,R14,R15$) are adapting the driver to multiple loads (configured identically) to be operated in parallel and share the sense line with a type of current-sense-averaging.

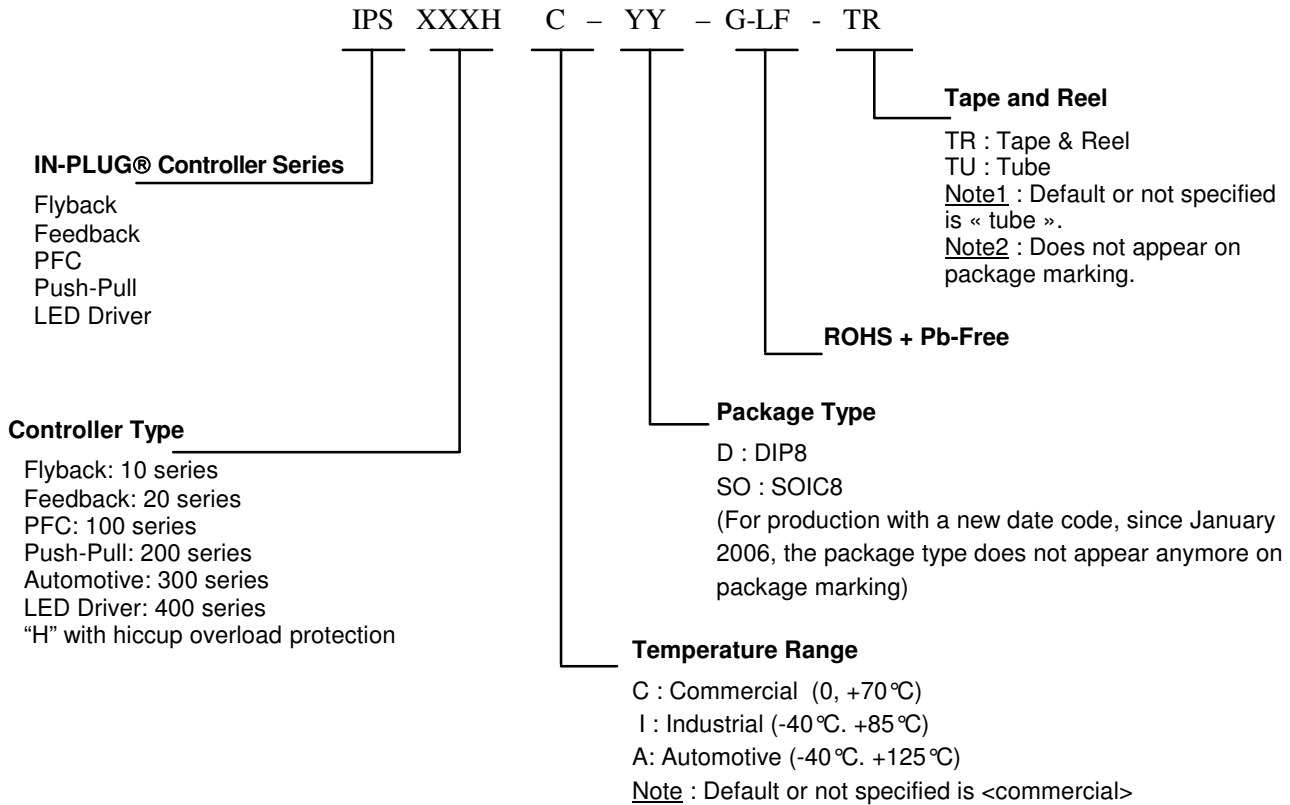
Note : It is NOT suggested to operate the driver without a properly designed string or set of strings. The overvoltage protection should prevent any severe problems, but it is a high-stress state for the components.

PACKAGE DIMENSIONS



ORDERING INFORMATION

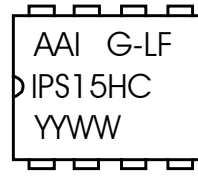
Part-Number



Example of Marking



Non-Green Package



Green ROHS + Pb-Free Package

(Note : For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

This ordering information is for commercial and industrial standard IN-PLUG® controllers ONLY. For custom controllers or for military temperature range, call AAI's sales representative.

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ASIC Advantage INC.

1290-B Reamwood Ave, Sunnyvale California 94089, USA
Tel: (1) 408-541-8686 Fax: (1) 408-541-8675
Websites: <http://www.in-plug.com> - <http://www.asicadvantage.com>