

**GENERAL PURPOSE
 SILICONE DIODE**

- ALL JUNCTIONS COMPLETELY PROTECTED WITH SILICON DIOXIDE
- COMPATIBLE WITH ALL WIRE BONDING AND DIE ATTACH TECHNIQUES EXCEPT SOLDER REFLOW

DEVICES

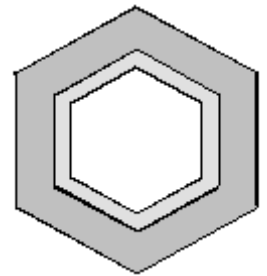
CD483B	CD645	CD5194
CD485B	CD647	CD5195
CD486B	CD649	CD5196

MAXIMUM RATING AT 25°C

Operating Temperature: -65°C to +175°C
 Storage Temperature: -65°C to +175°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

TYPE NUMBER	VRWM	MAXIMUM FORWARD VOLTAGE	IFSM $T_p = 1/120 \text{ S}$ $T_A = +25^\circ\text{C}$	MAXIMUM REVERSE LEAKAGE CURRENT @ +25°C		MAXIMUM CAPACITANCE @ $V_R = 4 \text{ VOLTS}$ $f = 1.0\text{MHz}$
	$V_{BR} @ 50\mu\text{A}$	$V_F @ 100\text{mA}$		$I_R @ V_R$		C_T
	VOLTS	VOLTS	A	nA	VOLTS	PICO FARADS
CD483B	80	0.8 – 1.0	2	25	70	-
CD485B	200	0.8 – 1.0	2	25	180	-
CD486B	250	0.8 – 1.0	2	25	225	-
CD645	270	0.8 – 1.0 ⁽¹⁾	5	50	225	20
CD647	480	0.8 – 1.0 ⁽¹⁾	5	50	400	20
CD649	720	0.8 – 1.0 ⁽¹⁾	5	50	600	20
CD5194	80	0.8 – 1.0	2	25	80	-
CD5195	200	0.8 – 1.0	2	25	200	-
CD5196	250	0.8 – 1.0	2	25	225	-



**27 MILS HEX,
 FLAT To FLAT**

NOTE: (1) Performed at 400mA pulsed.

TYPE NUMBER	I_o	I_o $T_A = +150^\circ\text{C}$	$V_F @ 400\text{mA}$	MAXIMUM REVERSE LEAKAGE CURRENT @ $T_A = +150^\circ\text{C}$		MAXIMUM FORWARD VOLTAGE @ -55°C	
			$T_A = +150^\circ\text{C}$	$I_R @ V_R$		$V_F @ I_F$	
	mA	mA	V	uA	nA	VOLTS	mA
CD483B	200	50	-	5	25	1.2	100
CD485B	200	50	-	5	25	1.2	100
CD486B	200	50	-	5	25	1.2	100
CD645	400	150	0.7 – 0.95	50	50	1.2	400
CD647	400	150	0.7 – 0.95	50	50	1.2	400
CD649	400	150	0.7 – 0.95	50	50	1.2	400
CD5194	200	50	-	5	25	1.2	100
CD5195	200	50	-	5	25	1.2	100
CD5196	200	50	-	5	25	1.2	100

▶ **DIE DIMENSIONS**

DESIGN DATA

METALIZATION

Top: (Cathode)....Au

Bottom: (Anode)..Al

AL Thickness...25,000A Min

Gold Thickness ...4,000A Min

CHIP THICKNESS ...10 Mils

Tolerances: All

Dimensions +/- 2 mils

