AAP149B

PRELIMINARY DATASHEET

Digital Electret Microphone (ECM) Pre-Amplifier

DESCRIPTION

The AAP149B Digital ECM Pre Amplifiers is part of an expanding line of mobile audio amplifiers. The core of the design includes the same Pre-Amplifier technology that was designed in co-operation with Plantronics, Inc. of Santa Cruz, CA for their audio headset products, with industry leading SNR and THD performance and low output impedance. The AAP149B is a digital realization of our core ECM Pre-Amplifier products, created by the inclusion of a 4th Order Sigma Delta ADC.

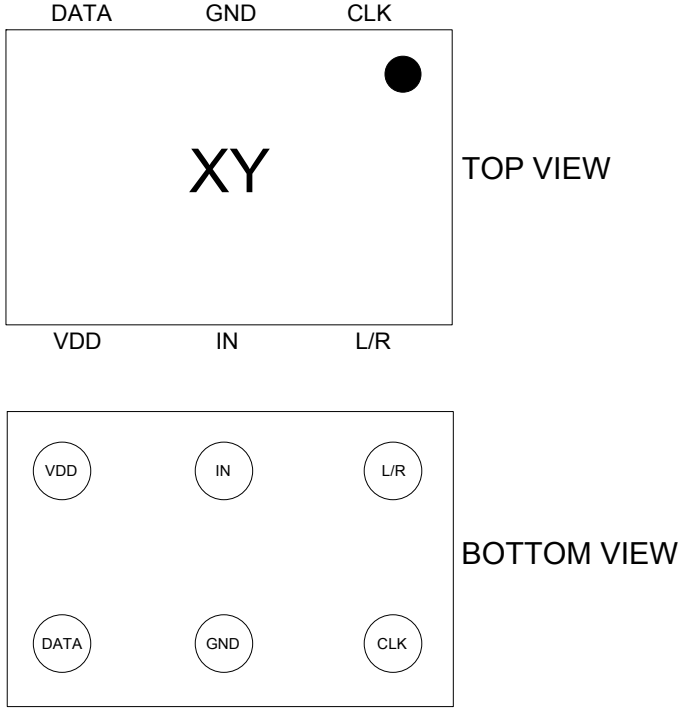
The ADC has a 20kHz signal bandwidth, with a PDM bit stream output and can run with a clock frequency of 1MHz to 3MHz. The single-bit modulator features an inherently linear output, as well as enabling noise shaping and shifting of quantization noise. The combination of a AAI's high performance Pre-Amplifier and ADC yields ultra-low noise performance, 5µV RMS typical with Cmic shorted, (gain dependent). The design also offers excellent RFI and EMI immunity.

Other features include a gain of 16.5dB, as well as ultra-low inputs capacitance and low quiescent current in sleep mode. Sleep mode is automatically detected by the clock frequency falling below 100kHz. Additionally, the AAP149B is configured to be compatible with stereo-audio applications, with provision of a Left and Right channel select. The AAP149B is offered in an RoHS compliant chip-scale 6-Pin Micro SMD, with thickness of 350µm maximum (including solder bumps).

FEATURES

- Ultra-Low Noise ECM Pre-Amplifier Core
- Integrated 4th Order Sigma Delta ADC, with 20kHz Signal Bandwidth, Bit Stream Output (PDM), and Clock
- Frequency of 1MHz to 3MHz
- 16.5dB Gain Option
- Ultra-Low Noise Performance (5µV RMS typical, Cmic = SC, varies with gain)
- Ultra-Low Input Capacitance - .2pF Typical
- Sleep Mode with Low Quiescent Current (< 40µA)
- Stereo-Audio Compatible with L/R Channel Select
- Chip-Scale Micro SMD Bumped Packaging, (810µm x 1200µm x 350µm)
- Custom Options of Various Gains (6dB to 30dB) and Supply Voltage Optimization (1.6V to 3.6V)

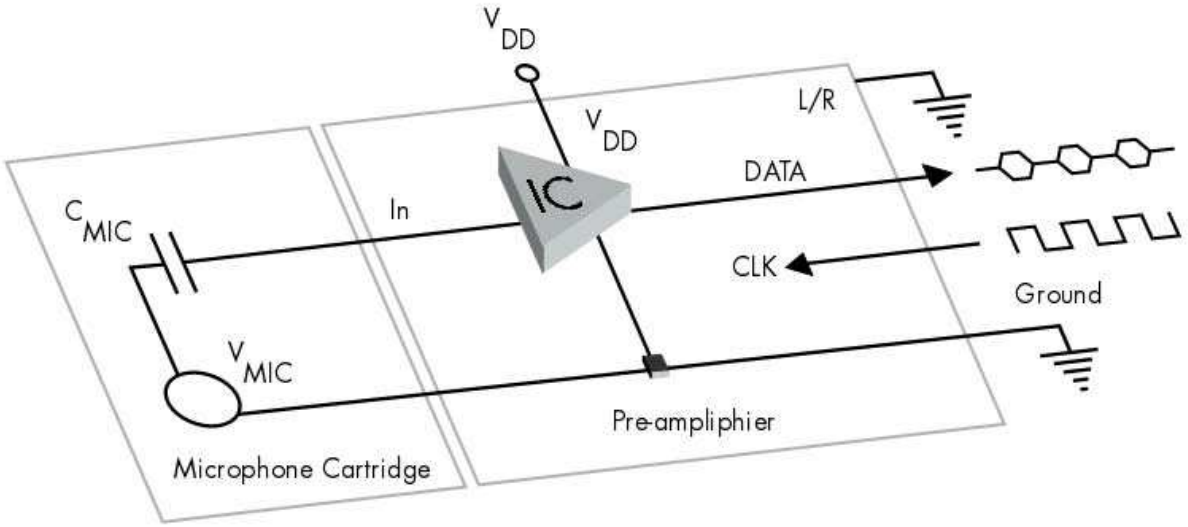
PIN CONFIGURATION: 6-Pin Micro SMD



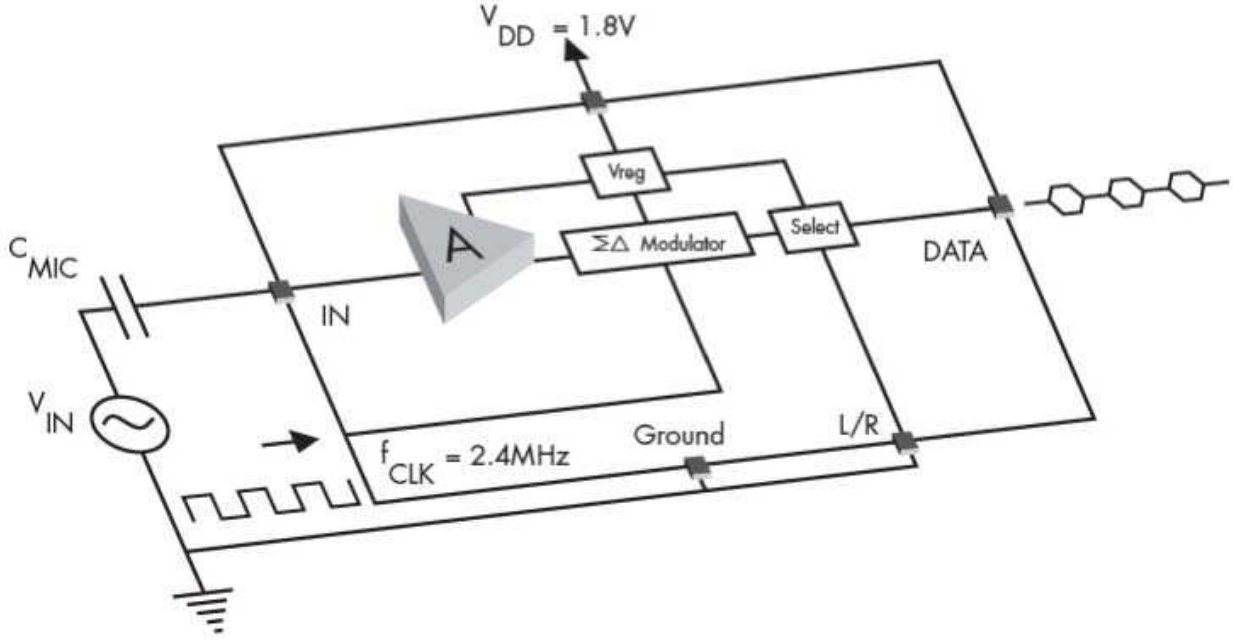
PIN DESCRIPTIONS

Signal	Description
CLK	ADC clock input of 1MHz to 3MHz.
GND	Supply pin ground.
DATA	Data output pin, selectable by L/R.
VDD	Analog power / VDD input, 1.6V to 3.6V.
IN	Analog signal input.
L/R	L/R channel select, setting 'L' or Left as the DATA (DATA1) output when set low or grounded (GND) or 'R' or Right as the DATA (DATA2) output when set high to VDD.

BLOCK DIAGRAM



TEST CIRCUIT



MAXIMUM RATINGS

PARAMETER	SYMBOL	PARAMETERS		UNITS	CONDITIONS
		MIN.	MAX.		
Power Supply	VDD	-0.5	5	V	Max voltage between VDD and GND that will not cause destruction
Analog Input	V_{in}	-0.5	0.5	V	Max voltage between IN and GND
Voltage on CLK	V_{CLK}		5	V	Without loading CLK
Voltage on L/R	$V_{L/R}$		5	V	Without loading L/R
Operating Ambient Temp		-40	85	ºC	
Storage Temp Range		-40	100	ºC	
Performance Operating Temp Range		-5	45	ºC	

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: T=25ºC, VDD=3.3V, V_{in}= -44dBVrms, f_{CLK}=2.4MHz, f_{DC}=50%, BW=20-20kHz, C_{mic}=3-5pF

PARAMETER	SYMBOL	PARAMETERS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
OPERATING SUPPLY							
Supply Voltage	VDD	1.6	3.3	3.6	V		
Operating Output Voltage	V_{op}	1.3	1.4	1.5	V		
Supply Current	IDD	599	665	732	µA		
PSRR		-70			dBFS	Input = 10mVp, 217 Hz square wave FFT response	
AC CHARACTERISTICS							
Transfer Function (AAP149B)	TF	16	16.5	17	dB	@ VDD=1.8V	Input = 10mVp shorted to GND
		21	21.5	22		@ VDD=3.3V	
Input Referred Noise (AAP149B)	e_n		5		µV RMS		
Lower Bandwidth	F_{LP}			25	Hz		
Upper Bandwidth	F_{HP}	20			kHz		
Lower -3dB Frequency	F_{low}		33		Hz	f_{CLK} = 2.4MHz	
Overload Margin (AAP149B)				75	mVp	@ 1% distortion	
				105		@ 10% distortion	
Dynamic Range	DNR		90		dB	Input shorted to GND	
Load Capacitance	C_L		10		pF		

PARAMETER	SYMBOL	PARAMETERS			UNITS	CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			0.2	pF	
Input Resistance	R_{IN}	20			GΩ	
START-UP						
Start-Up Period	t_{UP}			5	ms	Refer to Note 1 below
STANDBY MODE						
Wake-Up Time	T_{up}			10	ms	Refer to Note 2 below
Fall-Asleep Time	T_{down}			10	ms	Refer to Note 3 below
Standby Current	I_{sb}			40	µA	
Standby Clock Frequency	f_{CLKSBM}			100	kHz	Refer to Note 4 below
DIGITAL INPUT-OUTPUT SPECIFICATIONS						
Clock Frequency	f_{CLK}	1	2.4	3	MHz	
Clock Duty Cycle	f_{DC}	40	50	60	%	
Jitter Tolerance				0.5	ns	
Input/Output Voltage Low	V_{IOL}	-0.3		0.35 x VDD	V	I_{out} = 1.8mA
Input Voltage High	V_{IH}	0.65 x VDD		VDD + 0.3	V	I_{out} = 1.8mA
Outout Voltage High	V_{OH}	0.65 x VDD		VDD + 0.3	V	I_{out} = 1.8mA
Input Capacitance	C_{in}			0.2	pF	
Output Current at Low Voltage	I_L	1		10	mA	typical short circuit current at VDD=1.8V
Output Current at High Voltage	I_H	1		10	mA	typical short circuit current at VDD=1.8V
Clock Rise Time	t_{CR}			10	ns	R_L = 1M and C_L = 13pf
Clock Fall Time	t_{CF}			10	ns	R_L = 1M and C_L = 13pf
Delay Time for Data Valid	t_{DV}	18		40	ns	R_L = 1M and C_L = 13pf
Delay Time for Data High Z	t_{DH}			15	ns	R_L = 1M and C_L = 13pf

Note 1: Start-up period is measured when VDD becomes 1.8/3.3 V to the time when transfer function settles within 1 dB of its final value. After start-up period the ASIC can handle equivalent of 1 Pa without distortion (THD < 10%).
Note 2: The wake period is measured when the clock becomes higher then the stand-by clock frequency and the transfer function of ASIC settles within 1 dB of its final value.
Note 3: Fall-asleep period is measured when the clock frequency falls below the the stand-by frequency and the current drops to the stand-by current Isb.
Note 4: The stand-by mode is entered when the clock frequency is below the specified stand-by clock frequency.

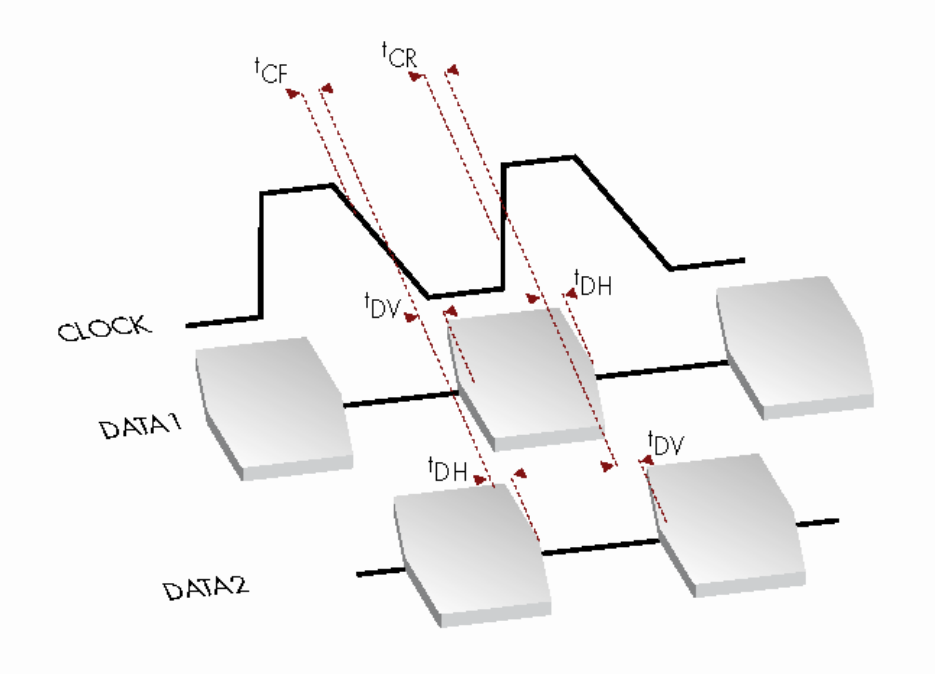
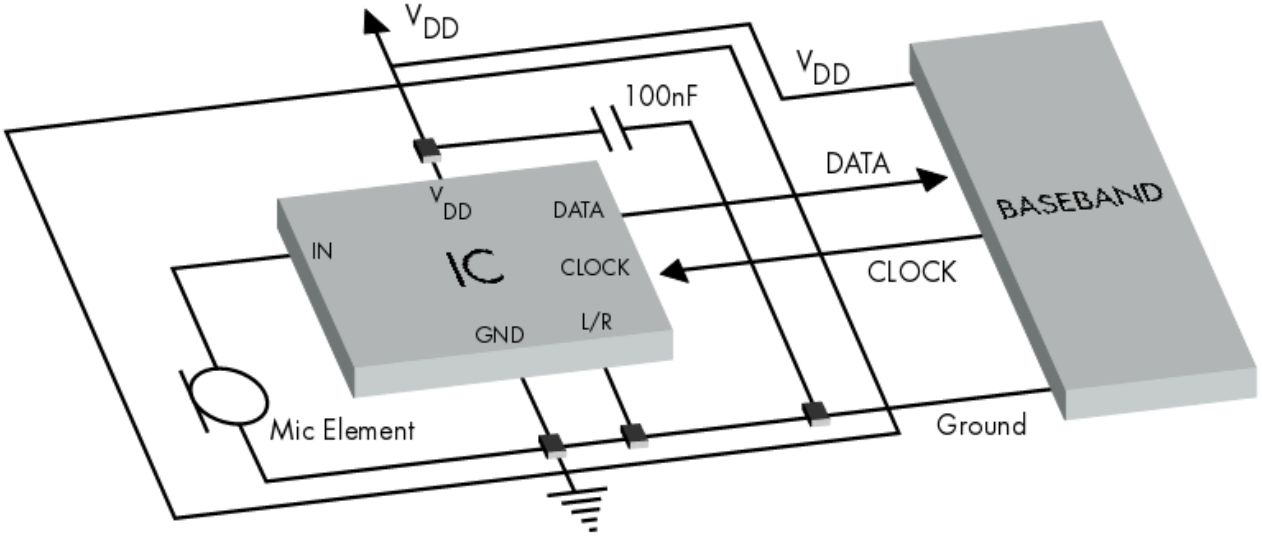


Figure 1. Timing diagram of CLK and DATA terminals

CHANNEL SELECTION

Channel	L/R pad selection
DATA1	GND
DATA2	VDD

INTERFACING WITH PC AUDIO CODEC

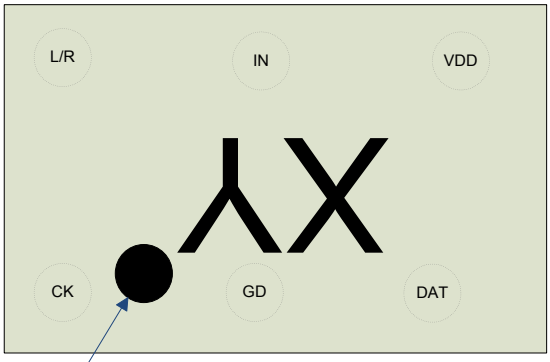


ORDERING INFORMATION

Ordering PN	Subgroup	Description	Temp. Range	Package	Packing Type	Packing Qty
AAP149B S-M6B-G-LF-W	Microphone ECM Interface	Digital Pre-Amplifier 16.5dB gain	S - Special -40°C to +85°C	6-pin Micro SMD	Waffle-Pack	400
AAP149B S-M6B-G-LF-TR	Microphone ECM Interface	Digital Pre-Amplifier 16.5dB gain	S - Special -40°C to +85°C	6-pin Micro SMD	7" T&R	3500

PACKAGE DIMENSIONS AND MARKING

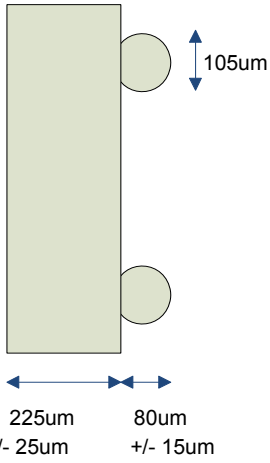
Top View, Bump-Side Down



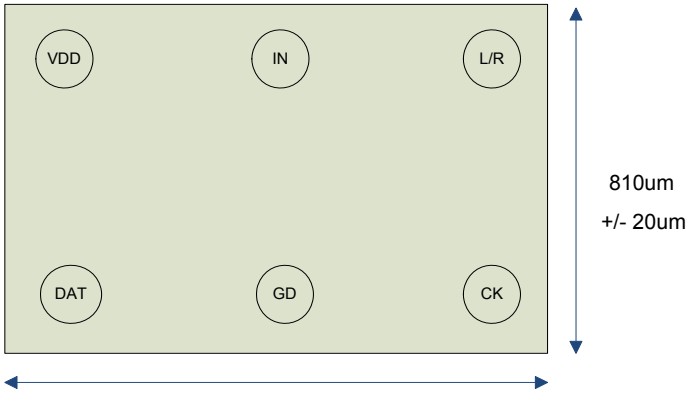
Laser marked orientation dot and
2 character unique lot code assigned
for each assembly order.

Orientation Dot

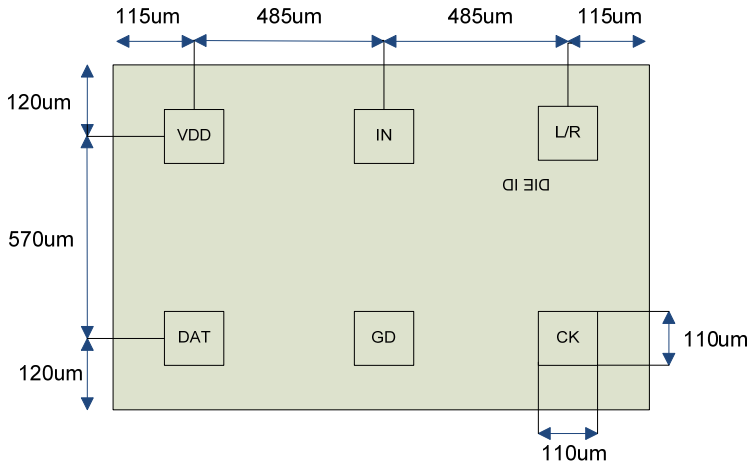
Side View



Bottom View, Bump-Side Up



Cut Dimensions, Bare Die, Active Area Up



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