

**DESCRIPTION**

The LX1912 operates as a Current Mode PWM Buck regulator that switches to PFM mode with light loads. The entire regulator function is implemented with few external components.

The LX1912 responds quickly to dynamic load changes using a high bandwidth error amplifier and internal compensation. Tight output voltage regulation is maintained with the compensated 800mV,  $\pm 2\%$  reference (line and temp regulation). With two external resistors the output voltage is easily programmed, from 800mV to 90% of  $V_{IN}$ .

The regulator is capable of providing an output load current of 1.0A, has no minimum load current requirement for stable operation. Current limit is cycle-by-cycle to protect the switch. Power conversion efficiency is maximized with low regulator IQ and PFM mode of operation.

The LX1912 operational range covers 4.0V to 6.0V, features include power on delay; soft start to limit inrush currents; and thermal shutdown during fault conditions.

The 6-pin TSOT package provides a small form factor with excellent power dissipation capability.

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

**KEY FEATURES**

- Internal Reference 800mV  $\pm 2\%$  Accuracy (Line and Temp.)
- 4.0V to 6.0V Input Range
- Internal Soft Start
- Adj. Output From 0.8V to 90% of  $V_{IN}$
- Output Current up to 1.0A
- Quiescent Current < 550 $\mu$ A, Typical @ 23 $^{\circ}$ C
- 1.2MHz PWM Frequency
- Over Voltage Protection

**APPLICATIONS**

- Portable Microprocessor Core Voltage Supplies
- 5V to 3V
- RoHS Compliant Product

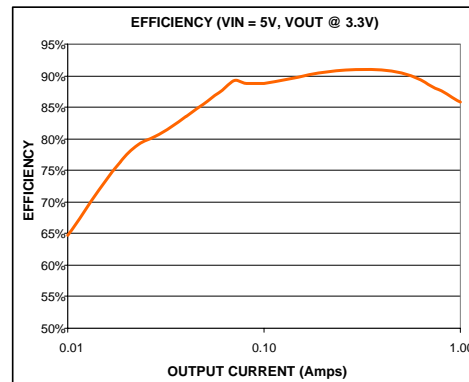
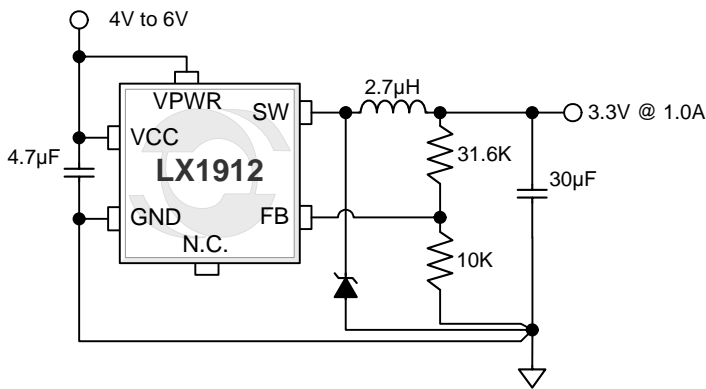
**PRODUCT HIGHLIGHT**


Figure 1 – LX1912 Circuit Topology and Typical Efficiency Performance

**PACKAGE ORDER INFO**

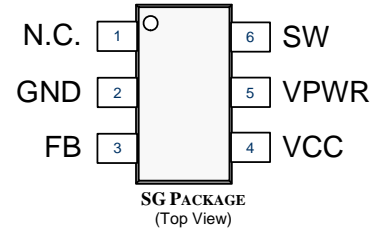
$T_A$ ( $^{\circ}$ C)	Input Voltage	Output Voltage Range	<b>SG</b> Plastic TSOT 6-Pin RoHS Compliant / Pb-free	Part Marking
0 to +70	4.0V – 6.0V	Adjustable	<b>LX1912CSG</b>	1912

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1912CSG-TR)

**ABSOLUTE MAXIMUM RATINGS**

Input Voltage (VCC and VPWR).....	-0.3V to 7.0V
SW to GND .....	-0.3V to (V <sub>IN</sub> + 0.3V)
V <sub>FB</sub> to GND .....	-0.3V to +2V
SW Peak Current .....	Internally Limited
Operating Junction Temperature Range (T <sub>J</sub> ).....	-40°C to +125°C
Storage Temperature Range, T <sub>A</sub> .....	-65°C to 150°C
Maximum Junction Temperature.....	150°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure) .....	260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

**PACKAGE PIN OUT**


RoHS / Pb-free 100% Matte Tin Lead Finish

N.C. – No Internal Connection

**THERMAL DATA**
**SG Plastic TSOT 6-Pin**

<b>THERMAL RESISTANCE-JUNCTION TO AMBIENT, <math>\theta_{JA}</math></b>	<b>134°C/W</b>
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Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .

The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

**FUNCTIONAL PIN DESCRIPTION**

Name	Description
VCC	Unregulated supply voltage input, ranging from +4V to 6.0V for internal analog control circuitry.
VPWR	Unregulated supply voltage for PMOSFET drain to drive the switch pin.
FB	Feedback input for setting programming output voltage.
GND	Circuit ground providing bias for IC operation and high frequency gate drive bias.
SW	Inductor and commutation diode connection point. Connects to internal PMOSFET source.

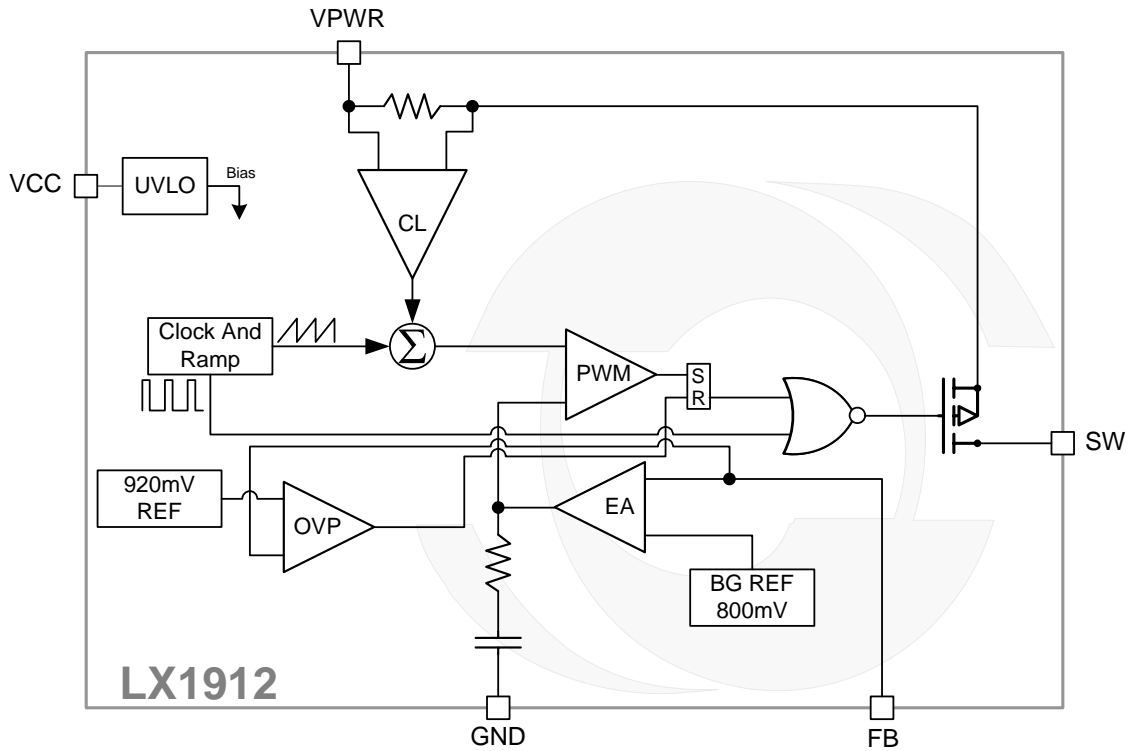
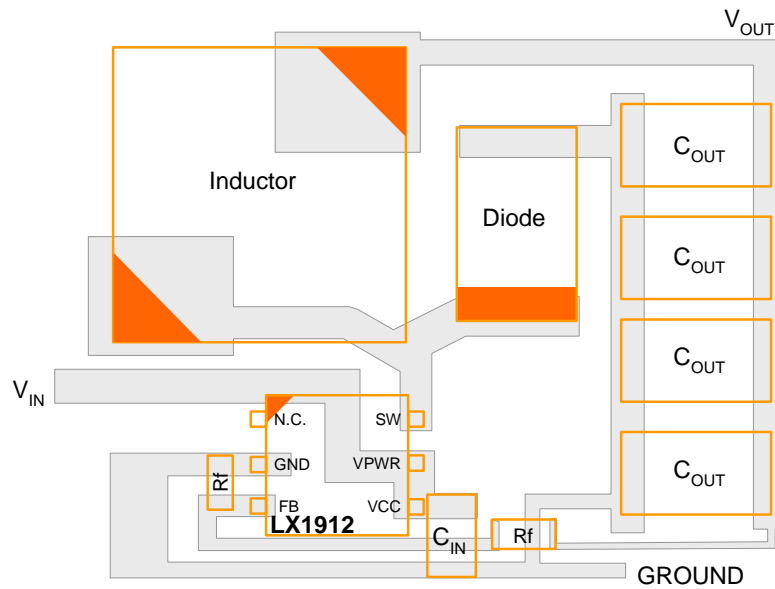
**ELECTRICAL CHARACTERISTICS**

 Specifications apply over junction temperature of:  $-20^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  for  $V_{CC} = V_{PWR} = 5\text{V}$  (except where otherwise noted). Typical values are at  $T_A=23^{\circ}\text{C}$ .

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Range <sup>1</sup>	VCC	Functional operation guaranteed by design	4.0		6.0	V
Feed Back Threshold	V <sub>FBT</sub>	$4.0\text{V} \leq V_{CC} \leq 6.0\text{V}$	784	800	816	mV
FB Input Current	I <sub>FB</sub>	V <sub>FB</sub> = 0.81V		40	75	nA
Error Amplifier	BW	Closed Loop		200		KHz
Quiescent Operating Current	I <sub>Q</sub> (Pin 4)	V <sub>FB</sub> > 0.825V, R <sub>LOAD</sub> Switch Pin < 1K $\Omega$		500	850	$\mu\text{A}$
Soft Start, V <sub>OUT</sub> Slew Rate	V <sub>O</sub>	Initial Power On or after Short Circuit		21	50	V/mS
P-Channel Switch ON Resistance	R <sub>DS(ON)</sub>	I <sub>SW</sub> = 1.0A		0.375	0.6	$\Omega$
Maximum Duty Cycle	D	I <sub>SW</sub> = 1.0A (assured by design, not ATE tested)		80		%
SW Leakage Current	I <sub>LEAK</sub>	V <sub>FB</sub> = 0.825V		0.01	5	$\mu\text{A}$
UVLO	Under Voltage Lockout	VCC Rising			3.00	V
	Under Voltage Lockout	VCC Falling	2.4			
	UVLO Hysteresis			0.15		
P-Channel Current Limit <sup>2</sup>	I <sub>LIM</sub>	Peak Current at Switch Pin (not DC current)	1.50	2.30		A
PWM Frequency	F <sub>OP-PWM</sub>	PWM Mode	820	1200	1920	KHz
PFM Mode Region	I <sub>O</sub>	PFM Mode Load Current Crossover		100		mA
Feed Back PSRR		1Hz < Frequency VCC < 10KHz		-40		dB
Closed Loop Load Regulation	Load Reg	V <sub>O</sub> = 1.2V, 50mA $\leq$ I <sub>O</sub> $\leq$ 1.0A, ckt figure 1		0.85		%V <sub>O</sub>
Thermal Shutdown	T <sub>SD</sub>	(assured by design, not ATE tested)	135	150		$^{\circ}\text{C}$

 Note 1: V<sub>IN</sub> vs V<sub>OUT</sub> ratio @ 1.0A LOAD IS SET AT V<sub>IN</sub> = V<sub>OUT</sub> + 1.0V

 Note 2: 1.0 amp operation @ 70 $^{\circ}\text{C}$  ambient depends on adequate heat sinking to keep T<sub>j</sub> below 125 $^{\circ}\text{C}$

**SIMPLIFIED BLOCK DIAGRAM**

**Figure 2 – LX1912 Block Diagram**
**PCB LAYOUT**

**Figure 3 – PCB Layout Considerations**

**APPLICATION NOTE****FUNCTIONAL DESCRIPTION**

The LX1912 is a Current Mode PWM regulator with internal compensation.

The internal PMOS high side switch is protected with current limit on a pulse by pulse basis and with thermal shutdown. Thermal shutdown is activated with a junction temperature of 160°C (typical) and has 20°C of hysteresis.

The regulator has an internal Power On Reset delay of 50-100µs to ensure all circuitry is operating before enabling the Switch output.

Soft Start is activated upon initial power-on, or following recovery from either thermal shutdown or short circuit. The Soft start control block generates a voltage ramp that clamps the error amplifier non-inverting reference voltage. As this clamp voltage rises, the duty cycle is gradually increased, thus limiting the peak inrush currents.

PWM / PFM mode of operation is determined by the load current condition. The PFM mode increases system efficiency by reducing the switching frequency thus switching losses. During light loading,  $I_{OUT} < 200\text{mA}$  typically, PFM mode becomes active, the switching frequency begins to decrease, the frequency change occurs over a continuous range, decreasing further as  $I_{OUT}$  decreases.

**OUTPUT OVER VOLTAGE PROTECTION**

The over voltage comparator compares the FB pin voltage to a voltage that is 15% higher than the internal referenced VREF. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

**OUTPUT VOLTAGE PROGRAMMING**

Resistors R1 and R2 program the output voltage. The total impedance of both feedback resistors should not exceed 50K Ohms to ensure optimal frequency stability. The value of R1 can be determined using the following equation, note VREF is also referred to as VFBT.

$$R1 = R2 \left[ \left( \frac{V_{OUT}}{V_{REF}} \right) - 1 \right]$$

**DIODE SELECTION**

A Schottky diode is required for switching speed and low forward voltage. Efficiency is determined mostly by the diode's forward voltage. The diode conducts 1-D%, for  $V_{OUT} = 1.2\text{V}$  this becomes 76% in a 5V system.

**INDUCTOR SELECTION**

Selecting the appropriate inductor type and value ensures optimal performance of the converter circuit for the intended application. A primary consideration requires the selection of an inductor that will not saturate at the peak current level. EMI, output voltage ripple, and overall circuit efficiency affect inductor choice. The inductor that works best depends upon the application's requirements and some experimentation with actual devices in-circuit is typically necessary to make the most effective choice.

**INDUCTOR SELECTION, CONT.**

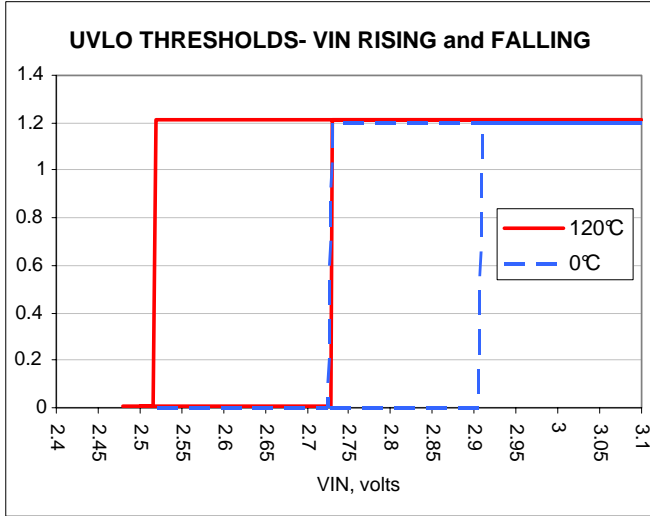
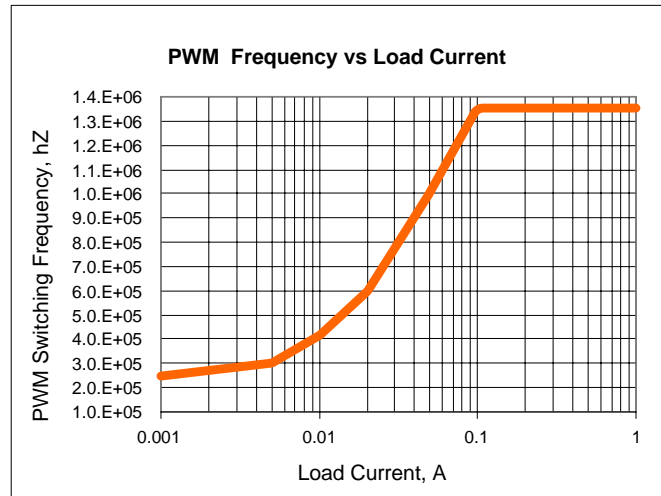
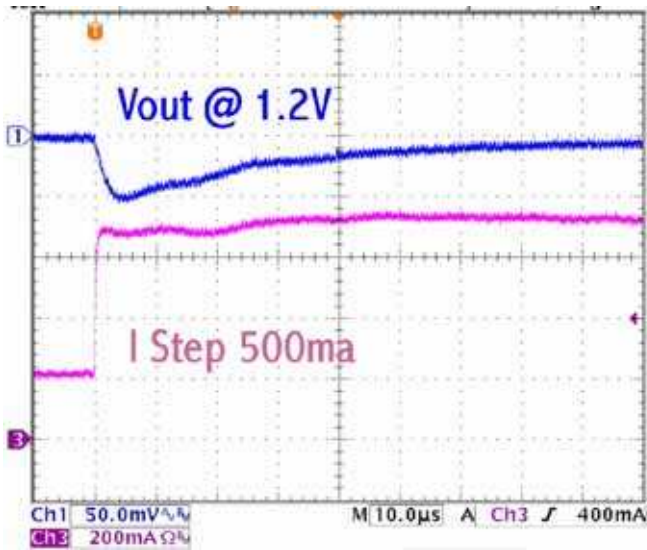
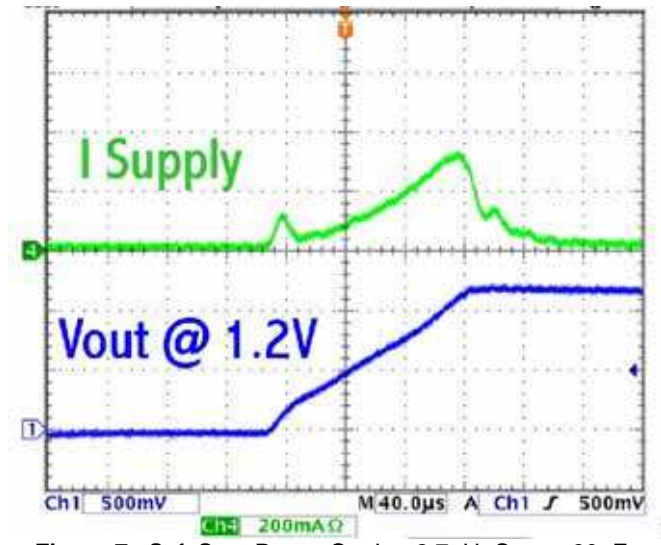
The LX1912 stability performance is optimized by using an inductor value of  $2.7\mu\text{H} \pm 20\%$ . The benefit of a larger inductor value can increase efficiency at the lower output currents and reduces output voltage ripple, thus output capacitance related to ripple filtering. Smaller inductors typically provide smaller package size (critical in many portable applications) at the expense of increasing output ripple current. Regardless of inductor value, selecting a device manufactured with a ferrite-core produces lower losses at higher switching frequencies and thus better overall performance. Larger inductors may lead to diminished Step-Load response.

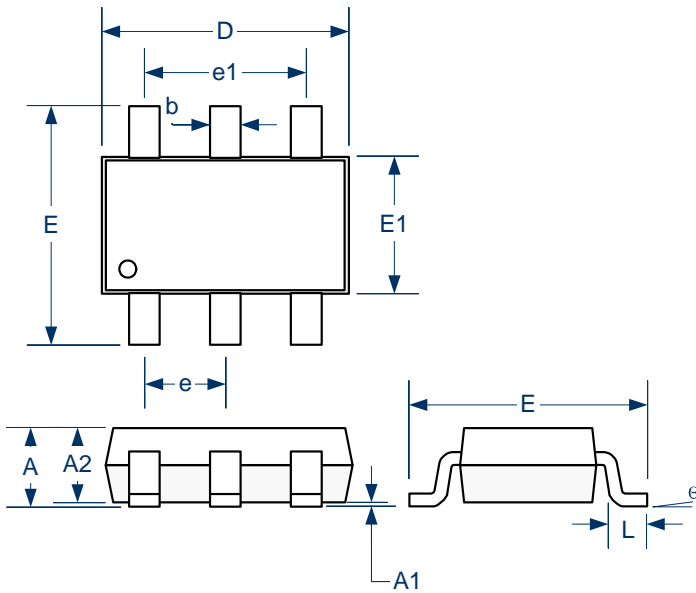
**CAPACITOR SELECTION**

To minimize ripple voltage, output capacitors with a low series resistance (ESR) are recommended. Multi-layer ceramic capacitors with X5R or X7R dielectric make an effective choice because they feature small size, very low ESR, a temperature stable dielectric, and can be connected in parallel to increase capacitance. Typical output capacitance values of 20 to 60µF have proven effective. Other low ESR capacitors such as solid tantalum, specialty polymer, or organic semiconductor, make effective choices provided that the capacitor is properly rated for the output voltage and ripple current. Finally, choose an input capacitor of sufficient size to effectively decouple the input voltage source impedance (e.g.,  $C_{IN} \geq 4.7\mu\text{F}$ ).

**LAYOUT CONSIDERATIONS**

The high peak currents and switching frequencies present in DC/DC converter applications require careful attention to device layout for optimal performance. Basic design rules include: (1) maintaining wide traces for power components (e.g., width > 50mils); (2) place CIN, COUT, the Schottky diode, and the inductor close to the LX1912; (3) minimizing trace capacitance by reducing the etch area connecting the SW pin to the inductor; and (4) minimizing the etch length to the FB pin to reduce noise coupling into this high impedance sense input. Other considerations include placing a 0.1µF capacitor between the LX1912 VOUT pin and GND pin to reduce high frequency noise and decoupling the VCC, VPWR pins using a 0.1µF capacitor.

**CHARACTERISTIC CURVES**

**Figure 4– Under Voltage Lockout for  $V_{IN}$** 

**Figure 5 – PFM / PWM Range of Output Switch**

**Figure 6 – Step Load Response 300mA to 800mA,  $L = 2.7\mu\text{H}$ ,  $C_{OUT} = 30\mu\text{F}$** 

**Figure 7– Soft Start Power On,  $L = 2.7\mu\text{H}$ ,  $C_{OUT} = 30\mu\text{F}$ ,  $I_{OUT} = 0\text{mA}_{DC}$**

**PACKAGE DIMENSIONS**
**SG 6 Pin TSOT**


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.00	-	0.039
A1	0.01	0.10	0.0004	0.004
A2	0.84	0.90	0.033	0.035
b	0.30	0.45	0.012	0.018
c	0.12	0.20	0.005	0.008
D	2.90 BSC		0.114 BSC	
E	2.80 BSC		0.110 BSC	
E1	1.60 BSC		0.063 BSC	
e1	1.90 BSC		0.075 BSC	
e	0.095 BSC		0.037 BSC	
L	0.30	0.50	0.012	
L2	0.25 BSC		0.010 BSC	

**Note:**

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.15mm (.006") on any side. Lead Dimension shall not include solder coverage.



**Microsemi**<sup>®</sup>

**LX1912**

**VREF @ 800mV, 1.0A, 1.2MHz PWM**

**PRODUCTION DATA SHEET**

**NOTES**

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