AKD4679-A

AK4679 Evaluation Board Rev.1

GENERAL DESCRIPTION

The AKD4679-A is an evaluation board for AK4679, 24bit stereo CODEC with Microphone/ Receiver/ Headphone/ Speaker/ Line amplifier as well as HF/Audio DSP. The AKD4679-A has the one Digital Audio I/F and two PCM I/F. It can achieve the interface with digital audio systems via optical connector and 10pin Port connector.

■ Ordering Guide

AKD4679-A --- Evaluation board for AK4679A

FUNCTION

- **DIR/DIT with optical input/output**
- **10pin Header for Digital Audio I/F and PCM I/F (Baseband, Bluetooth)**
- **BNC connector for an external clock input**
- **10pin Header for I^2C control mode**

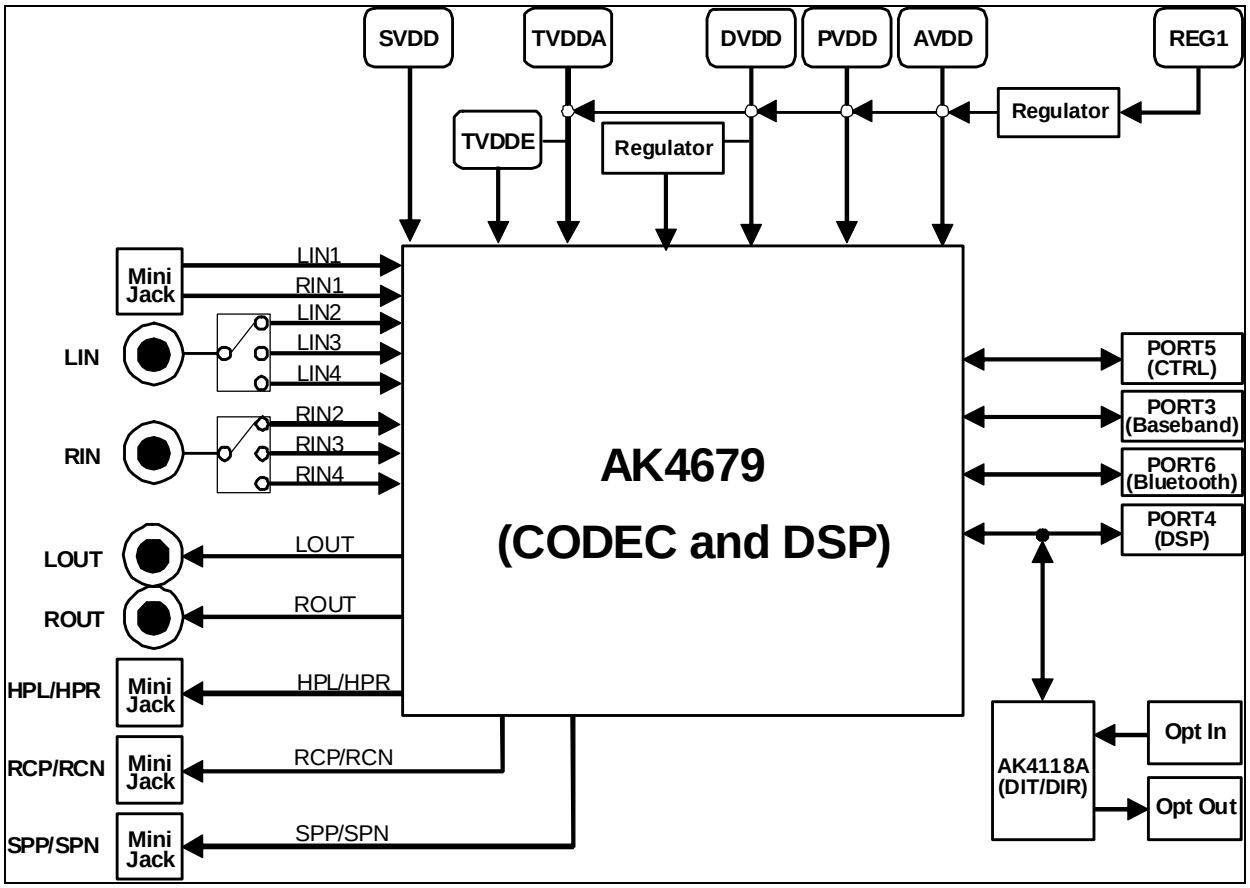

Figure 1. AKD4679-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation Sequence

1) Set up the Power Supply Lines.

Name of jack	Color of jack	Used for	Open / Connect	Default Setting
REG1	Red	Regulator T1: AVDD, DVDD, PVDD and TVDD of AK4679, VCC1 and VCC2 of Digital Logic.	Should be always connected when default setting.	+4.2V
SVDD	Orange	SVDD of AK4679.	Should be always connected.	+4.2V
AVDD	Orange	AVDD of AK4679.	Should be always connected when AVDD of AK4679 is not supplied from regulator T1. In this case, “JP20” is set to “Open”.	Open
DVDD	Orange	DVDD of AK4679.	Should be always connected when DVDD of AK4679 is not supplied from regulator T1. In this case, “JP26” is set to “Open”.	Open
PVDD	Orange	PVDD of AK4679.	Should be always connected when PVDD of AK4679 is not supplied from regulator T1. In this case, “JP24” is set to “Open”.	Open
TVDD1	Orange	TVDDA , TVDDE of AK4679.	Should be always connected when TVDDA, TVDDE of AK4679 is not supplied from regulator T1. In this case, “JP29” is set to “Open” and the supplied voltage should be the same as TVDD1.	Open
VCC1	Orange	Digital Logic.	Should be always connected when Digital Logic is not supplied from regulator T1. In this case, “JP31” is set to “Open” and the supplied voltage should be the same as TVDD1.	Open
VCC2	Orange	Digital Logic.	Should be always connected when Digital Logic is not supplied from regulator T1. In this case, “JP66” is set to “Open” and the supplied voltage should be the same as TVDD1.	Open
D3V	Orange	Digital Logic and AK4118A.	Should be always connected.	+3.3V
AGND	Black	Analog Ground	Should be always connected	GND
DGND	Black	Digital Ground	Should be always connected	GND

Table 1. Set up the power supply lines

Each supply line should be distributed from the power supply unit.

2) Setup the Audio I/F Evaluation Mode.

(a) Evaluation of A/D using DIT of AK4118A

(b) Evaluation of D/A using DIT of AK4118A

(c) Evaluation of A/D using interface signals are fed externally.

(b) Evaluation of D/A using interface signals are fed externally.

3) Setup the PCM I/F evaluation mode.

(a) SYNCA and BICKA are fed from on-board clock generator.

(b) SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

(c) SYNCB and BICKB are fed from on-board clock generator.

(d) SYNCB and BICKB are fed externally via PORT6 (Bluetooth Module).

4) Jumper pins and SW Setting

5) Power on.

The AK4679 should be reset once bringing SW2 (PDN) “L” upon power-up.

2) Setup the Audio I/F Evaluation Mode.

■Clock Mode

External Slave Mode

In case of AK4679 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4679 and AK4118A.
The AK4118A must be set to master mode.

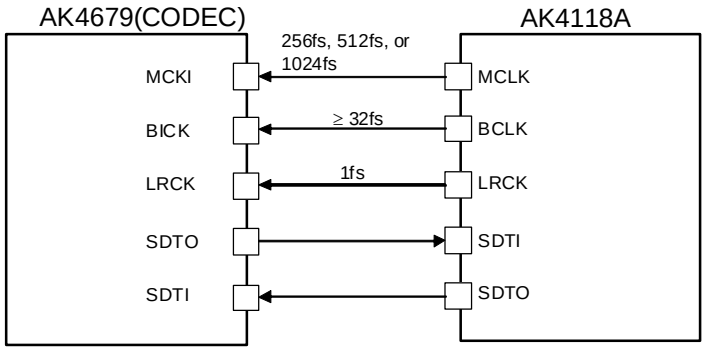

Figure 2. EXT Slave Mode

PLL Slave Mode

In case of AK4679 evaluation using external clock, it is necessary to correspond to audio interface format for AK4679.

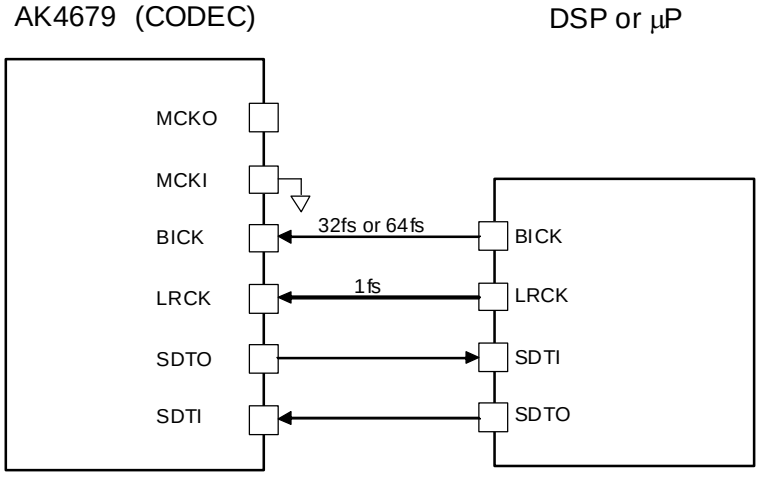

Figure 3. PLL Slave Mode (PLL Reference Clock: BICK pin)

■Board Setting

1) R108, R109, R110, R111, R114, R115, R116, R117 must be set to open.

2) R108 pad and CL104 Pad (1) , R109 pad and CL105 Pad (1), R110 pad and CL106 Pad (1), R111 pad and CL107 Pad (1) must be connected.
CL104 Pad (2), CL106 Pad (2), CL107 Pad (2) must be connected to GND.

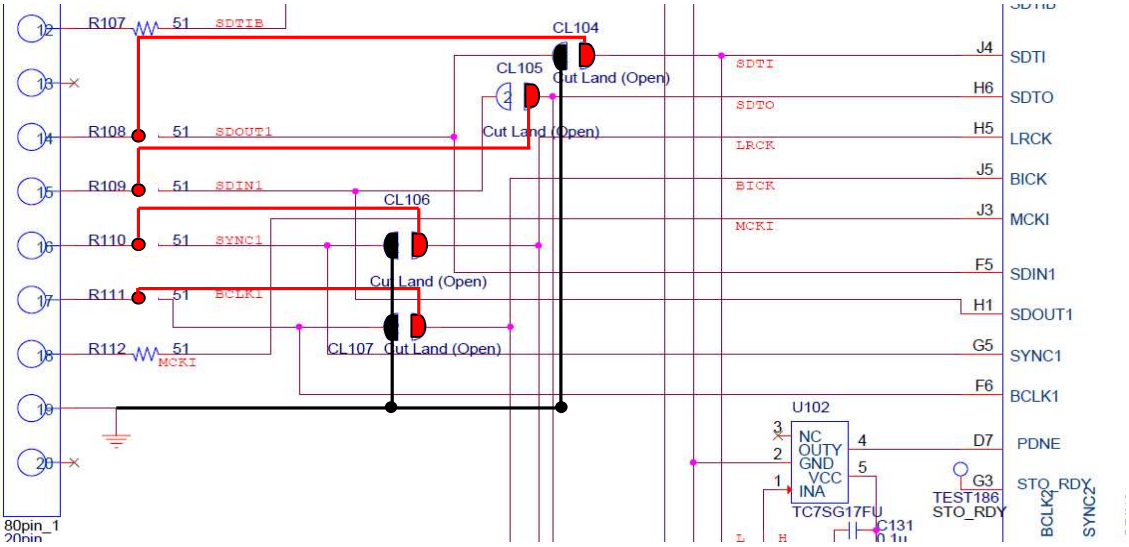

Figure 4. A/D and D/A board setting

(a) Evaluation of A/D using DIT of AK4118A

(a-1) Clock Mode: Ext Slave Mode

(a-2) Jumper Setting

X2(X'TAL) and PORT2(DIT) are used. Nothing should be connected to PORT1(DIR), PORT4(DSP) and J12(EXT).

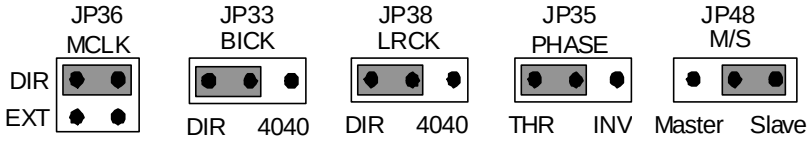

Figure 5. Setting of evaluation of A/D using DIT of AK4118A

*** JP50, JP51, JP53~55, JP60~65: Open**

(a-3) Board Setting: Figure 4

(a-4) Path Setting

Example of path Setting: LineIN1→ADC→SDTO

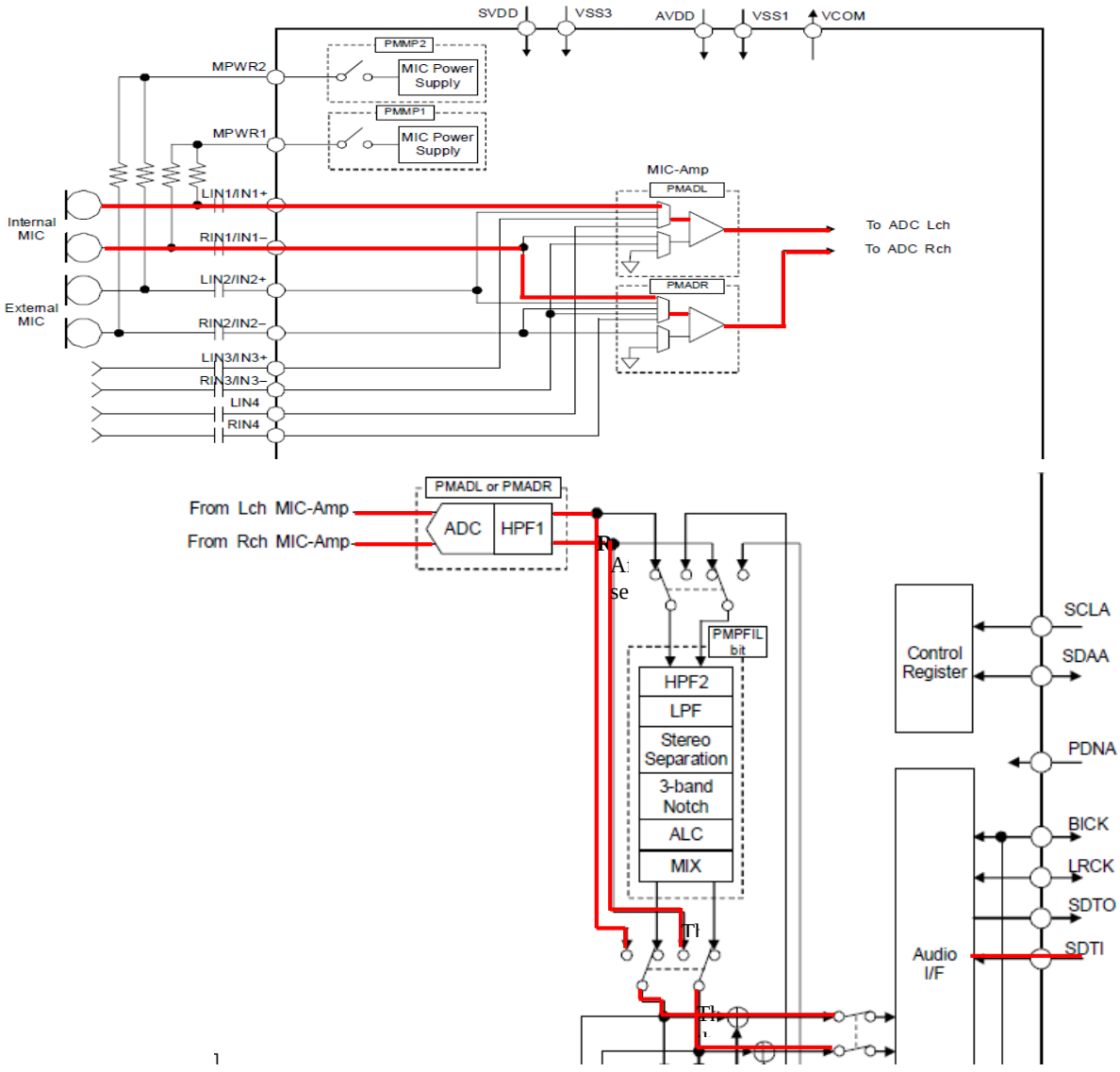

Figure 6. Example of A/D Path setting

(b) Evaluation of D/A using DIR of AK4118A

(b-1) Clock Mode: Ext Slave Mode

(b-2) Jumper Setting

PORT1(DIR) is used. Nothing should be connected to PORT2(DIT), PORT4(DSP), X2(X'TAL) and J12(EXT).

Figure 7. Setting of D/A using DIR of AK4118A

***JP50, JP51, JP53~55, JP60~65: Open**

(b-3) Board Setting: Figure 4

(b-4) Path Setting

Example of path Setting: SDTI→DAC→Lineout

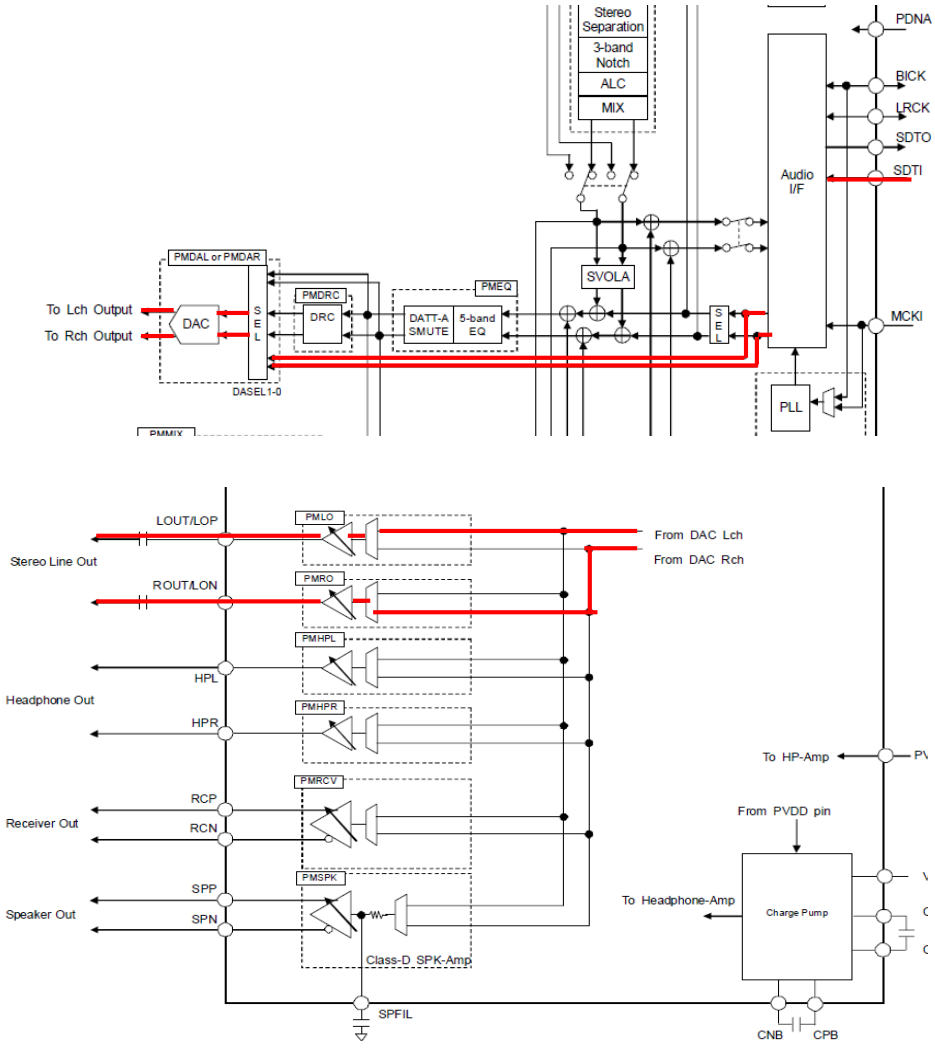

Figure 8. Example of D/A Path setting

(c) Evaluation of A/D using interface signals are fed externally.

(c-1) Clock Mode: PLL Slave Mode

(c-2) Jumper Setting

PORT3 (Baseband) and JP105 (DSP2) are used. Nothing should be connected to PORT1(DIR), PORT2(DIT), PORT4(DSP), X2(X'TAL) and J12(EXT).

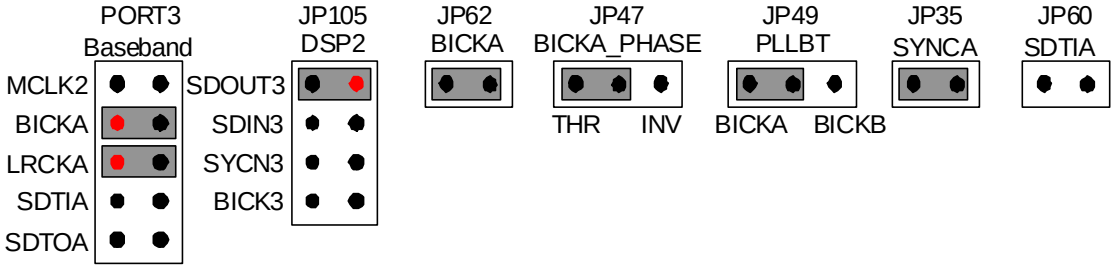

Figure 9. Setting of A/D using external clock

*** JP33~JP38, JP43, JP45, JP48, JP51, JP53~55, JP61, JP64, JP65: Open**

(c-3) Board Setting: Default

(c-4) Path Setting

Example of path Setting: LineIN1→ADC→SDTOA

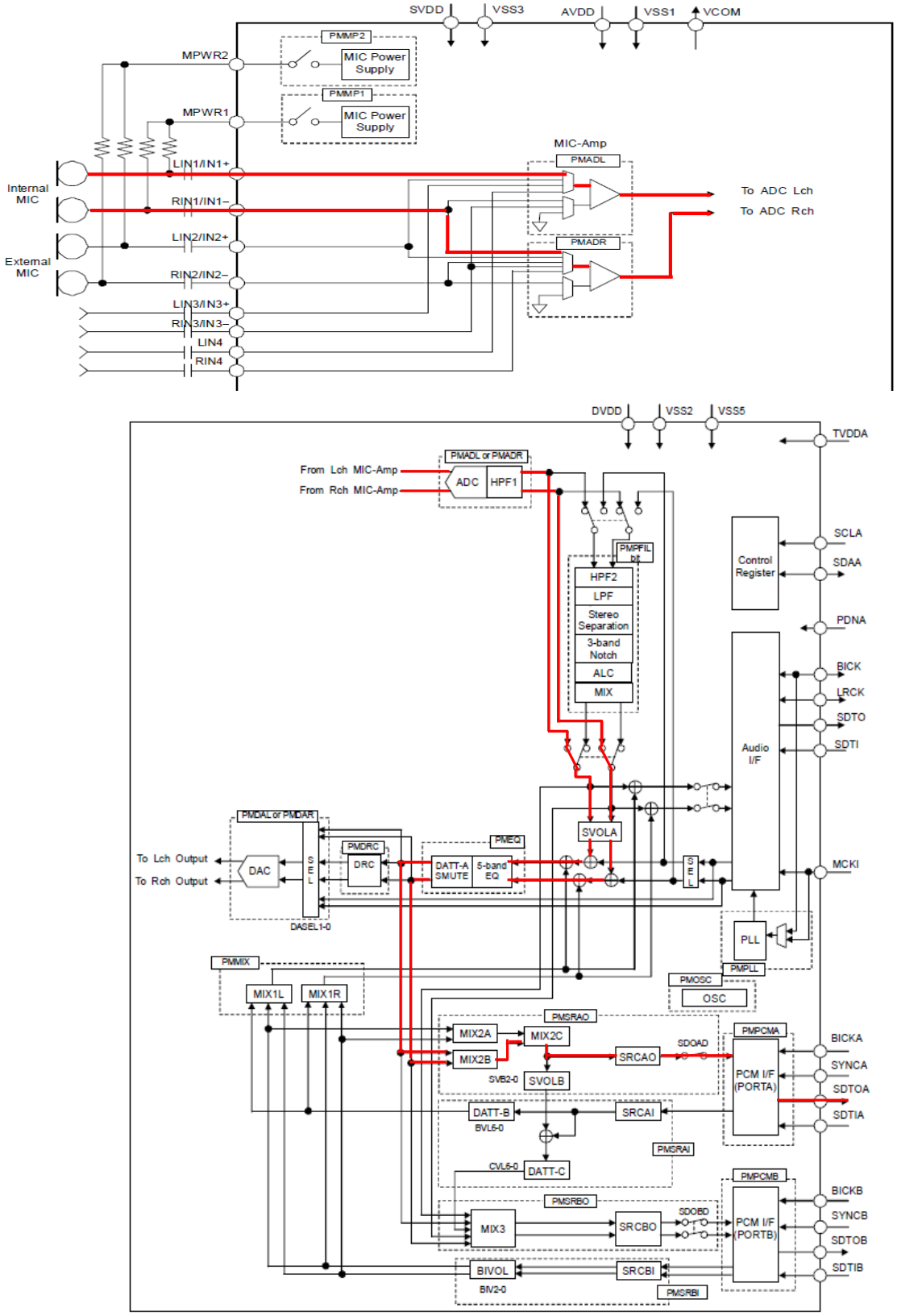

Figure 10. Example of A/D Path setting2

(d) Evaluation of D/A using interface signals are fed externally.

(d-1) Clock Mode: PLL Slave Mode

(d-2) Jumper Setting

PORT3 (Baseband) is used. Nothing should be connected to PORT1(DIR), PORT2(DIT), PORT4(DSP), X2(X'TAL) and J12(EXT).

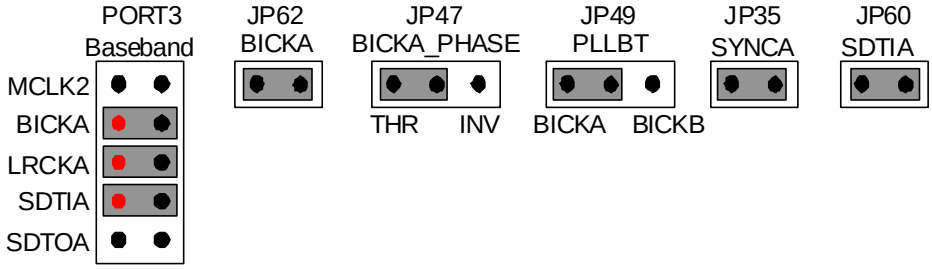

Figure 11. Setting of D/A using external clock

***JP33~JP38, JP43, JP45, JP48, JP51, JP53~55, JP61, JP64, JP65: Open**

(d-3) Board Setting: Default

(d-4) Path Setting

Example of path Setting：SDTIA→DAC→Lineout

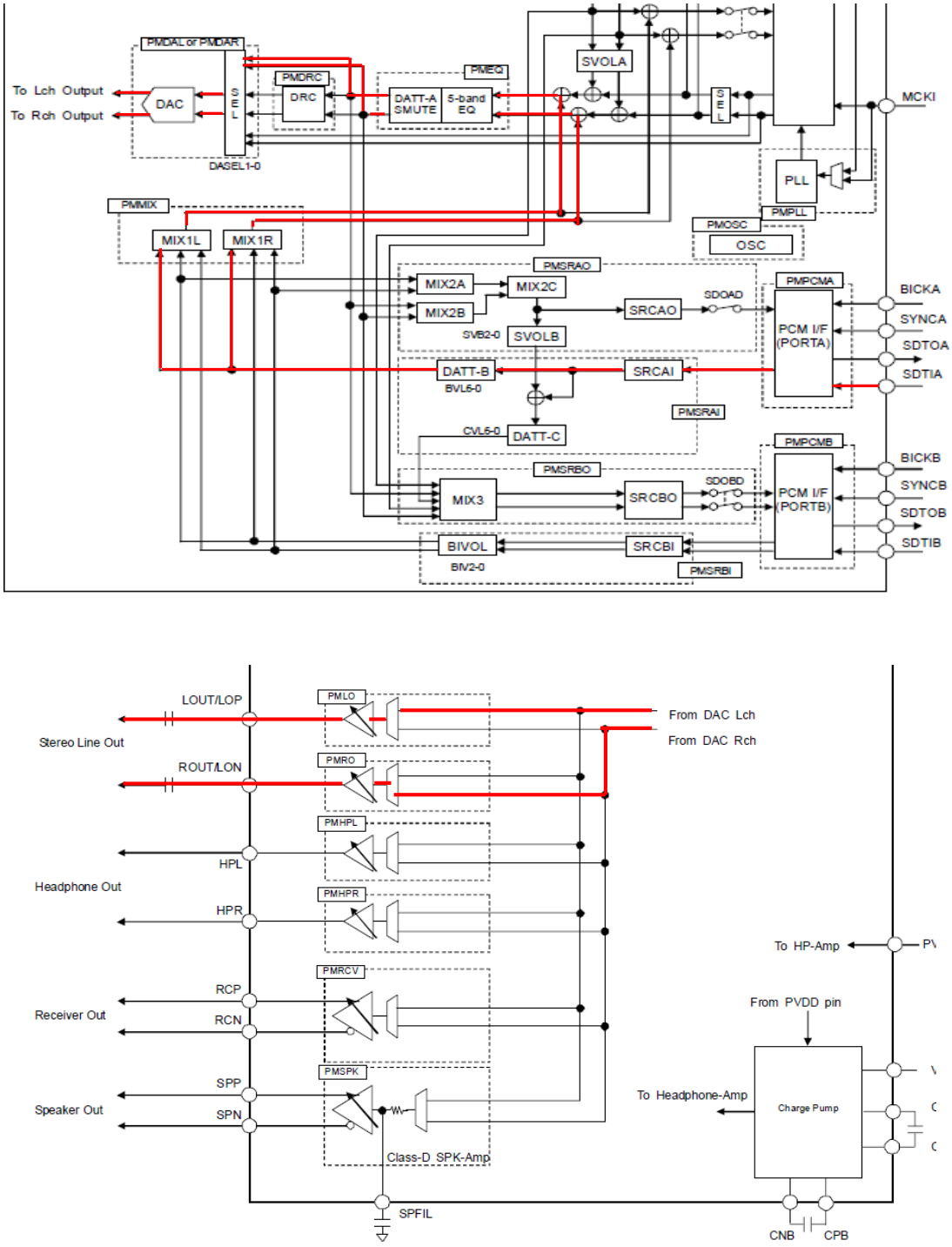

Figure 12. Example of D/A Path setting2

3) Setup the PCM I/F Evaluation Mode

■Clock Setting

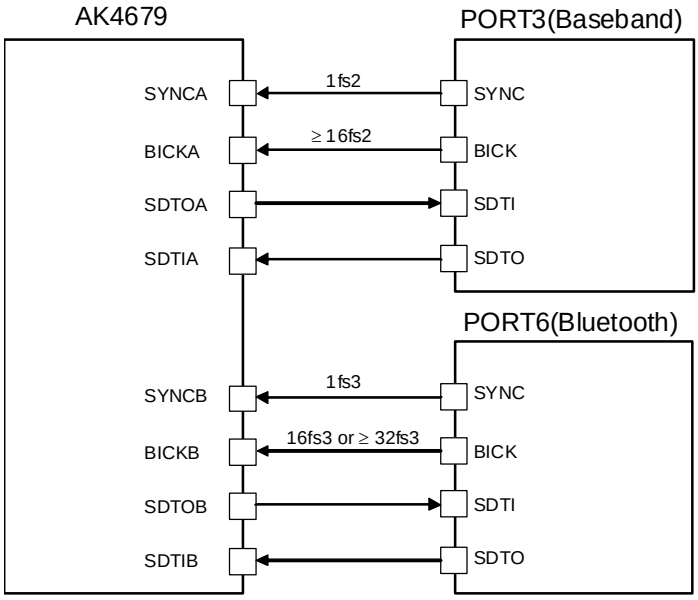

Figure 13. PCM I/F A and B

■Board Setting

1) R108, R109, R110, R111, R114, R115, R116, R117 must be set to open.

2) CL108, CL109, CL110 must be set to open.

3) R108 pad and CL104 Pad (1), R109 pad and CL105 Pad (1), R110 pad and CL106 Pad (1), R111 pad and CL107 Pad (1) must be connected.
CL104 Pad (2), CL106 Pad (2), CL107 Pad (2) must be connected to GND.

4) R114 pad and CL108 Pad (1), R115 pad and CL109 Pad (1), R116 pad and CL110 Pad (1), R117 pad and CN102 34pin must be connected.

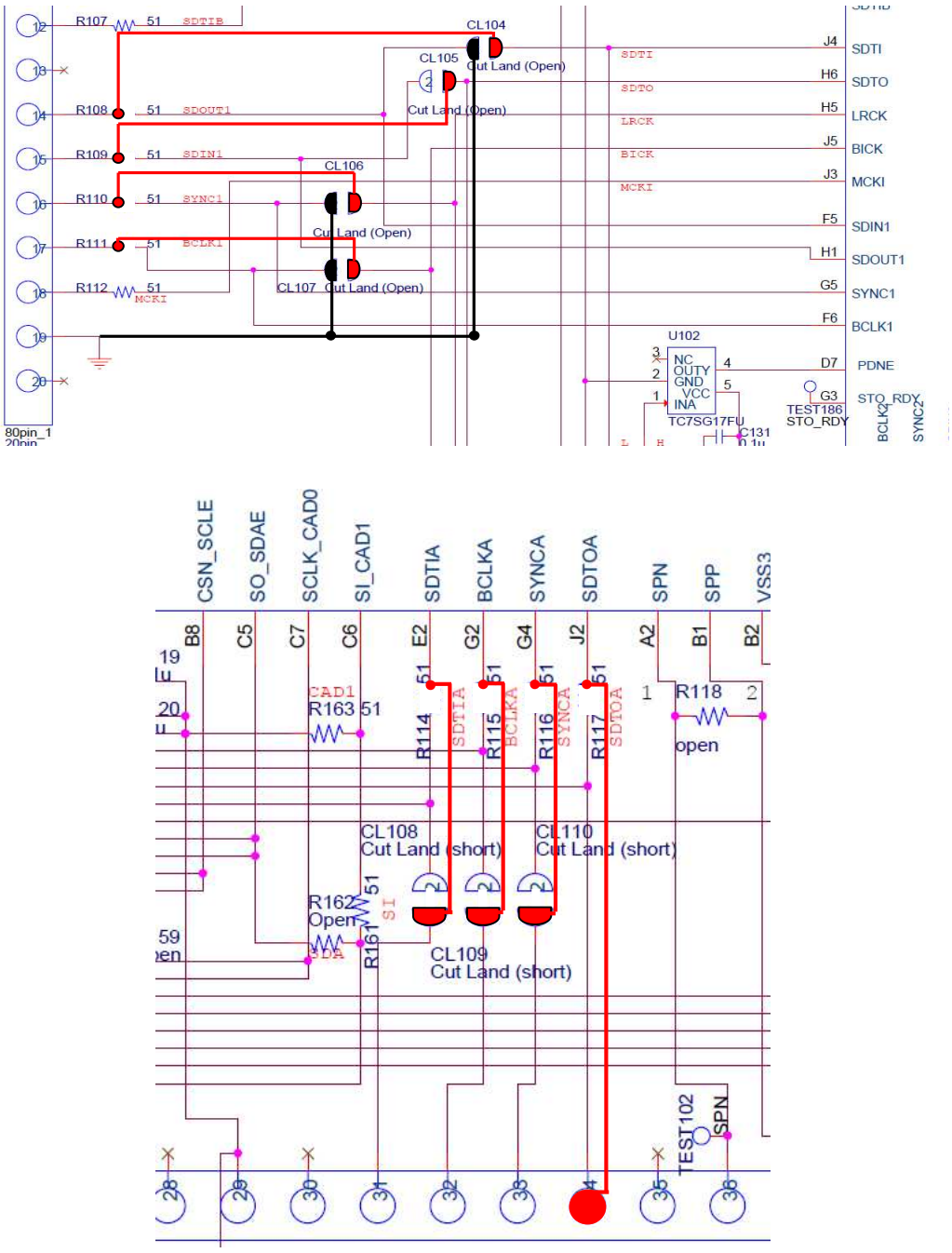

Figure 14. PCM I/F board setting

(3-1). PCM I/F A

(a) SYNCA and BICKA are fed from on-board clock generator.

X1(X'Tal) and PORT3(Baseband) are used. Nothing should be connected to PORT6(Bluetooth).
Please set JP42 (BCFS2) to the required frequency. Follows are setting in BICKA=32fs.

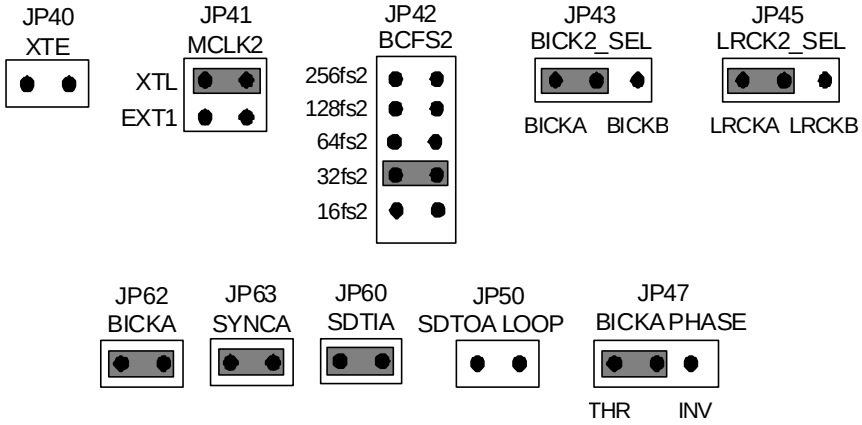

Figure 15. Setting of SYNCA and BICKA are fed from on-board clock generator.

JP47 (BICKA PHASE) is jumper which decides polarity of BICKA, "THR" or "INV" should be selected according to the PCM I/F format.
In case of loop-back "SDTOA → SDTIA", JP50 (SDTOA LOOP) is set to "SHORT".

(b) SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

PORT3 (Baseband Module) is used.
SYNCA and BICKA should be supplied from PORT3.

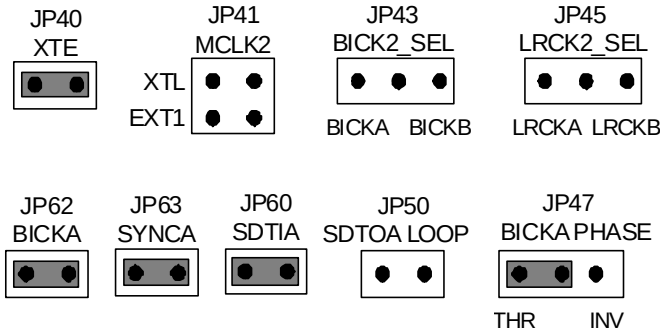

Figure 16. Setting of SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

JP47 (BICKA PHASE) is jumper which decides polarity of BICKA, "THR" or "INV" should be selected according to the PCM I/F format.
In case of loop-back "SDTOA → SDTIA", JP50 (SDTOA LOOP) is set to "SHORT".

(3-2). PCM I/F B

(a) SYNCB and BICKB are fed from on-board clock generator.

X1(X'Tal) and PORT6(Bluetooth) are used. Nothing should be connected to PORT3(Baseband).
Please set JP42 (BCFS2) to the required frequency. Follows are setting in BICKB=32fs.

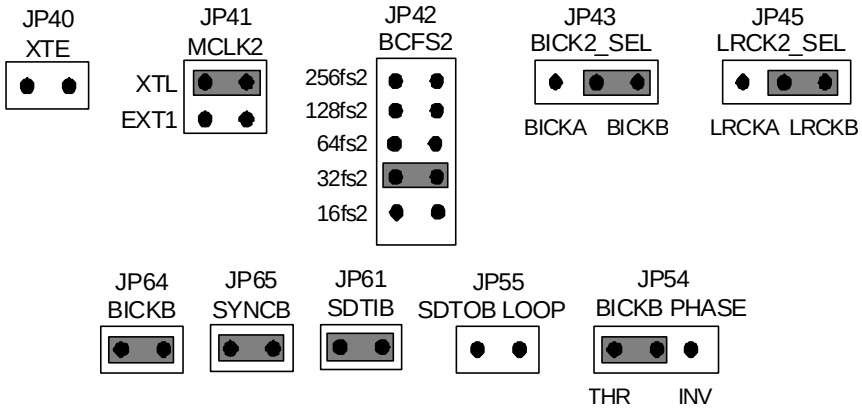

Figure 17. Setting of SYNCB and BICKB are fed from on-board clock generator.

JP54 (BICKB PHASE) is jumper which decides polarity of BICKB, "THR" or "INV" should be selected according to the PCM I/F format.
In case of loop-back "SDTOB → SDTIB", JP55 (SDTOB LOOP) is set to "SHORT".

(b) SYNCB and BICKB are fed externally via PORT6 (Bluetooth Module).

PORT6 (Bluetooth Module) is used.
SYNCB and BICKB should be supplied from PORT6.

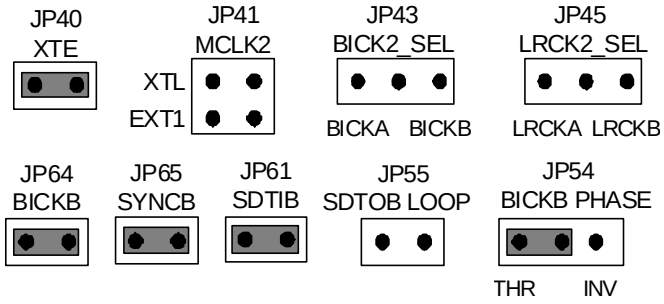

Figure 18. Setting of SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

JP54 (BICKB PHASE) is jumper which decides polarity of BICKB, "THR" or "INV" should be selected according to the PCM I/F format.
In case of loop-back "SDTOB → SDTIB", JP55 (SDTOB LOOP) is set to "SHORT".

4) Other Jumper pins Setup

[JP16 (LOUT_SEL)]: The selection of output signal to J1(BNC jack) connector.
LOUT : Connect to LOUT signal. (Default)
HPL : Connect to HPL signal.

[JP17 (HPL JACK)]: The selection of analog signal of HPL pin
SHORT : Analog signal of HPL pin is output from J3 (mini jack) connector. (Default)
OPEN : Analog signal of HPL pin is output from J1 (BNC jack) connector.

[JP19 (HPR JACK)]: The selection of analog signal of HPR pin
SHORT : Analog signal of HPR pin is output from J3 (mini jack) connector. (Default)
OPEN : Analog signal of HPR pin is output from J4 (BNC jack) connector.

[JP20 (AVDD_SEL)]: The selection of AVDD.
SHORT : AVDD is supplied from the regulator (“AVDD” jack should be open). (Default)
OPEN : AVDD is supplied from “AVDD” jack.

[JP21 (ROUT_SEL)]: The selection of output signal to J4(BNC jack) connector.
ROUT : Connect to ROUT signal. (Default)
HPR : Connect to HPR signal.

[JP23 (LIN_SEL)]: The selection of input signal from J5(BNC jack) connector.
LIN2 : Connect to LIN2/IN2+ pin. (Default)
LIN3 : Connect to LIN3/IN3+ pin.
LIN4 : Connect to LIN4 pin.

[JP24 (PVDD_SEL)]: The selection of PVDD.
SHORT : PVDD is supplied from the regulator (“PVDD” jack should be open). (Default)
OPEN : PVDD is supplied from “PVDD” jack.

[JP25 (RIN_SEL)]: The selection of input signal from J7(BNC jack) connector.
RIN2 : Connect to RIN2/IN2- pin. (Default)
RIN3 : Connect to RIN3/IN3- pin.
RIN4 : Connect to RIN4 pin.

[JP26 (DVDD_SEL)]: The selection of DVDD.
SHORT : DVDD is supplied from the regulator (“DVDD” jack should be open). (Default)
OPEN : DVDD is supplied from “DVDD” jack.

[JP29 (TVDD_SEL)]: The selection of TVDD.
SHORT : TVDD is supplied from the regulator (“TVDD” jack should be open). (Default)
OPEN : TVDD is supplied from “TVDD” jack.

[JP30 (GND)]: Analog ground and Digital ground
SHORT : Common. (The connector “DGND” can be open.)
OPEN : Separated. (Default)

[JP31 (VCC_SEL)]: The selection of VCC.
SHORT : VCC is supplied from the regulator (“VCC1” jack should be open). (Default)
OPEN : VCC is supplied from “VCC1” jack.

[JP32 (MKFS)]: The selection of MCLK frequency. (Open)
256fs : 256fs.
512fs : 512fs.
1024fs : 1024fs.
384/768fs: Not to use.

[JP34 (BCFS)]: The selection of BICK frequency. (Open)
64fs-384: Don’t use.
32fs-384: Don’t use.
64fs : 64fs
32fs : 32fs

[JP66 (VCC2_SEL)]: The selection of VCC2.
SHORT : VCC2 is supplied from the regulator (“VCC2” jack should be open). (Default)
OPEN : VCC2 is supplied from “VCC2” jack.

[JP100 (INPUT SEL1)]: The selection of input signal to LIN1/IN1+/DMDAT pin
LIN1/IN1+: Analog signal is input from J2 (mini jack) connector. (Default)
DMDAT : Digital microphone data is input to DMDAT pin.

[JP101 (INPUT SEL2)]: The selection of input signal to RIN1/IN1-/DMCLK pin
RIN1/IN1-: Analog signal is input from J2 (mini jack) connector. (Default)
DMCLK : DMCLK for digital microphone is supplied to CN5.

[JP102 (MPWR1 SEL)]: The selection of Mic-power1.
SHORT : MIC-power1 is supplied.
OPEN : MIC-power1 is not supplied. (Default)

[JP103 (MPWR2 SEL)]: The selection of Mic-power2.
SHORT : MIC-power2 is supplied.
OPEN : MIC-power2 is not supplied. (Default)

[JP104 (DMIC PWR)]: The selection of Mic-power for Digital MIC.
SHORT : MIC-power for Digital MIC is supplied to CN6.
OPEN : MIC-power for Digital MIC is not supplied. (Default)

5) Setup the DIP SW.

Upper-side is “ON(H)” and lower-side is “OFF(L)”.

[S1] (SW DIP-6): Mode setting for AK4679 and AK4118A.

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF2	AK4118A Audio Format Setting See Table 3		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	AK4118A Master Clock Setting : See Table 4		OFF
5	CAD0	Slave Address 0 Input pin		ON
6	I2S	Control Interface Mode Select Pin		ON
		I2S	SPI	

Table 2. Mode Setting for AK4679 and AK4118A

DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
L	L	L	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
L	L	H	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
L	H	L	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
L	H	H	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
H	L	L	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
H	L	H	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
H	H	L	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
H	H	H	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 3. Setting for AK4118A Audio Interface Format

OCKS1	MCKO1	X’tal	
L	256fs	256fs	Default
H	512fs	512fs	

Table 4. Setting for AK4118A Master Clock

■ Function of the Toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (DIR) : Resets the AK4118A. Keep “H” during normal operation.
The AK4118A should be resets once bringing “L” upon power-up.

[SW2] (PDN) : Resets the AK4679. Keep “H” during normal operation.
The AK4679 should be resets once bringing “L” upon power-up.

■ Indication for LED

[LED1] (UNLOCK): Monitor INT0 pin of the AK4118A.
LED turns on when some error has occurred to AK4118A.

■ Control Box

The AKD4679-A should be connected to a PC via an USB control box. The USB control box is connected to a PC with an USB cable and the AKD4679-A with 10-pin flat cable.

Figure 19. Connection of Control Box

■ Analog Input/Output Circuits

(1) Input Circuits

(1-1) LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 Input Circuits

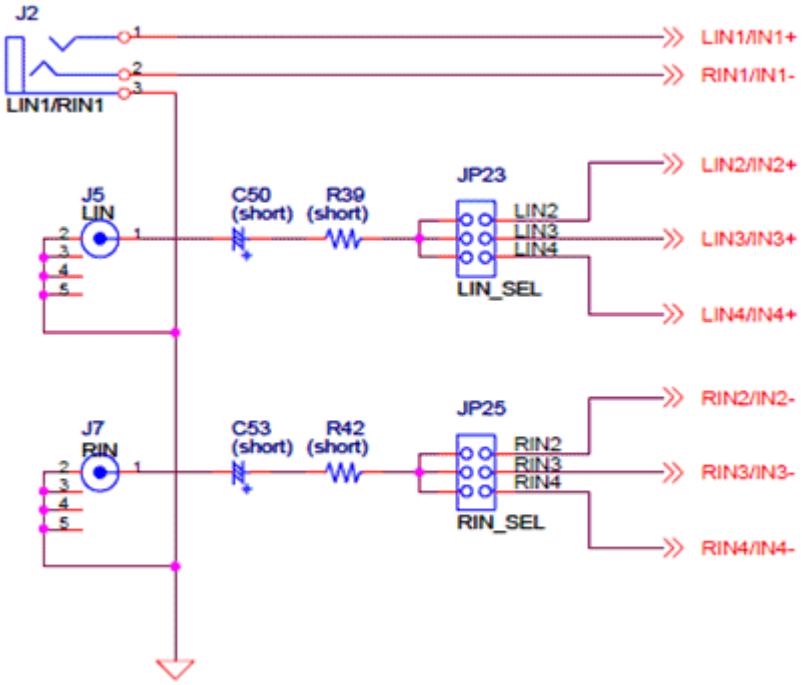

Figure 20. LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 Input Circuits

LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 share J5/J7.
JP23 (LIN_SEL) and JP25 (RIN_SEL) select each path.

(1-2) MIC Power1, MIC Power2 Input Circuits

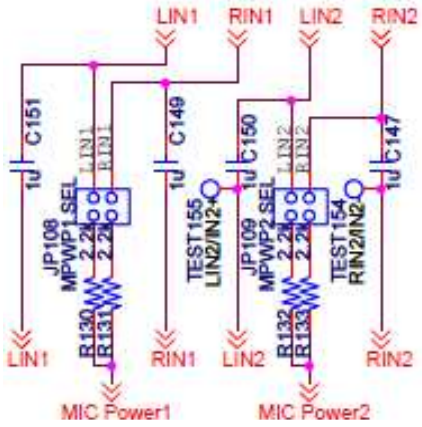

Figure 21. MIC Power1, MIC Power2 Input Circuits

Supplying MIC power1 to LIN1/RIN1 and Supplying MIC Power2 to LIN2/RIN2 are selected by JP108 and JP 109.

(2) Output Circuits

(2-1) LOUT/ROUT and HP Output Circuit

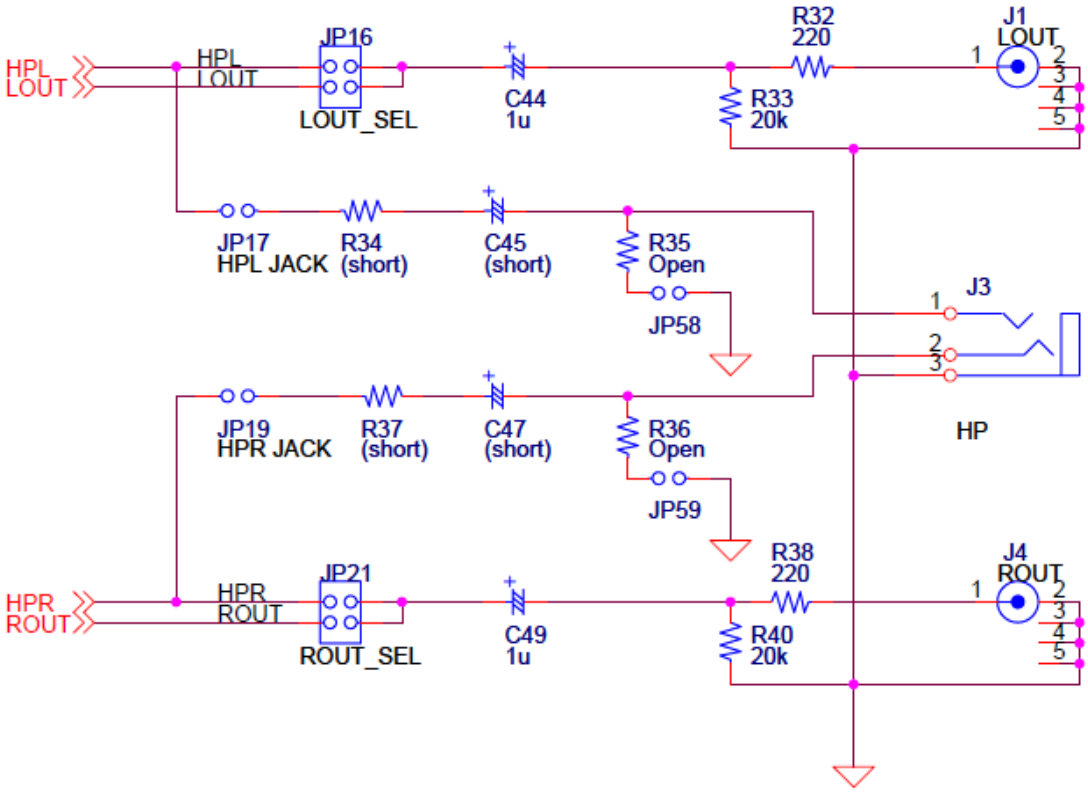

Figure 22. LOUT/ROUT and HP Output Circuit

LOUT/ROUT and HPL/HPR share J1/J4.
JP16 (LOUT_SEL) and JP21 (ROUT_SEL) select each path.

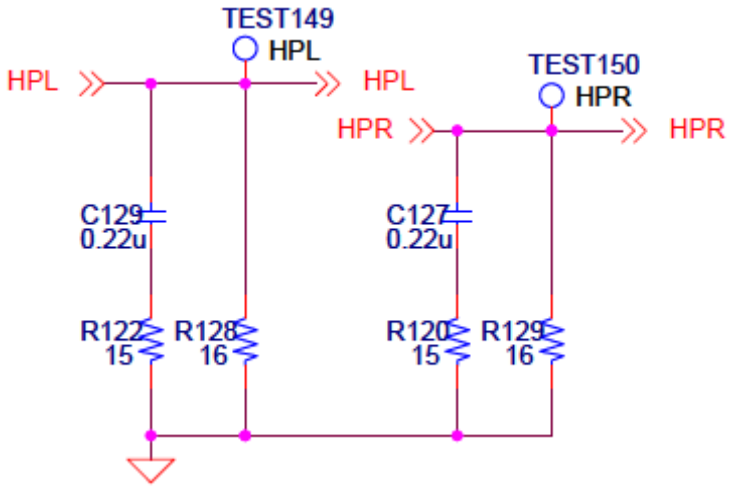

Figure 23. HP-amp Oscillation Prevention Circuit

HP-amp Oscillation Prevention Circuit is composed by C129 and R122.
R128 and R129 are load resistance for HP Output.

(2-2) SPK and RCV Output Circuit

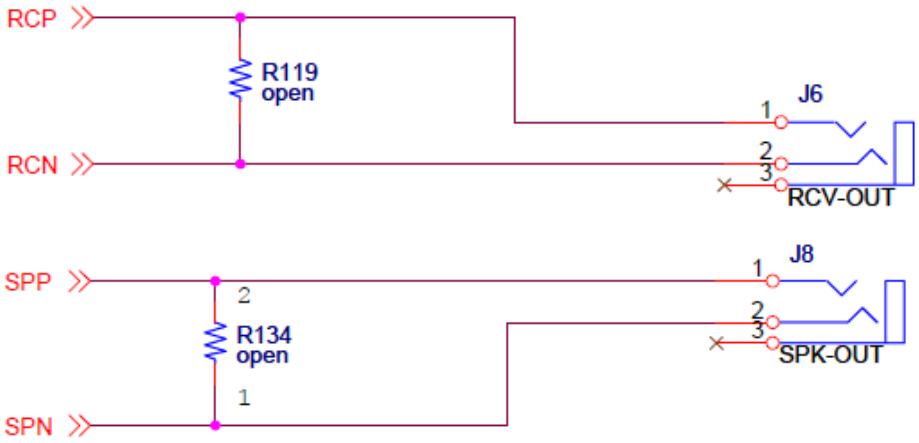

Figure 24. SPK and RCV Output Circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an Control Box by a 10wire flat cable. When running this control soft on the Windows 2000/XP/Vista/7, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver.
3. Then please evaluate according to the following descriptions.

[Support OS]
Windows 2000 / XP / Vista / 7 (32bit) (XP compatible mode is recommended for Vista / 7)
64bit OS's are not supported.
Windows 95 / 98 / Me / NT are not supported.

■ Operation Screen

1. Start up the control program following the process above.
2. After the evaluation board's power is supplied, the AK4679 must be reset once bring SW2 (PDN) "L" to "H", and Click [Dummy Command] button.
3. The operation screen is shown below.

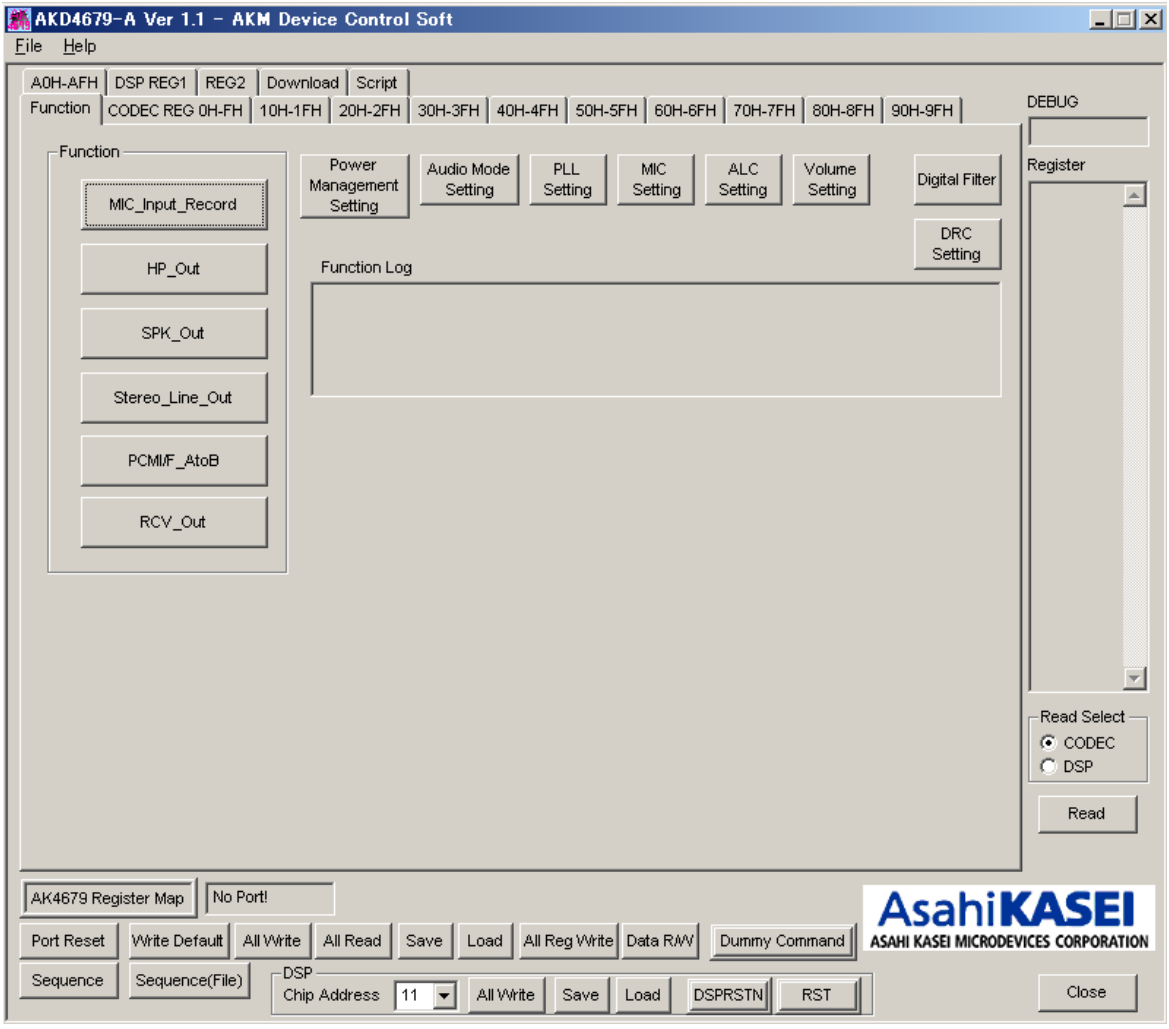

Figure 25. Window of Control Soft

■ Function Button

[MIC_Input_Record]

When [MIC_Input_Record] button is clicked,
[LIN2/RIN2 → MICL/R → ADCL/R → ALC → Audio I/F → SDTO] sequence is set up.
Set up the evaluation board is referred to 2) (a) Evaluation of A/D using DIT of AK4118A.

[HP_Out]

When [HP_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → HPL/HPR] sequence is set up.
Set up the evaluation board is referred to 2) (b) Evaluation of D/A using DIR of AK4118A.

[SPK_Out]

When [SPK_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → SPP/SPN] sequence is set up.
Set up the evaluation board is referred to 2) (b) Evaluation of D/A using DIR of AK4118A.

[Stereo_Line_Out]

When [Stereo_Line_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → LOUT/ROUT] sequence is set up.
Set up the evaluation board is referred to 2) (b) Evaluation of D/A using DIR of AK4118A.

[PCM IF_AtoB]

When [PCMIF_AtoB] button is clicked,
[SDTIA→PCM I/F A→SRCAI→DATT-C→MIX3→PCM I/F B→SDTOB &
SDTIB→PCM I/F B→BIVOL→MIX2A→MIX2C→SRCAO→PCM I/F A→SDTOA] sequence is set up.
Set up the evaluation board is referred to
3) (a) SYNCA and BICKA are fed from on-board clock generator (for PCM I/F A PCM I/F B)
or 3) (c) SYNCB and BICKB are fed from on-board clock generator (for PCM I/F B PCM I/F B)

[RCV_Out]

When [RCV_Out] button is clicked,
[SDTIA→PCM I/F A→SRCAI→DATT-B→MIX1R→5-Band EQ→DATT-A→DACR→RCP/RCN]
sequence is set up.
Set up the evaluation board is referred to
3) (a) SYNCA and BICKA are fed from on-board clock generator

■Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-B)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-B).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset (PDN pin = “L”), use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area
    (on the right of the main window).
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

12. [Dummy Command]: Write a dummy command
    After the evaluation board power is supplied, the AK4679 must be reset once bring SW2 (PDN) “L” to “H”, and then the [Dummy Command] button should be clicked once to reset the register setting of the AK4679.

***Refer to the board manual of AK7719 for a control setup of DSP.**

■ Tab Functions

1. [Function]: Function control

This tab is for function control.
Each operation is executed by the function buttons on the left side of the screen.

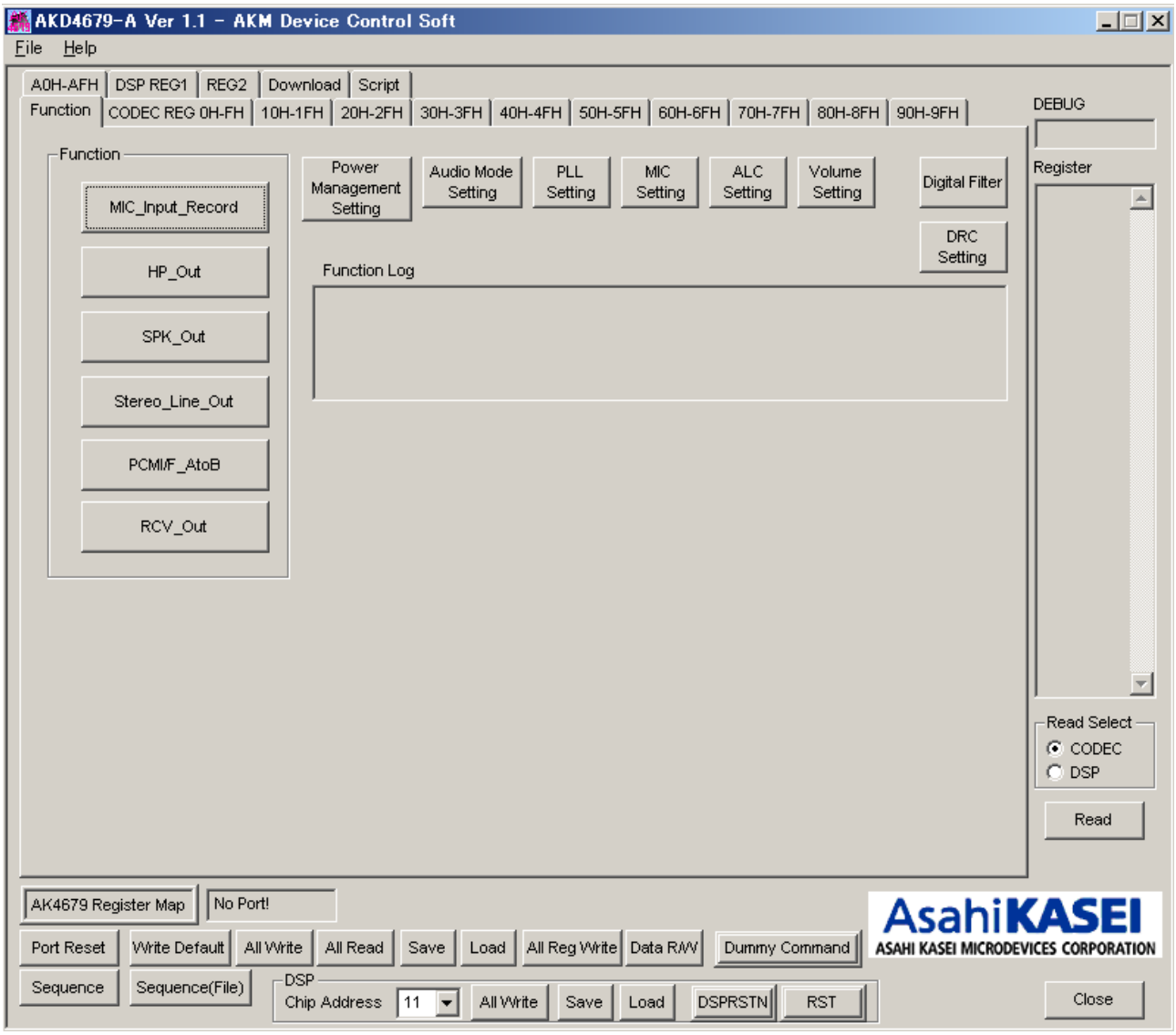

Figure 26. Window of [Function]

1-1. Power Management Setting

When [Power Management Setting] button is clicked, the window as shown in Figure 27 opens.
This window is for Power Management Setting.
Refer to the datasheet for register settings of the AK4679.

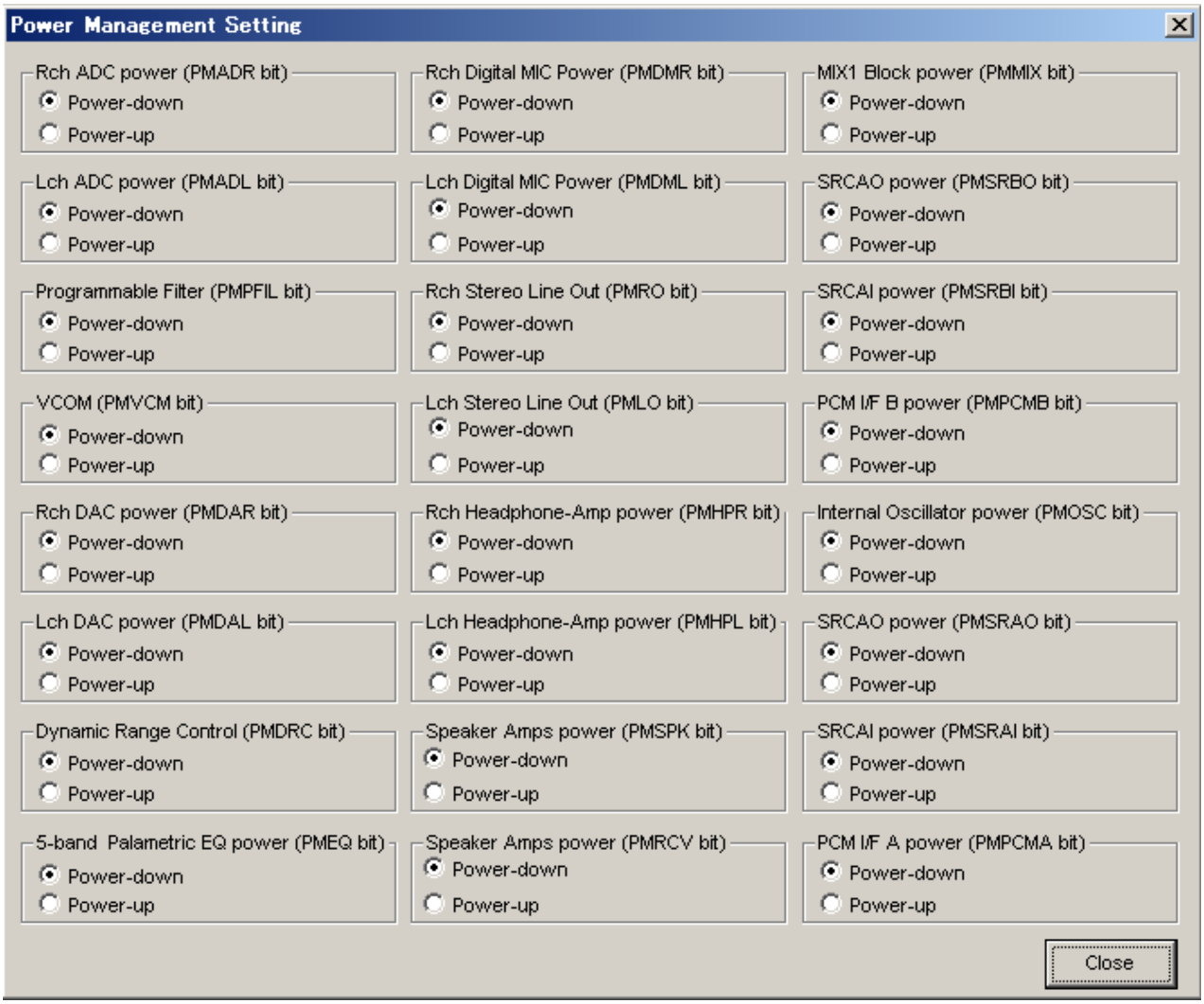

Figure 27. Window of [Power Management Setting]

1-2. Audio Mode Setting

When [Audio Mode] button is clicked, the window as shown in Figure 28 opens.
This window is for Audio Mode Setting.
Refer to the datasheet for register settings of the AK4679.

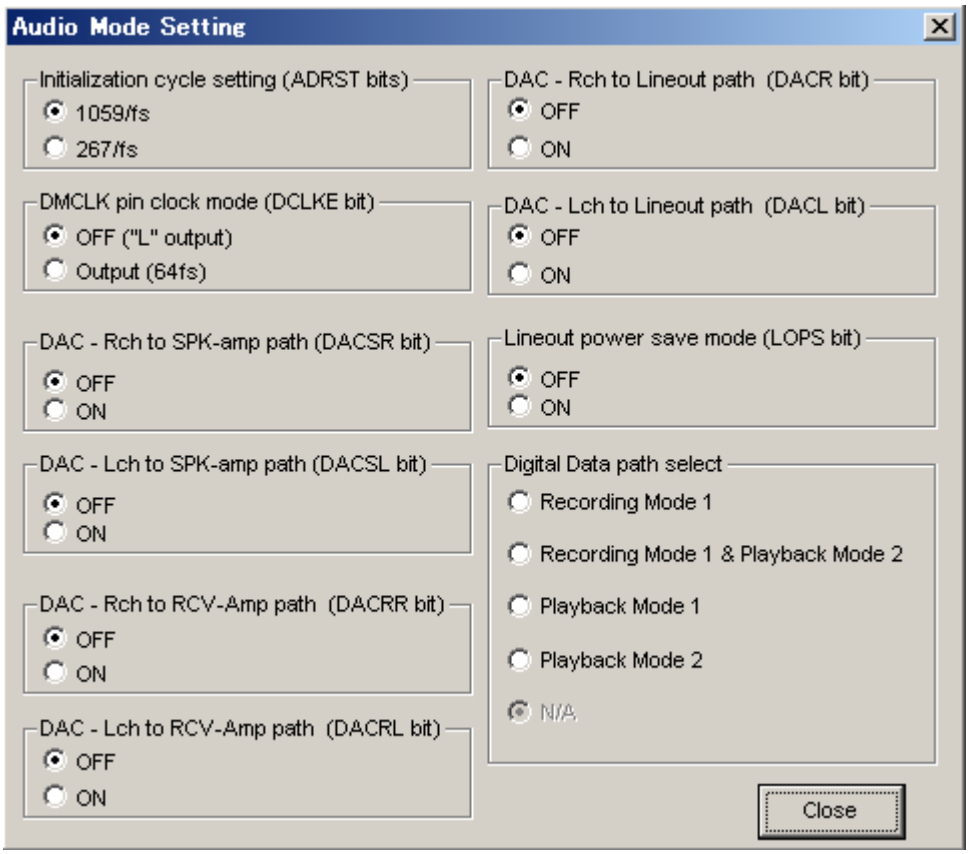

Figure 28. Window of [Audio Mode Setting]

1-3. System Clock, Audio I/F Setting

When [PLL Setting] button is clicked, the window as shown in Figure 29 opens.
This window is for System Clock and Audio I/F Setting
Refer to the datasheet for register settings of the AK4679.

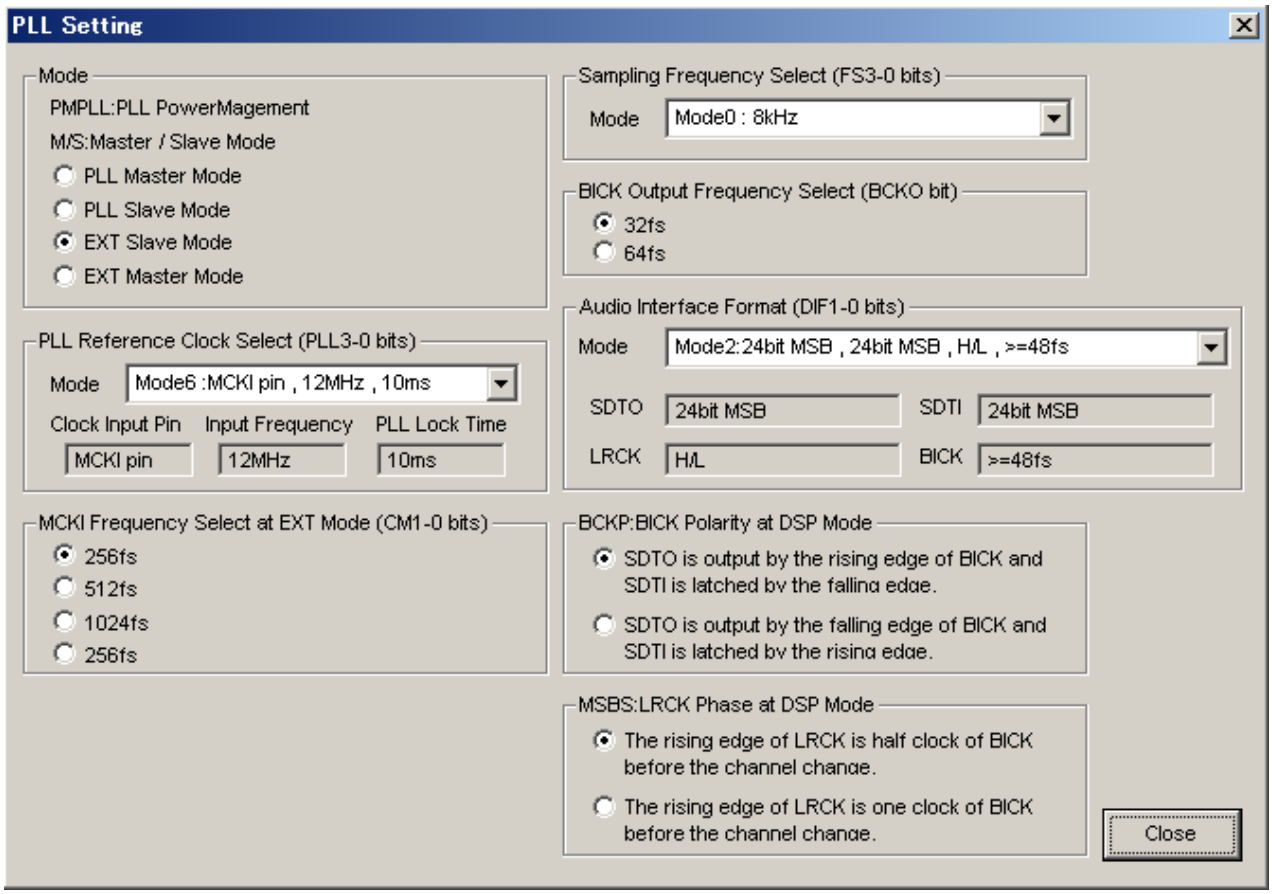

Figure 29. Window of [PLL Setting]

1-4. MIC Setting

When [MIC Setting] button is clicked, the window as shown in Figure 30 opens.
This window is for MIC Setting.
Refer to the datasheet for register settings of the AK4679.

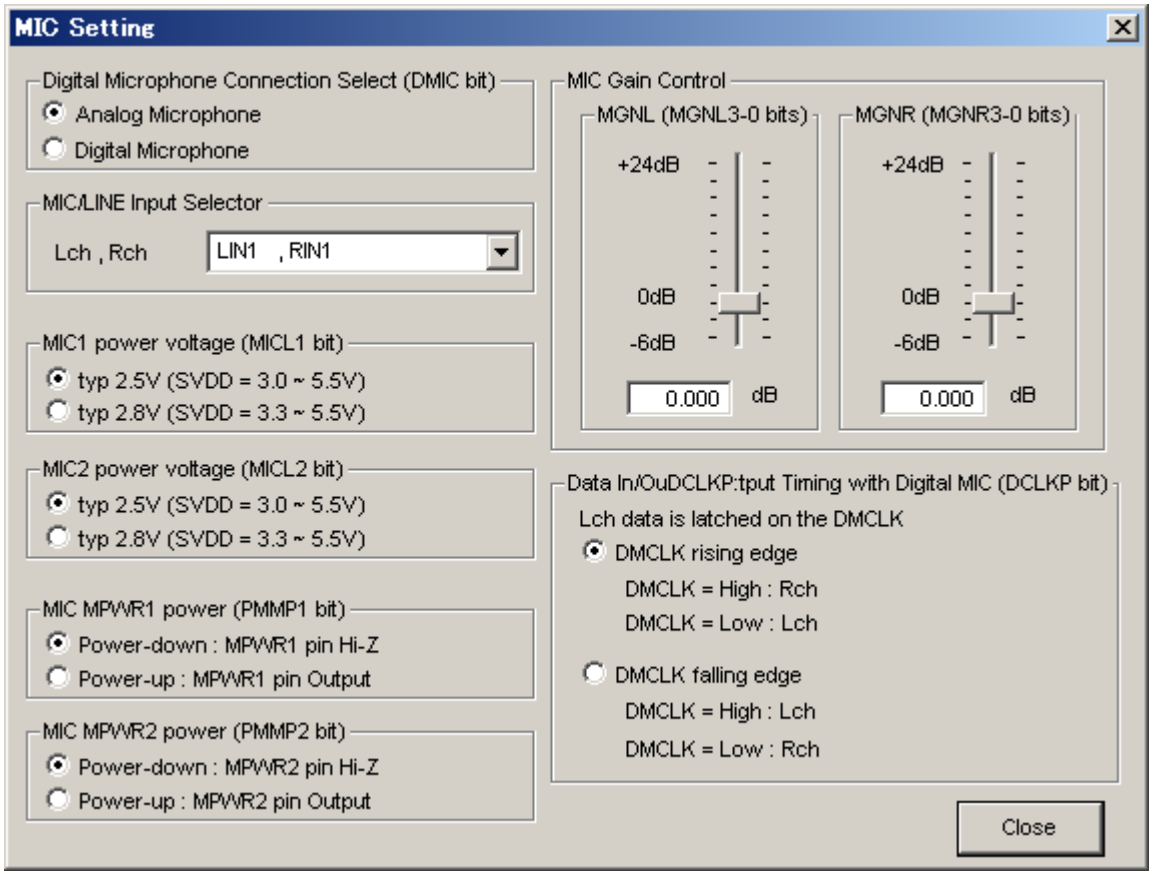

Figure 30. Window of [MIC Setting]

1-5. ALC Setting

When [ALC Setting] button is clicked, the window as shown in Figure 31 opens.
This window is for ALC setting.
Refer to the datasheet for register settings of the AK4679.

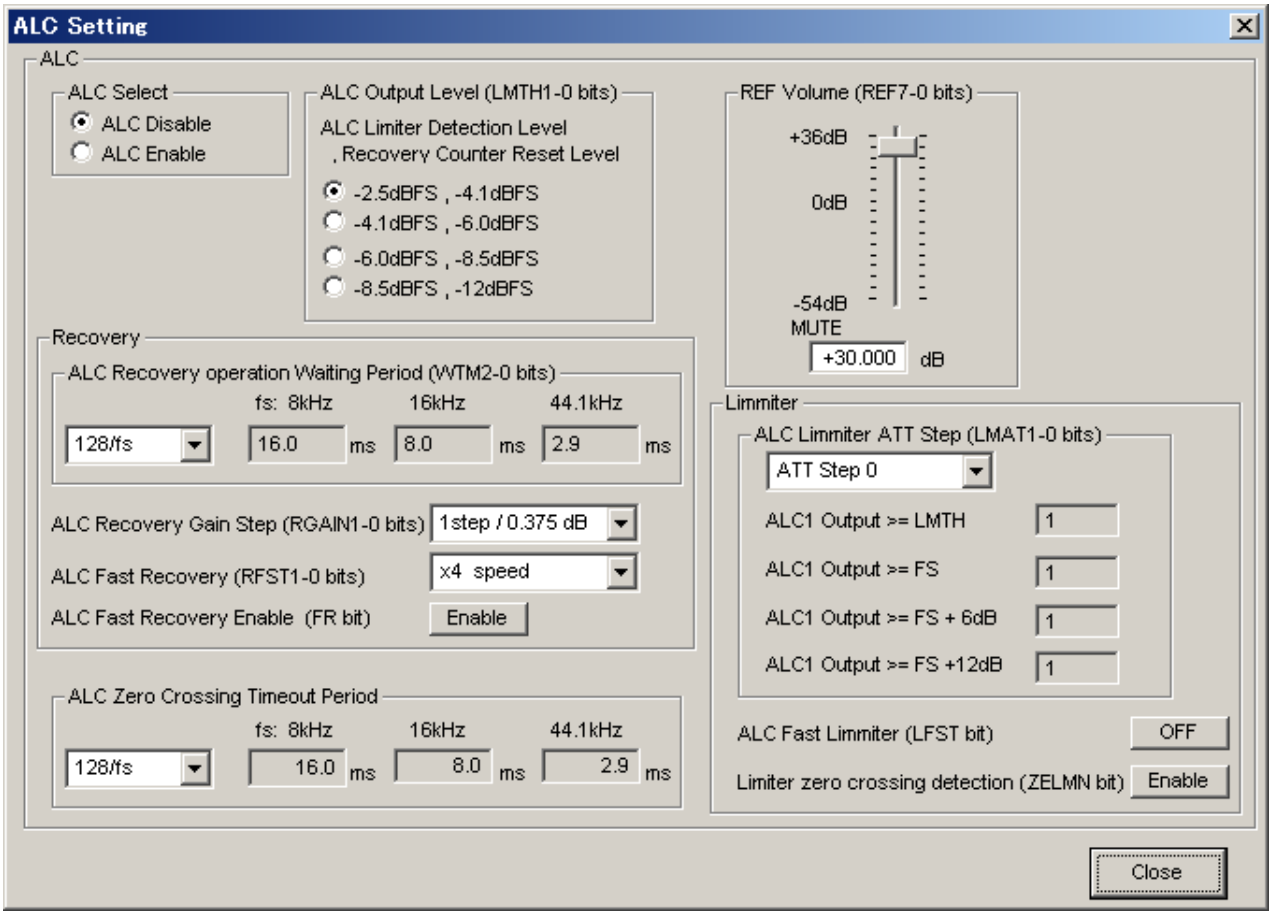

Figure 31. Window of [ALC Setting]

1-6. Volume Setting

When [Volume Setting] button is clicked, the window as shown in Figure 32 opens.
This window is for Volume setting.
Refer to the datasheet for register settings of the AK4679.

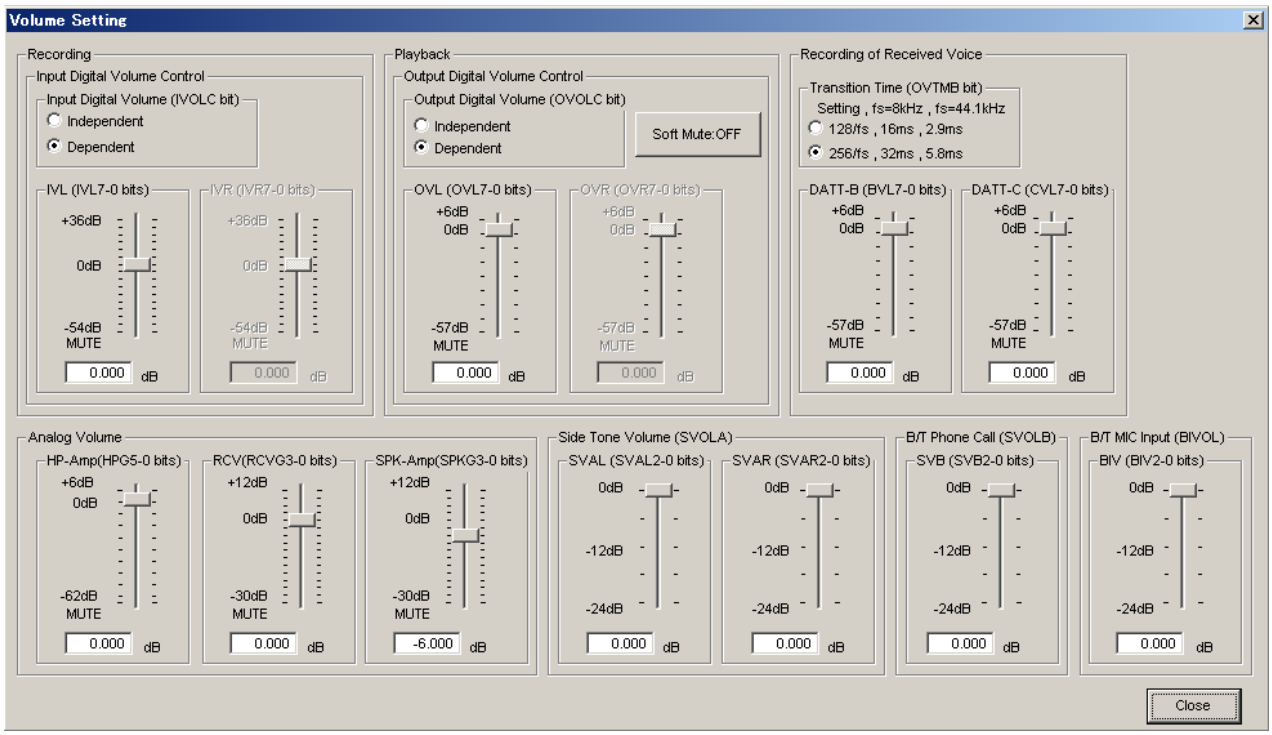

Figure 32. Window of [Volume Setting]

Register map

10H	RCVG3	RCVG2	RCVG1	RCVG0	SPKG3	SPKG2	SPKG1	SPKG0
11H	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
12H	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0

The volume can be controlled by slide bars.
Register writing is made on every slide bar move.

After the volume slide is moved, it is reflected on to the register map and data writing dialog box.

Volume Control by Pull-down Menu

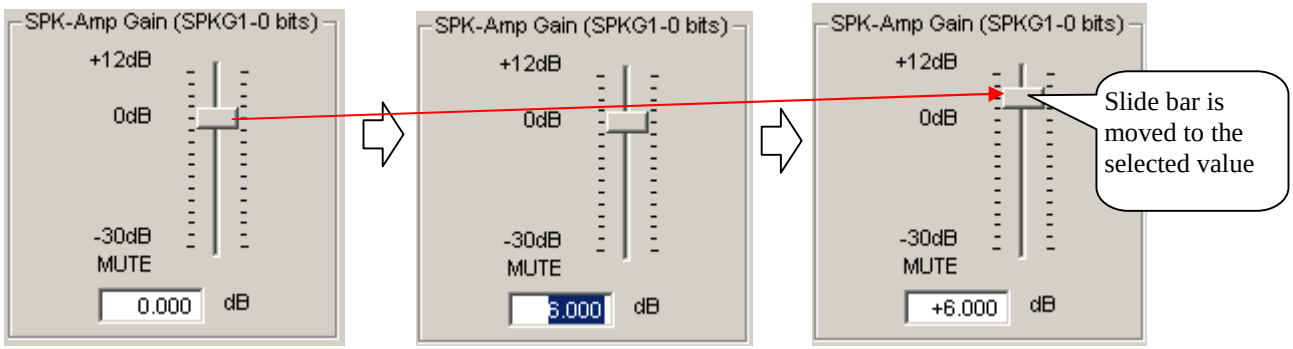

Figure 33. Volume Control by Pull-down Menu

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that written in the dialog box. Use the mouse or arrow keys on the keyboard for small adjustments.

1-7. Digital Filter Setting

When [Digital Filter Setting] button is clicked, the window as shown in Figure 34 opens.
Refer to the datasheet for register settings of the AK4679.
A calculation of a coefficient of Digital Programmable Filters such as HPF / LPF and EQ filters, a register writing and a frequency response checking of HPF / LPF and EQ filter can be made.

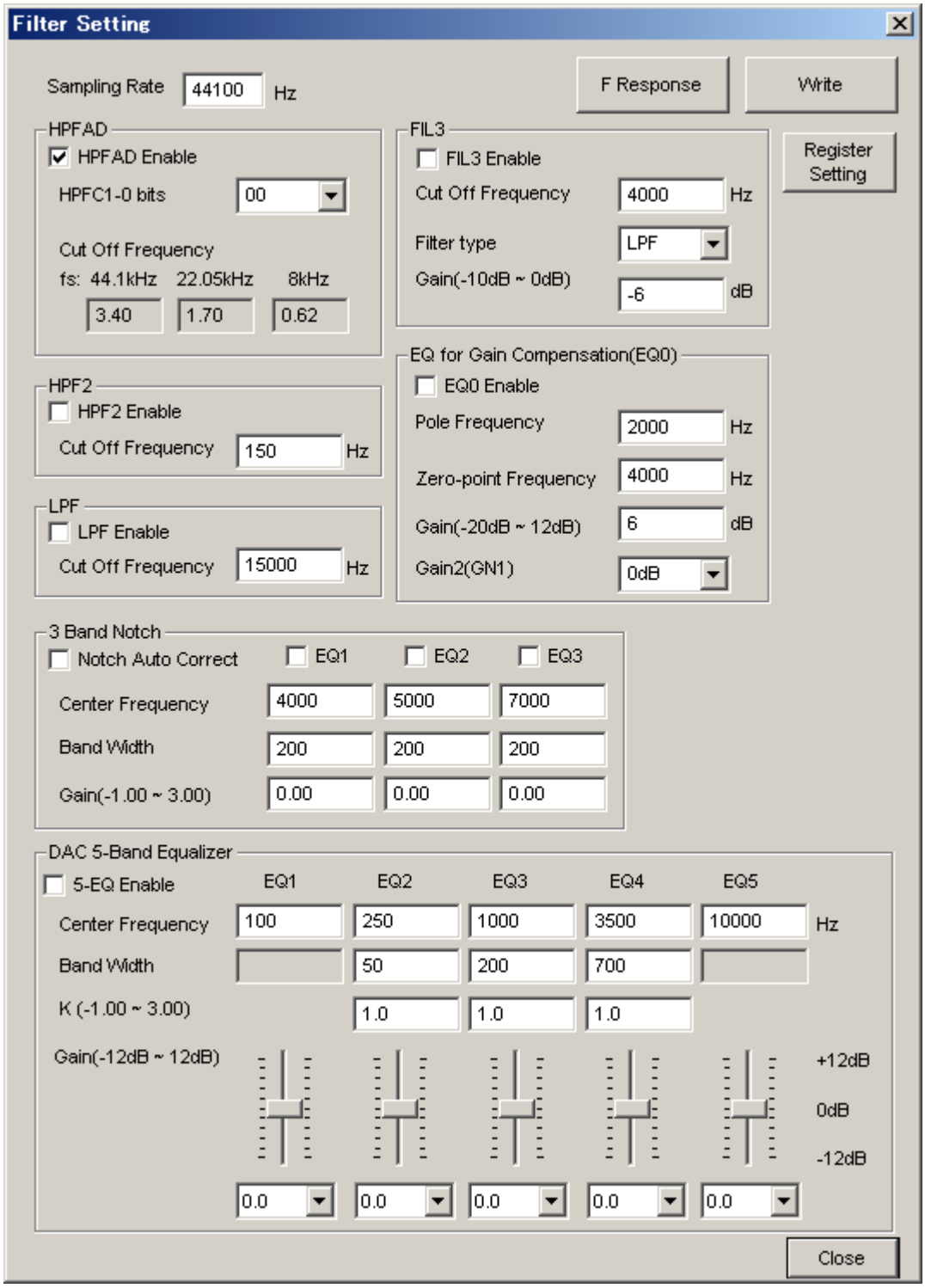

Figure 35. Window of [Digital Filter Setting]

1-7-1. Parameter Setting

(1) Please set a parameter of each Filter.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF2		
Cut Off Frequency	Low pass filter cut off frequency	fs/1000 ≤ Cut Off Frequency ≤ (0.497 * fs)
FIL3		
Cut Off Frequency	FIL3 cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Gain	-10≤ Gain < 0
EQ for Gain Compensation(EQ0)		
Pole Frequency	EQ0 Pole Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Zero-point Frequency	EQ0 Zero-point Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Gain	-20≤ Gain < 12
3 Band Equalizer		
EQ1-3 Center Frequency	EQ1-3 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-3 Band Width	EQ1-3 Band Width (Note 1)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-3 Gain	EQ1-3 Gain (Note 2)	-1≤ Gain < 3
DAC 5-Band Equalizer		
Center Frequency	LPF1 EQ1-5 HPF1 Center Frequency	fs/1000 ≤ Cut Off Frequency < (0.497 * fs)
Band Width	EQ2-4 Band Width	1Hz ≤ Band Width < (0.497 * fs)
Gain	LPF1 EQ1-5 HPF1 Gain	-12 ≤ Gain ≤ 12

Note 1. Gain difference is a bandwidth of 3dB from center frequency.

Note 2. When the gain is smaller than 0, EQ becomes a notch filter.

(2) “HPFAD Enable”, “HPF Enable” , “LPF Enable” “FIL3 Enable”, “EQ0 Enable”, “EQ1”, “EQ2”, “EQ3”, Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed.

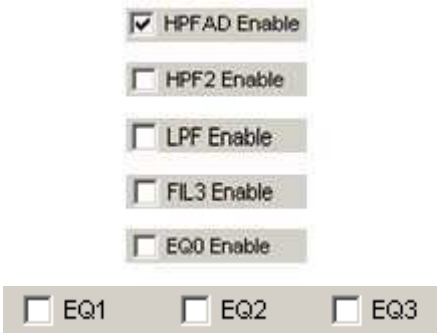

Figure 36. Filter ON/OFF setting button

1-7-2. Calculation of Register

Register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

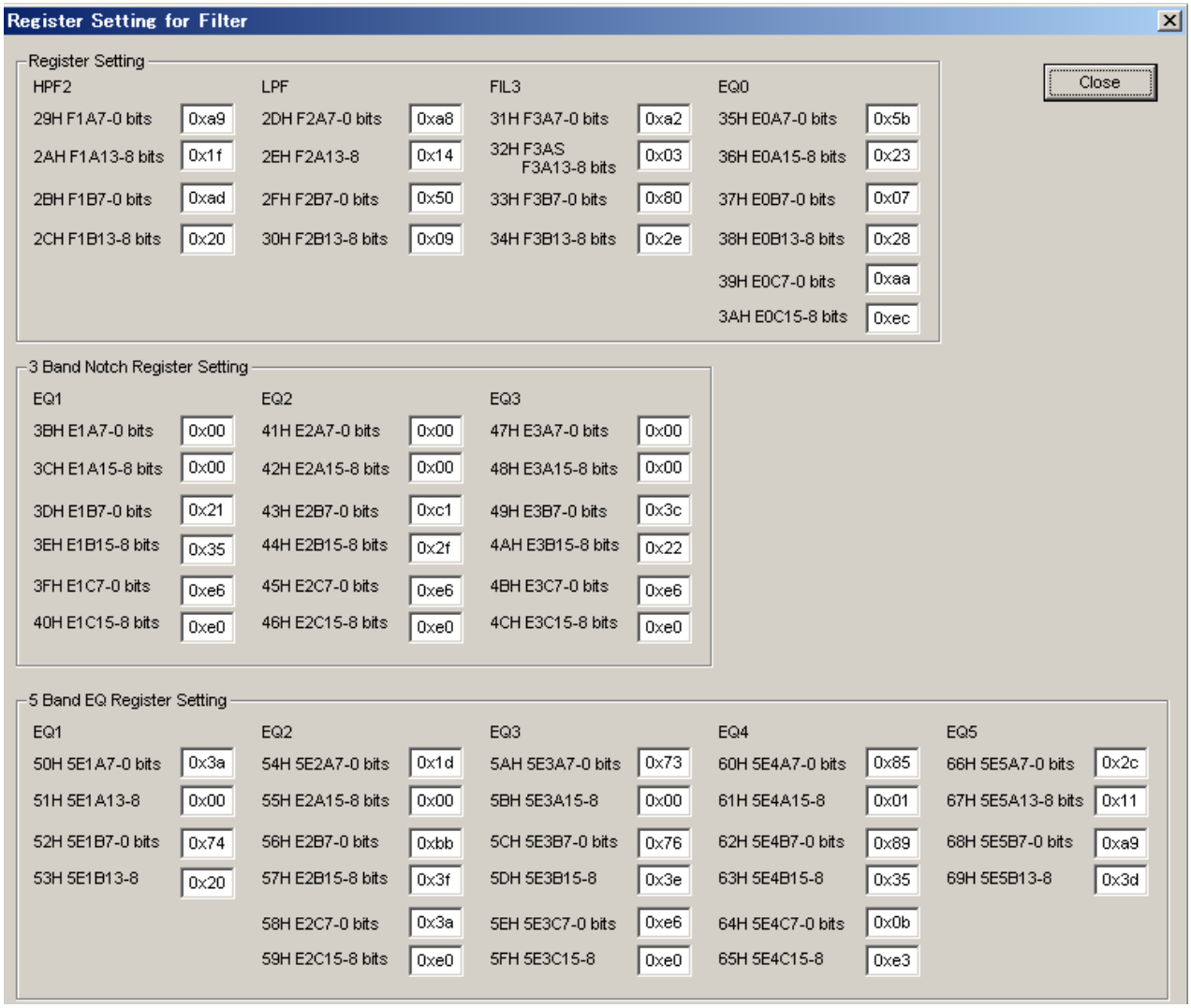

Figure 37. Register setting calculation result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

1-7-3. Indication of Frequency Characteristic

Frequency characteristic is displayed when push a [F Response] button. Then, a register set point is also updated. Change “Frequency Range”, and indication of a frequency characteristic is updated when push a [UpDate] button.

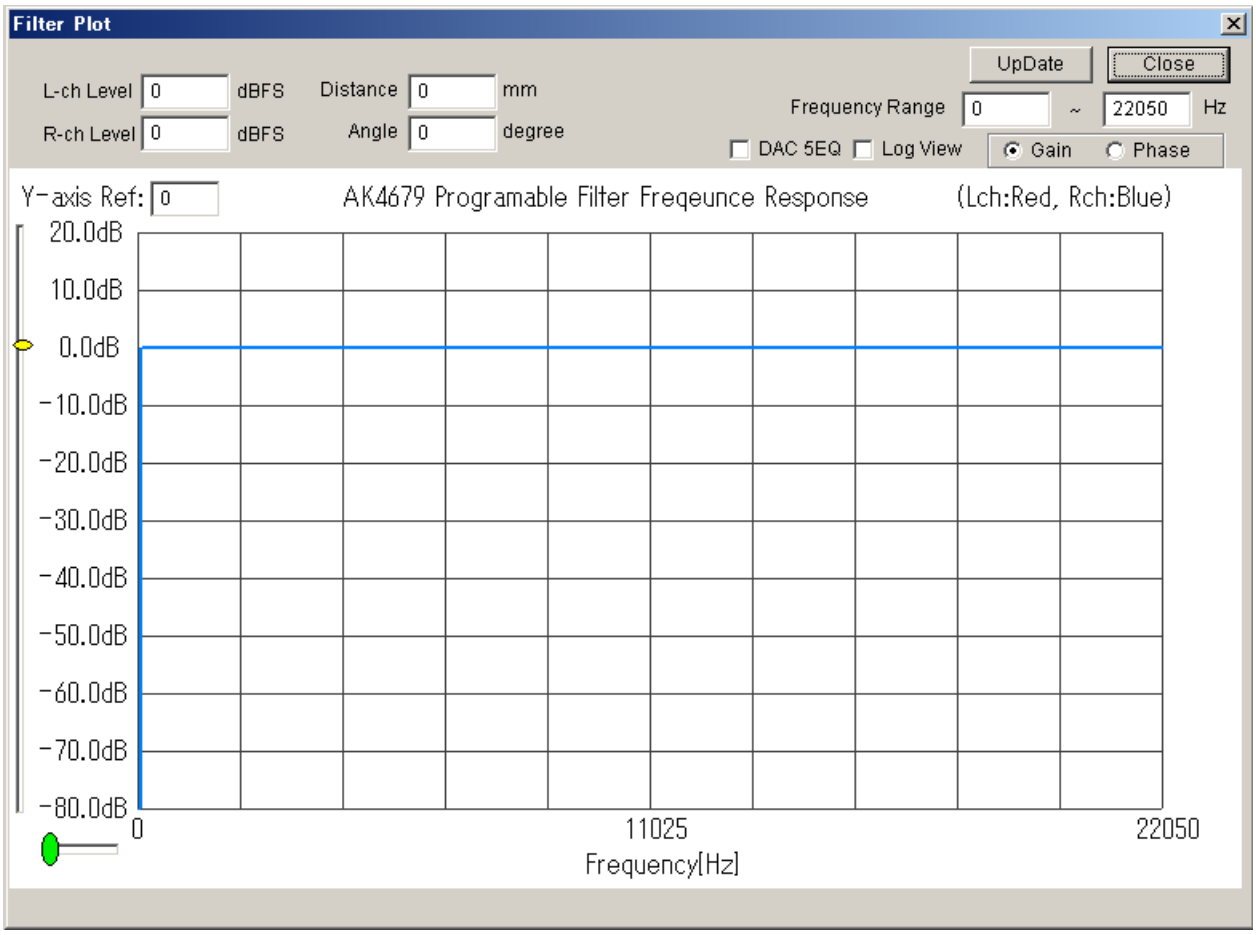

Figure 38. A frequency characteristic indication result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

1-7-4. Filter Setting

(a) 3-band Equalizer, DAC 5-band Equalizer

The filter setting can be executed by dragging the number to each equalizers in the mouse.
Band Width can be adjusted in the operation of Center Frequency, K and Gain right-clicking in the operation of the left-click.

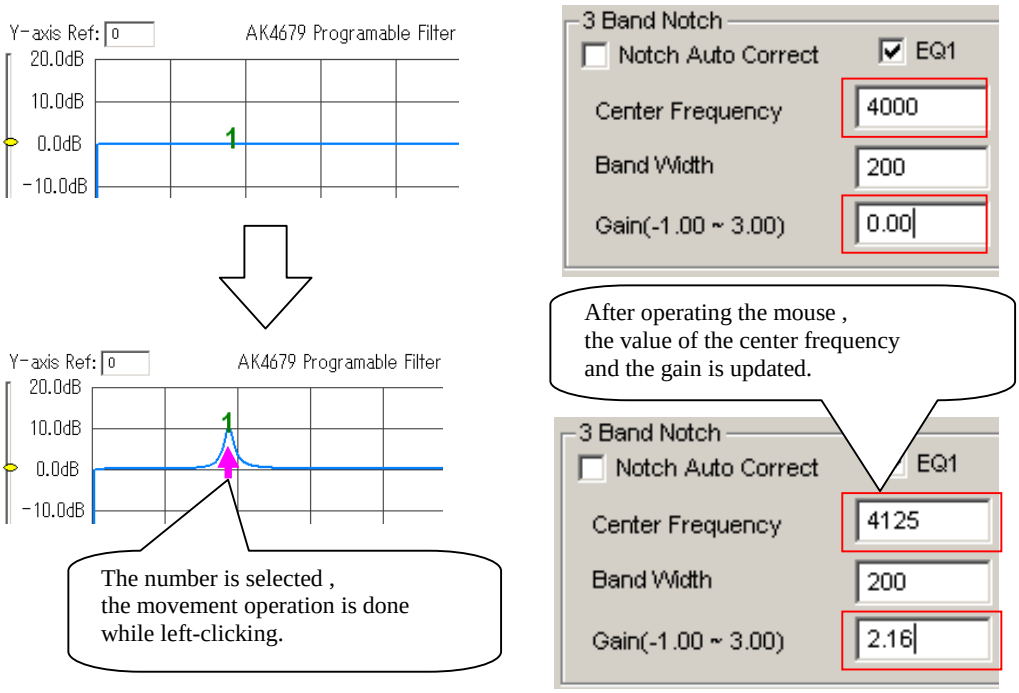

Figure 39. Filter Setting (Right-clicking operation)

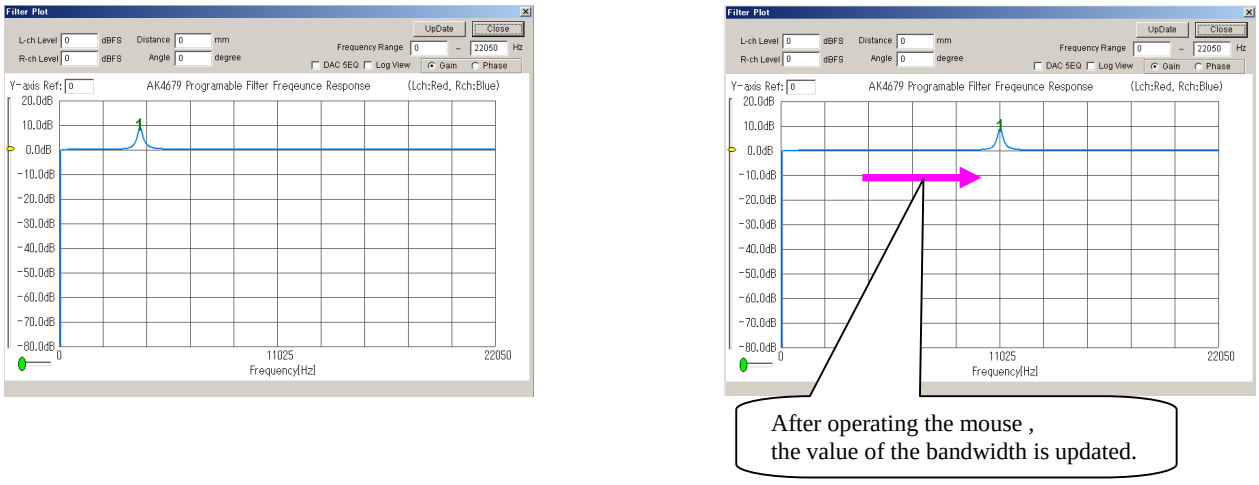

Figure 40. Filter Setting (Left-clicking operation)

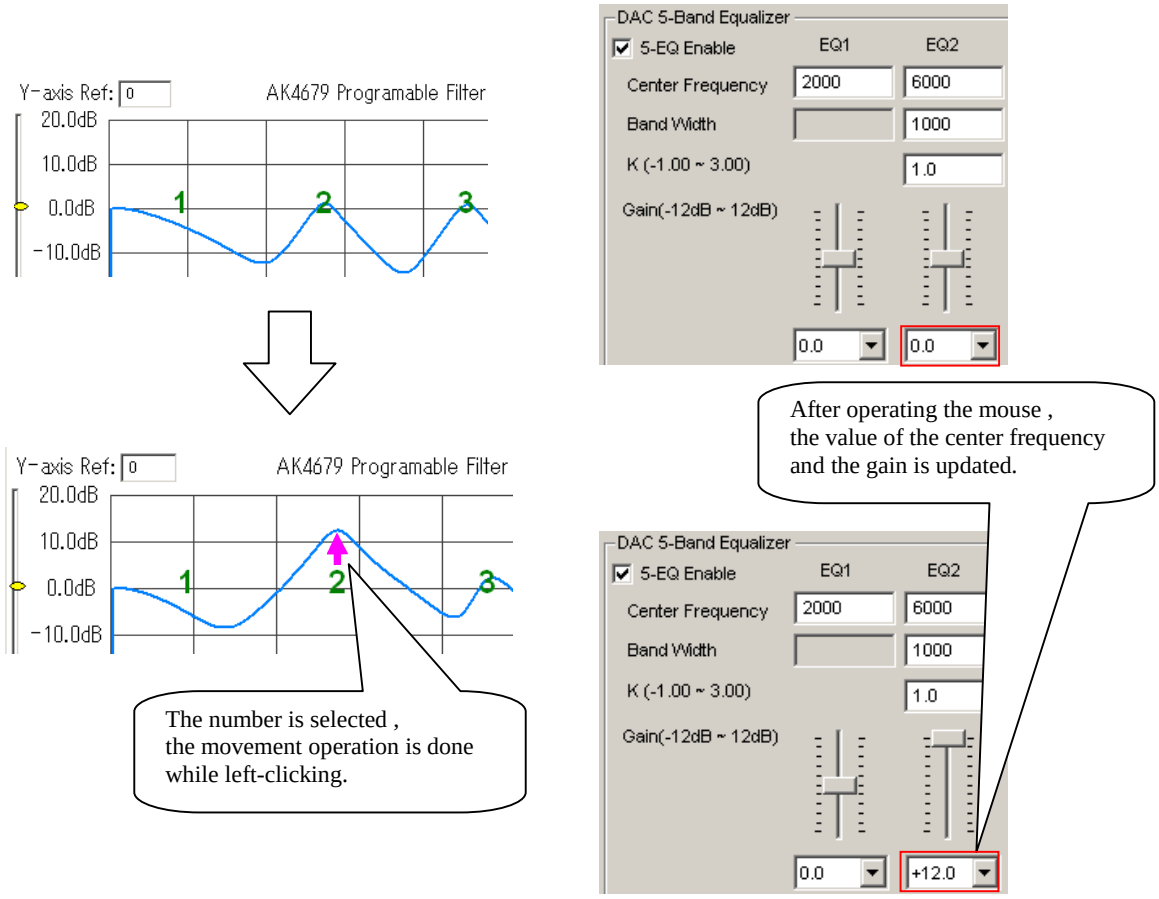

Figure 41. Filter Setting(Gain-Control operation)

1-8. DRC Setting

When [DRC Setting] button is clicked, the window as shown in Figure 42 opens.
This window is for DRC setting.
Refer to the datasheet for register settings of the AK4679.

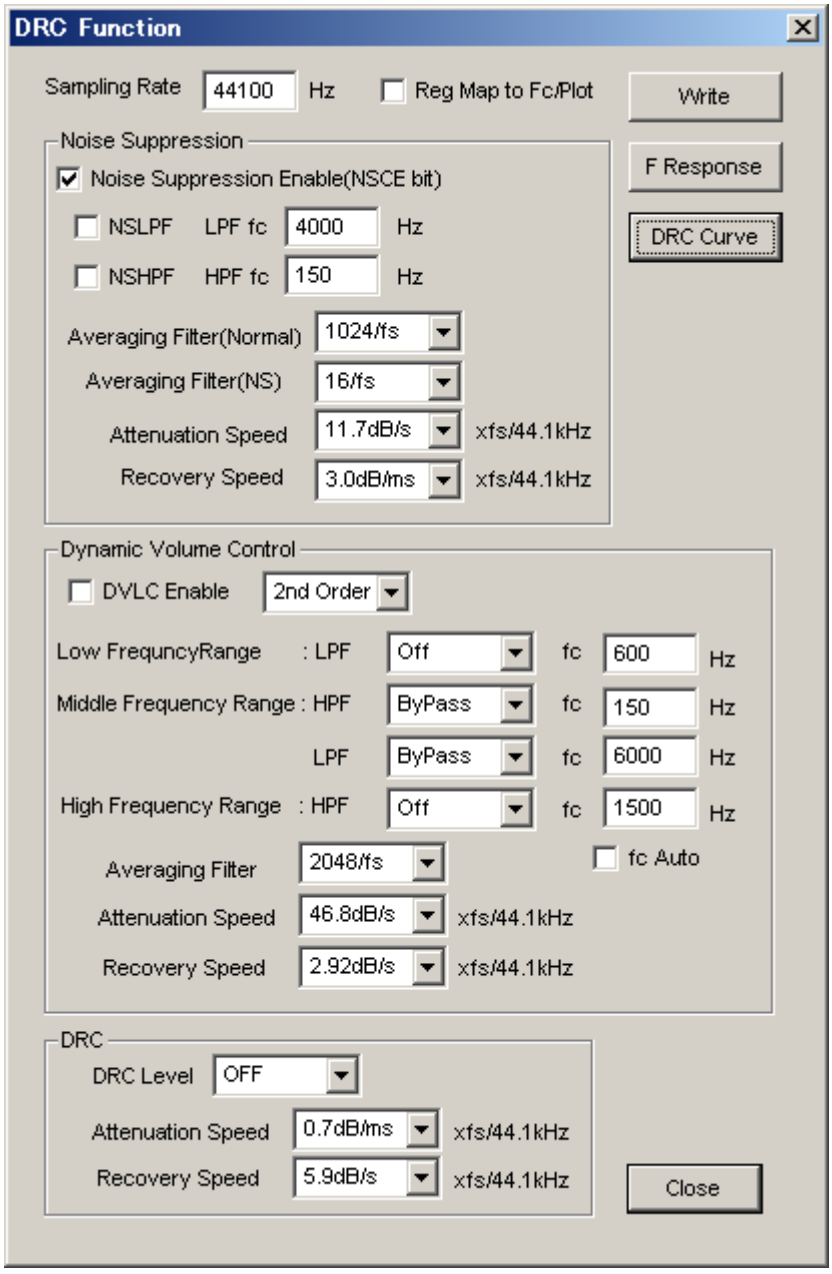

Figure 43. Window of [DRC Setting]

1-8-1. Parameter Setting

(1) Please set a parameter of each Filter and Gain.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
Noise Suppression		
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Reference Value Setting	-9 ≤ Gain < -54 (Note 3)
Threshold Level	Noise Suppression Threshold Low/High Level	-82.5≤ Threshold Level < -36.0 (Note 4)
Dynamic Volume Control		
Low Frequency Range		
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0 (Note 5)
Middle Frequency Range	Low Frequency Range	
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0
High Frequency Range		
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0

Note 3. Gain step of “Reference Value of Noise Suppression” is 3dB.

Note 4. Gain step of “Threshold level Value of Noise Suppression” is 3dB.

Note 5. Gain step of “Volume point Value of Dynamic Volume Control” is 3dB.

(2) When “NSLPF” button is checked, the filter is enabled. When “NSHPF” button is checked, the filter is enabled. When “DVLC Enable” button is checked, the filters of Low/Middle/High Range are enabled according to setting of pull-down menu. When “fc Auto” button is checked, the frequency response of low frequency and high frequency ranges becomes flat automatically.

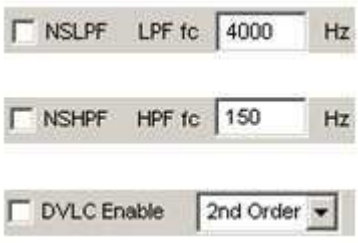

Figure 44. Filter ON/OFF setting button

1-8-2. Frequency Response

Frequency characteristic is displayed when pushing a [F Response] button. Then, a register set point is also updated. When changing “Frequency Range”, frequency characteristic indication window is updated after [UpDate] button is pushed.

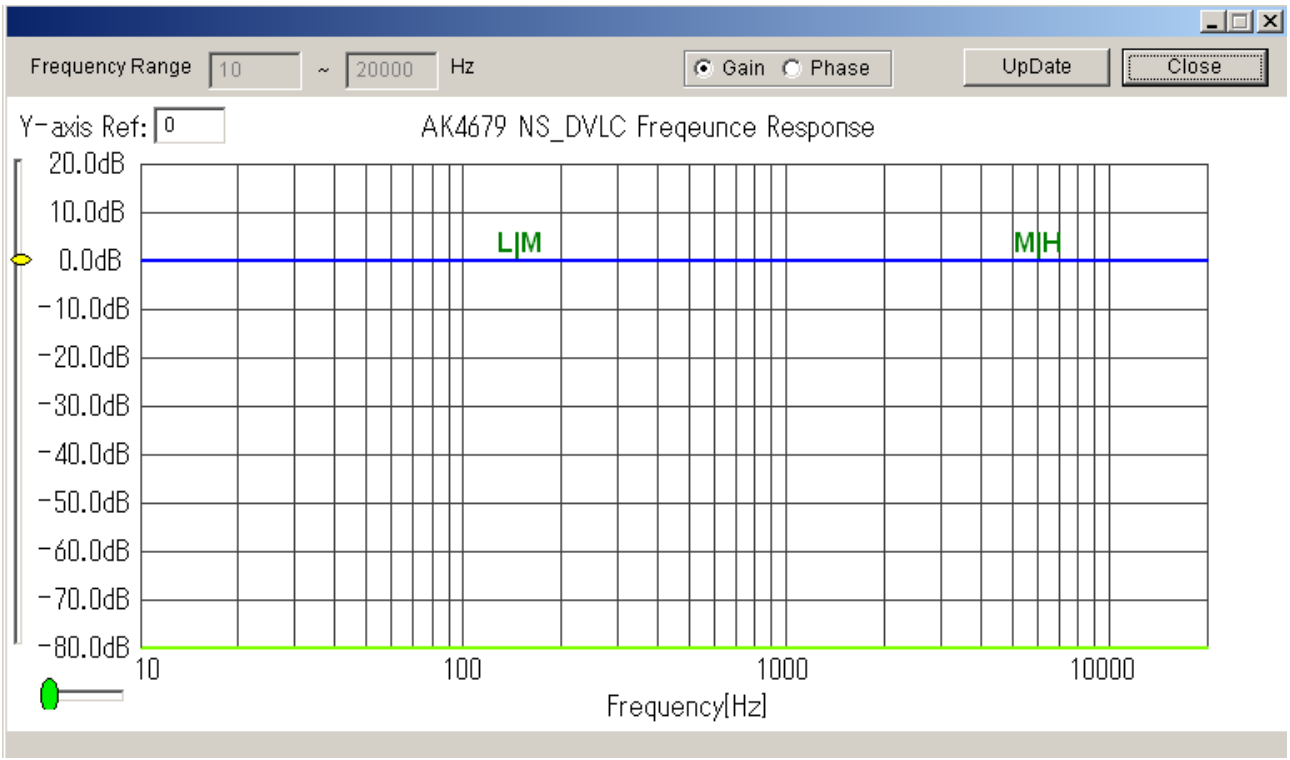

Figure 45. A frequency characteristic indication result

Followings are the cases when a register set value is updated.

(1). When [Register Setting] button was pushed.
(2). When [Frequency Response] button was pushed.
(3). When [UpDate] button was pushed on a frequency characteristic indication window.
(4). When set ON/OFF of a check button “fc Auto”

1-8-3. Filter Setting

The filter setting can be executed by checking the “NSLPF”, “NSHPF” or “DVLC Enable” button.
Band width can be adjusted in the operation of Center Frequency in the operation of the left-click and Filter selecting in the [DRC Setting] window.

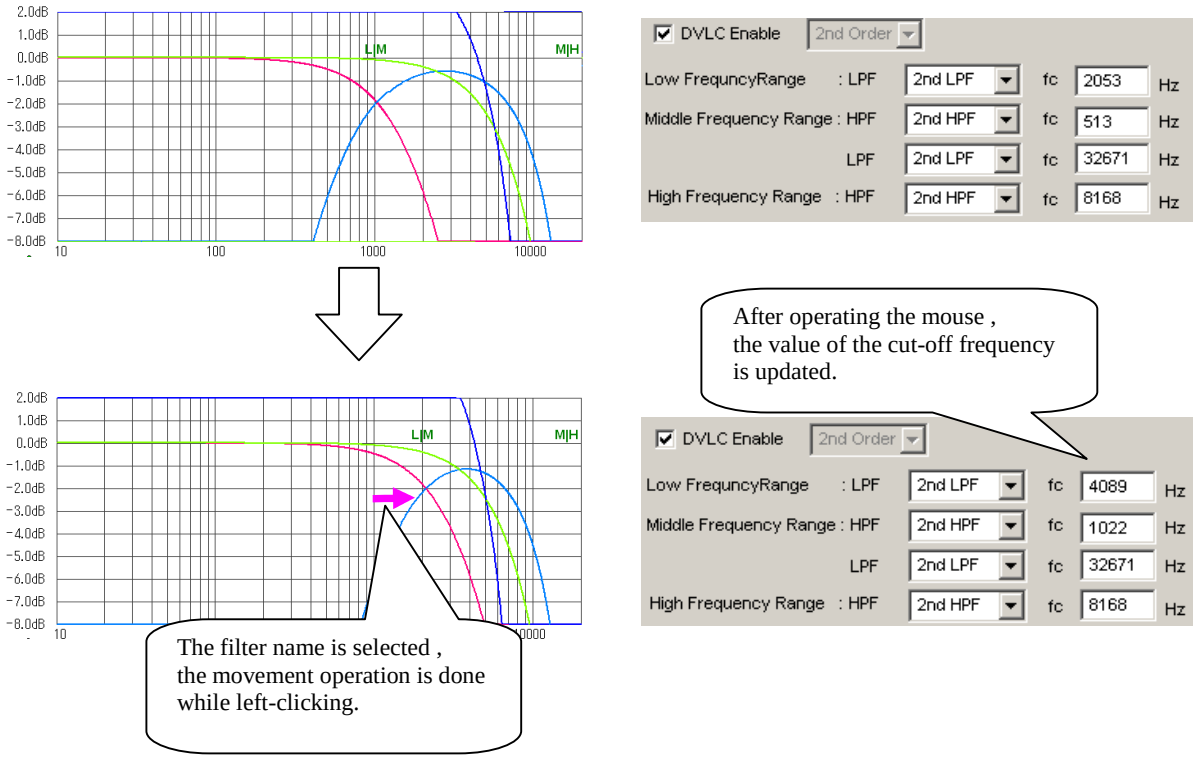

Figure 46. Filter Setting (Left-clicking operation)

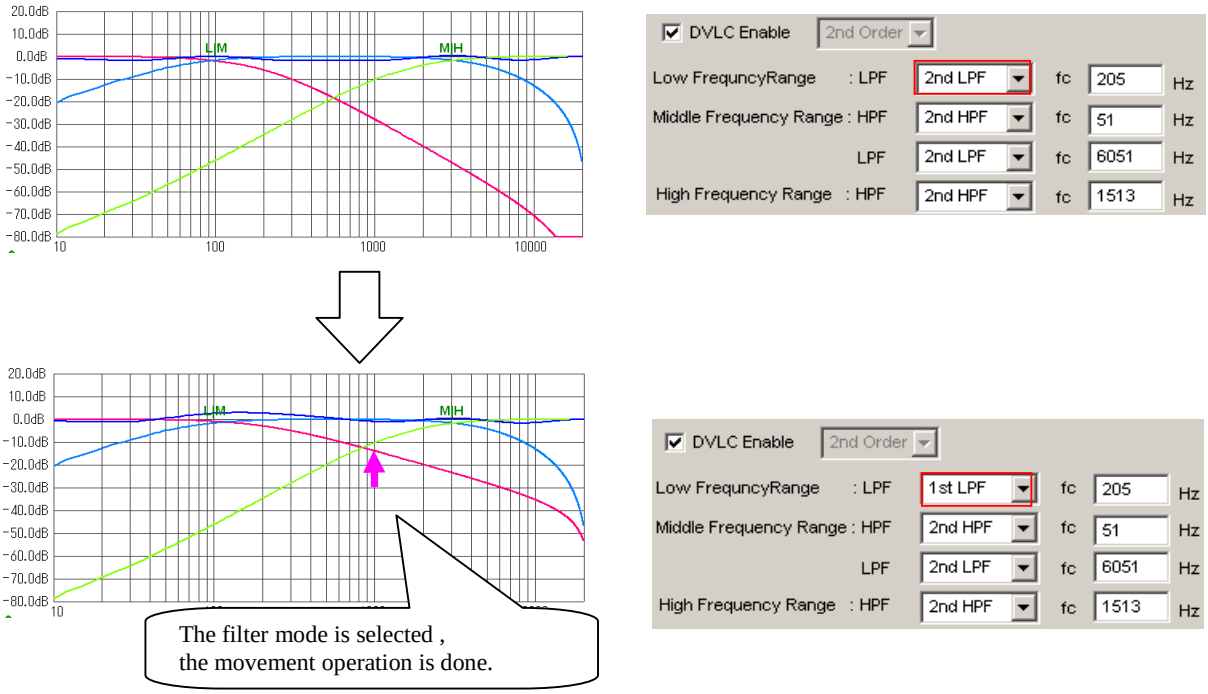

Figure 47. Filter Setting (Filter Selecting)

1-8-4. Noise Suppression

Noise Suppression Control is displayed when “NS” button is checked after [DRV Curve] button is pushed. Then, a register set point is also updated.

Noise Suppression Threshold Low Level and Reference Value can be adjusted by the left-click.

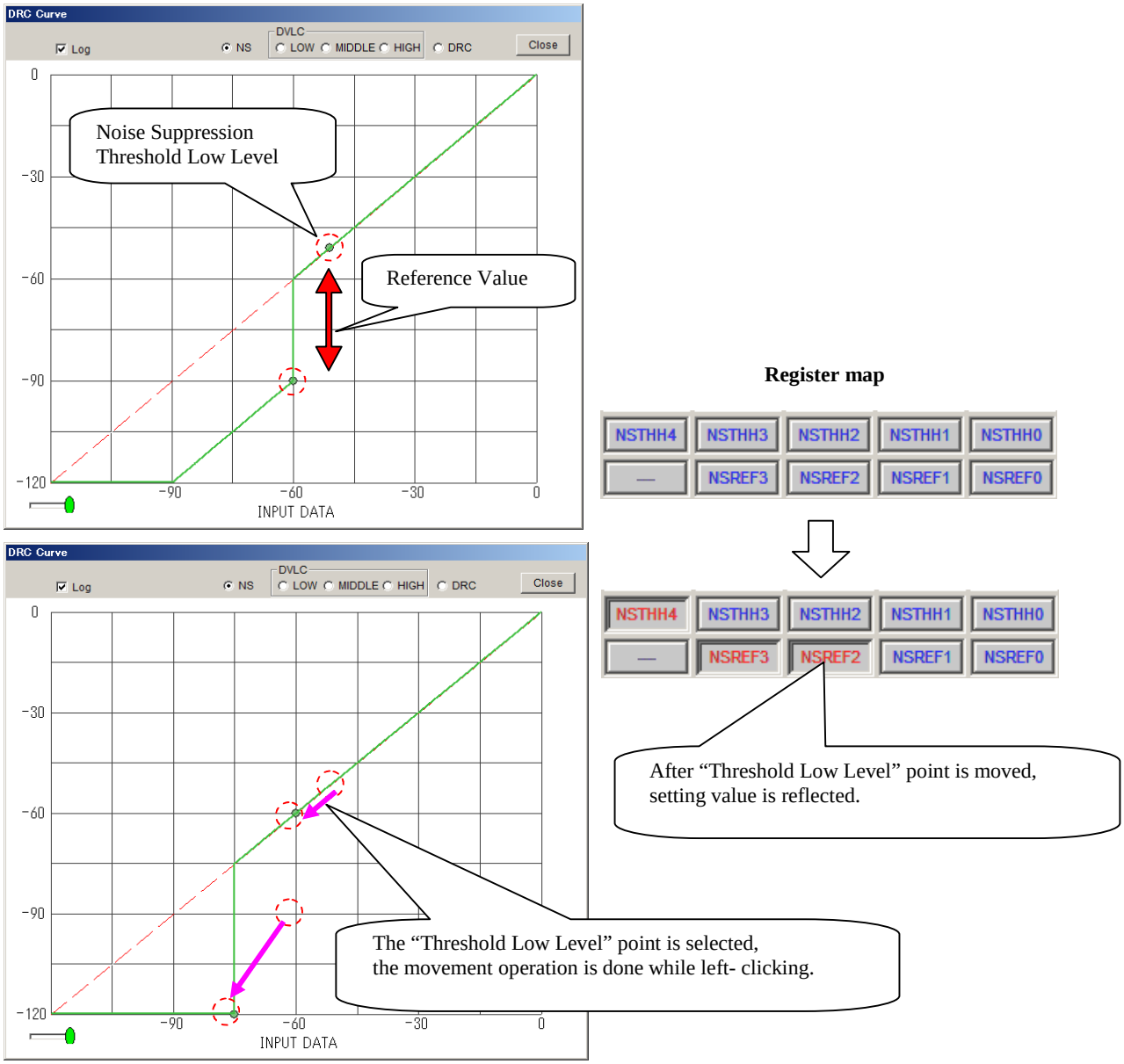

Figure 48. Noise Suppression Setting

1-8-5. Dynamic Volume Control

Dynamic Volume is displayed when “Low”, ”Middle” or “High” buttons in “DVLC” is checked after [DRV Curve] button is pushed.
Then, a register set point is also updated.

Dynamic Volume Control Points can be adjusted by the left-click.

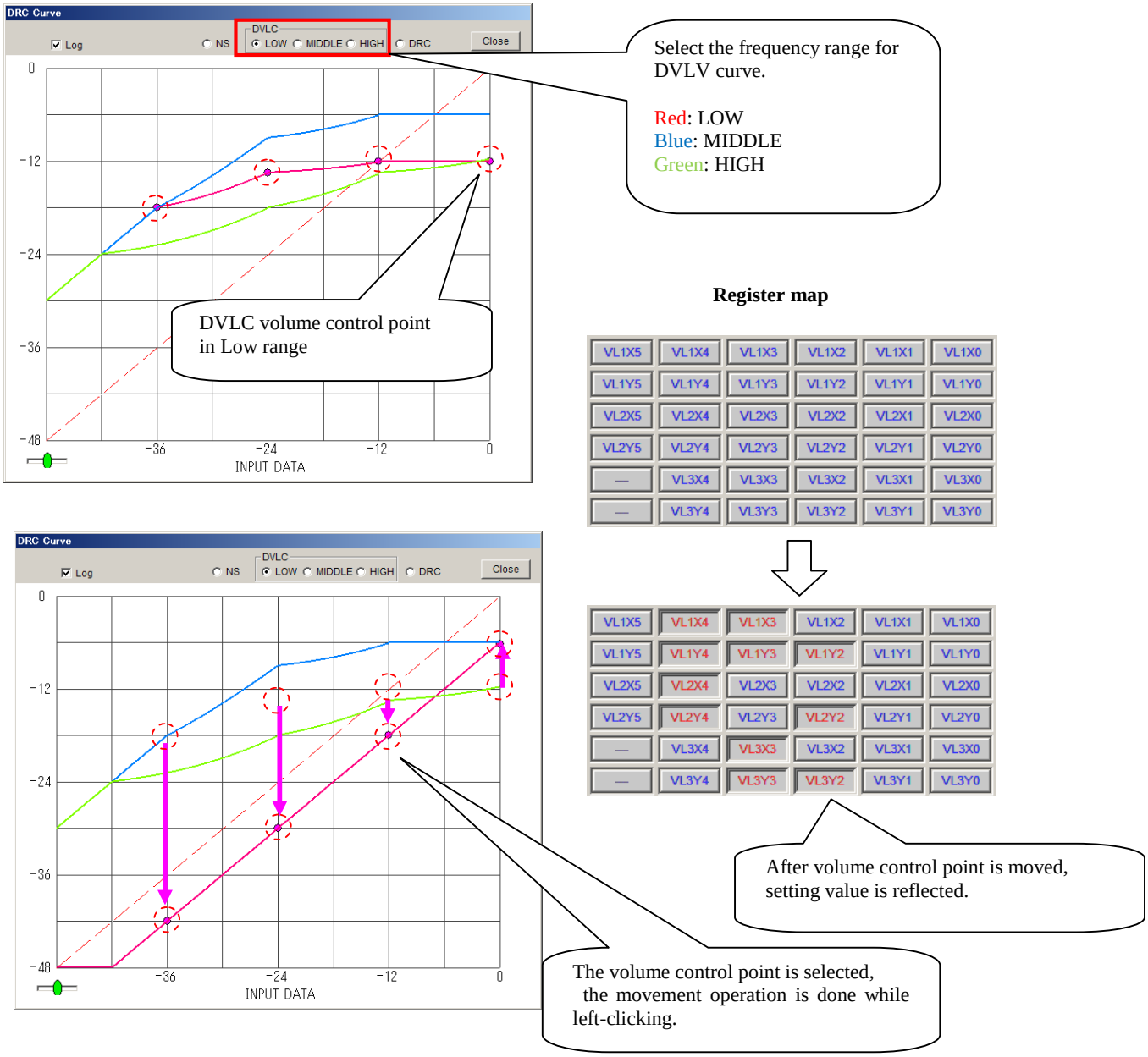

Figure 49. DVLC Curve Setting

1-8-6. Dynamic Range Control

Dynamic Range Control is displayed when “DRC” button is checked after [DRV Curve] button is pushed. Then, a register set point is also updated.

Dynamic Range Compression Level can be adjusted by the left-click.

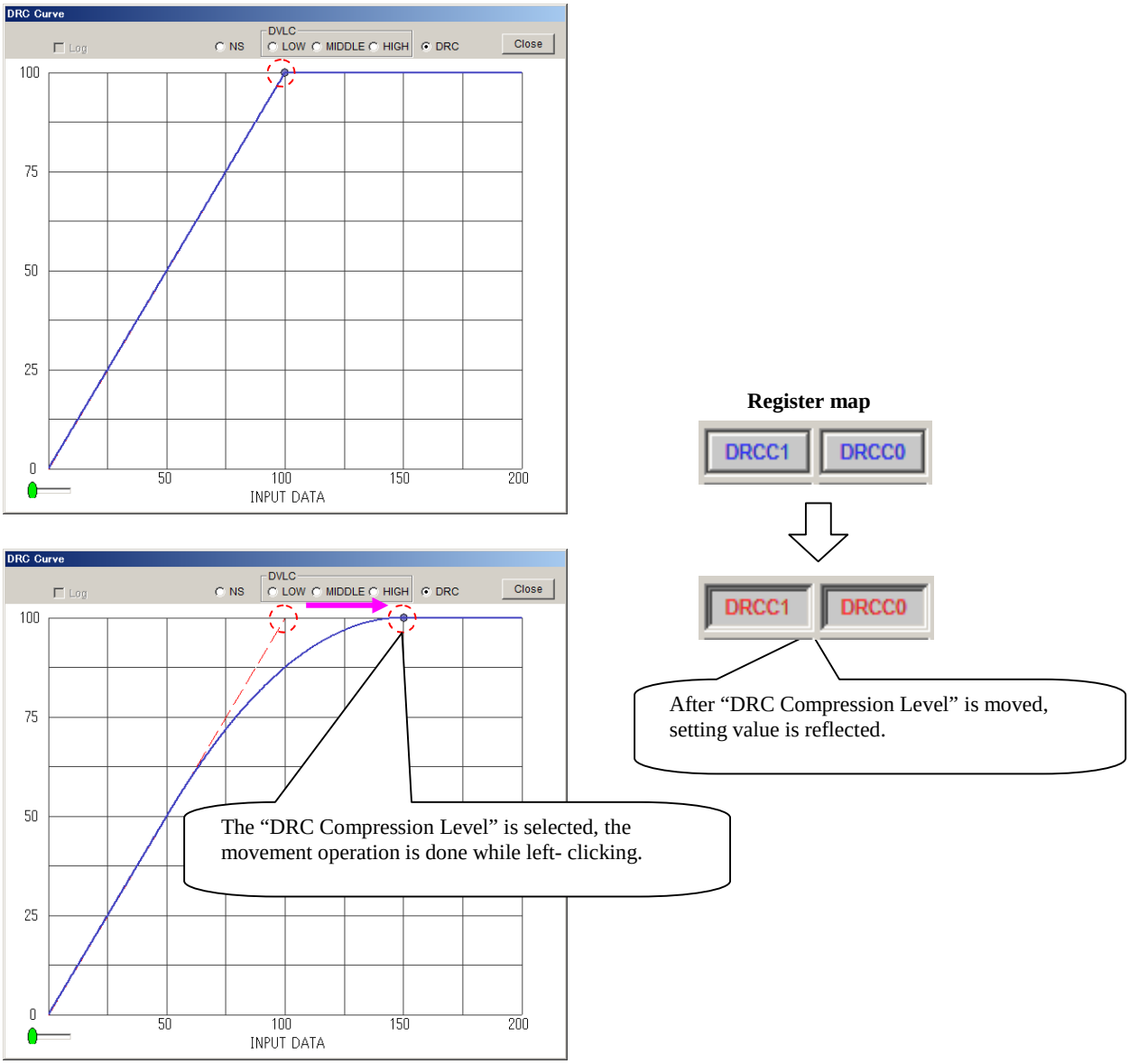

Figure 50. Dynamic Range Control Setting

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

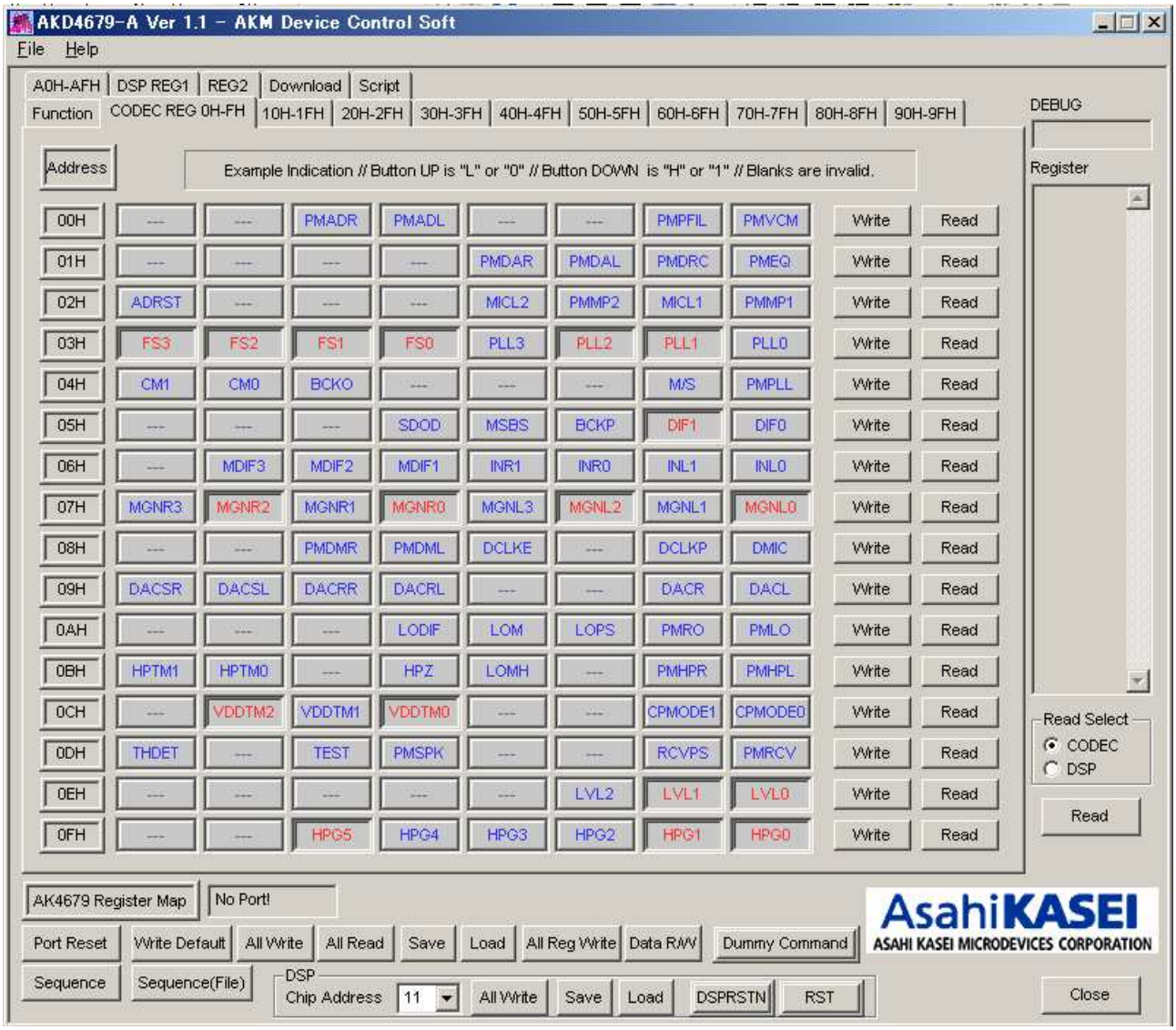

Figure 51. Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

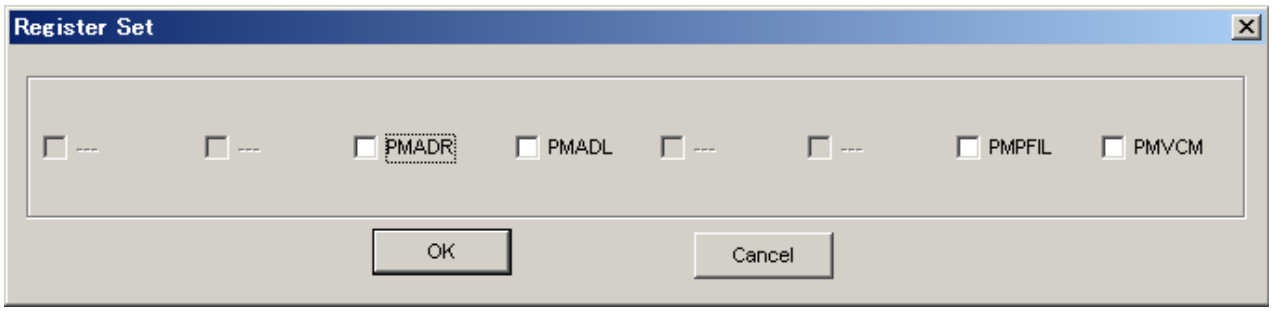

Figure 52. Window of [Register Set]

[Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

[Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

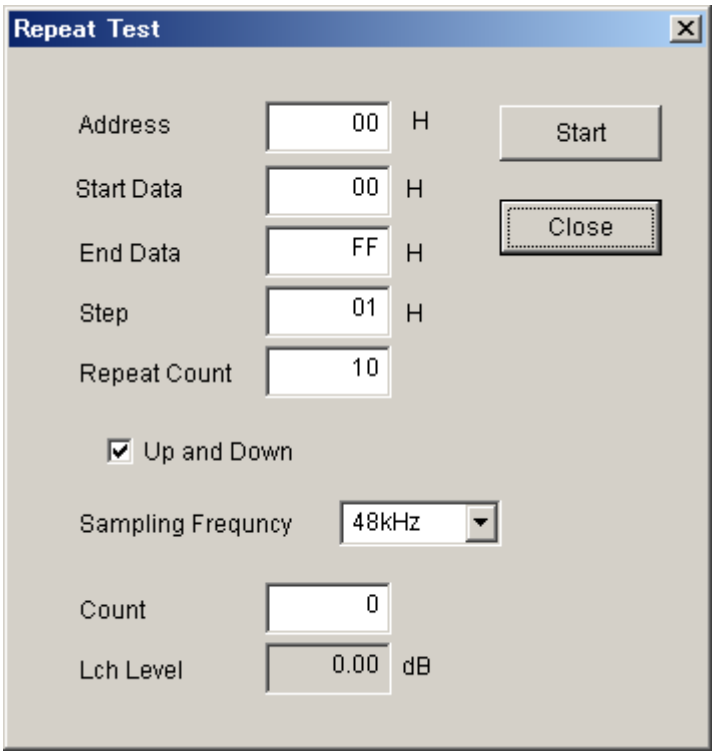

Figure 53. Window of [Repeat Test]

[Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

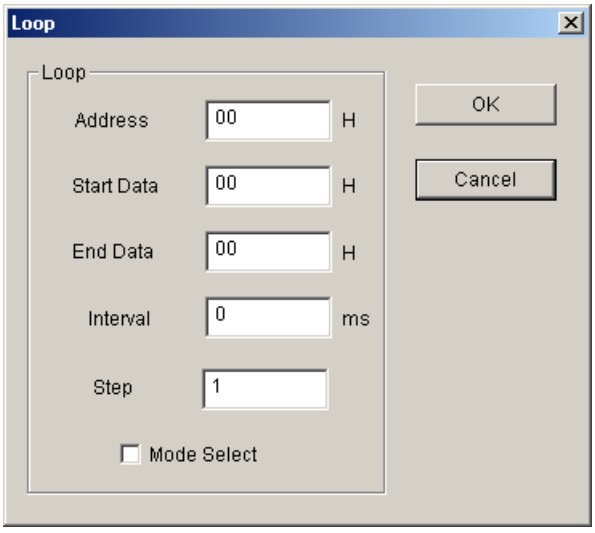

Figure 54. Window of [Loop]

Dialog Boxes

[All Reg Write]

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

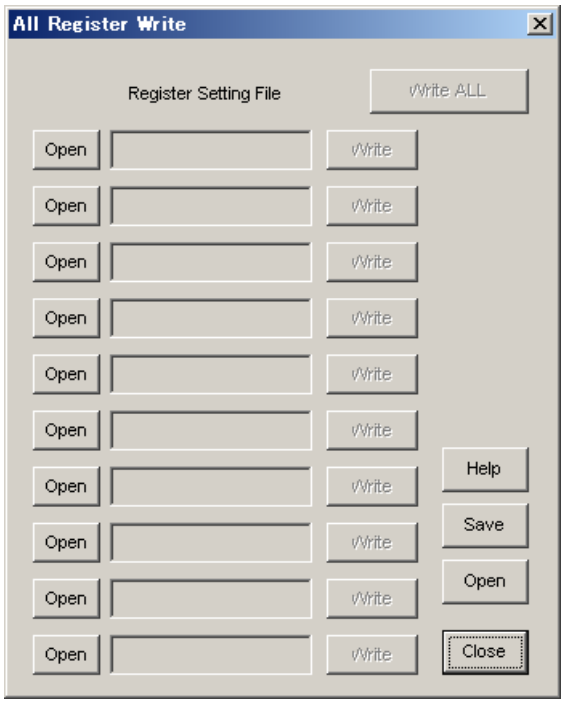

Figure 55. Window of [All Register Write]

[Open (left)] : Selecting a register setting file (*.akr).
[Write] : Executing register writing.
[Write All] : Executing all register writings.
Writings are executed in descending order.
[Help] : Help window is popped up.
[Save] : Saving the register setting file assignment. The file name is “*.mar”.
[Open (right)] : Opening a saved register setting file assignment “*. mar”.
[Close] : Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

[Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

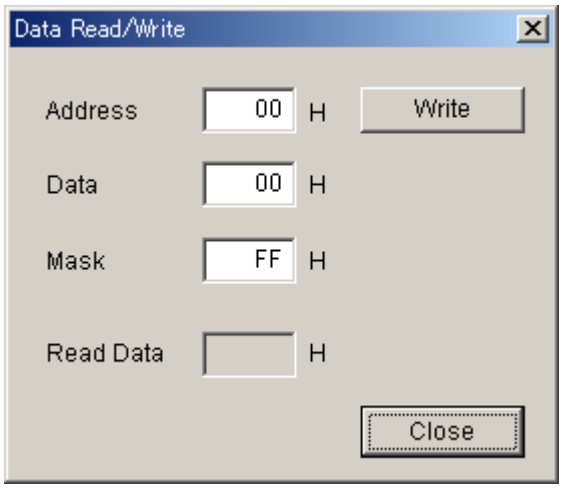

Figure 56. Window of [Data Read/Write]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write] : Writing to the address specified by “Address” box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

[Sequence]

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

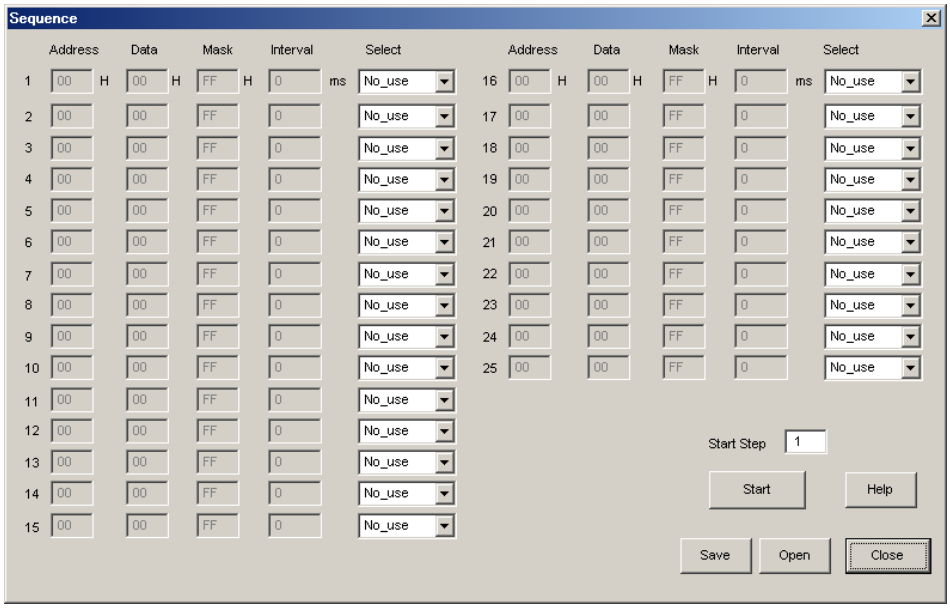

Figure 57. Window of [Sequence]

Sequence Setting

Set register sequence by following process bellow.

(1)Select a command

Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >

- No_use : Not using this address
- Register : Register writing
- Reg(Mask) : Register writing (Masked)
- Interval : Taking an interval
- Stop : Pausing the sequence
- End : Finishing the sequence

(2)Input sequence

[Address] : Data address
[Data] : Writing data
[Mask] : Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval] : Interval time

Valid boxes for each process command are shown bellow.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

Control Buttons

The function of Control Button is shown bellow.

[Start] : Executing the sequence
[Help] : Opening a help window
[Save] : Saving sequence settings as a file. The file name is "*.aks".
[Open] : Opening a sequence setting file "*.aks".
[Close] : Closing the dialog box and finish the process.

Stop of the Sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

[Sequence(File)]

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the “Sequence setting dialog” can be applied in this dialog.

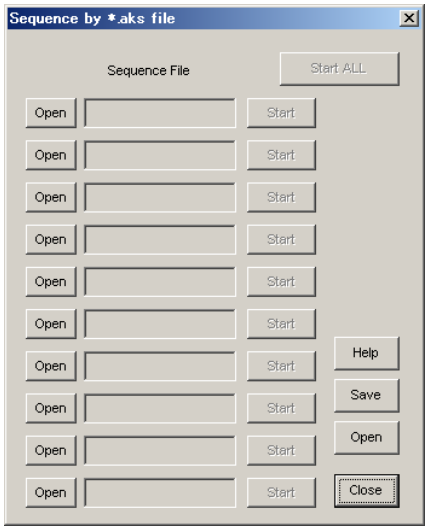

Figure 58. Window of [Sequence(File)]

[Open (left)] : Opening a sequence setting file (*.aks).
[Start] : Executing the sequence setting.
[Start All] : Executing all sequence settings.
Sequences are executed in descending order.
[Help] : Pop up the help window.
[Save] : Saving sequence setting file assignment. The file name is “*.mas”.
[Open(right)] : Opening a saved sequence setting file assignment “*. mas”.
[Close] : Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
(2) When “Stop” is selected in the sequence the process will be paused and a pop-up message will appear. Click “OK” to continue the process.

Figure 59. Window of [Sequence Pause]

Measurement Result

[Measurement condition]

- Measurement Unit : Audio Precession System Two Cascade
- MCLK : 11.2896MHz
- BICK : 64fs
- fs : 44.1kHz
- Power Supply : AVDD=DVDD=PVDD=TVDD=TVDDE=1.8V, VDDE=1.2V, SVDD=4.2V
- Band Width : 22Hz ~ 20kHz
- Measurement Mode : PLL Slave Mode
- Temperature : Room Temperature

[Measurement Result]

1. ADC

a). LIN1, RIN1 pins, MGNL=MGNR=+18dB, single-ended mode

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	81.5 / 81.5	dB
D-Range (-60dBFS Input, A-weighted)	87.1 / 87.0	dB
S/N (A-weighted)	87.4 / 87.4	dB

b). LIN1, RIN1 pins, MGNL=MGNR=0dB, single-ended mode

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	82.7 / 82.3	dB
D-Range (-60dBFS Input, A-weighted)	92.3 / 92.3	dB
S/N (A-weighted)	93.3 / 93.2	dB

2. DAC

a) Line out (LOUT/ROUT pins, LVL=0dB, R_L=10kΩ)

Parameter	Result Lch / Rch	Unit
S/(N+D) (0dBFS Input)	81.2 / 81.1	dB
S/N (A-weighted)	93.3 / 93.3	dB

b) Mono Line Out (LOP/LON pins, LVL=0dB, R_L=10kΩ)

Parameter	Result	Unit
S/(N+D) (0dBFS Input)	73.3	dB
S/N (A-weighted)	96.2	dB

c) Mono Receiver Out (RCP/RCN pins, RCVG=-6dB, R_L=32Ω)

Parameter	Result	Unit
S/(N+D) (0dBFS Input)	59.7	dB
S/(N+D) (0dBFS Input, RCVG=0dB)	56.7	dB
S/N (A-weighted)	95.3	dB
Output Noise Level (RCVG=-9dB)	-103.4	dBV

d) HP Out (HPL/HPR pins, HPG=0dB, R_L=32Ω)

Parameter		Result Lch	Result Rch	Unit
Output Voltage (R_L=32Ω)	HPG=-4dB	1.58	1.58	Vpp
	HPG=0dB	2.521	2.50	
Output Voltage (R_L=16Ω)	HPG=-4dB	1.56	1.56	Vpp
	HPG=0dB	0.83	0.83	Vrms
S/(N+D) (R_L=32Ω)	HPG=-4dB	71.6	71.8	dB
	HPG=0dB	70.8	70.9	
S/(N+D) (R_L=16Ω)	HPG=-4dB	66.3	66.4	dB
	HPG=0dB	24.7	23.9	
S/N (A-weighted)		95.8	95.7	dB
Output Noise Level (A-weighted, HPG=-14dB)		-106.7	-106.7	dBV

e) SPK Out (SPPL/SPNL, SPPR/SRNR pins, SPKG=0dB, R_L=8Ω+10uH)

Parameter		Result	Unit
Output Power	SVDD=5.0V THD+N=10% SPKG=-3dB	1.52	W
	SVDD=4.2V THD+N=10% SPKG=-3dB	1.07	
	SVDD=4.2V THD+N=1% SPKG=0dB	0.87	
	SVDD=3.7V THD+N=1% SPKG=-6dB	0.67	
Output Voltage (-3dBFS Input)		5.40	Vpp
S/(N+D) (SVDD=3.7V, Po=0.35W)		60.0	dB
Output Noise Level (A-Weighted)		-82.0	dBV

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
12/04/04	KM111200	1	First edition	-	

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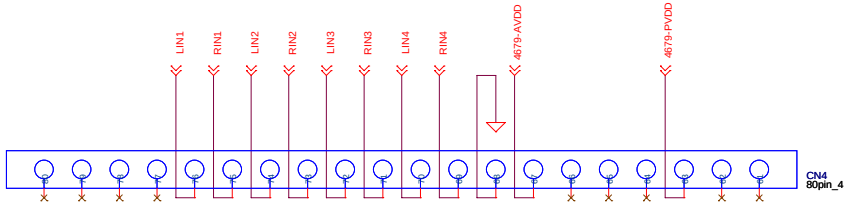

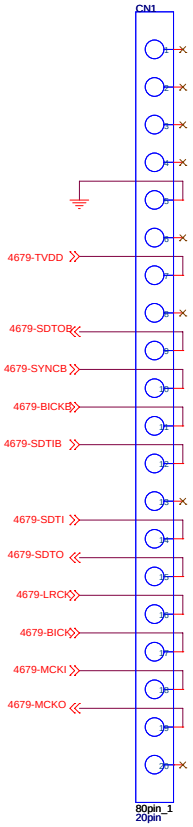

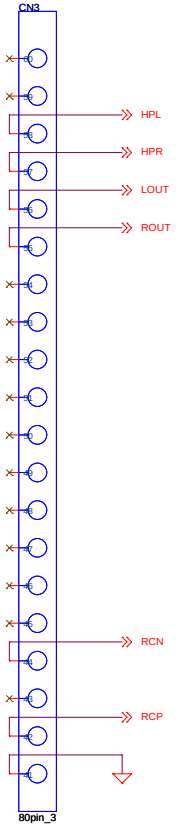

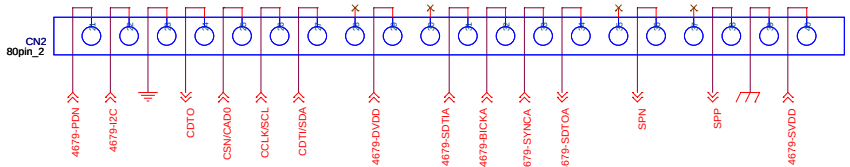

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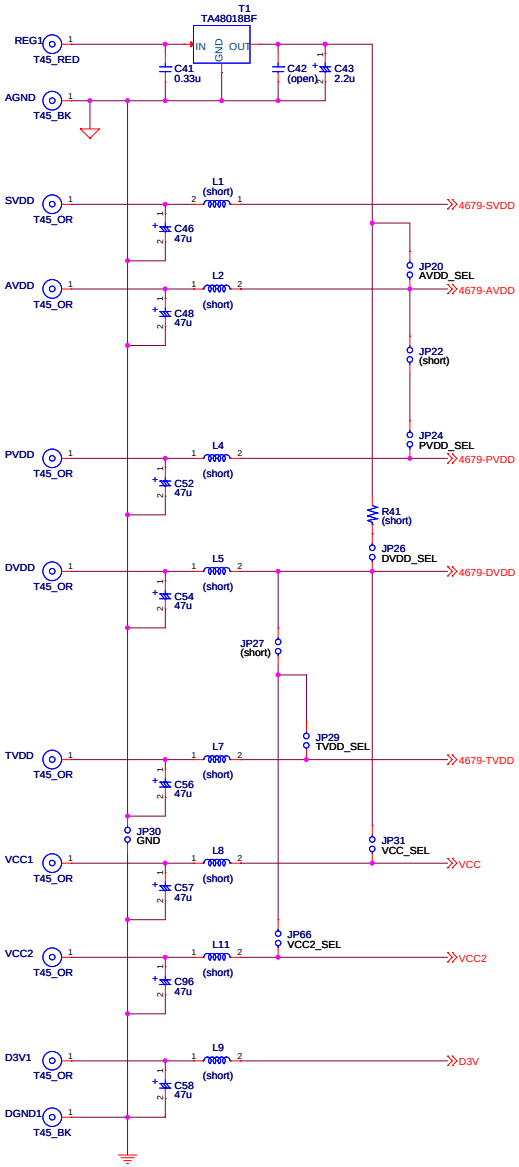
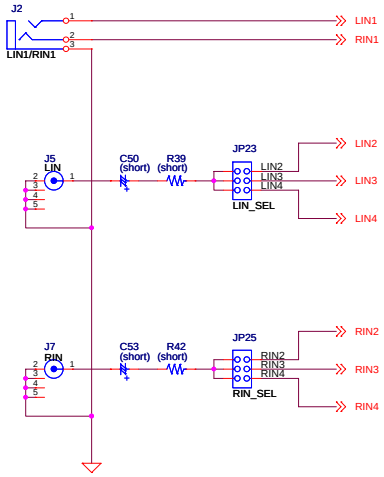
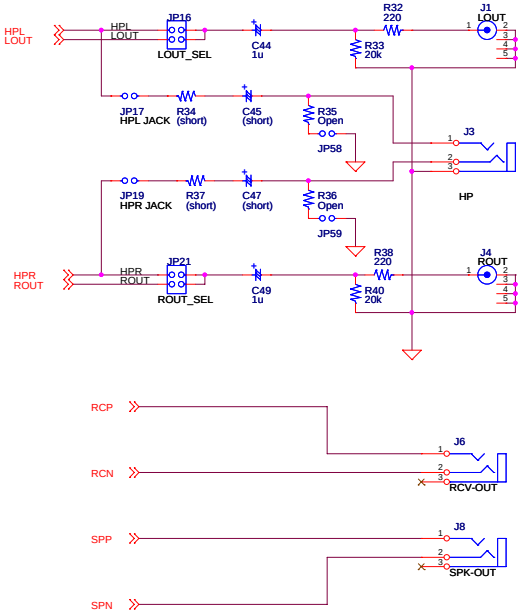
Size A2	Document Number Under SUB Board	Rev 0
Date: Thursday, July 07, 2011	Sheet 1 of 5	







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Size: A2	Document Number: Power Supply, I/O	Rev: 0
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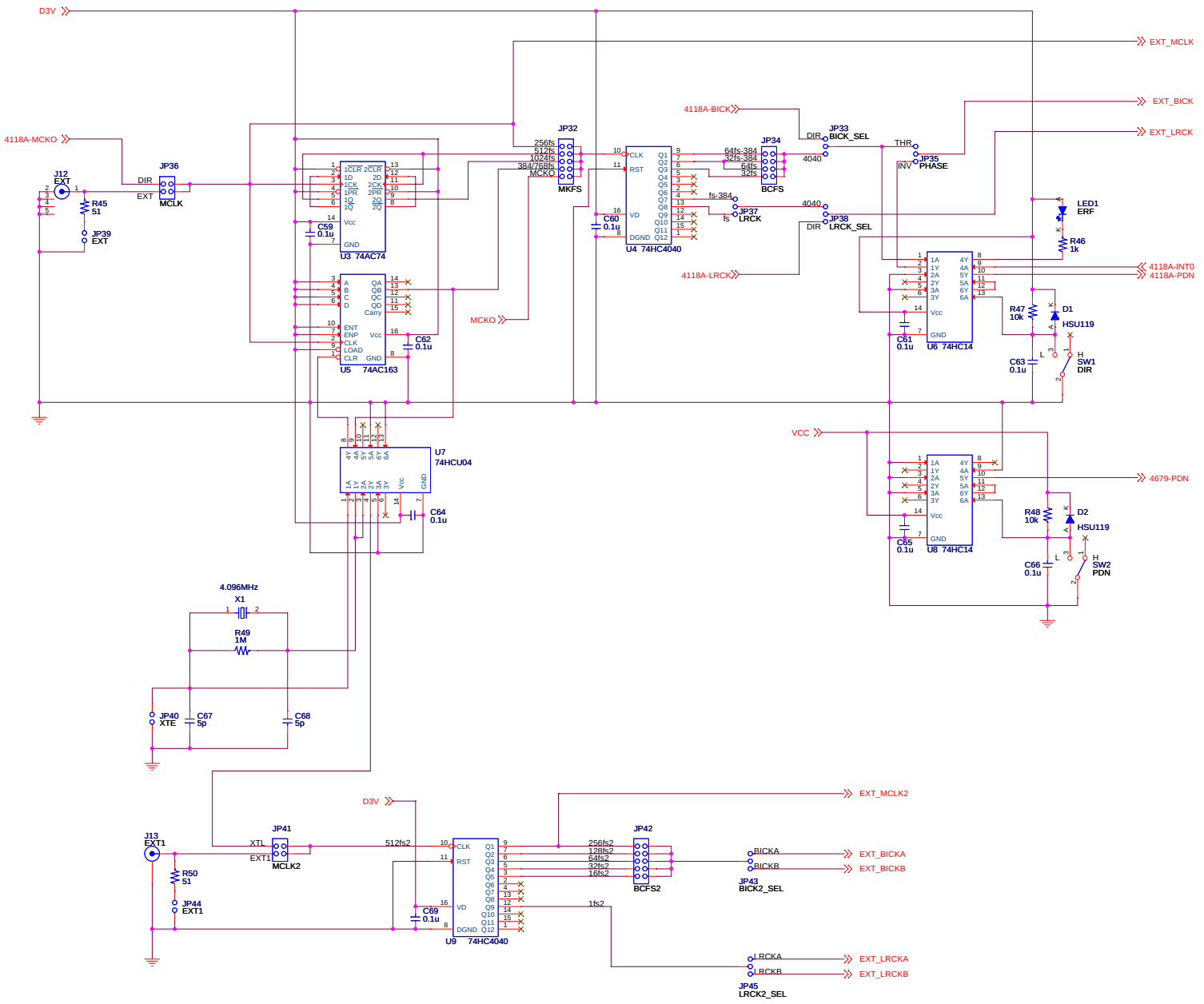

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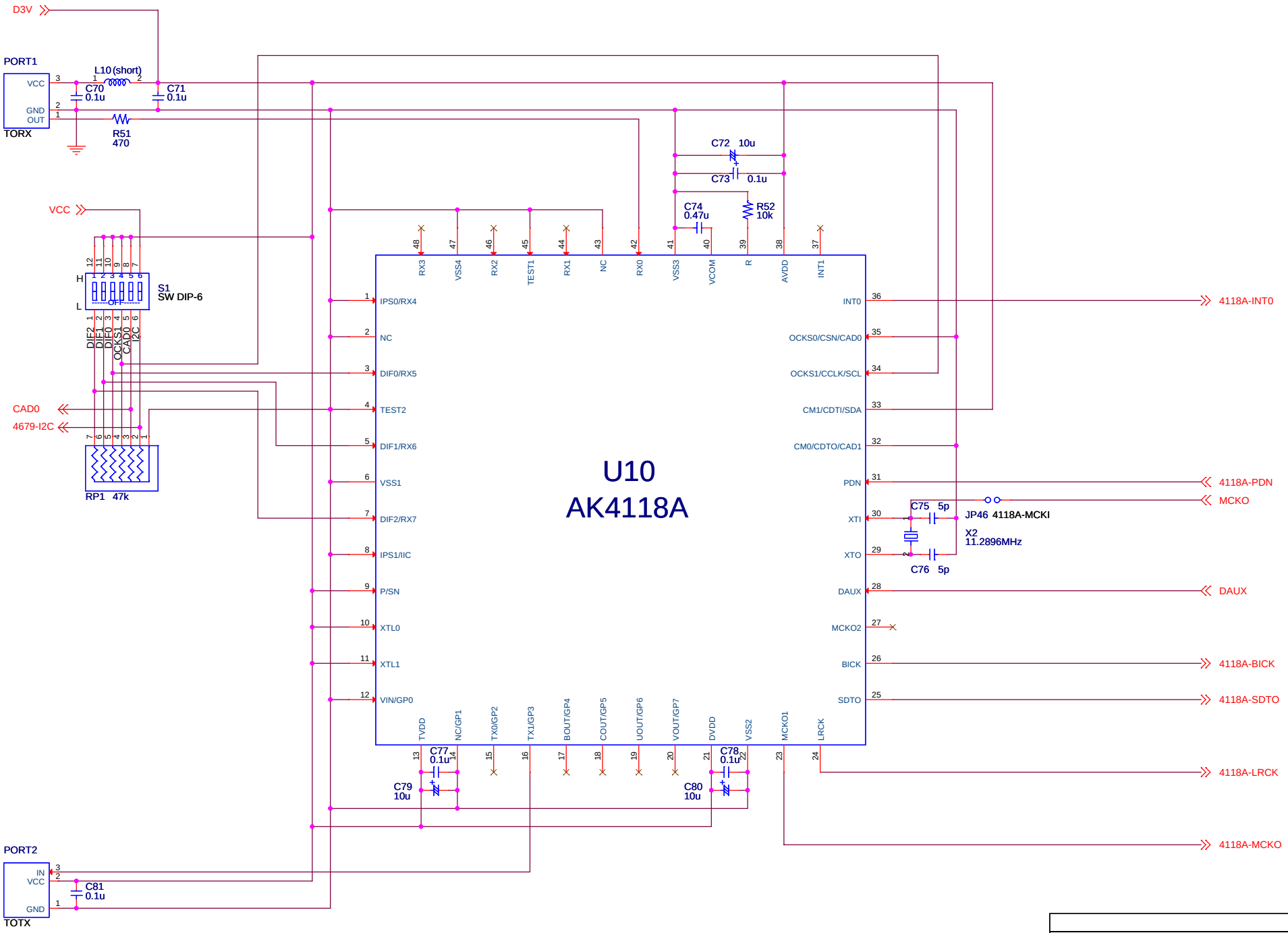

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Size A3	Document Number DIR/DIT	Rev 0
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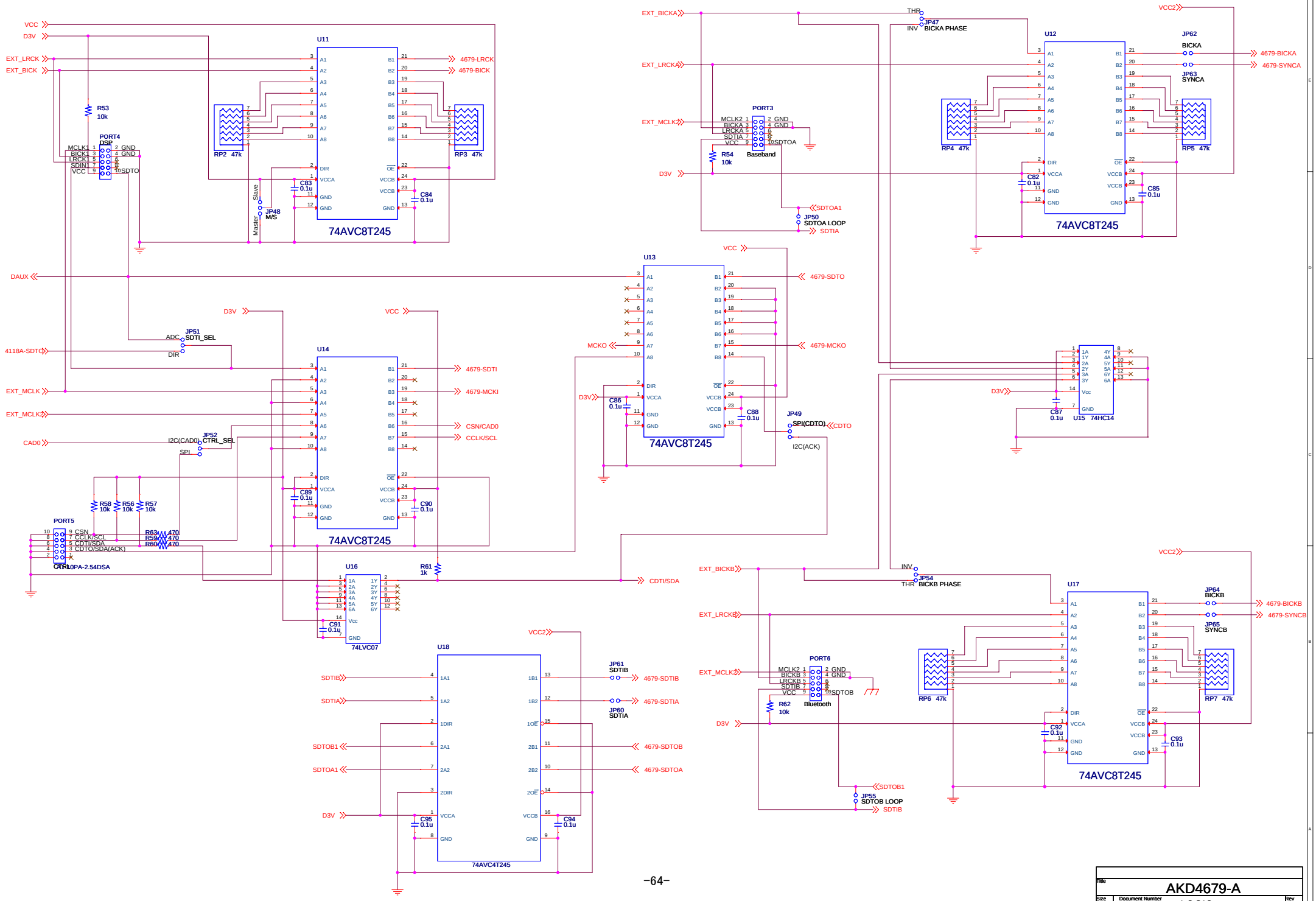

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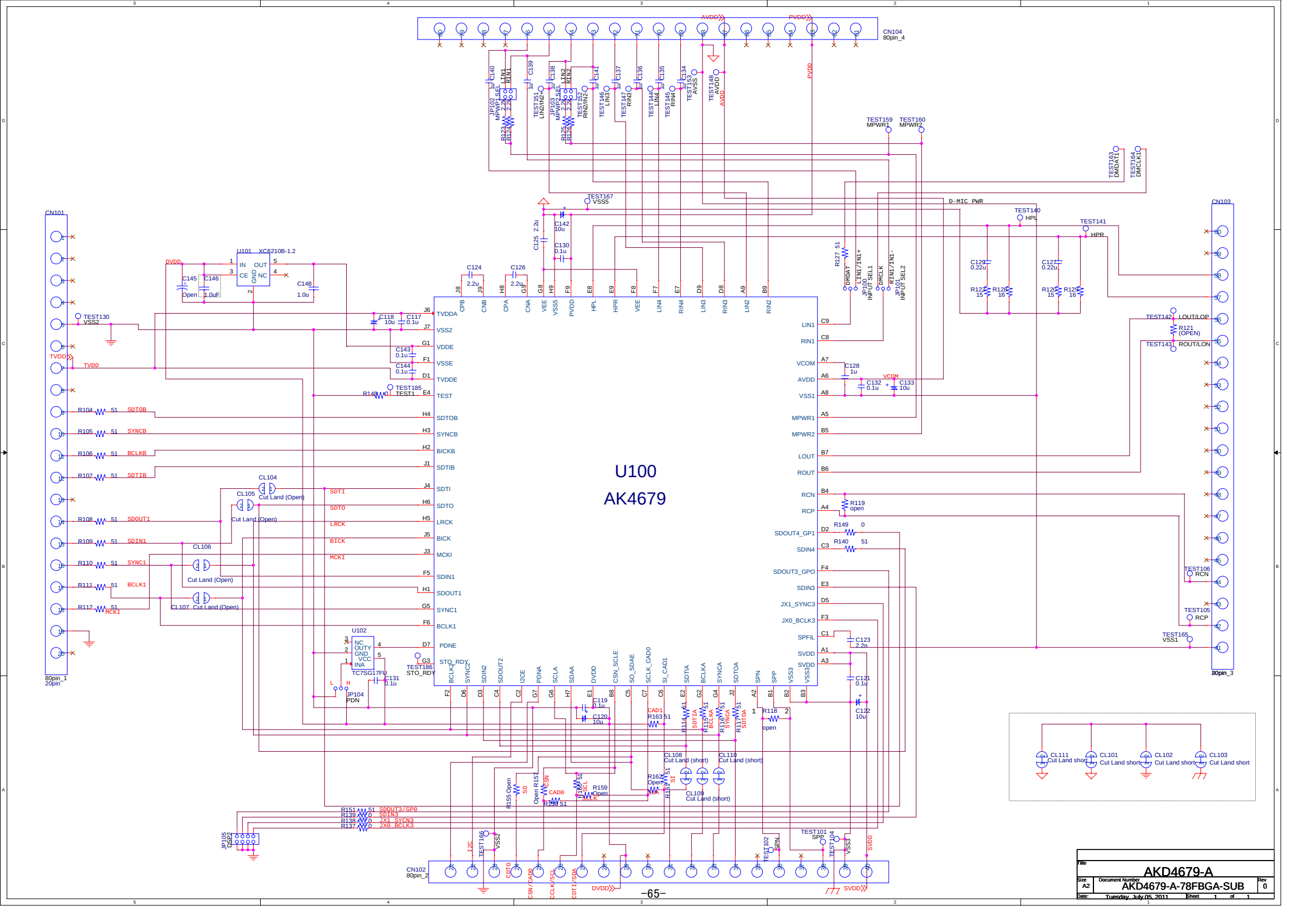
Size A2	Document Number LOGIC	Rev 0
Date: Thursday, July 07, 2011	Sheet 5 of 5	



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Size A2	Document Number AKD4679-A-78FBGA-SUB		Rev 0
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