AKD5353
Evaluation board Rev.C for AK5353

GENERAL DESCRIPTION

AKD5353 is an evaluation board for 96kHz 24bit A/D converter AK5353. AKD5353 includes the input buffer circuit and also has a digital interface transmitter. Further, the AKD5353 can evaluate direct interface with AKM's D/A converter evaluation boards.

■ Ordering guide

AKD5353 --- Evaluation board for AK5353

FUNCTION

- **On-board single-ended input buffer circuit**
- **On-board clock generator**
- **Compatible with 2 types of interface**
  - **Direct interface with AKM's D/A converter evaluation boards**
  - **On-board AK4103 as DIT which transmits optical output**
- **BNC connector for an external clock input**

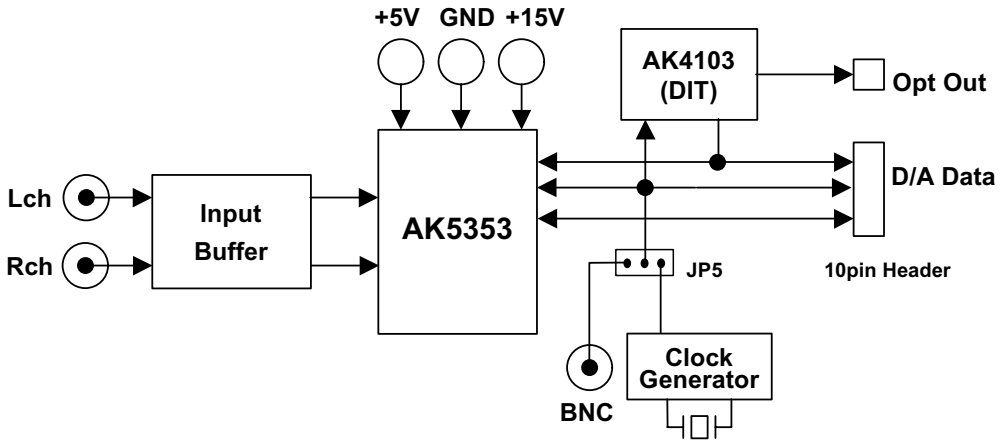


Figure 1. AKD5353 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Analog Inputs

J1(AINL) and J2(AINR) are used.
The analog inputs are single-ended and each signal range is nominally 3.0Vpp@5V.
It is proportional to VA (Vin=0.6xVA).

■ Operation sequence

1) Set up the power supply lines.

[+15V]	(orange)	= +12 ~ +15V (Note 2)
[+5V]	(red)	= 4.75 ~ 5.25V (Note 3)
[AGND]	(black)	= 0V
[DGND]	(black)	= 0V

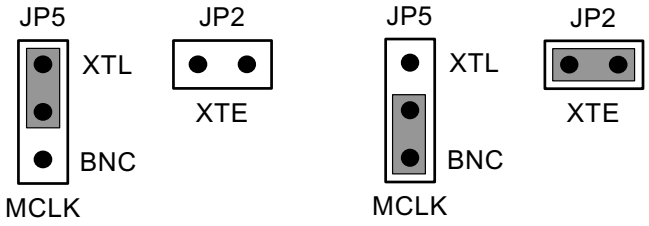
Note: 1. Each supply line should be distributed from the power supply unit.
2. JP100(REG) should be open and "+5V" jack should be shorted if VA and VD of the AK5353 are supplied from "+5V" jack .
3. JP100(REG) should be shorted and "+5V" jack should be open if VA and VD of the AK5353 are supplied from the regulator.

2) Set-up the evaluation modes, jumper pins and DIP switches (See the followings.)

3) Power on.
The AK5353 should be reset once bringing SW2 (PDN) "L" upon power-up.

■ Clock selection

Selection of clock source
In case of using X'tal on board select XTL on JP5(MCLK) and should be open JP2(XTE).
On the other hand, using external clock through a BNC connector (J3), select BNC on JP5(MCLK) and short JP2(XTE).

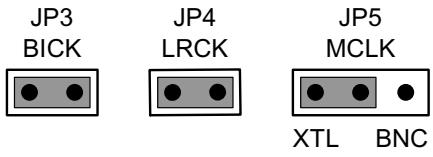


Using X'tal on board **Using BNC**

■ Evaluation mode

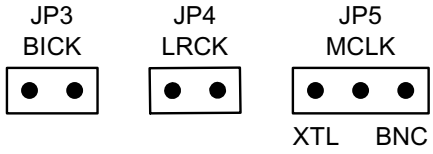
1) DIT Selection of clock mode

PORT1 (TOTX176) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. JP6 and JP7 should be selected same mode as AK5353. In case of using external clock through a BNC connector (J3), select BNC on JP5 (MCLK) and short JP2 (XTE).



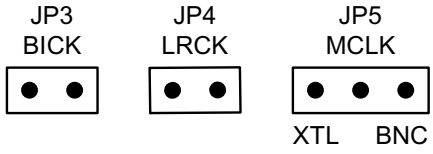
2) Using D/A converter board

The AK5353 can be evaluated by distortion analyzer using various AKM's D/A converter evaluation boards. They can be connected by 10pin flat cable via PORT2 (4Serial). If the AKD5353 feeds all interface signals (MCLK, SCLK, LRCK) to D/A converter board, jumper set up is same as 1) (See above). If all interface signals are fed from D/A converter board, jumper set up is same as 3) (See below).



3) All interface signals (MCLK, SCLK, LRCK) are fed from the external circuit through PORT2

PORT2 (4Serial) is used. JP3, 4 and 5 should be open.



■ DIP Switch set up list

[SW3]: Sets the mode of AK4103.

No.	Pin	ON	OFF
1	Validity	1	0
2	FS0	1	0
3	FS1	1	0

Table 1. DIP switch list for AK4103

■ SW1 Setting

1) V bit Setting

V bit can be set by No.1 switch.

SW1:No.1	Validity
ON	Valid (Default)
OFF	Invalid

2) C bit Setting

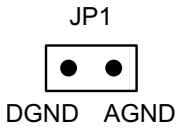
Bits 1-0 of Channel Status Byte 3 in consumer mode can be set by FS1-0 pins.
FS1-0 pins are set by No.2 and No.3 switches.

SW:No.3 (FS1)	SW:No.2 (FS0)	Fs	Byte 3 Bits 1-0
OFF	OFF	44.1kHz	00
OFF	ON	Default	01
ON	OFF	48kHz	10
ON	ON	32kHz	11

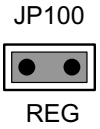
Table 2. Sampling frequency setting (Consumer mode)

■ Other jumper pins set up

[JP1] (DGND-AGND): Analog ground and digital ground
open: separated <default>
short: common (The connector "DGND" can be open.)



[JP100] (REG): Power supply of AK5353
short: VDD is supplied from the regulator
("+5V" jack should be open). <default>
open: VDD is supplied from "+5V" jack.



■ The function of the toggle SW.

[SW2]: Resets the AK5353 and AK4103. Keep "H" during normal operation.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit :Audio Precision, System two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz(48kHz), 40Hz~40kHz(96kHz)
- Bit : 24bit
- Power Supply : VA=VD=5V
- Interface : DIT
- Temperature : Room

fs=48kHz, VD=VA=5V

	L[dB]	R[dB]	BW
S/(N+D)	84.1	84.3	20kHzLPF
DR	95.3	95.4	20kHzLPF
	97.8	97.8	20kHzLPF+A-Weighted
S/N	95.4	95.4	20kHzLPF
	97.8	97.8	20kHzLPF+A-Weighted

fs=96kHz, VD=VA=5V

	L[dB]	R[dB]	BW
S/(N+D)	84.7	84.3	40kHzLPF
DR	95.3	95.3	40kHzLPF
	100.3	100.3	40kHzLPF+A-Weighted
S/N	95.3	95.3	40kHzLPF
	100.3	100.3	40kHzLPF+A-Weighted

Plots

[Measurement condition]

- Measurement unit: Audio Precision, System two, Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=DVDD=TVDD=5V
- Interface : DIT
- Temperature : Room

fs=48kHz

Figure 1-1. FFT (1kHz, -1dBFS input)
Figure 1-2. FFT (1kHz, -60dBFS input)
Figure 1-3. FFT (Noise floor)
Figure 1-4. THD+N vs. Input Level (fin=1kHz)
Figure 1-5. THD+N vs. fin (Input Level=-1dBFS)
Figure 1-6. Linearity (fin=1kHz)
Figure 1-7. Frequency Response (Input Level=-1dBFS)
Figure 1-8. Crosstalk (Input Level=-1dBFS)

fs=96kHz

Figure 2-1. FFT (1kHz, -1dBFS input)
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(1) fs=48kHz

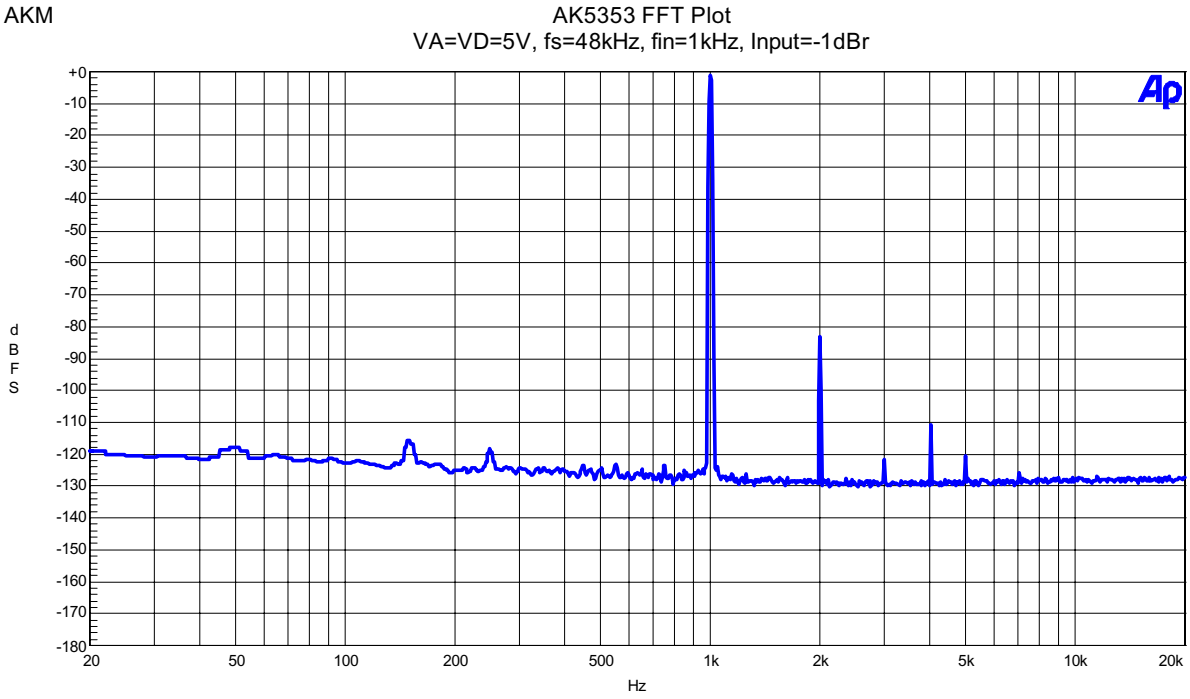

Figure 1-1. FFT (1kHz, -1dBFS input)

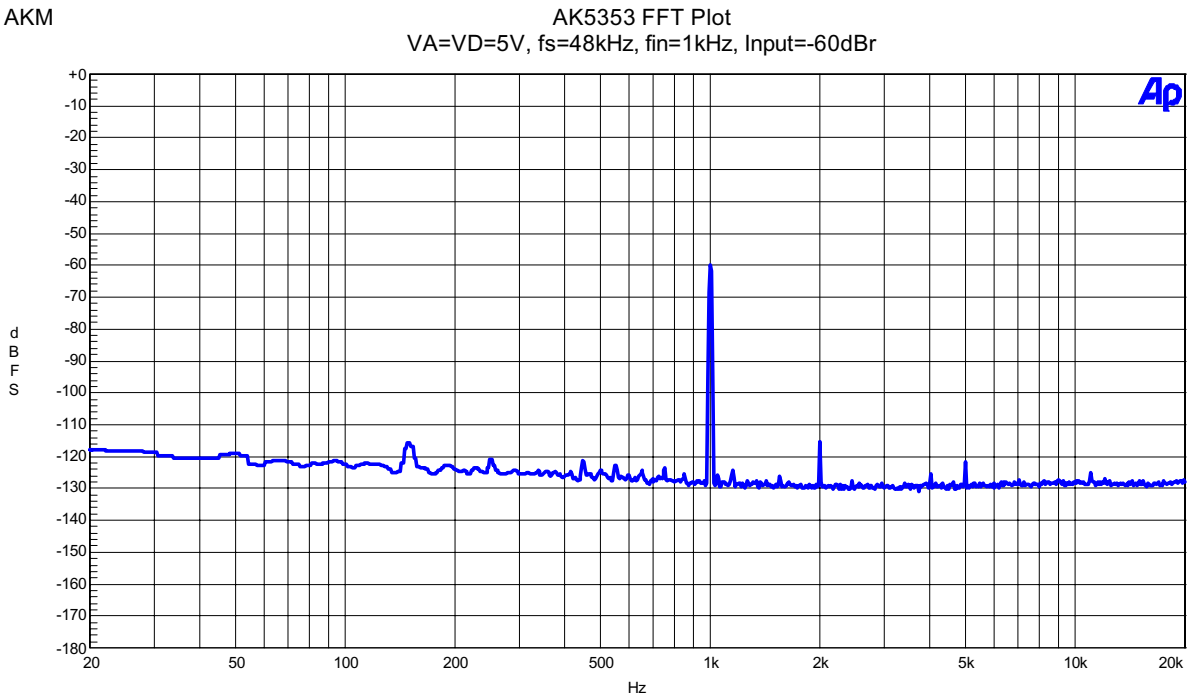

Figure 1-2. FFT (1kHz, -60dBFS input)

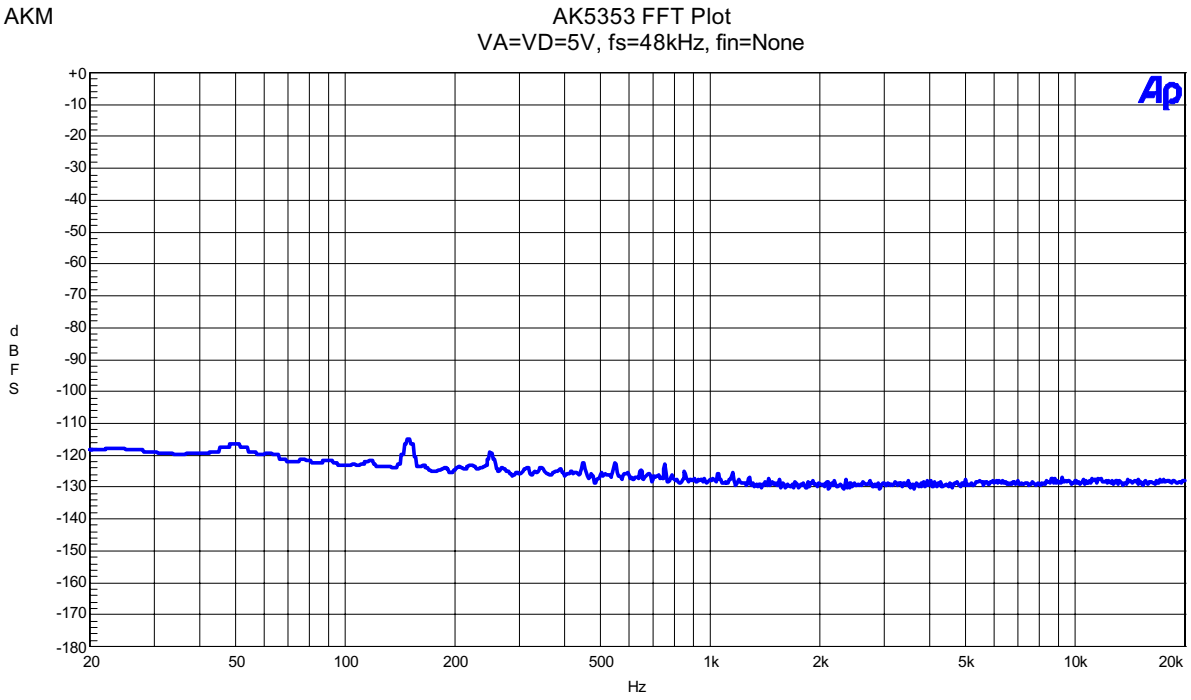

Figure 1-3. FFT (Noise floor)

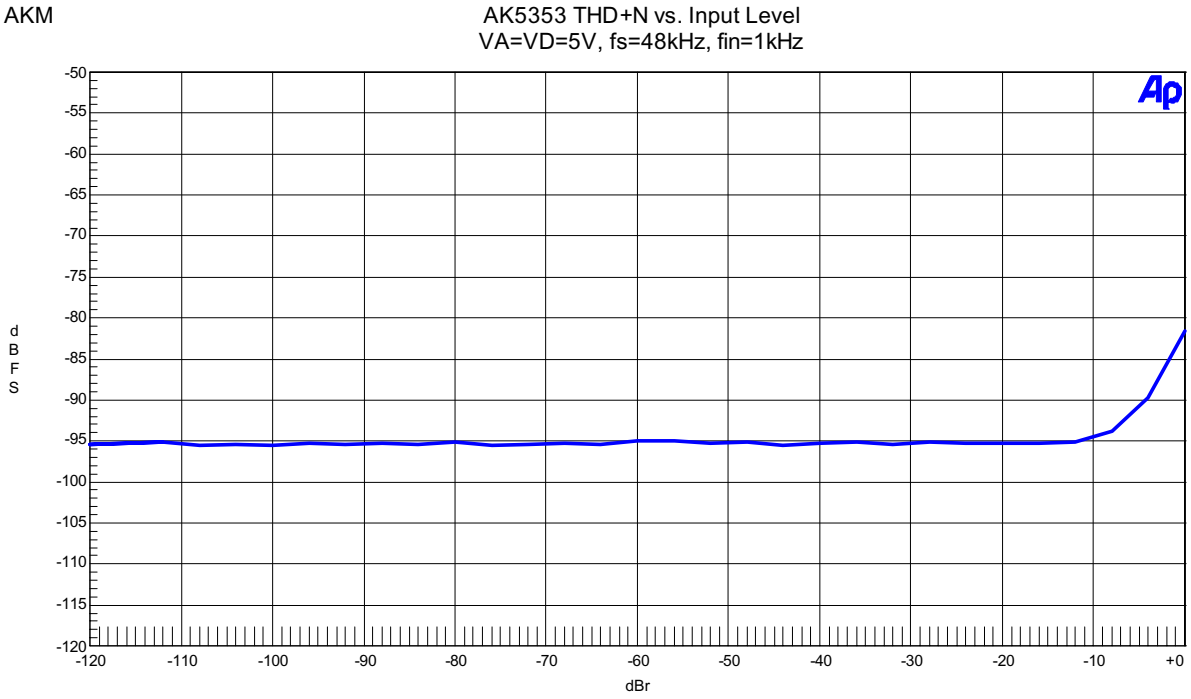

Figure 1-4. THD+N vs Input Level (fin=1kHz)

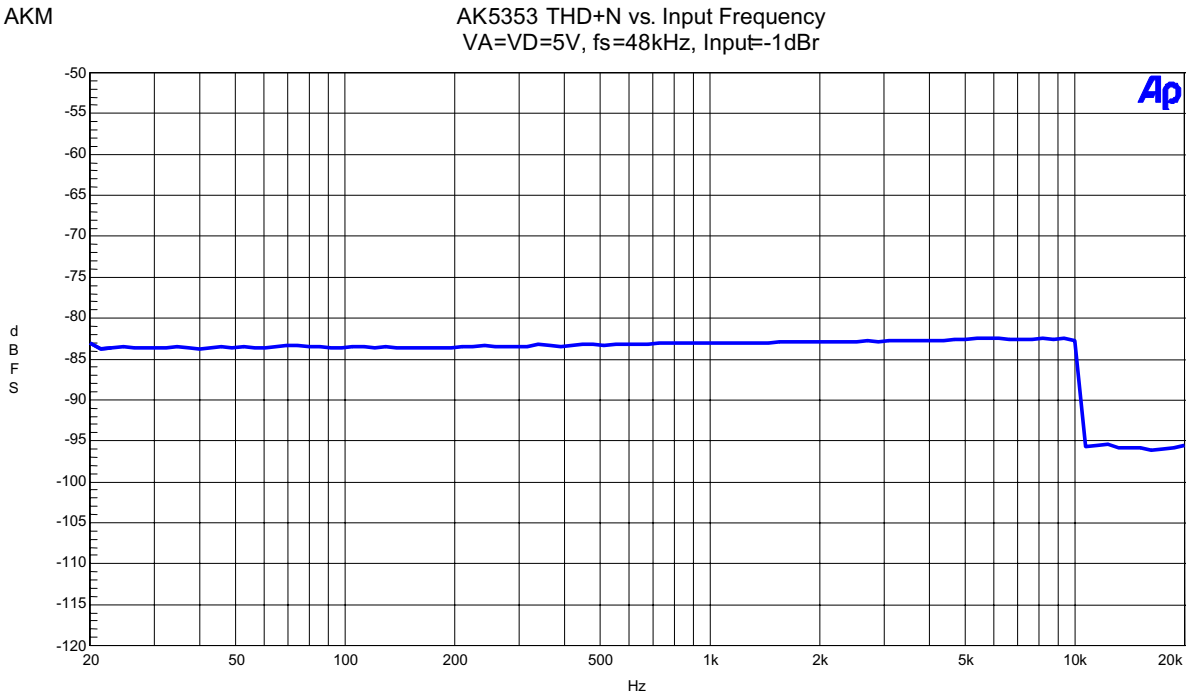

Figure 1-5. THD+N vs fin (Input Level=-1dBFS)

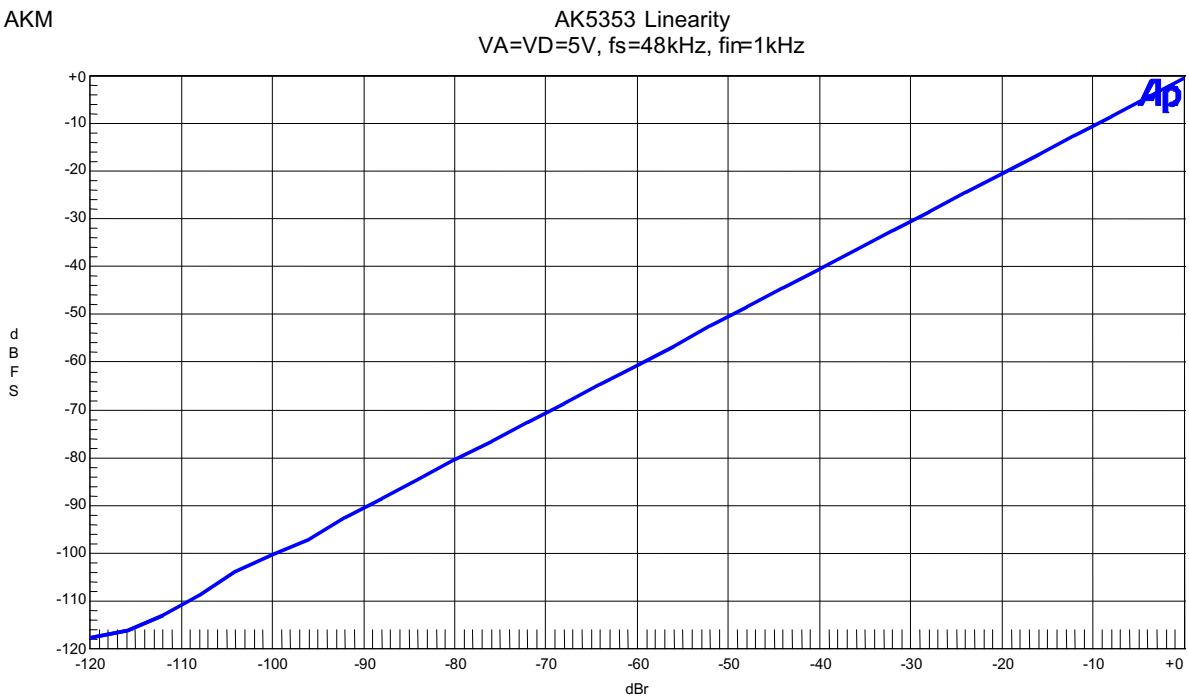

Figure 1-6. Linearity (fin=1kHz)

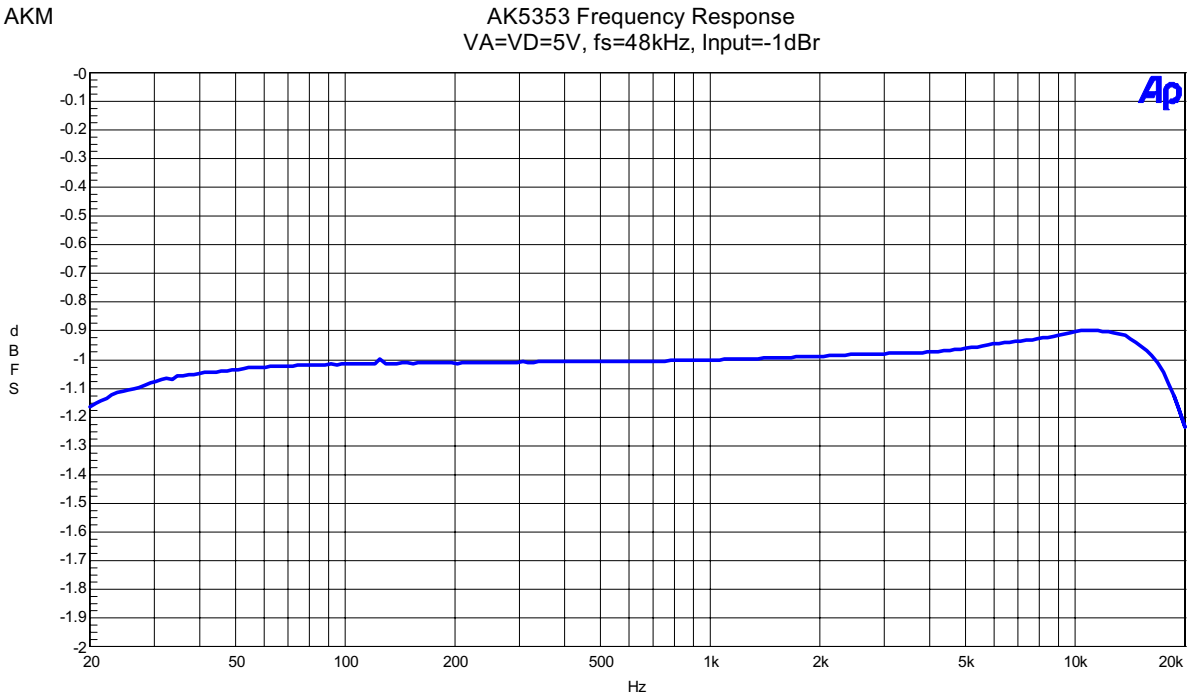

Figure 1-7. Frequency Response (Input Level=-1dBFS)

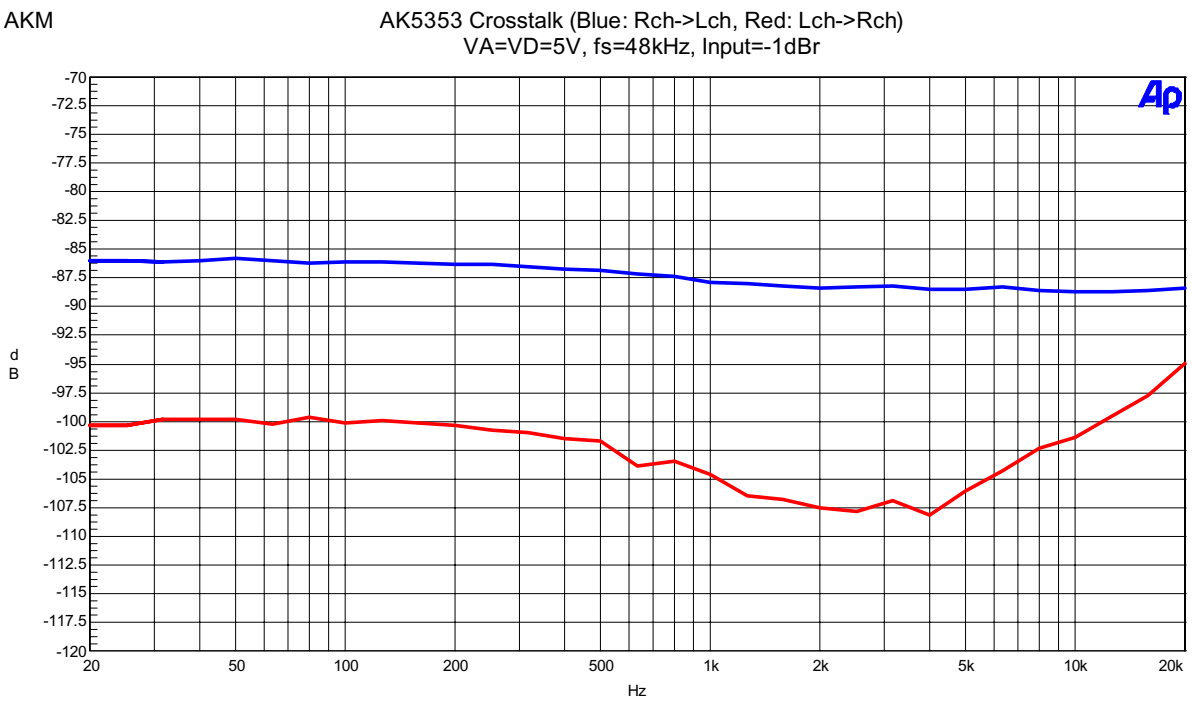

Figure 1-8. Crosstalk (Input Level=-1dBFS)

(2) fs=96kHz

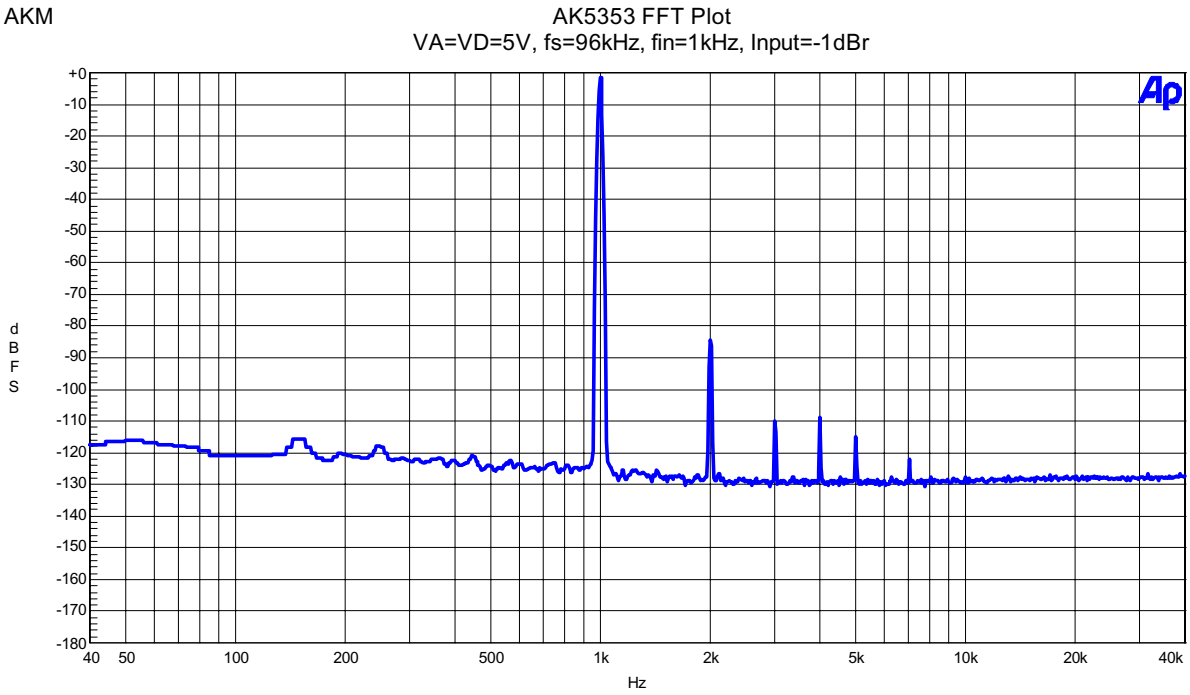

Figure 2-1. FFT (1kHz, -1dBFS input)

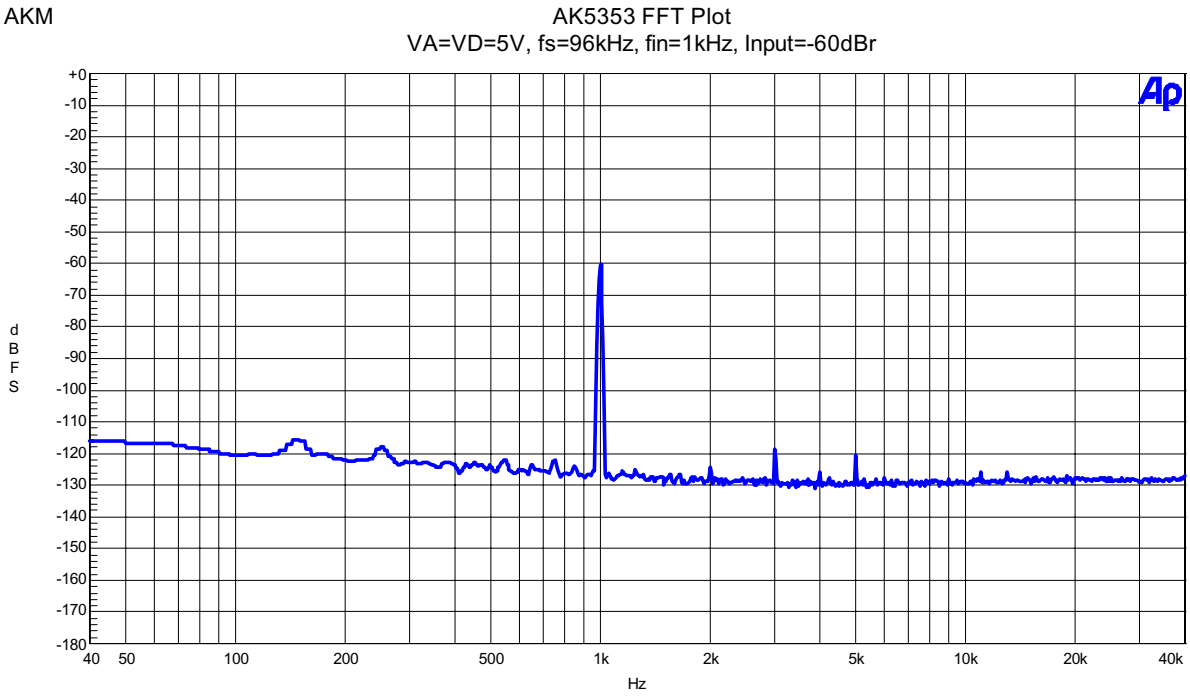

Figure 2-2. FFT (1kHz, -60dBFS input)

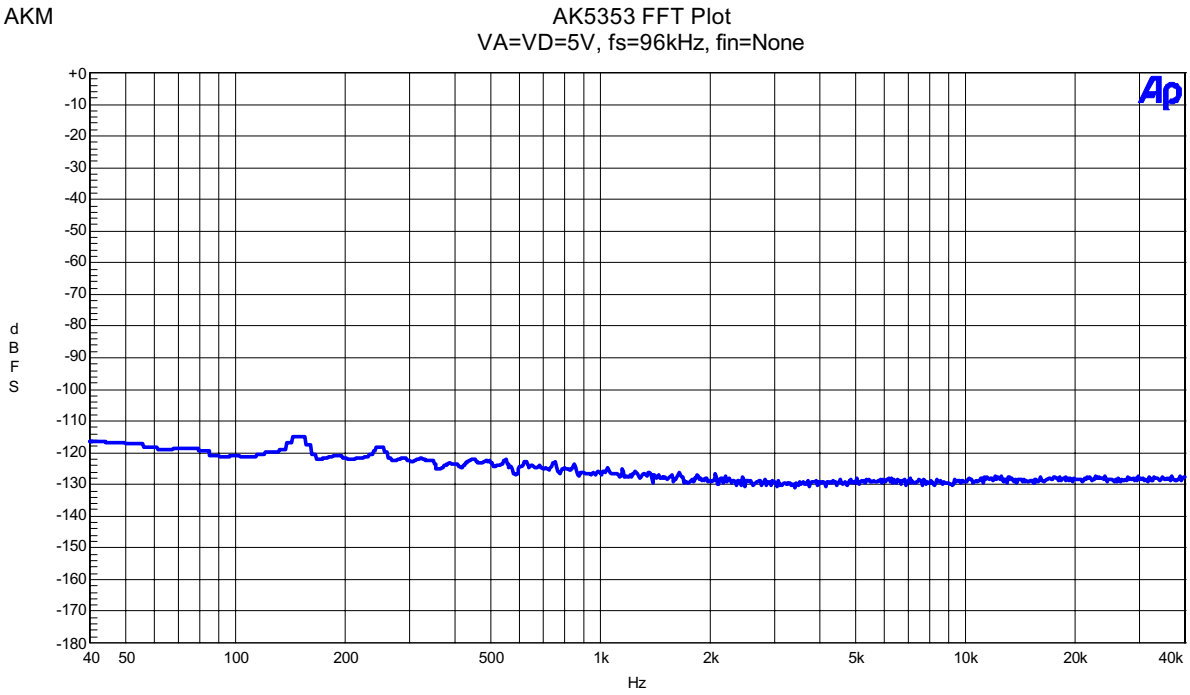

Figure 2-3. FFT (Noise floor)

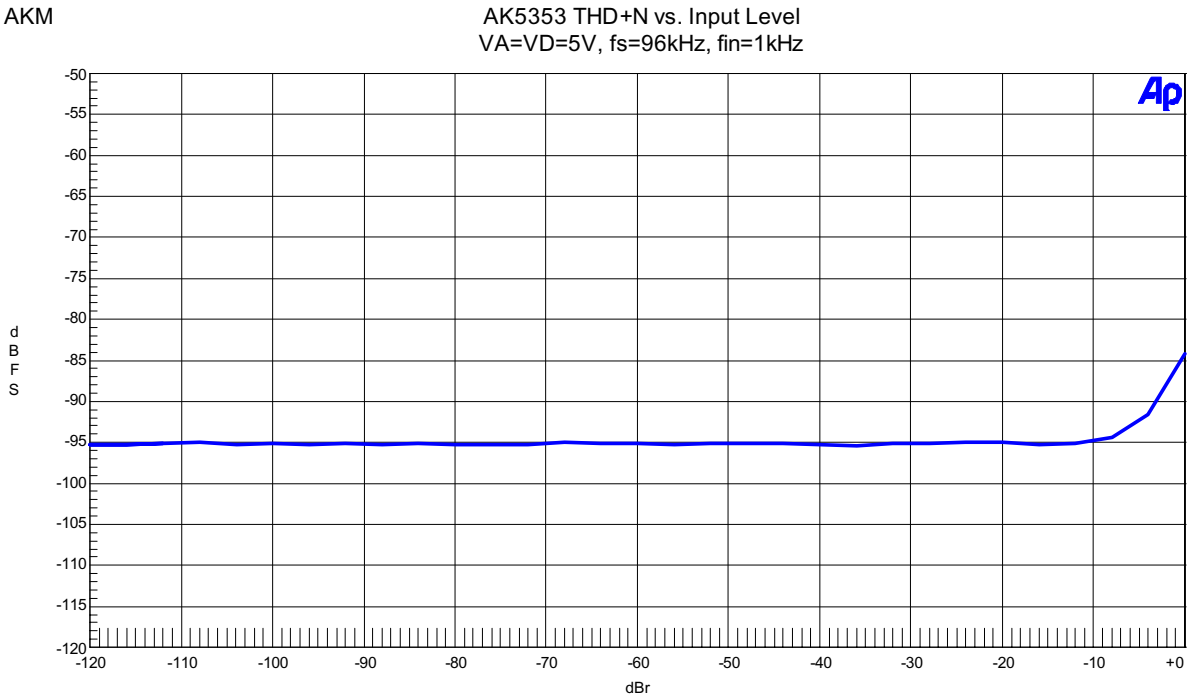

Figure 2-4. THD+N vs Input Level (fin=1kHz)

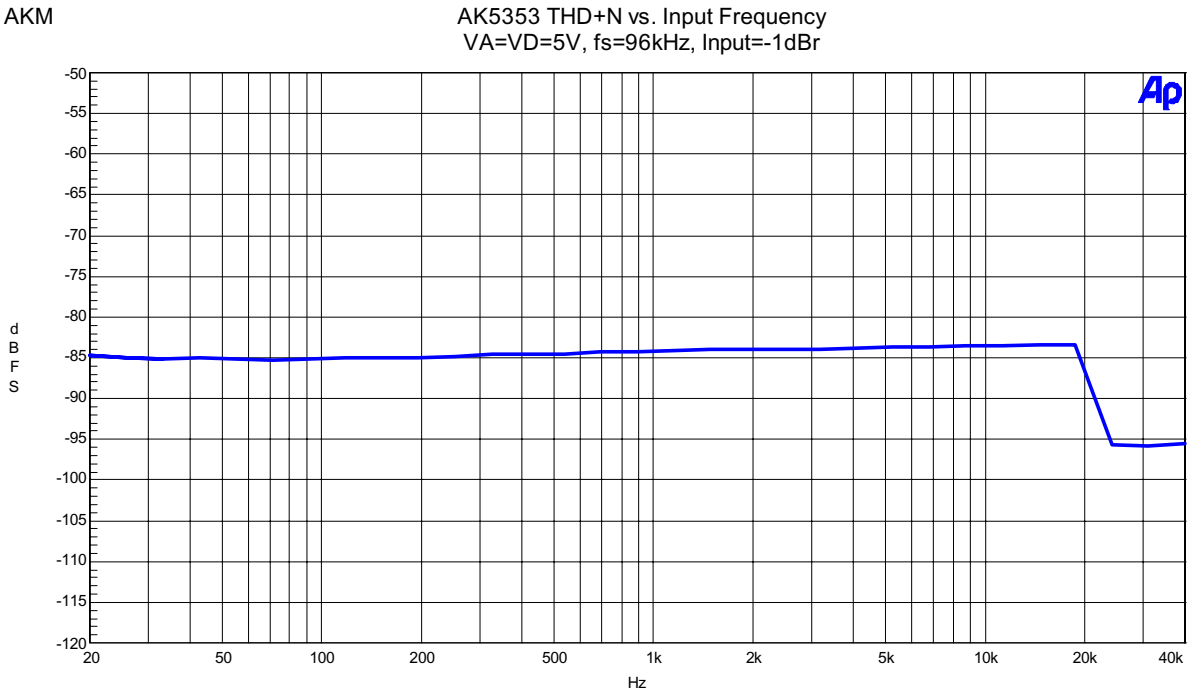

Figure 2-5. THD+N vs fin (Input Level=-1dBFS)

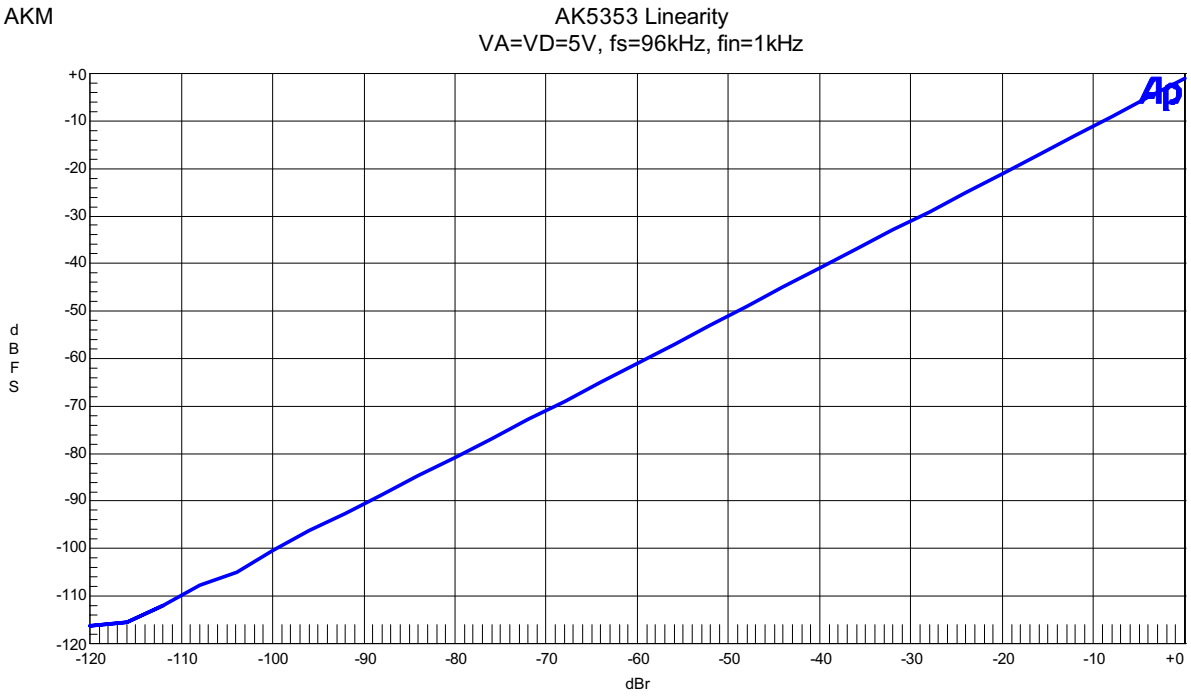

Figure 2-6. Linearity (fin=1kHz)

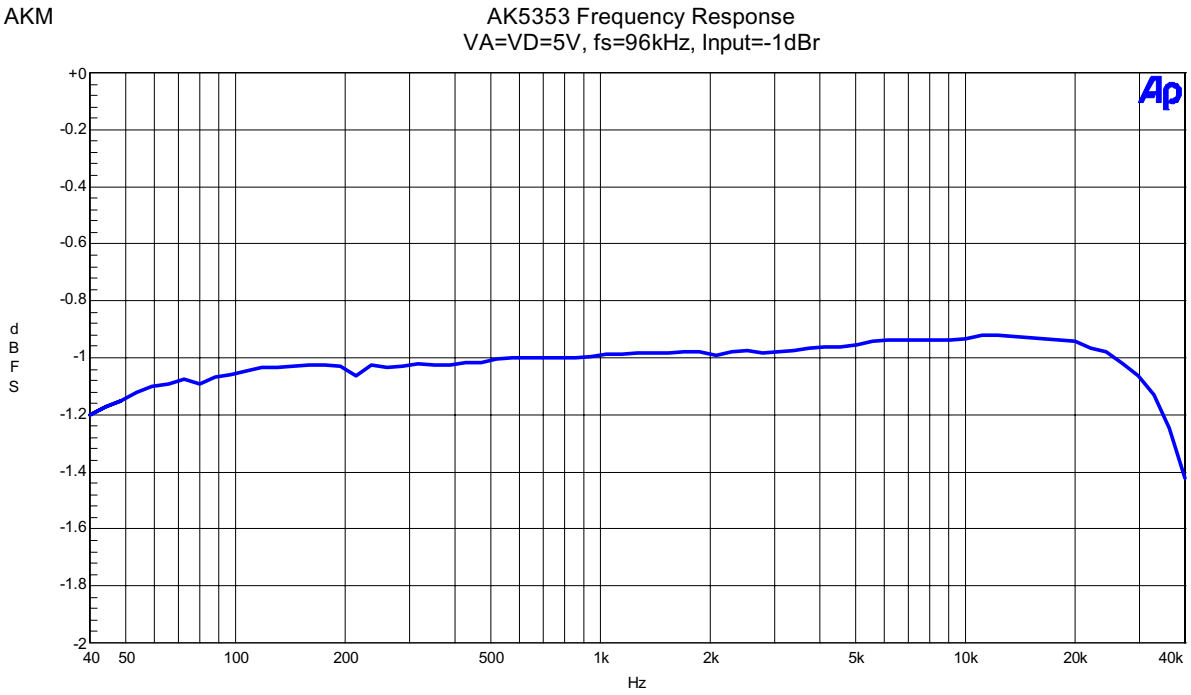

Figure 2-7. Frequency Response (Input Level=-1dBFS)

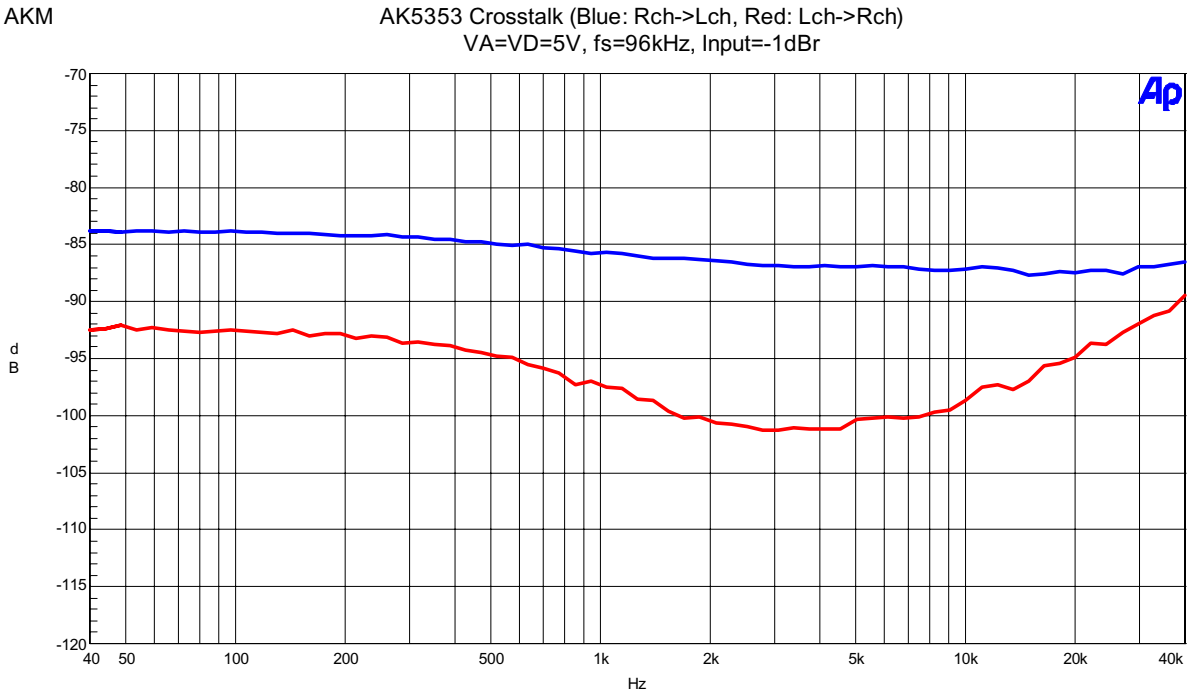

Figure 2-8. Crosstalk (Input Level=-1dBFS)

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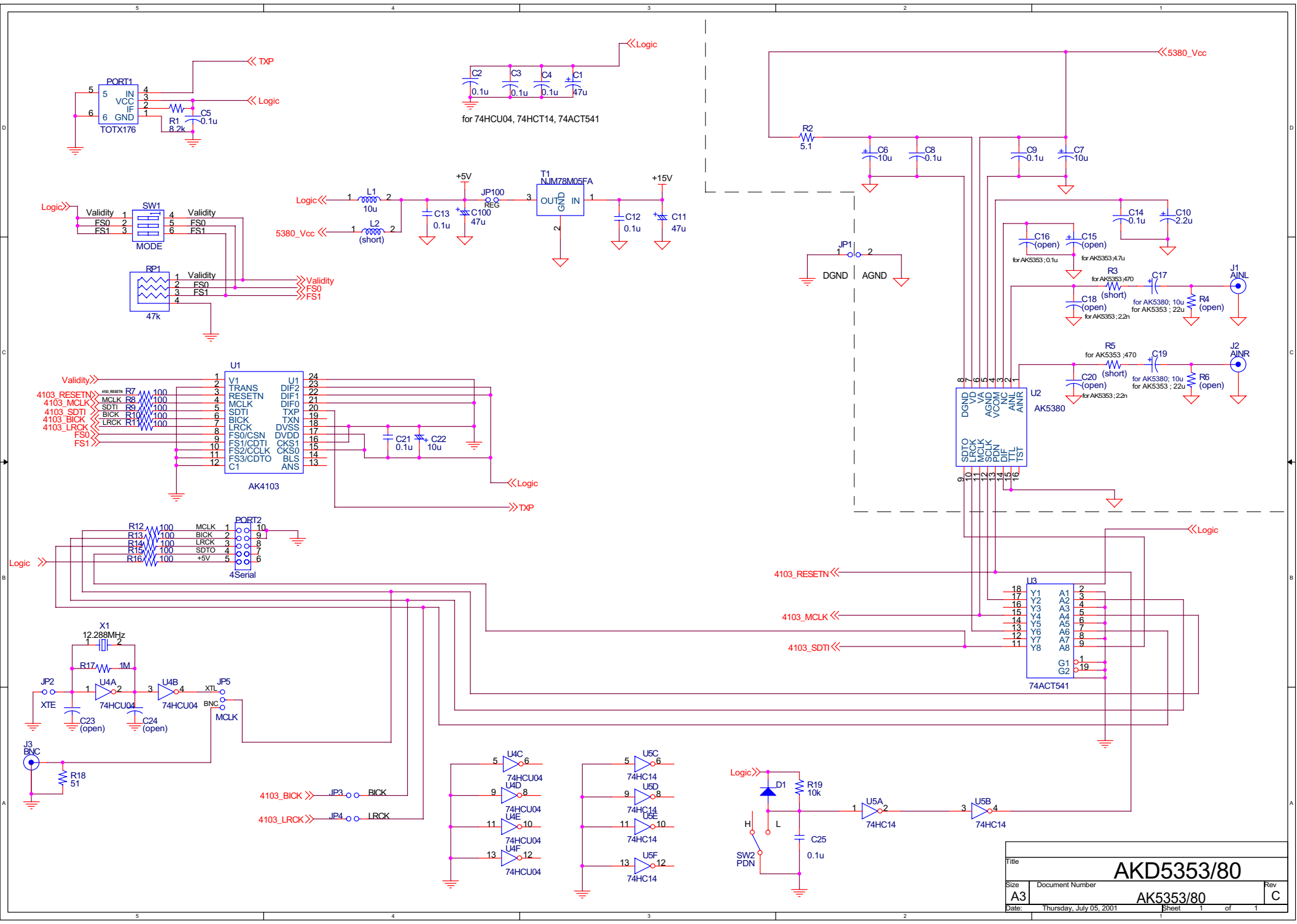
PORT1
TOTX176
TXP
Logic
R1
8.2k
C5
0.1u
for 74HCU04, 74HCT14, 74ACT541
C2
C3
C4
C1
0.1u
47u
5380_Vcc
R2
5.1
C6
10u
C8
0.1u
C9
0.1u
C7
10u
SW1
MODE
Validity
FS0
FS1
RP1
47k
L1
10u
L2
(short)
C13
C100
REG
JP100
T1
NJM78M05FA
OUT
GND
IN
+5V
+15V
C12
C11
JP1
DGND
AGND
C14
C10
2.2u
C16
(open)
C15
(open)
for AK5353 ; 0.1u
for AK5353 ;4.7u
R3
(short)
C17
C18
(open)
for AK5353 ;470
for AK5380; 10u
for AK5353 ; 22u
for AK5353 ; 2.2n
R4
(open)
J1
AINL
R5
C19
C20
R6
J2
AINR
U2
AK5380
DGND
VD
VA
AGND
VCOM
NC
AINL
AINR
SDTO
LRCK
MCLK
SCLK
PDN
DIF
TTL
TST
U1
AK4103
TRANS
RESETN
MCLK
SDTI
BICK
LRCK
FS0/CSN
FS1/CDTI
FS2/CCLK
FS3/CDTO
C1
V1
DIF2
DIF1
DIF0
TXP
TXN
DVSS
DVDD
CKS1
CKS0
BLS
ANS
4103_RESETN
4103_MCLK
4103_SDTI
4103_BICK
4103_LRCK
R7
R8
R9
R10
R11
100
C21
0.1u
C22
10u
PORT2
4Serial
R12
R13
R14
R15
R16
MCLK
BICK
LRCK
SDTO
+5V
U3
74ACT541
X1
12.288MHz
R17
1M
JP2
XTE
U4A
74HCU04
U4B
74HCU04
JP5
XTL
BNC
MCLK
C23
(open)
C24
(open)
J3
BNC
R18
51
JP3
BICK
JP4
LRCK
U4C
U4D
U4E
U4F
74HCU04
U5C
U5D
U5E
U5F
74HC14
D1
R19
10k
SW2
PDN
H
L
C25
0.1u
U5A
U5B
74HC14
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Size
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Rev
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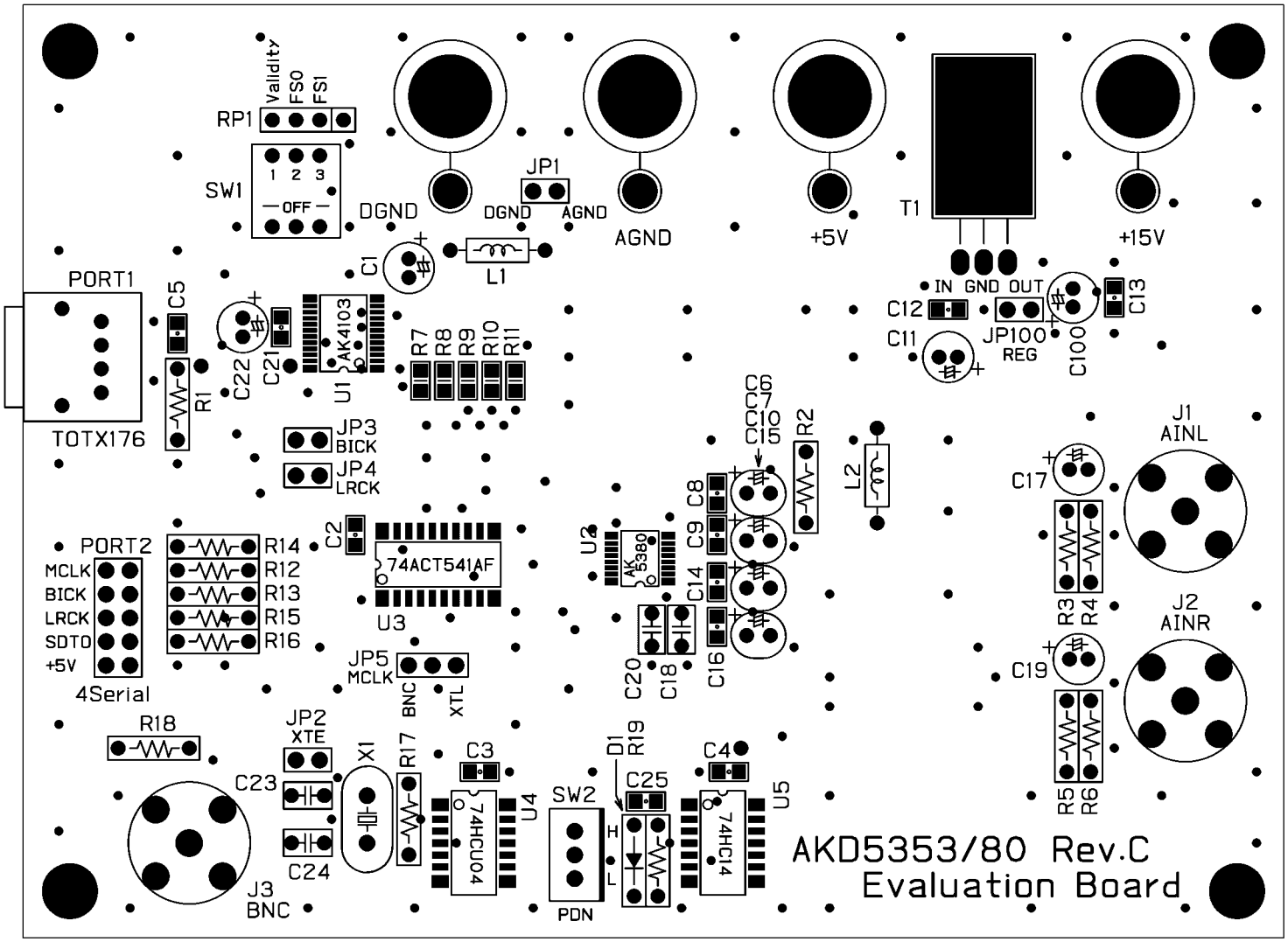
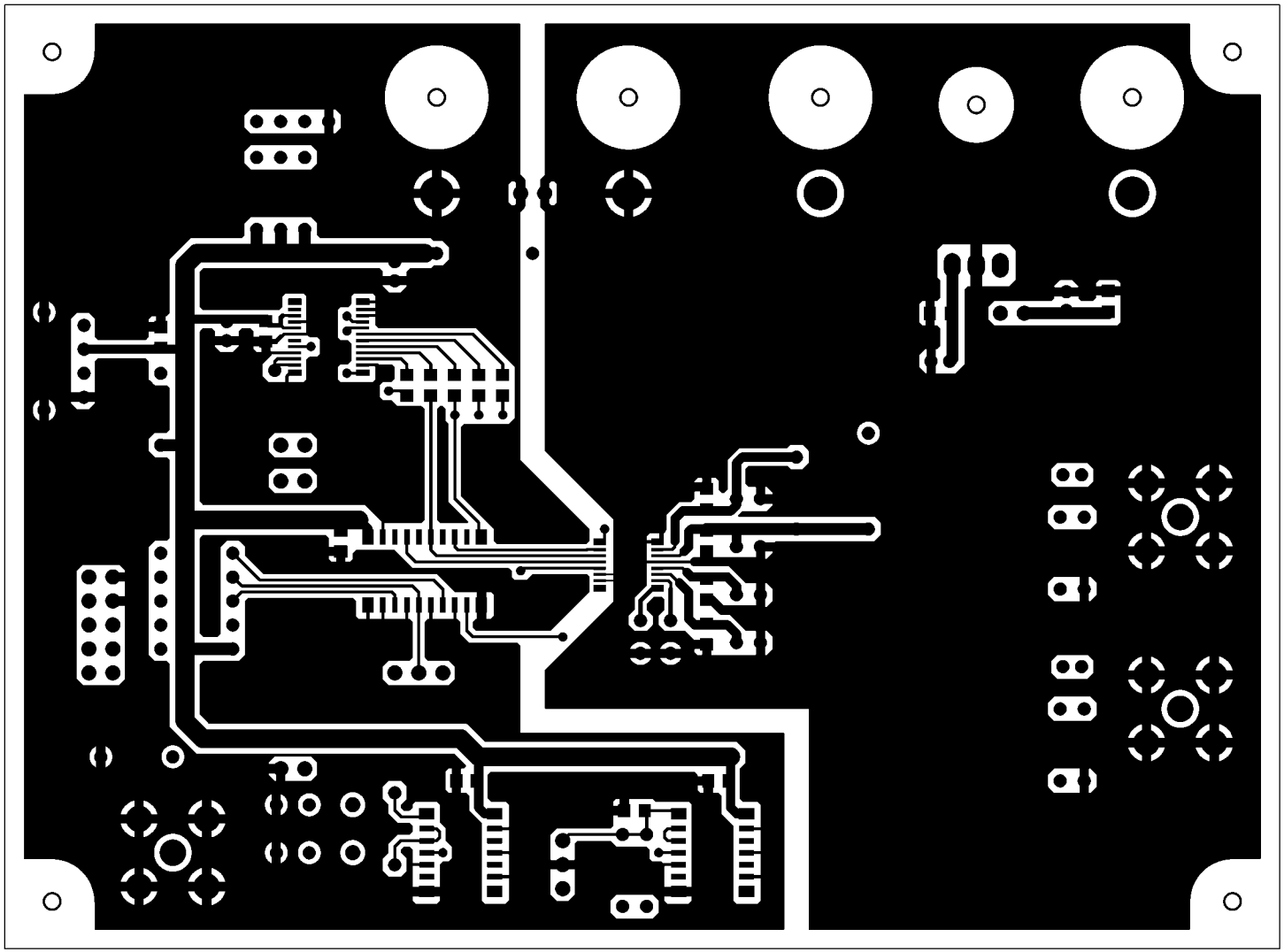
1
of
1



AKD5353/80 Rev.C L1 SR SILK



AKD5353/80 Rev.C L1

AKD5353/80 Rev.C L2