AKD4953-A
Evaluation board Rev.2 for AK4953

GENERAL DESCRIPTION

The AKD4953-A is an evaluation board for the AK4953 24bit CODEC with built-in PLL and MIC/HP/SPK Amplifier. The AKD4953-A has the interface with AKM's A/D evaluation boards. Therefore, it's easy to evaluate the AK4953. The AKD4953-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering Guide

AKD4953-A --- Evaluation board for AK4953
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin header for serial control interface**

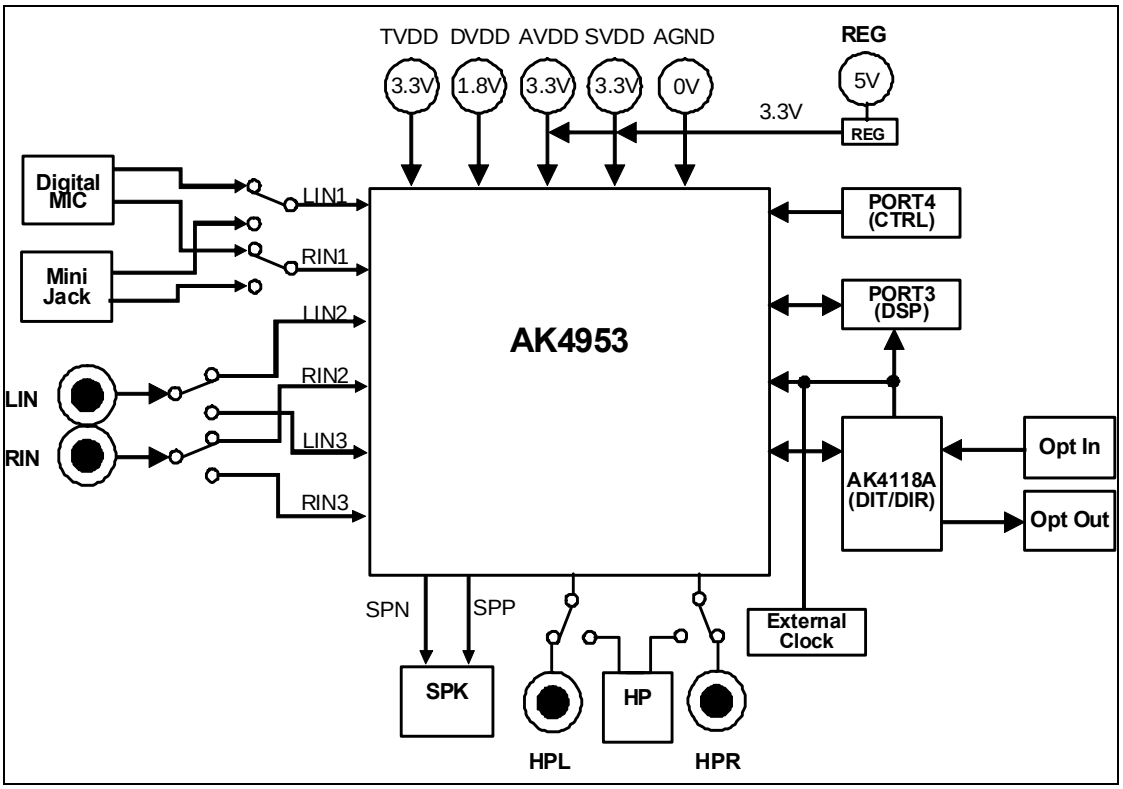


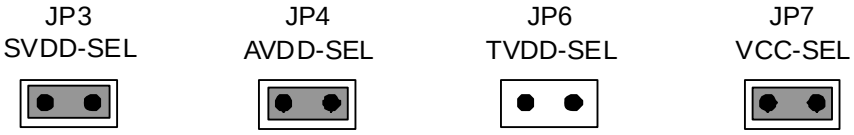
Figure 1. AKD4953-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation Sequence

(1) Set up the power supply lines.

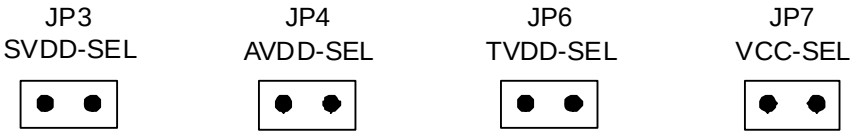
(1-1) In case of using the regulator. <Default>



Name of Jack	Color	Default Setting	Using
REG	red	5V	for regulator (3.3V output : AVDD ,SVDD)
AVDD	orange	Open	for AVDD of AK4953
SVDD	orange	Open	for SVDD of AK4953
DVDD	orange	1.6~2.0V (typ1.8V)	for DVDD of AK4953
TVDD	orange	1.6~3.5V (typ3.3V)	for TVDD of AK4953
VCC	orange	Open	for logic
D3V	orange	2.7~3.6V (typ3.3V)	for AK4118A and logic
AGND	black	0V	for analog ground
DGND	black	0V	for logic ground

Table 1. Set up of power supply lines

(1-2) In case of using the power supply connectors.



Name of Jack	Color	Default Setting	Using
REG	red	Open	No using
AVDD	orange	3.0~3.5V (typ3.3V)	for AVDD of AK4953
SVDD	orange	0.9~5.5V (typ3.3V)	for SVDD of AK4953
DVDD	orange	1.6~2.0V (typ1.8V)	for DVDD of AK4953
TVDD	orange	1.6~3.5V (typ3.3V)	for TVDD of AK4953
VCC	orange	1.6~3.5V (typ3.3V)	for logic(This voltage must be same as TVDD)
D3V	orange	2.7~3.6V (typ3.3V)	for AK4118A and logic
AGND	black	0V	for analog ground
DGND	black	0V	for logic ground

Table 2. Set up of power supply lines

* Each supply line should be distributed from the power supply unit.

(2) Set up the evaluation mode, jumper pins and DIP switch. (See the followings.)

(3) Power on.

The AK4953 and AK4114 should be reset once bringing SW1 (PDN) and SW2 (DIR) “L” upon power-up.
Click the reset button on the control software after releasing the reset by SW1= “H”.

■ Evaluation mode

In case of using the AK4118A when evaluating the AK4953, both the AK4953 and AK4118A's audio interface formats must be matched.
Reter to the datasheet for AK4953's audio interface format, and Table 3 for AK4118's audio interface format.
The AK4118A operates at fs of 32kHz or more. If the fs is slower than 32kHz, please use other mode.
In addition, MCLK of AK4118A supports 256fs and 512fs. When evaluating in a condition except above, please use other mode.
Refer to the datasheet for register setting of the AK4953.

Applicable Evaluation Mode

(1) Evaluation of A/D using DIT of AK4118A.
  (1-1) Setting with External Slave Mode

(2) Evaluation of D/A using DIR of AK4118A. <Default>
  (2-1) Setting with External Slave Mode

(3) Evaluation of A/D, D/A using PORT3 (DSP).
  (3-1) Setting with PLL Master Mode
  (3-2) Setting with PLL Slave Mode
  (3-3) Setting with External Slave Mode

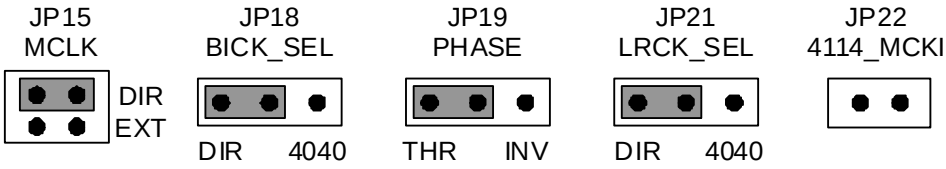
(4) Evaluation of Loop-back.
  (4-1) Setting with PLL Master Mode
  (4-2) Setting with PLL Slave Mode
  (4-3) Setting with External Slave Mode

(1) Evaluation of A/D using DIT of AK4118A.

(1-1) Setting with External Slave Mode

X1 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, Registers of the AK4953 should be set to "EXT Slave Mode".
MCKI, BICK and LRCK are supplied from the AK4118A, and SDTO of the AK4953 is output to the AK4118A.

The jumper pins should be set as follows.

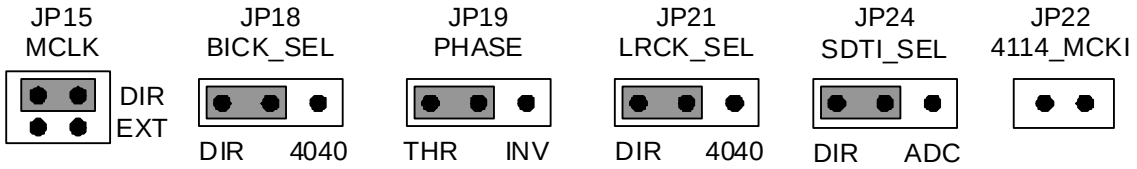


(2) Evaluation of D/A using DIR of AK4118A. <Default>

(2-1) Setting with External Slave Mode

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, Registers of the AK4953 should be set to "EXT Slave Mode".

The jumper pins should be set as follows.



(3) Evaluation of A/D, D/A using PORT3 (DSP).

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).

(3-1) Setting with PLL Master Mode

The master clock is input from MCKI of PORT3 (DSP). An internal PLL circuit generates MCKO, BICK, and LRCK.

JP23 (M/S) should be set to "Master". In addition, Registers of the AK4953 should be set to "PLL Master Mode".

SDTI, SDTO, LRCK and BICK of PORT3 are respectively connected with SDTO, SDTI, LRCK and BICK of DSP. When MCKO is supplied to DSP, test pin (MCKO) should be directly connected to DSP.

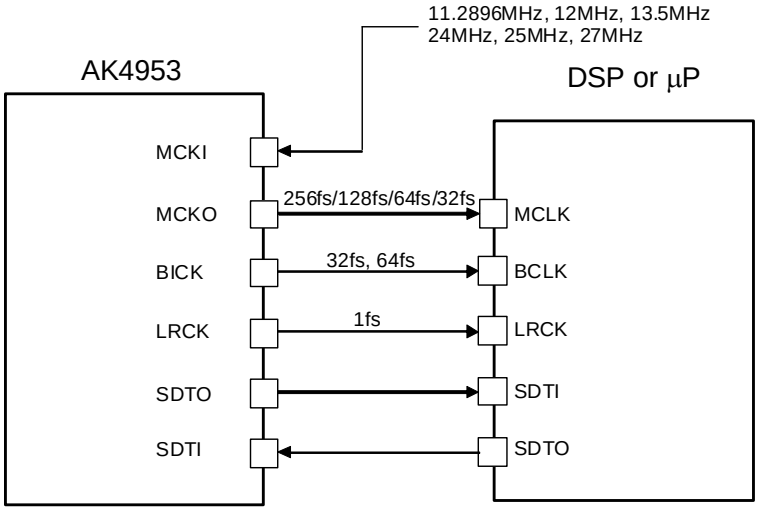
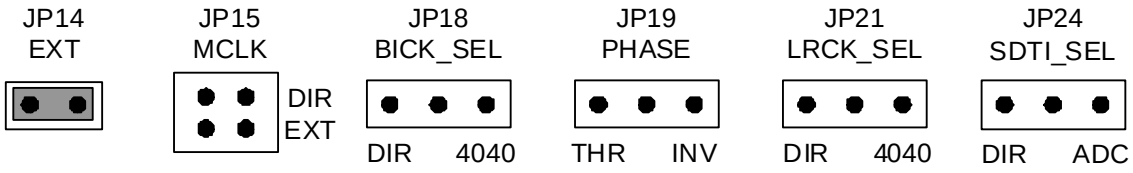


Figure 2. PLL Master Mode

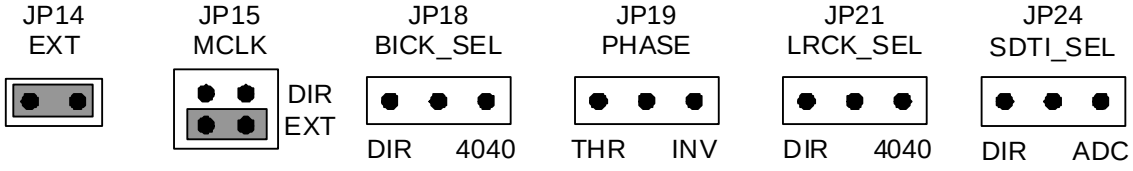
①Supplied Master Clock (MCKI) from MCLK (PORT3).

The jumper pins should be set as follows.



②Supplied Master Clock (MCKI) from J11.

The jumper pins should be set as follows.



*When a termination (51Ω) is not used, JP14 (EXT) should be open.

(3-2) Setting with PLL Slave Mode

A reference clock of PLL is selected among the input clocks supplied from PORT3 (DSP) to MCKI, BICK or LRCK pin. The required clock to the AK4953 is generated by an internal PLL circuit.
JP23 (M/S) should be set to "Slave".

(3-2-1) PLL Reference Clock: MCKI pin

Registers of the AK4953 should be set to "PLL Slave Mode" (Reference Clock: MCKI).
BICK and LRCK inputs should be synchronized with MCKO output. However the phase between MCKO and LRCK dose not matter.

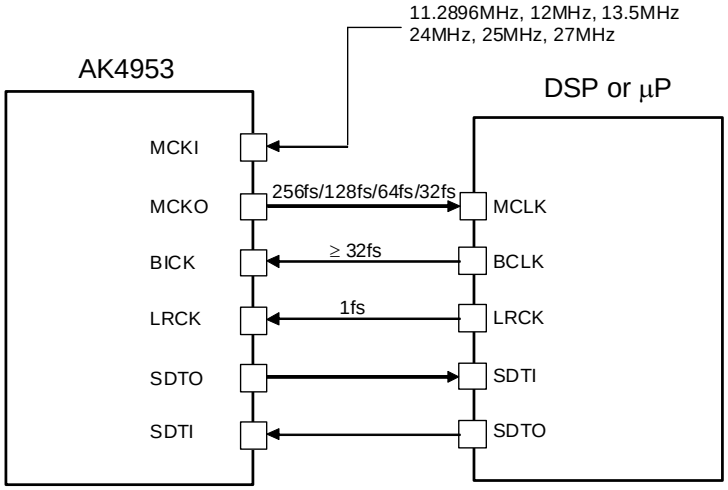
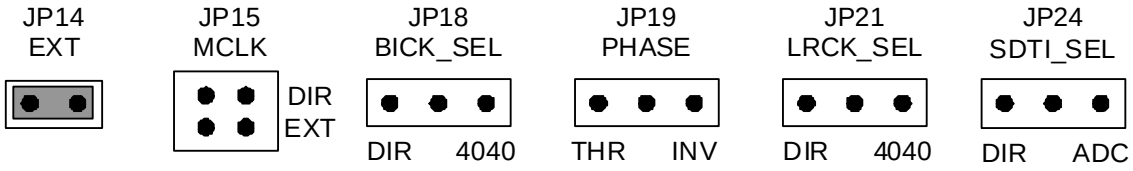


Figure 3. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

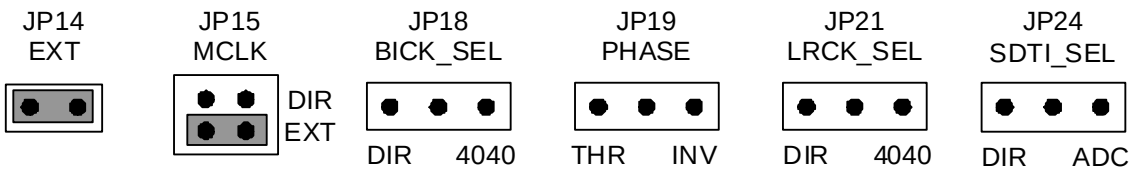
① Supplied Master Clock (MCKI) from MCLK (PORT3).

The jumper pins should be set as follows.



② Supplied Master Clock (MCKI) from J11.

The jumper pins should be set as follows.



*When a termination (51Ω) is not used, JP14 (EXT) should be open.

(3-2-2) PLL Reference Clock: BICK pin

Registers of the AK4953 should be set to "PLL Slave Mode" (Reference Clock = BICK).

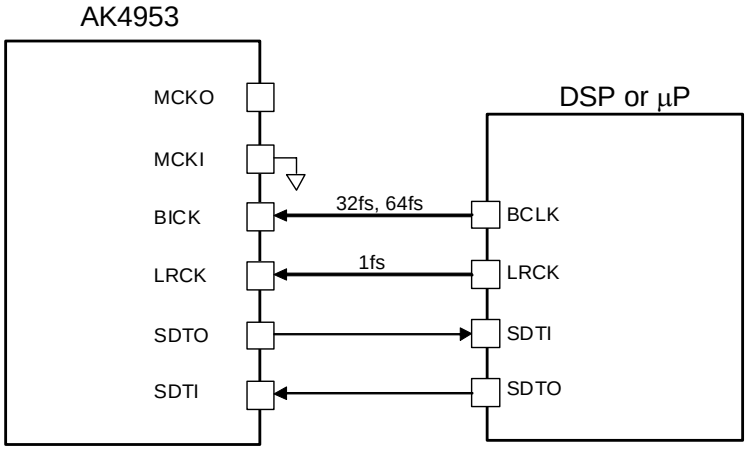
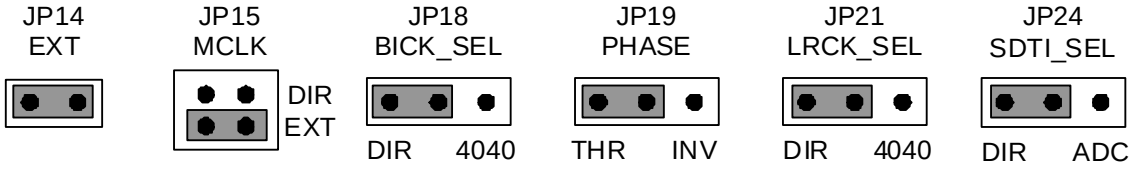


Figure 4. PLL Slave Mode 2(PLL Reference Clock: BICK pin)

① Evaluation using DIR (Optical Link) of AK4118A

PORT1 (DIR) is used.

The jumper pins should be set as follows.

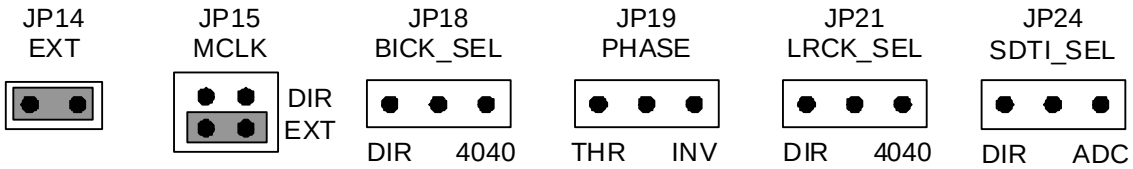


*The AK4118A supports fs up to 32kHz, and BICK outputs 64fs clock. In case of other clocks, use other evaluation modes.

② Evaluation connecting with external DSP

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR).
SDTI, BICK, LRCK of PORT3 should be connected to SDTO, BICK, LRCK for DSP.

The jumper pins should be set as follows.



*When a termination (51Ω) is not used, JP14 (EXT) should be open.

(3-3) Setting with External Slave Mode

MCLK, BICK, LRCK, and SDTI are input from PORT3 (DSP).
JP23 (M/S) should be set to "Slave". In addition, Registers of the AK4953 should be set to "EXT Slave Mode".

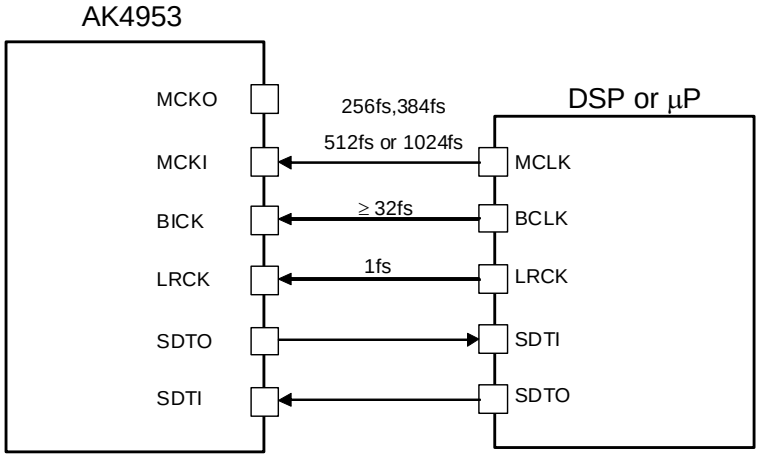
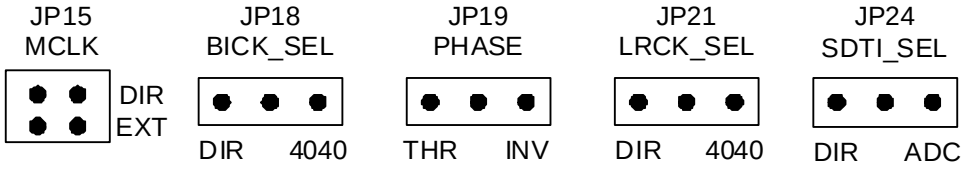


Figure 5. EXT Slave Mode

The jumper pins should be set as follows.



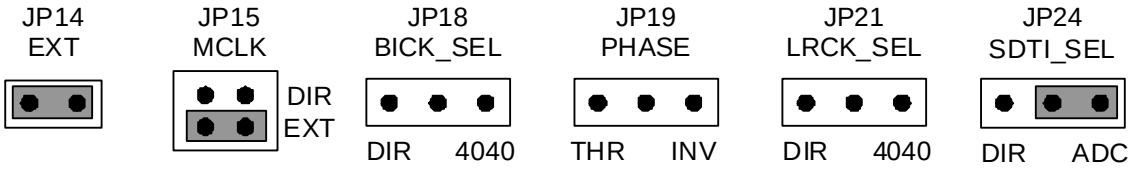
(4) Evaluation of Loop-back.

(4-1) Setting with PLL Master Mode

Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
JP23 (M/S) should be set to "Master". In addition, Registers of the AK4953 should be set to "PLL Master Mode".

(4-1-1) In case of supplying MCLK from J11 (EXT)

The jumper pins should be set as follows.



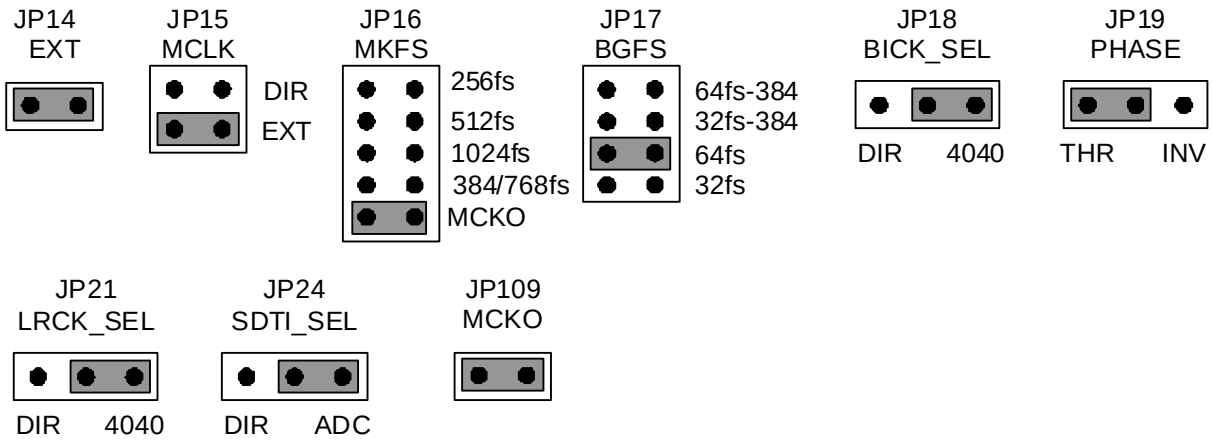
* When a termination (51Ω) is not used, JP14 (EXT) should be open.

(4-2) Setting with PLL Slave Mode

BICK and LRCK are generated on the AKD4953-A by dividing MCKO from the AK4953. The generated BICK and LRCK is input to the AK4953.
JP23 (M/S) should be set to "Slave". In addition, Registers of the AK4953 should be set to "PLL Master Mode" (Reference Clock: MCKI).
Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).

(4-2-1) In case of supplying MCLK from J11 (EXT)

The jumper pins should be set as follows.



*When a termination (51Ω) is not used, JP14 (EXT) should be open.

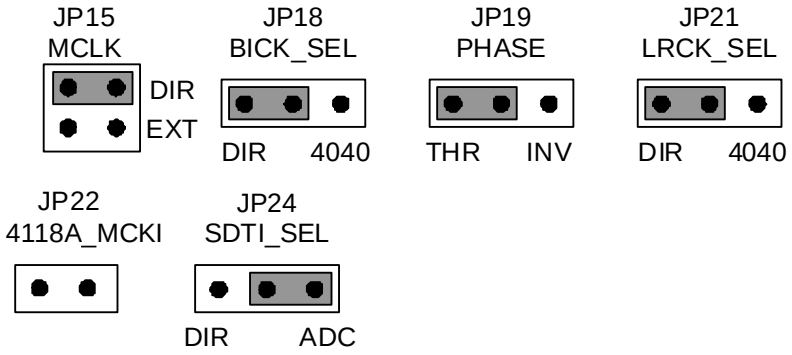
(4-3) Setting with External Slave Mode

JP23 (M/S) should be set to "Slave". In addition, Registers of the AK4953 should be set to "EXT Slave Mode".
Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).

(4-3-1) In case of using clocks from AK4118A

X1 (12.288MHz) is used.

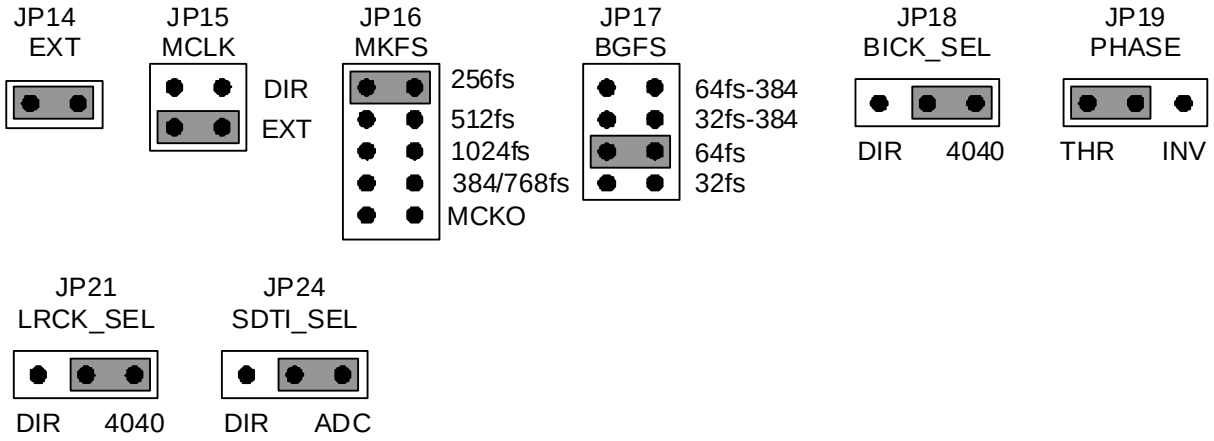
The jumper pins should be set as follows.



(4-3-2) In case of using the clock divider on the board

① In case of supplying MCLK from J11 (EXT)
(MCLK=256fs, BICK=64fs)

The jumper pins should be set as follows.



* When a termination (51Ω) is not used, JP14 (EXT) should be open.

■ DIP Switch Set Up

[S1] (SW DIP-6): Mode setting of the AK4953 and AK4118A.

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4118A Audio Format Setting See Table 4		H
2	DIF1			L
3	DIF0			L
4	OCKS1	AK4118A Master Clock Setting : See Table 5		L
5	CAD0	AK4953Control Mode Setting : See Table 6		L
6	I2C	I2C Bus	3-Wire Serial	H

Table 3. Mode Setting of the AK4953 and AK4118A

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64 -128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64 -128fs	I	

Table 4. AK4118A Audio Interface Format Setting

OCKS1	MCKO1	X'tal	
0	256fs	256fs	Default
1	512fs	512fs	

Table 5. AK4118A Master Clock Setting

■ Jumper Pins Set Up

Main Board

[JP1] (GND): Analog ground and Digital ground
OPEN: Separated.
SHORT: Common. (The connector "DGND" can be open.) <Default>

[JP16] (MKFS): MCLK Frequency
256fs: 256fs <Default>
512fs: 512fs
1024fs: 1024fs
384fs: 384fs
MCKO: MCKO of the AK4953

[JP17] (BCFS): BICK Frequency
64fs-384: 64fs (When MCLK is 384fs.)
32fs-384: 32fs (When MCLK is 384fs.)
64fs: 64fs (When MCLK is 256fs or 512fs or 1024fs.) <Default>
32fs: 32fs (When MCLK is 256fs or 512fs or 1024fs.)

[JP20] (LRCK): LRCK Frequency
fs: When MCLK is 256fs or 512fs or 1024fs. <Default>
fs-384: When MCLK is 384fs.

[JP22] (4114-MCKI): AK4118A Clock Source
OPEN: X'tal of AK4118A is used. <Default>
SHORT: MCKO of the AK4953 is supplied to the AK4118A.

Sub Board

[JP101] (CSN/CAD0): Control Mode Setting
CSN: I2Cpin= "L"
CAD0: I2Cpin= "H" <Default>

[JP108] (CDTIO/SDA): Control Mode Setting
CDTIO: I2Cpin= "L"
SDA: I2Cpin= "H" <Default>

[JP109] (MCKO): MCKO Output Circuit
OPEN: <Default>
SHORT: When dismantle MCKO

■ The function of the toggle SW

*Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Power down of AK4953. Keep "H" during normal operation.

[SW2] (DIR): Power down of AK4118A. Keep "H" during normal operation.
Keep "L" when AK4118A is not used.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4118A. LED turns on when an error has occurred to AK4118A.

■ Serial Control

The AKD4953 can be connected to the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4953. Table 6 shows switch and jumper settings for serial control. 3-WIRE Mode should be selected in Table 6.

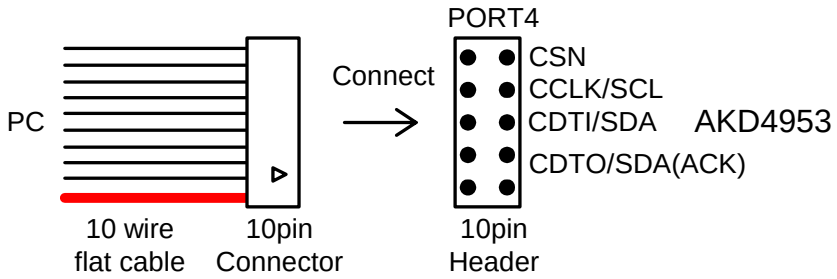


Figure 6. Connect of 10 wire flat cable

Mode		S1		JP25	
		CAD0	I2C	CTRL-SEL	
3-WIRE		L	L	3-WIRE	
I2C	CAD=0	L	H	I2C	Default
	CAD=1	H	H		

Table 6. AK4953 Control Mode Setting

■ Analog Input/Output Circuits

(1) Input Circuits

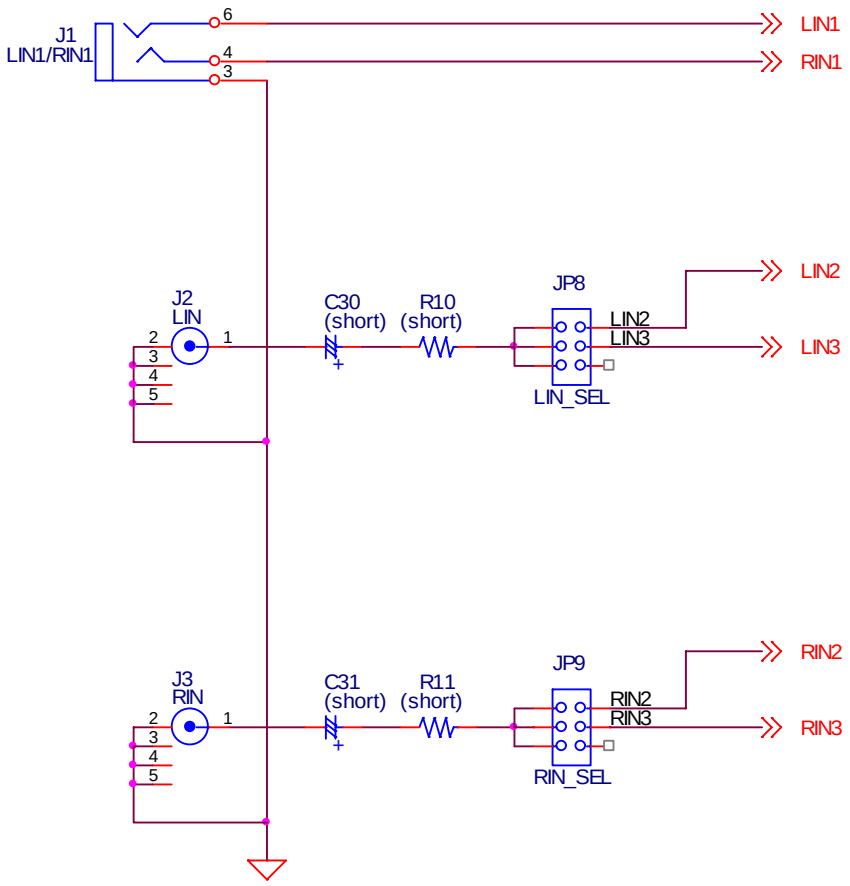
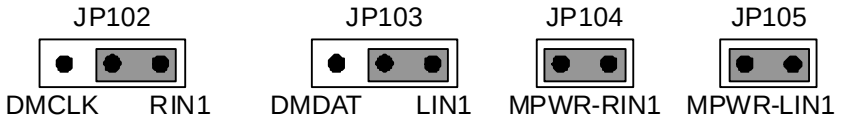


Figure 7. LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 Input Circuits

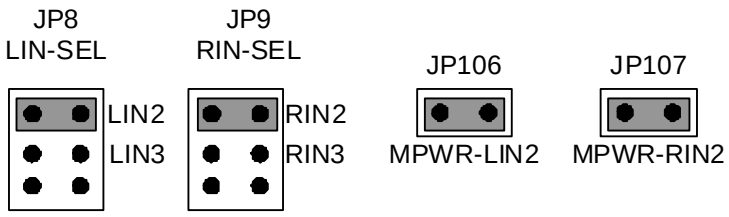
(1-1) LIN1/RIN1Input Circuit <Default>

LIN1/RIN1 is input from J1.
When the Mic Power is not used, JP104 and JP105 should be set to open.



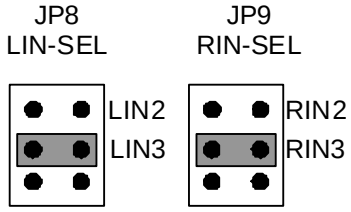
(1-2) LIN2/RIN2 Input Circuit <Default>

LIN2/RIN2 is input from J2/J3.
When the Mic Power is not used, JP106 and JP107 should be set to open.



(1-3) LIN3/RIN3 Input Circuit

LIN3/RIN3 is input from J2/J3.



(1-4) Digital Mic Input Circuit

(2) Output Circuits

(2-1) HPL/HPR Output Circuit

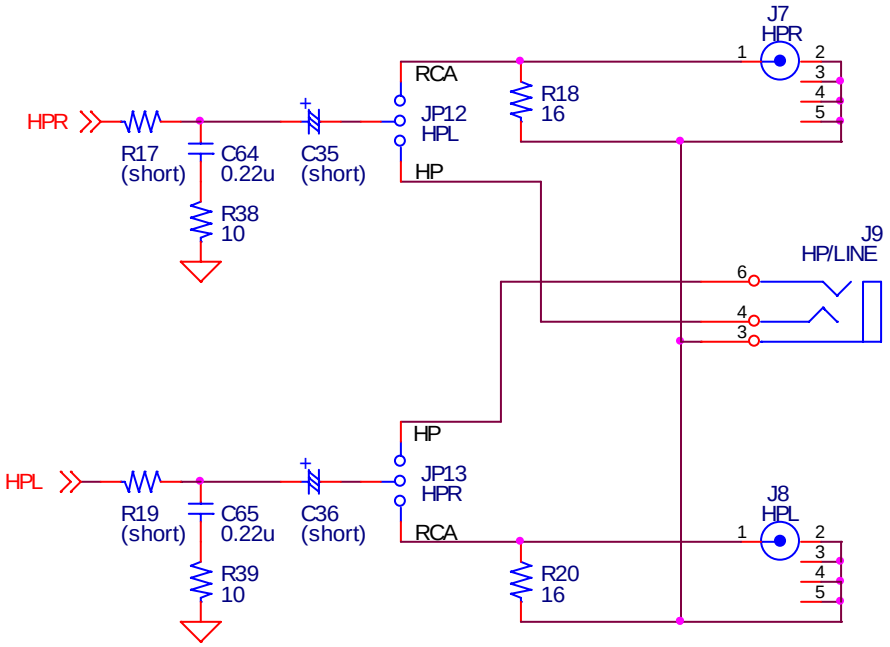
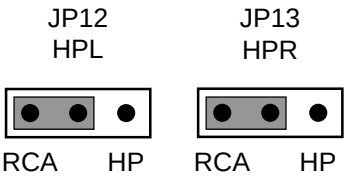
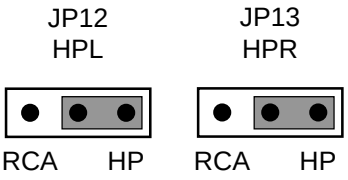


Figure 8. HPL/HPR Output Circuit

(2-1-1) In case that HPL/HPR is output from J7 and J8. <Default>



(2-2-2) In case that HPL/HPR is output from J9.



(2-3) SPP/SPN Output Circuit <Default>

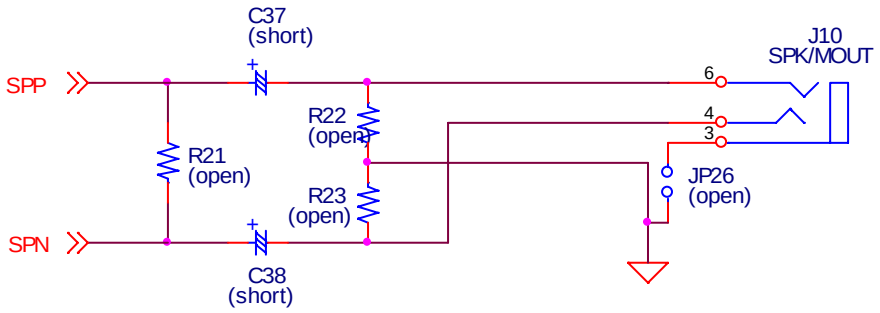


Figure 9. SPP/SPN Output Circuit

SPP/SPN is output from J10.

* AKM assumes no responsibility for the trouble when using the above circuit examples.

AK4953 Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Then please evaluate according to the following descriptions.

■ Operation Screen

1. Start up the control program following the process above.
2. After the evaluation board's power is supplied, the AK4953 must be reset once bring SW1 (toggle Switch) "L" to "H", and Click [RESET] button.
3. The operation screen is shown below.

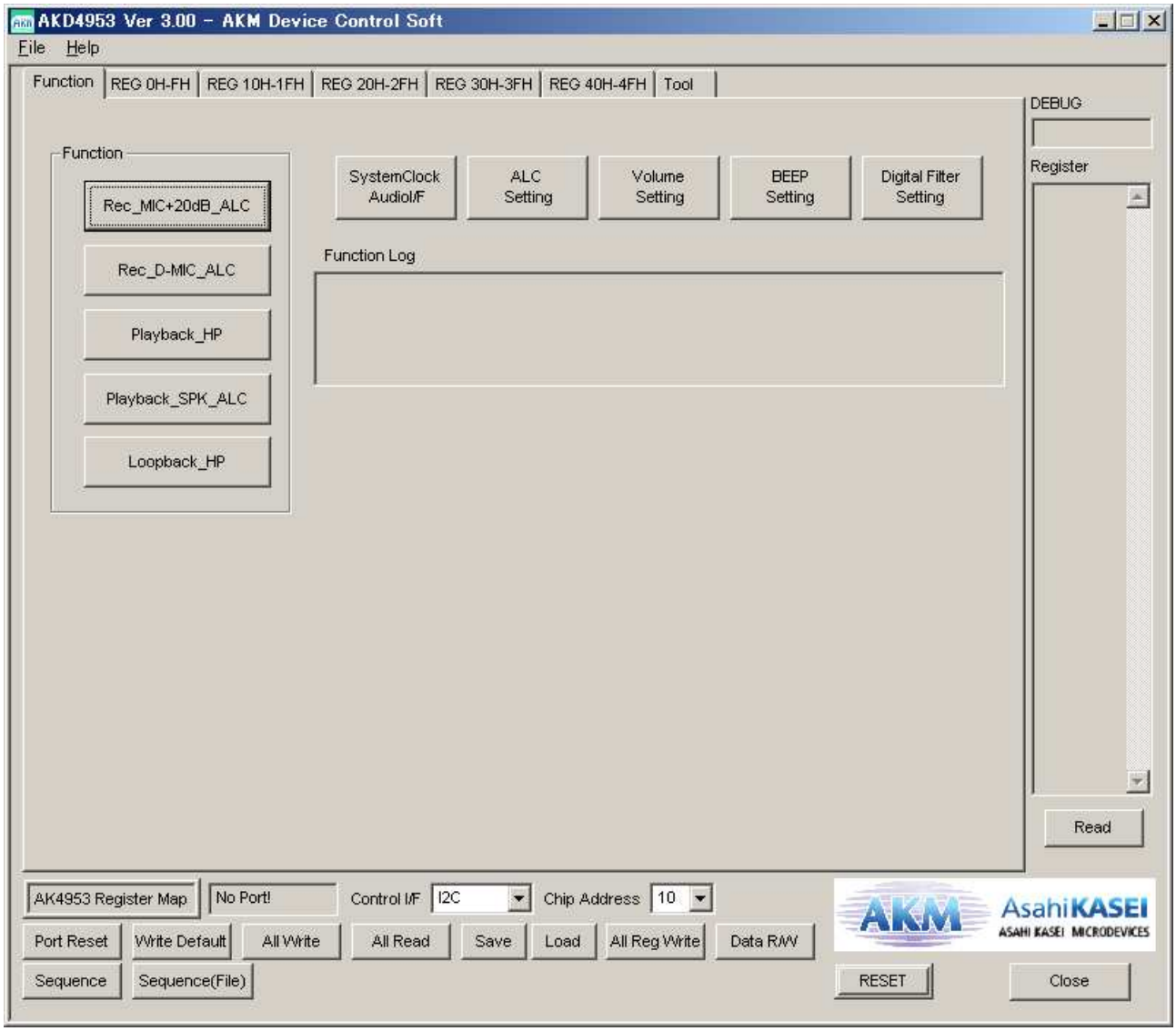


Figure 10. Window of Control Soft

■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area (on the right of the main window). This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.
12. [RESET]:Writes a reset command
    After the evaluation board power is supplied, the AK4953 must be reset once bring SW1 (toggle Switch) “L” to “H”, and then the [RESET] button should be clicked once to reset the register setting of the AK4953.

■ Tab Functions

1. [Function]: Function control

This tab is for function control.
Each operation is executed by the function buttons on the left side of the screen.

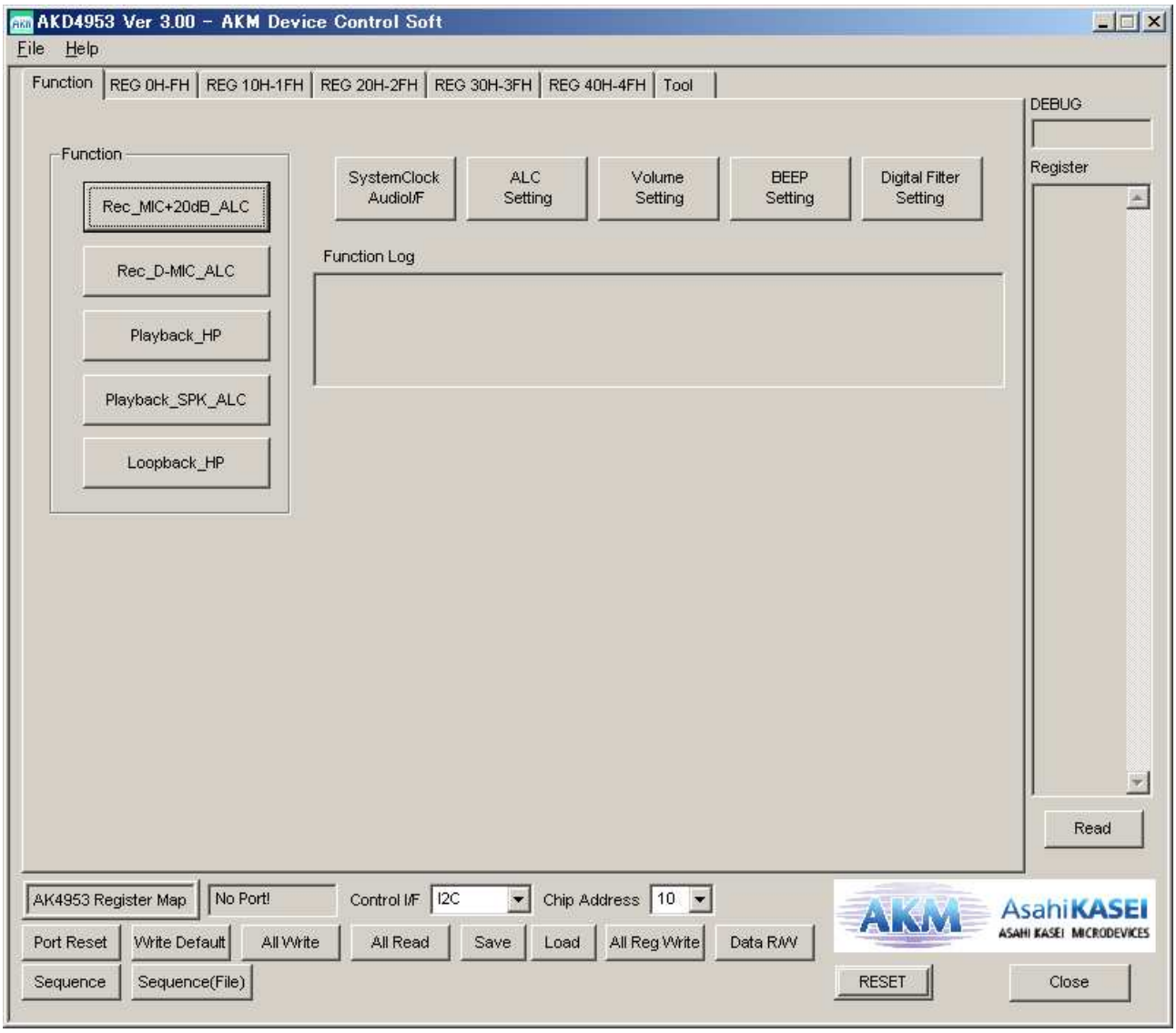


Figure 11.Window of [Function]

1-1. System Clock, Audio I/F Setting

When [System Clock Audio I/F] button is clicked, the window as shown in Figure 12 opens.
This window is for System Clock and Audio I / F Setting.
Refer to the datasheet for register settings of the AK4953.

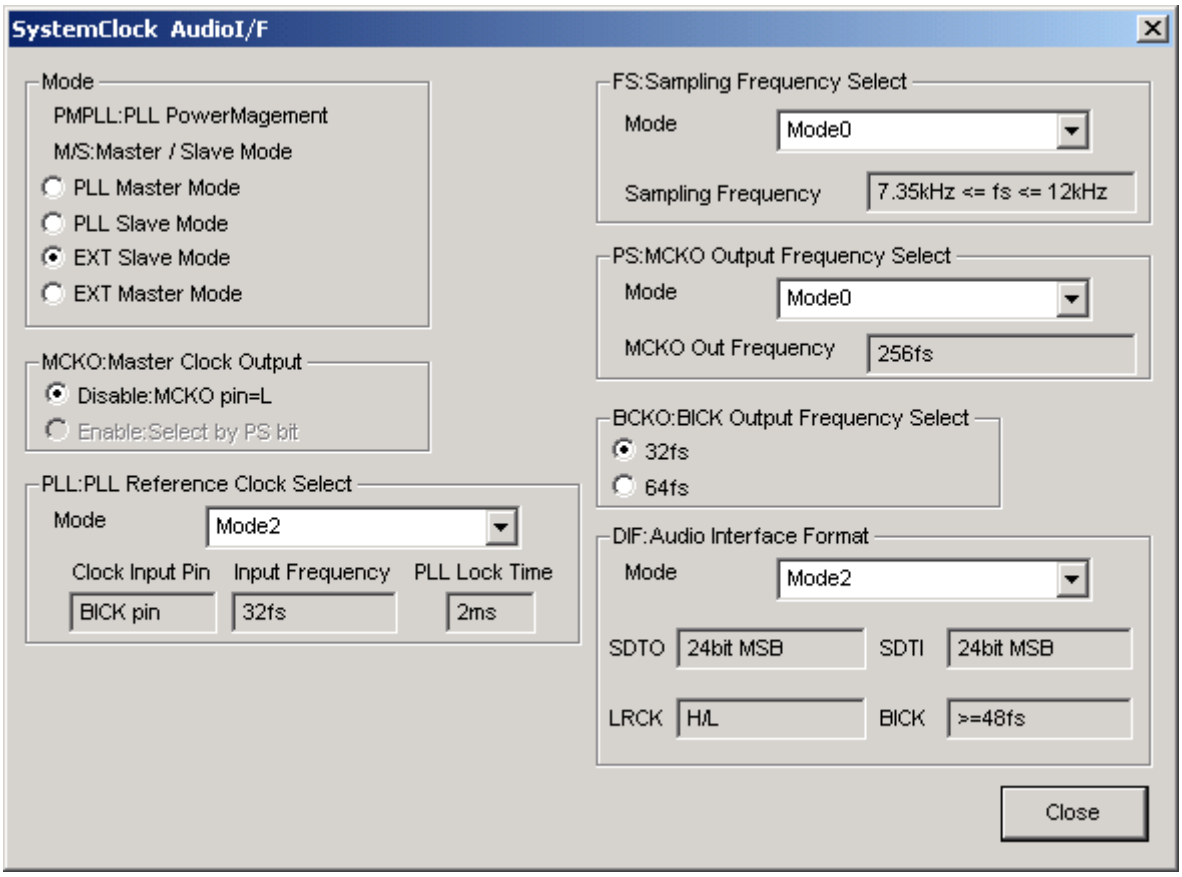


Figure 12. Window of [SystemClock AudioI/F]

1-2. ALC Setting

When [ALC Setting] button is clicked, the window as shown in Figure 13 opens.
This window is for ALC setting.
Refer to the datasheet for register settings of the AK4953.

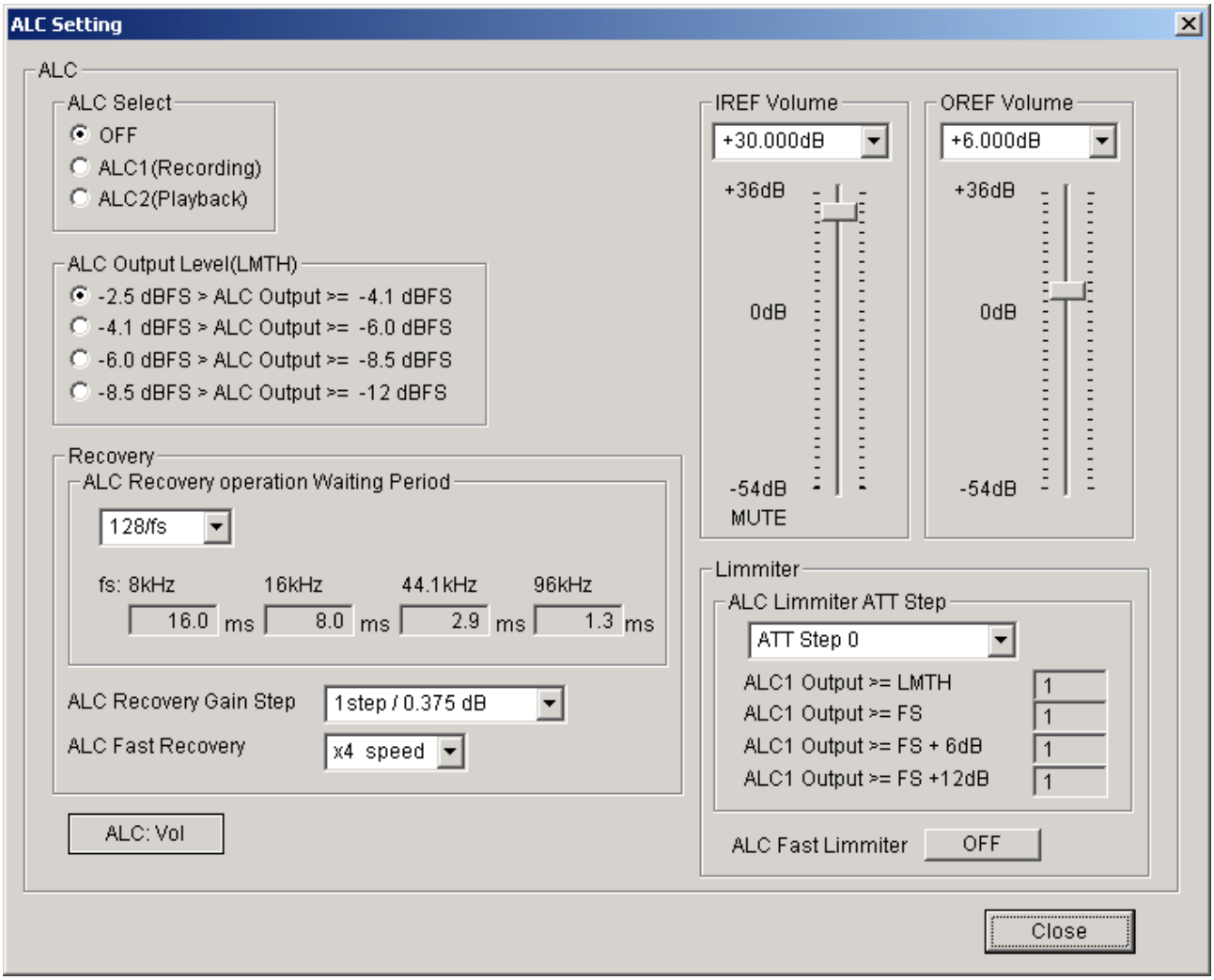
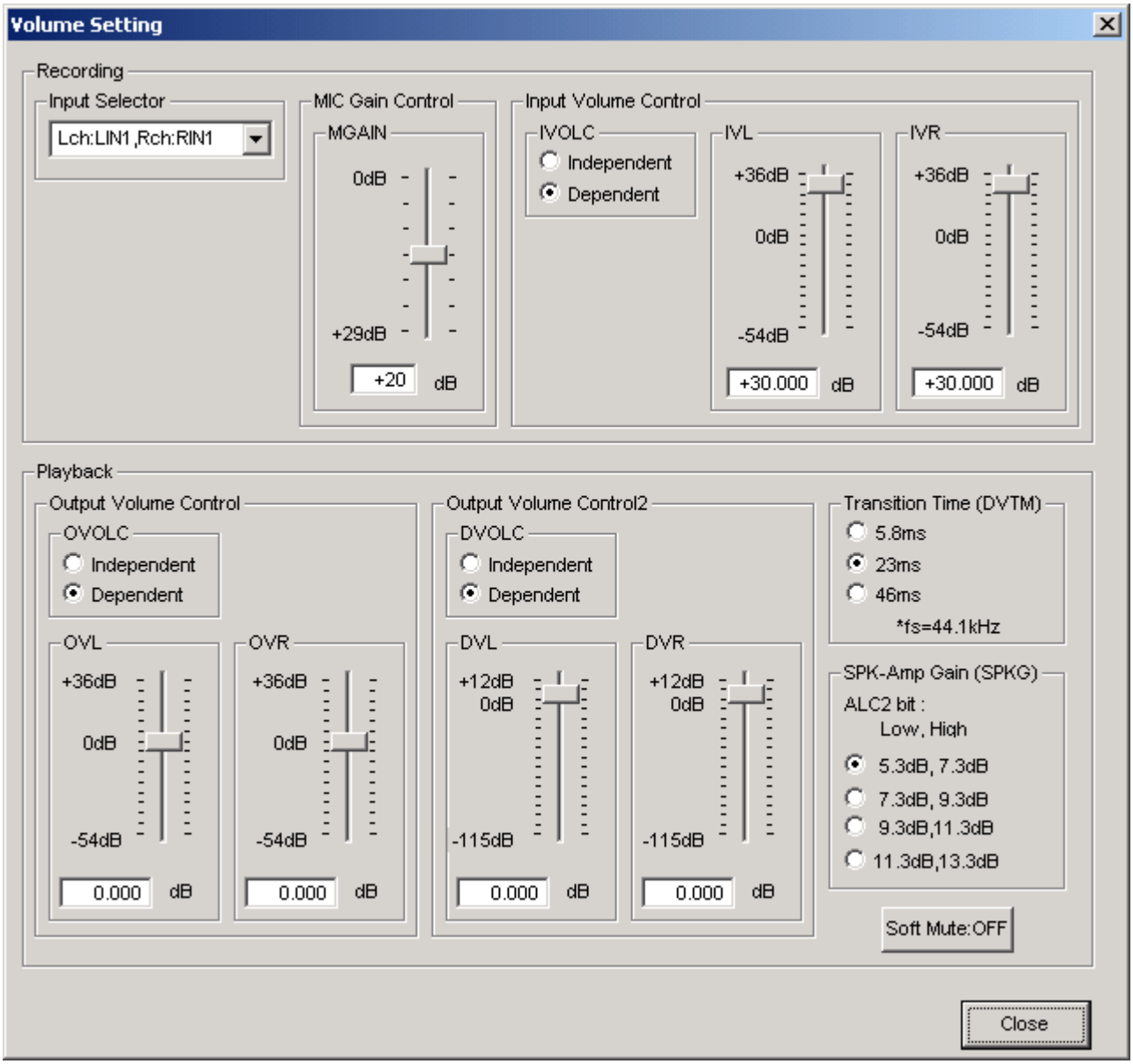


Figure 13. Window of [ALC Setting]

1-3. Volume Setting

When [Volume Setting] button is clicked, the window as shown in Figure 14 opens.
This window is for Volume setting.
Refer to the datasheet for register settings of the AK4953.



Register map

Figure 14. Window of [Volume Setting]

The volume can be controlled by slide bars.
A register writing is made on every slide bar move.

After the volume slide is moved, it is reflected on to the register map and data writing dialog box.

Volume Control by Pull-down Menu

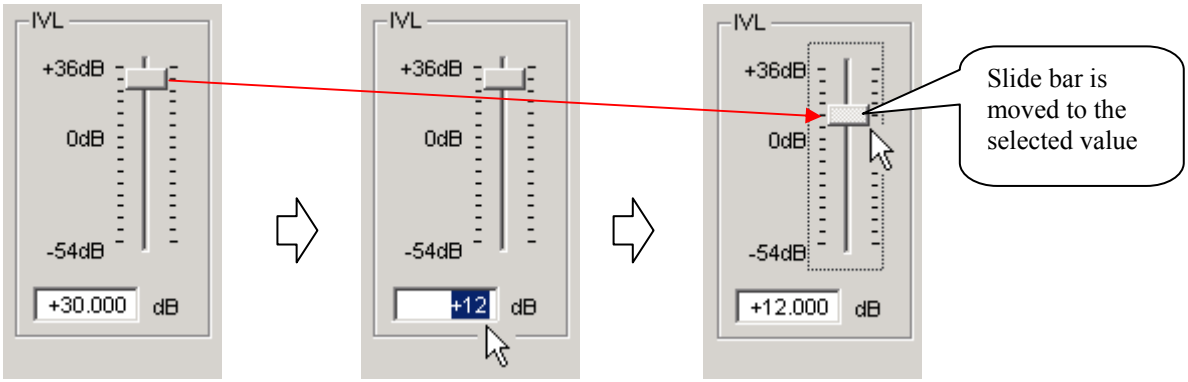


Figure 15. Window of [Volume]

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that written in the dialog box. Use the mouse or arrow keys on the keyboard for small adjustments.

1-4. Beep Setting

When [Beep Setting] button is clicked, the window as shown in Figure 16 opens.
This window is for Beep setting.
Refer to the datasheet for register settings of the AK4953.

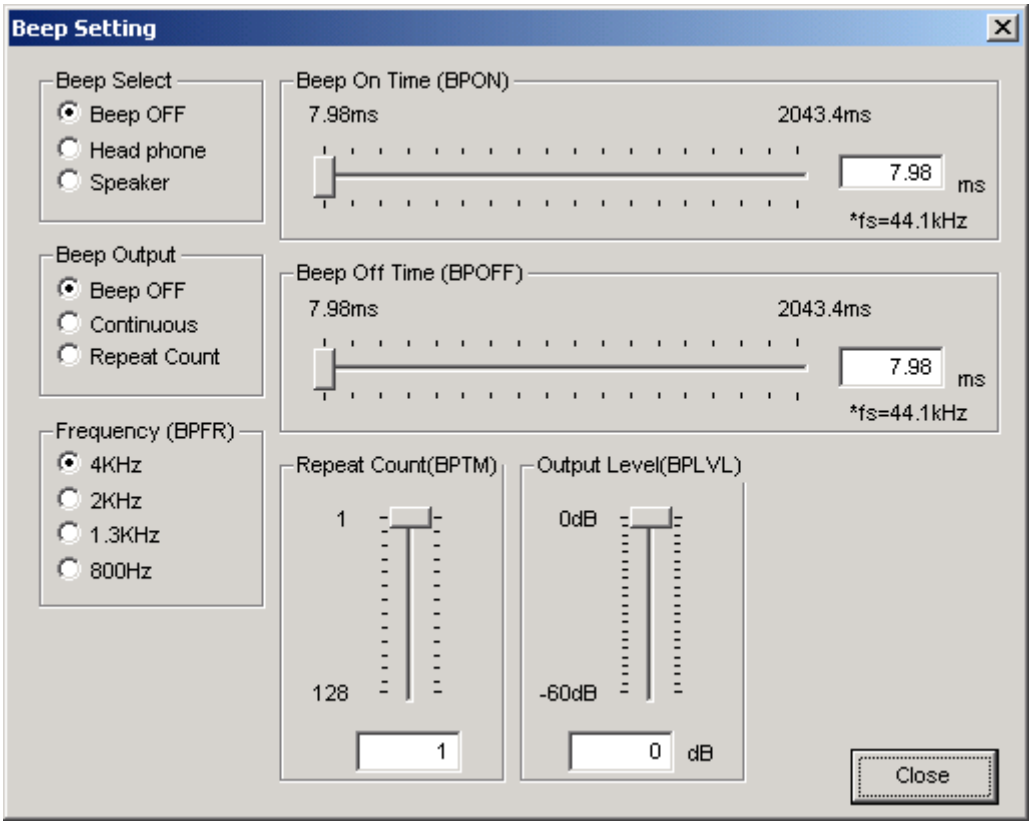


Figure 16. Window of [Beep Setting]

1-5. Digital Filter Setting

A calculation of a coefficient of Digital Programmable Filters such as HPF and EQ filters, a register writing and a frequency response checking of HPF and EQ filter can be made.
When [Digital Filter] button is clicked, the window as shown in Figure 17 opens.
Refer to the datasheet for register settings of the AK4953.

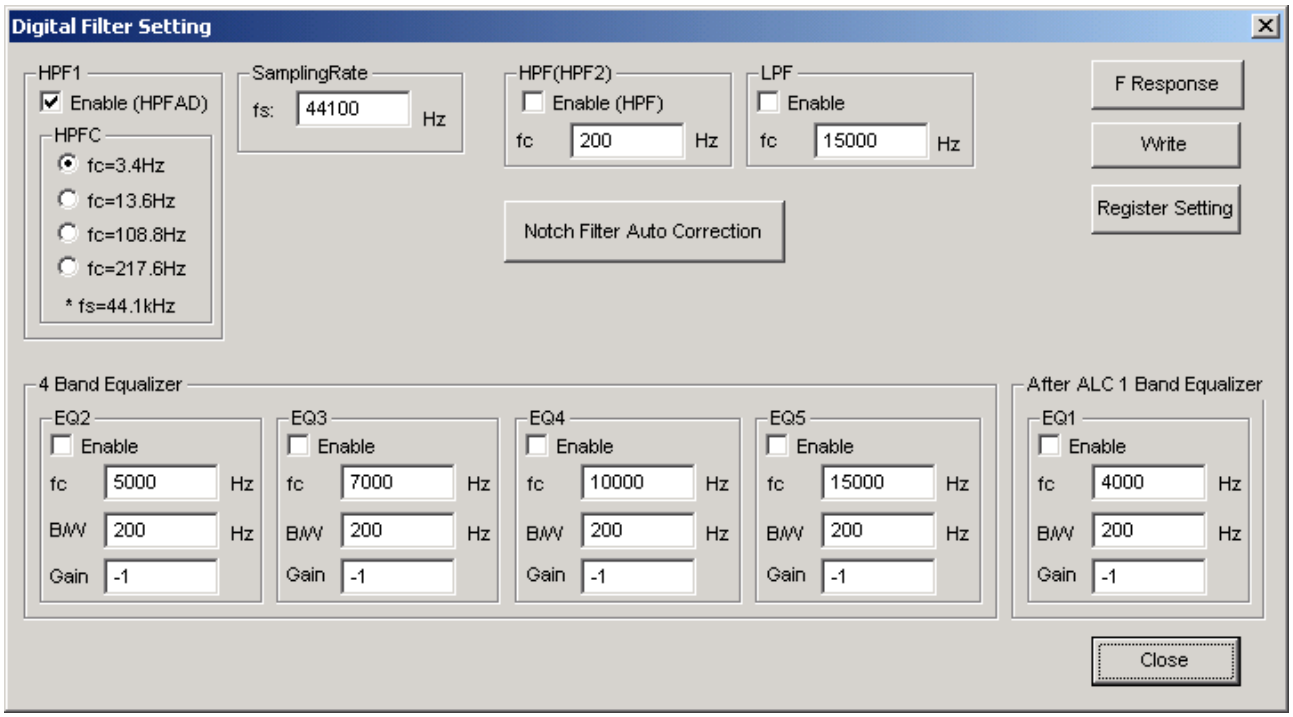


Figure 17. Window of [Digital Filter Setting]

1-5-1. parameter Setting

(1) Please set a parameter of each Filter.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
LPF		
Cut Off Frequency	Low pass filter cut off frequency	fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs)
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-5 Band Width	EQ1-5 Band Width (Note 1)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-5 Gain	EQ1-5 Gain (Note 2)	-1≤ Gain < 3

Note 1. A gain difference is a bandwidth of 3dB from center frequency.
Note 2. When a gain is smaller than 0 , EQ becomes a notch filter.

(2) “FIL3”, “EQ0”, “LPF”, “HPF”, “HPFAD”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5” Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed. (“1-5-4. automatic correction of the center frequency of a notch filter”)

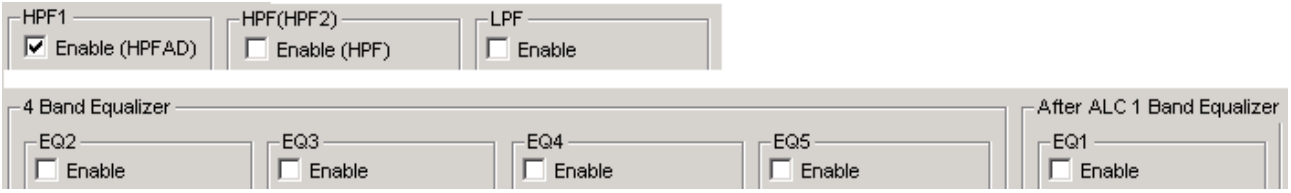


Figure 18. Filter ON/OFF setting button

1-5-2. A calculation of a register

A register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

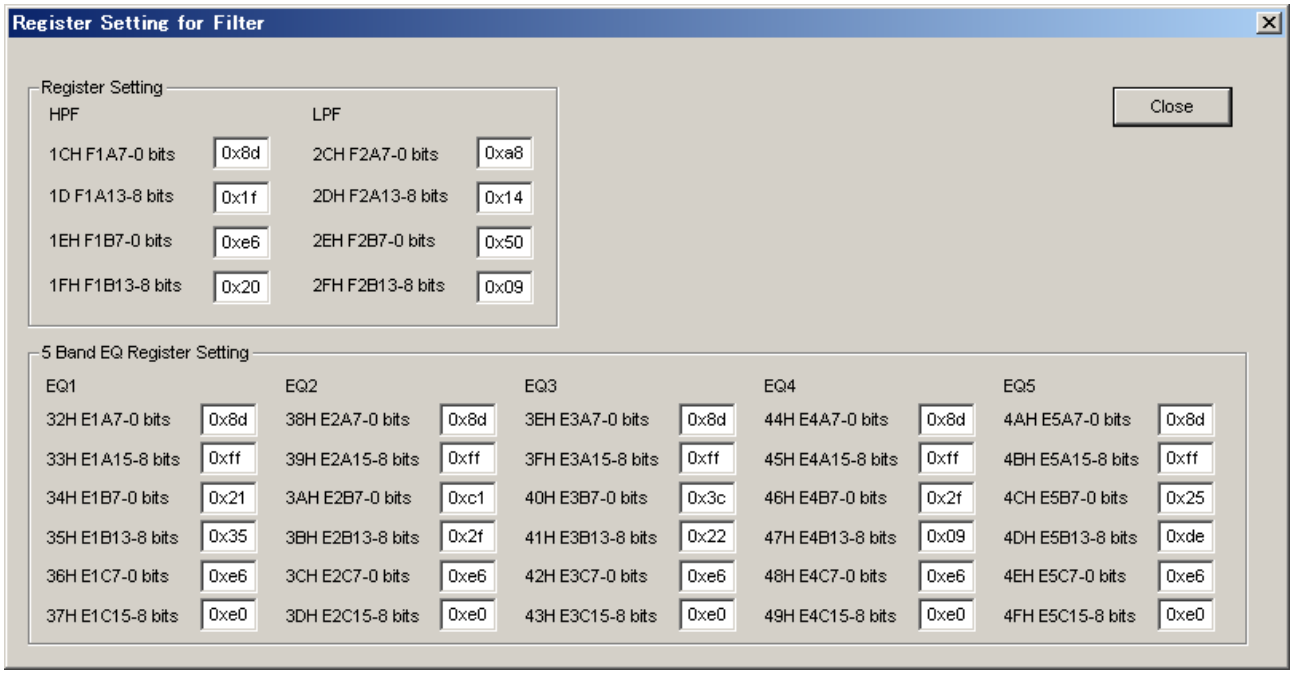


Figure 19. A register setting calculation result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

1-5-3. Indication of a frequency characteristic

A frequency characteristic is displayed when push a [Frequency Response] button. Then, a register set point is also updated.
Change "Frequency Range", and indication of a frequency characteristic is updated when push a [UpDate] button.

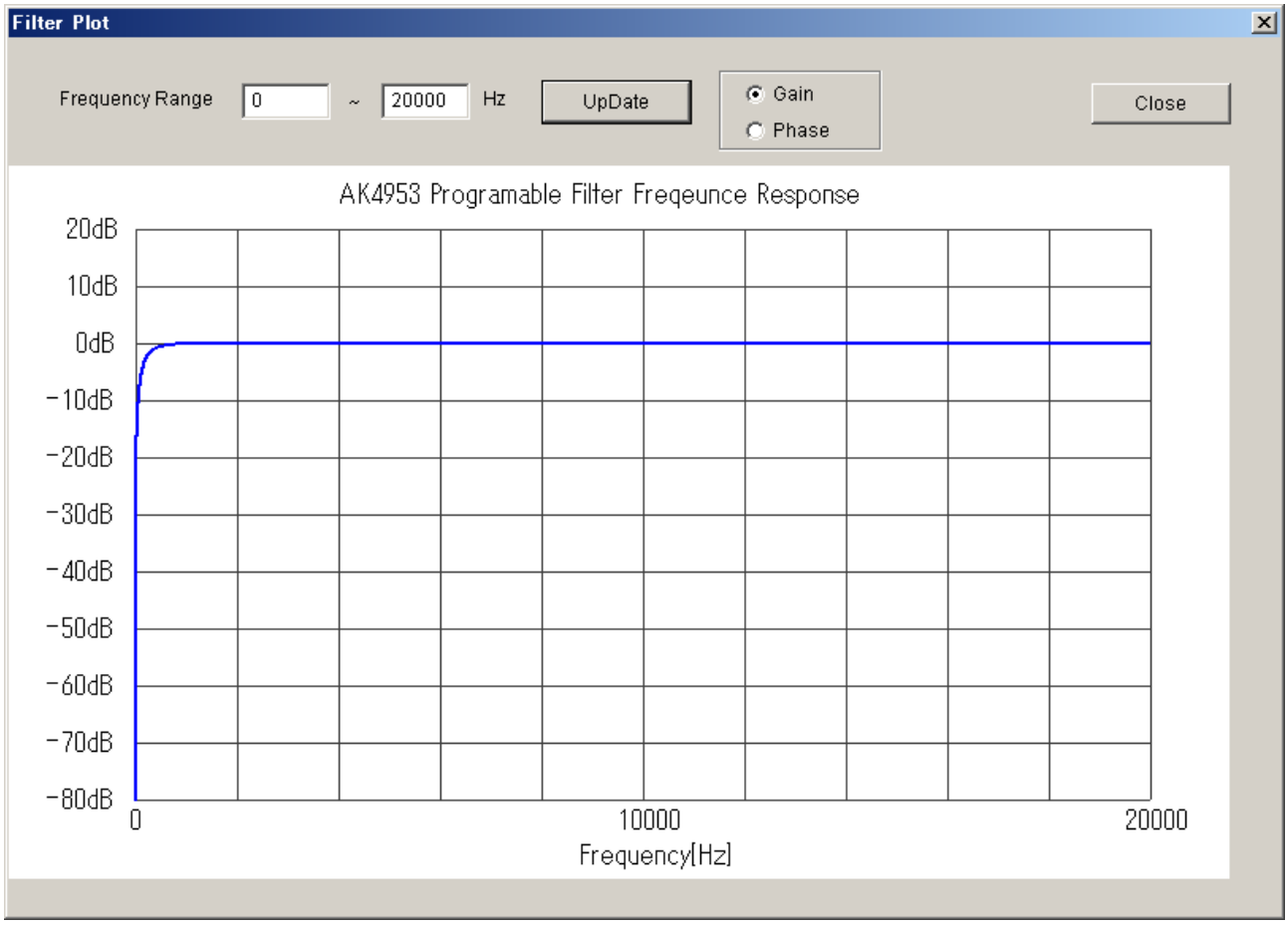


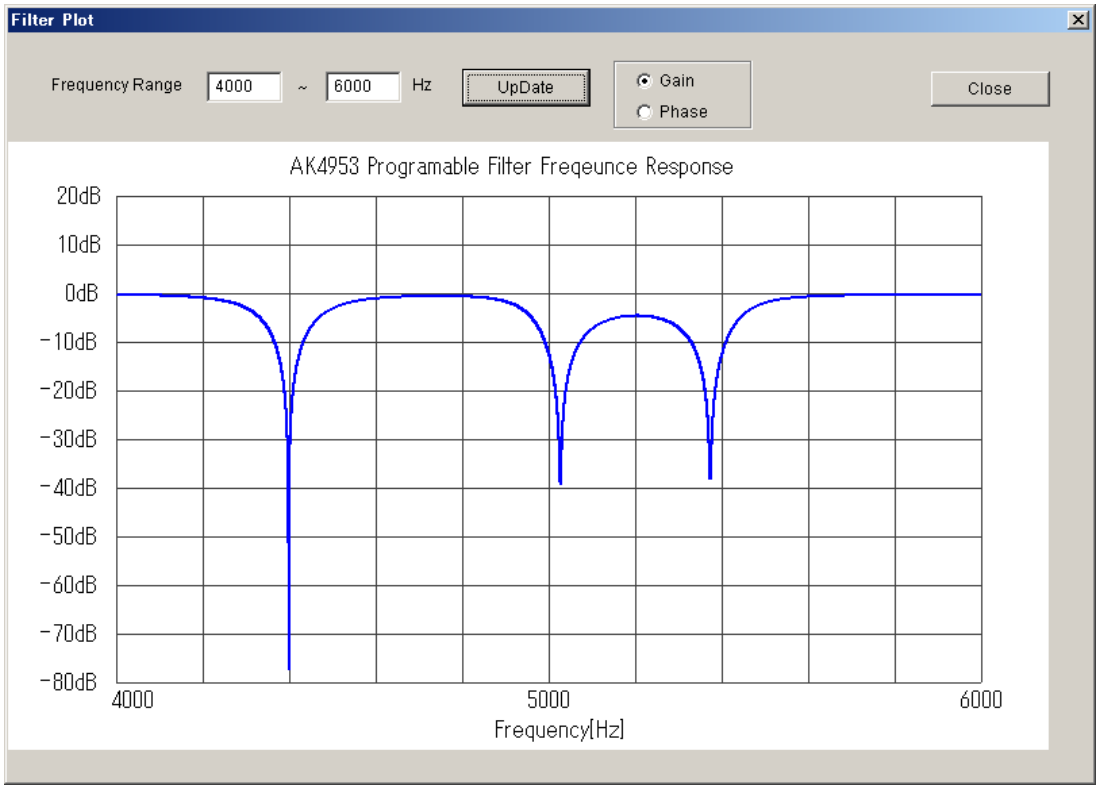
Figure 20. A frequency characteristic indication result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

1-5-4. Automatic correction of the center frequency of a notch filter

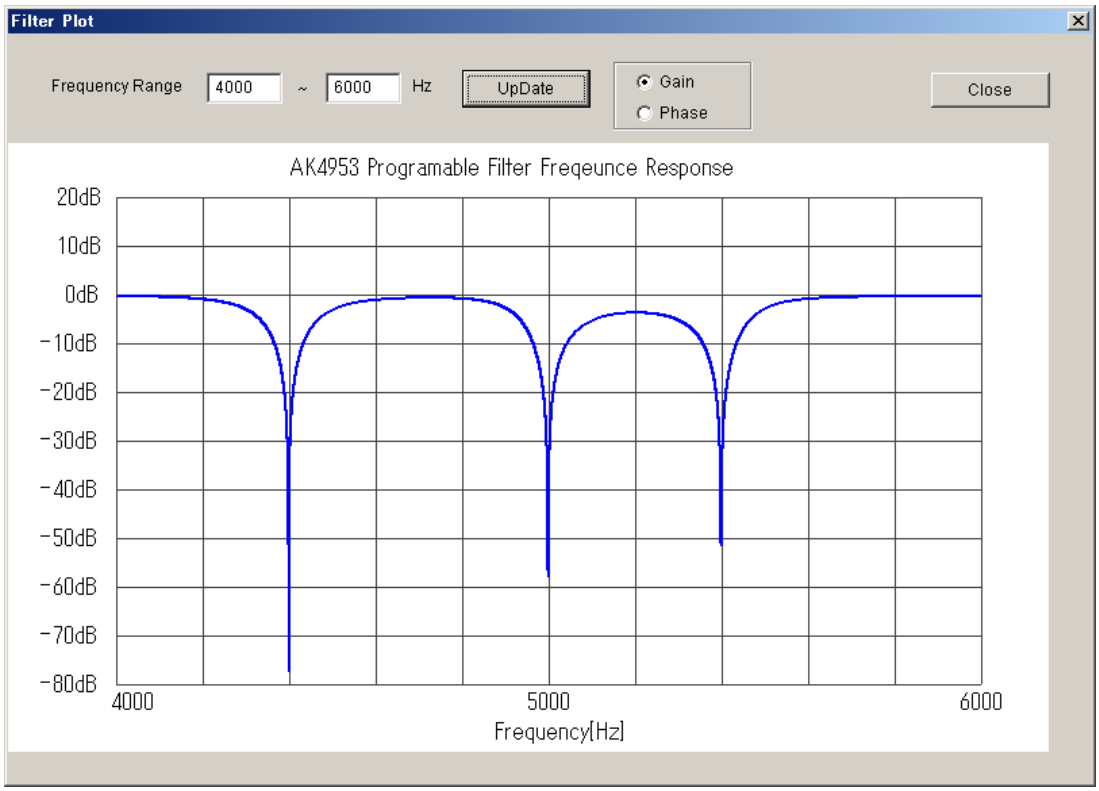
When set a gain of 5 band Equalizer to -1, Equalizer becomes a notch filter. When the center frequencies of plural notch filters are adjacent, produce a gap to central frequency (Figure 21). When check "a Notch Filter Auto Correction" button, perform automatic correction of central frequency of a notch filter, display register setting after automatic correction and a frequency characteristic (Figure 22). This automatic correction is valid for a Equalizer Band which is set its gain to "-1".

(Note) When distance among center frequency is smaller than band width, there is a possibility that automatic correction is not performed properly. Please confirm a correction result by indication of a frequency characteristic.



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width: 200Hz(3 band common)

Figure 21. When there is no center frequency revision



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width : 200Hz(3 band common)

Figure 22. When there is a center frequency revision

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

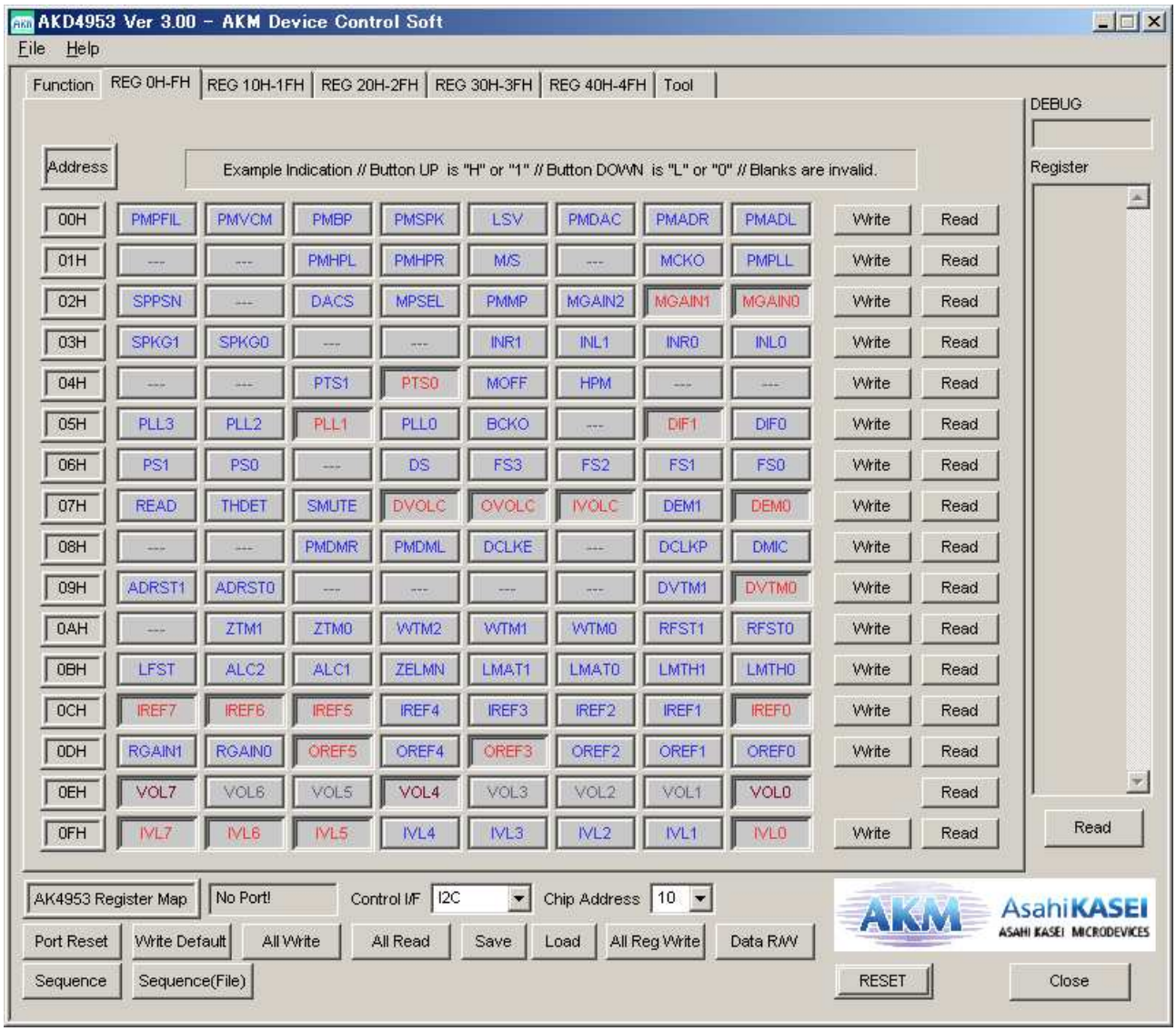


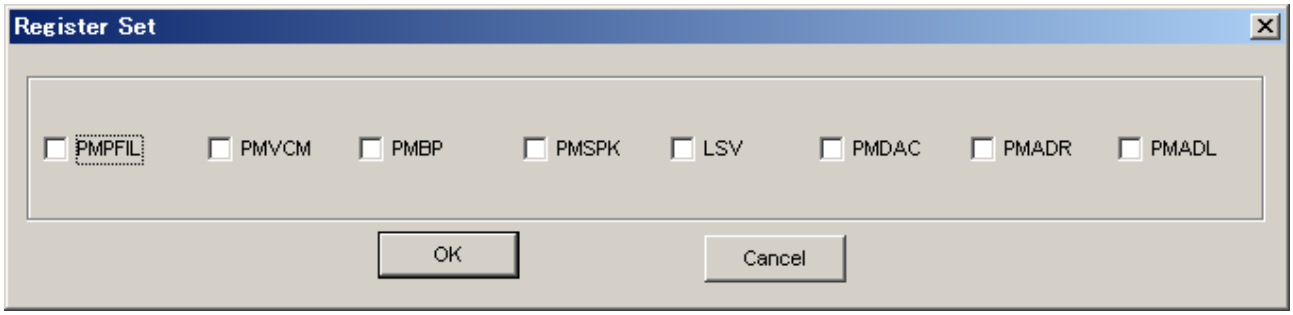
Figure 23.Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.



[Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

3. [Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

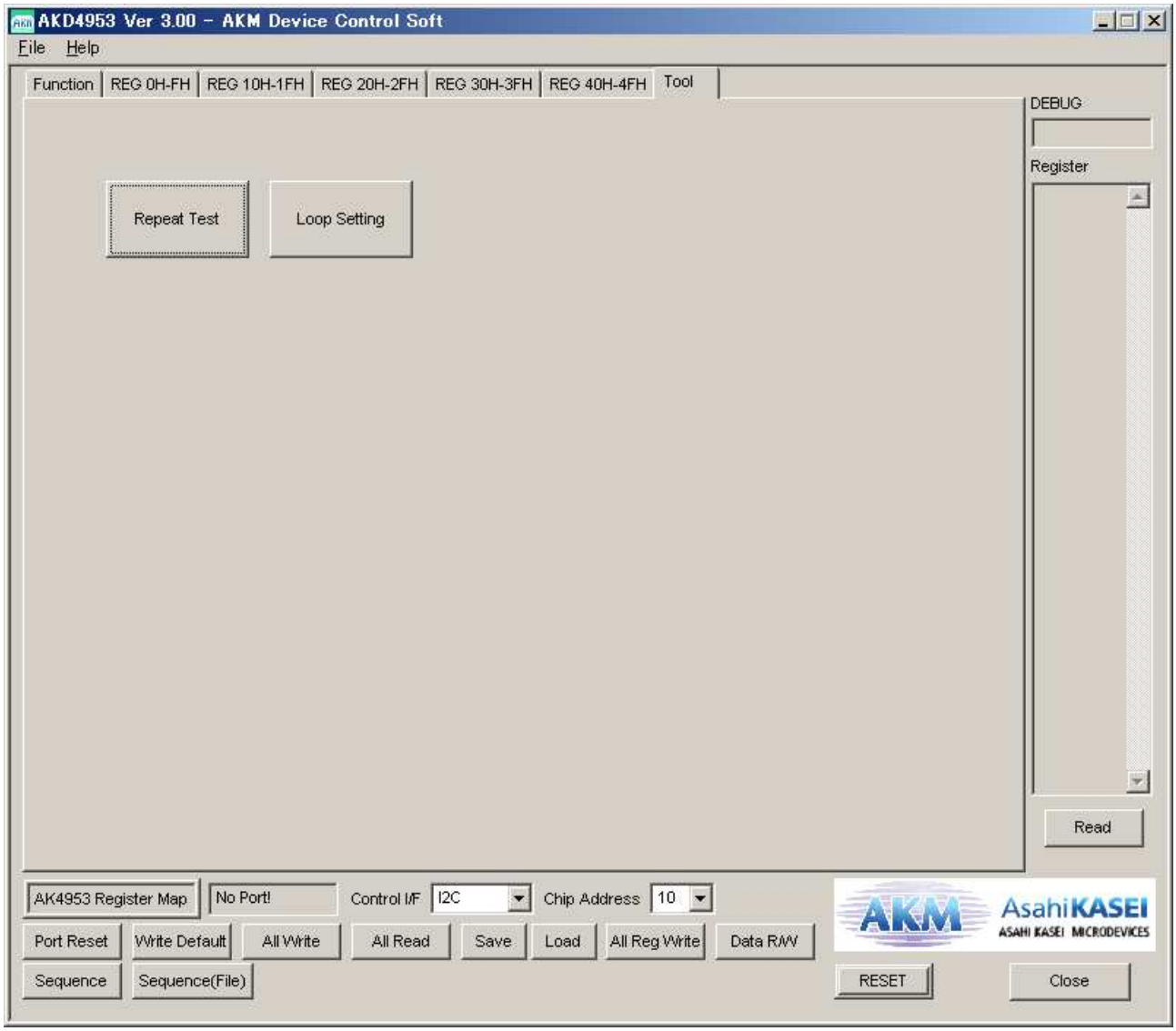


Figure 24.Window of [Tool]

■ Dialog Boxes

1. [All Req Write]: All Req Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

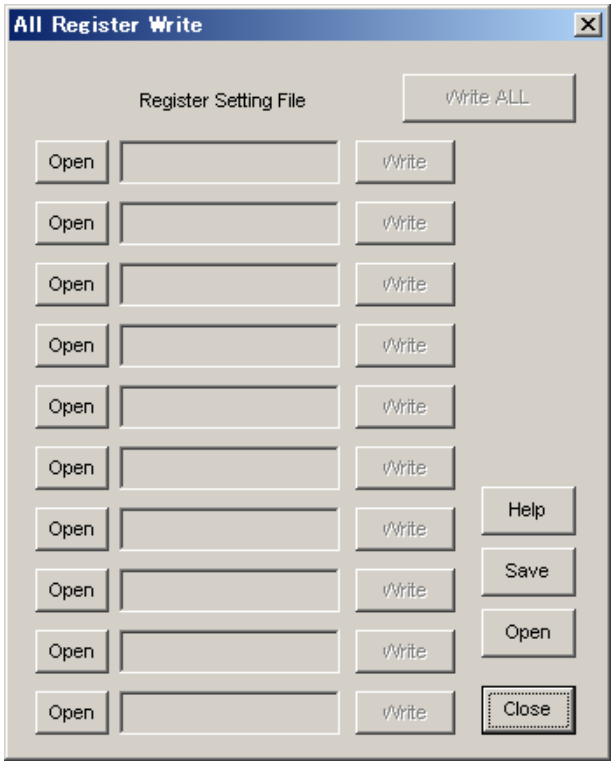


Figure 25. Window of [All Reg Write]

[Open (left)]: Selecting a register setting file (*.akr).
[Write]: Executing register writing.
[Write All]: Executing all register writings.
Writings are executed in descending order.

[Help]: Help window is popped up.
[Save]: Saving the register setting file assignment. The file name is "*.mar".
[Open (right)]: Opening a saved register setting file assignment "*. mar".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

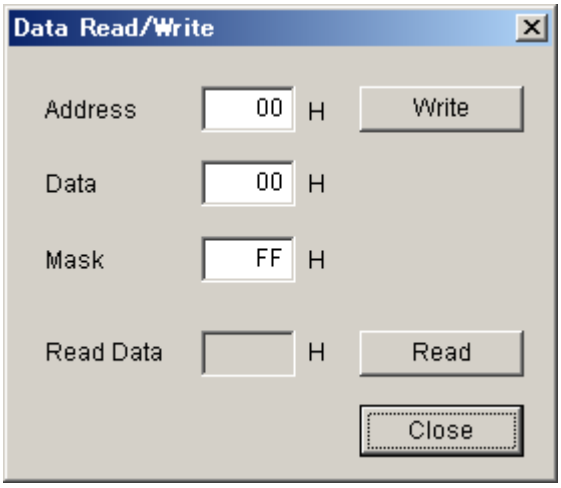


Figure 26. Window of [Data R/W]

Address Box: Input data address in hexadecimal numbers for data writing.
Data Box: Input data in hexadecimal numbers.
Mask Box: Input mask data in hexadecimal numbers.
This is "AND" processed input data.

[Write]: Writing to the address specified by "Address" box.

[Read]: Reading from the address specified by "Address" box.
The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

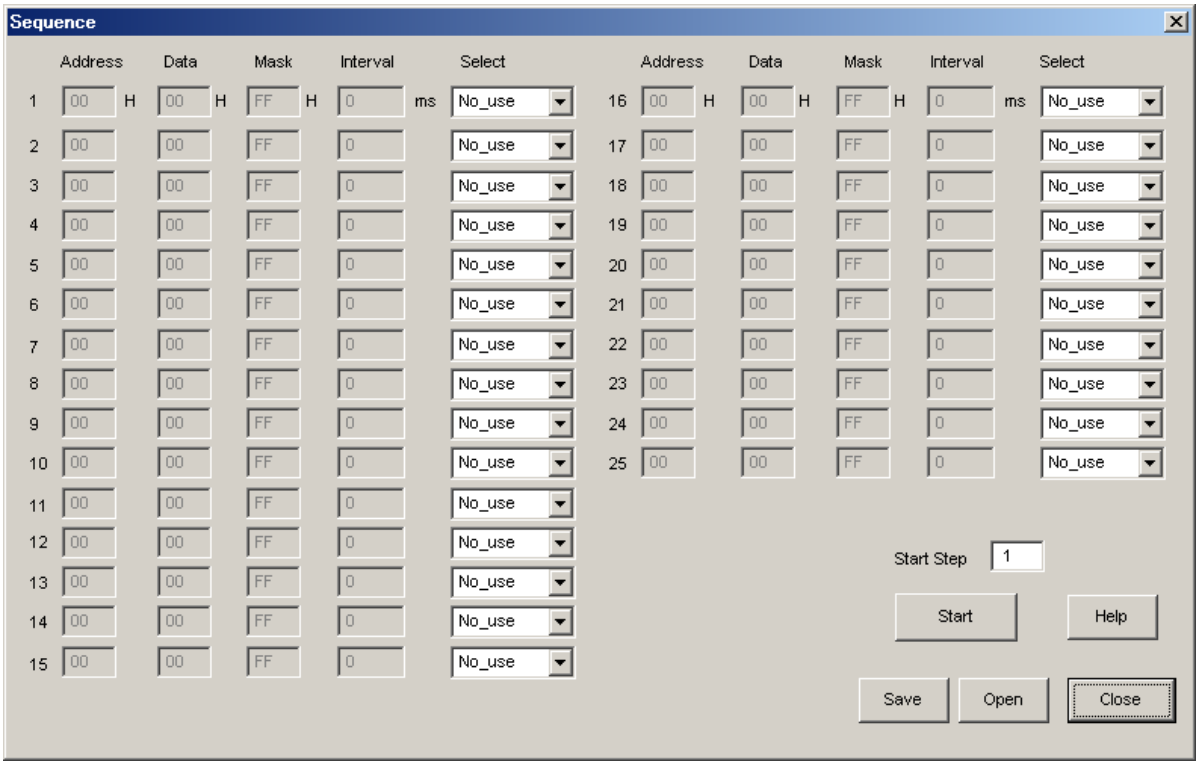


Figure 27. Window of [Sequence]

Sequence Setting

Set register sequence by following process bellow.

(1) Select a command
Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.
< Select Pull-down menu >
· No_use: Not using this address
· Register: Register writing
· Reg(Mask): Register writing (Masked)
· Interval: Taking an interval
· Stop: Pausing the sequence
· End: Finishing the sequence

(2) Input sequence
[Address]: Data address
[Data]: Writing data
[Mask]: Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval]: Interval time
Valid boxes for each process command are shown bellow.
· No_use: None
· Register: [Address], [Data], [Interval]
· Reg(Mask): [Address], [Data], [Mask], [Interval]
· Interval: [Interval]
· Stop: None
· End: None

Control Buttons

The function of Control Button is shown bellow.

[Start]: Executing the sequence

[Help]: Opening a help window
[Save]: Saving sequence settings as a file. The file name is "*.aks".
[Open]: Opening a sequence setting file "*.aks".
[Close]: Closing the dialog box and finish the process.

Stop of the sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.

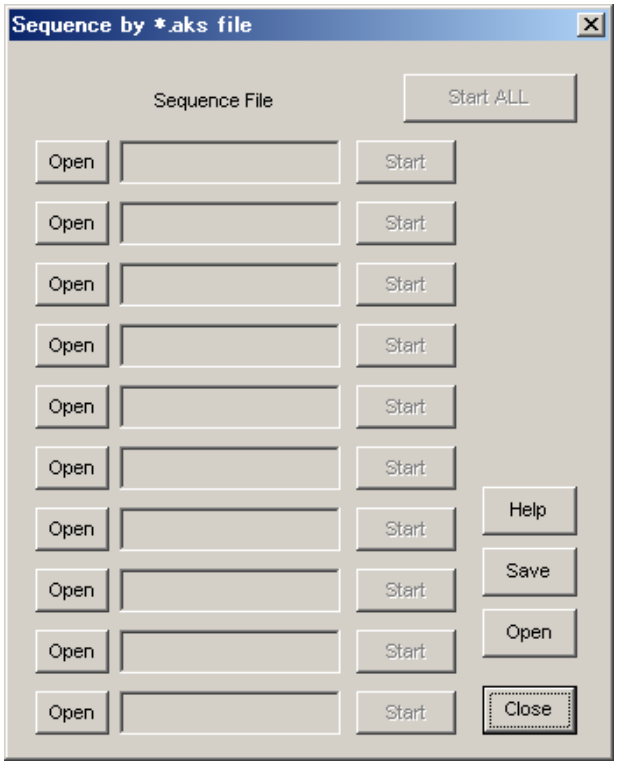


Figure 28. Window of [Sequence(File)]

[Open (left)]: Opening a sequence setting file (*.aks).
[Start]: Executing the sequence setting.
[Start All]: Executing all sequence settings.
Sequences are executed in descending order.

[Help]: Pop up the help window.
[Save]: Saving sequence setting file assignment. The file name is "*.mas".
[Open(right)]: Opening a saved sequence setting file assignment "*. mas".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
(2) When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.

Figure 29.Window of [Sequence Pause]

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCKI : 256fs (11.2896MHz,24.576MHz)
- BICK : 64fs
- fs : 44.1kHz,96kHz
- Bit : 24bit
- Measurement Mode : EXT Slave Mode
- Power Supply : SVDD=AVDD=TVDD=3.3V, DVDD=1.8V
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz
- Temperature : Room

[Measurement Results]

1. ADC

	Result		Unit
	Lch	Rch	
ADC: LIN1/RIN1 → ADC → IVOL, IVOL=0dB, ALC=OFF, MGAIN = +20dB			
fs=44.1kHz, BW=20kHz			
S/(N+D) (-1dBFS)	82.6	82.6	dB
DR (-60dBFS, A-Weighted)	88.1	88.1	dB
S/N (A-weighted)	88.1	88.1	dB
fs=96kHz, BW=40kHz			
S/(N+D) (-1dBFS)	78.4	78.3	dB
DR (-60dBFS, A-Weighted)	88.1	88.1	dB
S/N (A-weighted)	88.1	88.1	dB

2. DAC

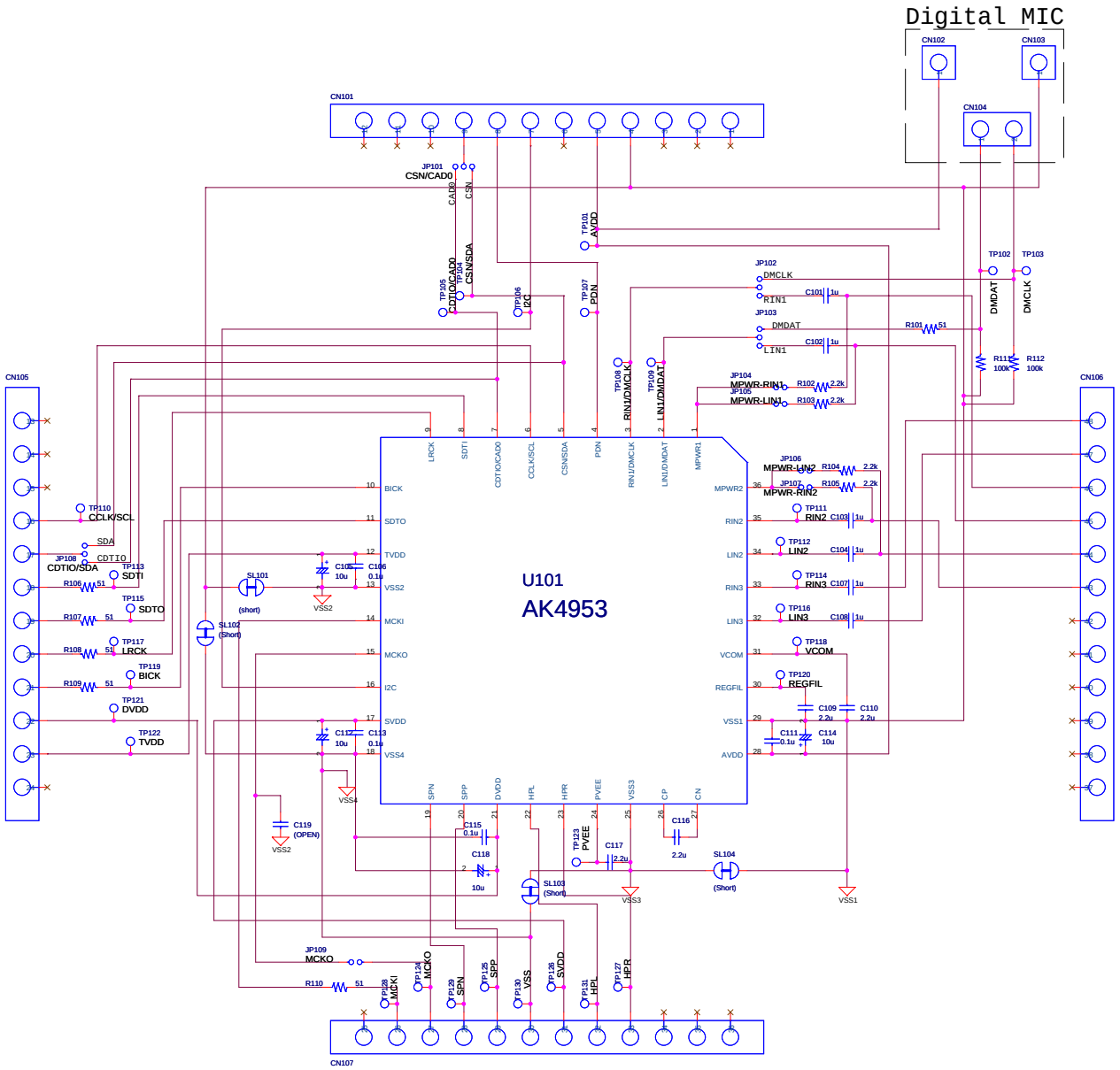
	Result		Unit
	Lch	Rch	
Headphone-Amp: DAC → HPL/HPR, ALC=OFF,OVOL=DVOL=0dB, RL=16Ω			
S/(N+D) fs=44.1kHz, BW=20kHz (-3dBFS)	80.0	80.4	dB
S/(N+D) fs=96kHz, BW=40kHz (-3dBFS)	78.9	77.6	dB
S/N (A-weighted)	96.5	96.5	dB
Speaker-Amp: DAC → SPP/SPN, IVOL=DVOL=0dB, R_L=8Ω			
fs=44.1kHz, BW=20kHz			
S/(N+D) (-0.5dBFS)	70.2		dB
S/N (A-Weighted)	97.9		dB

REVISION HISTORY

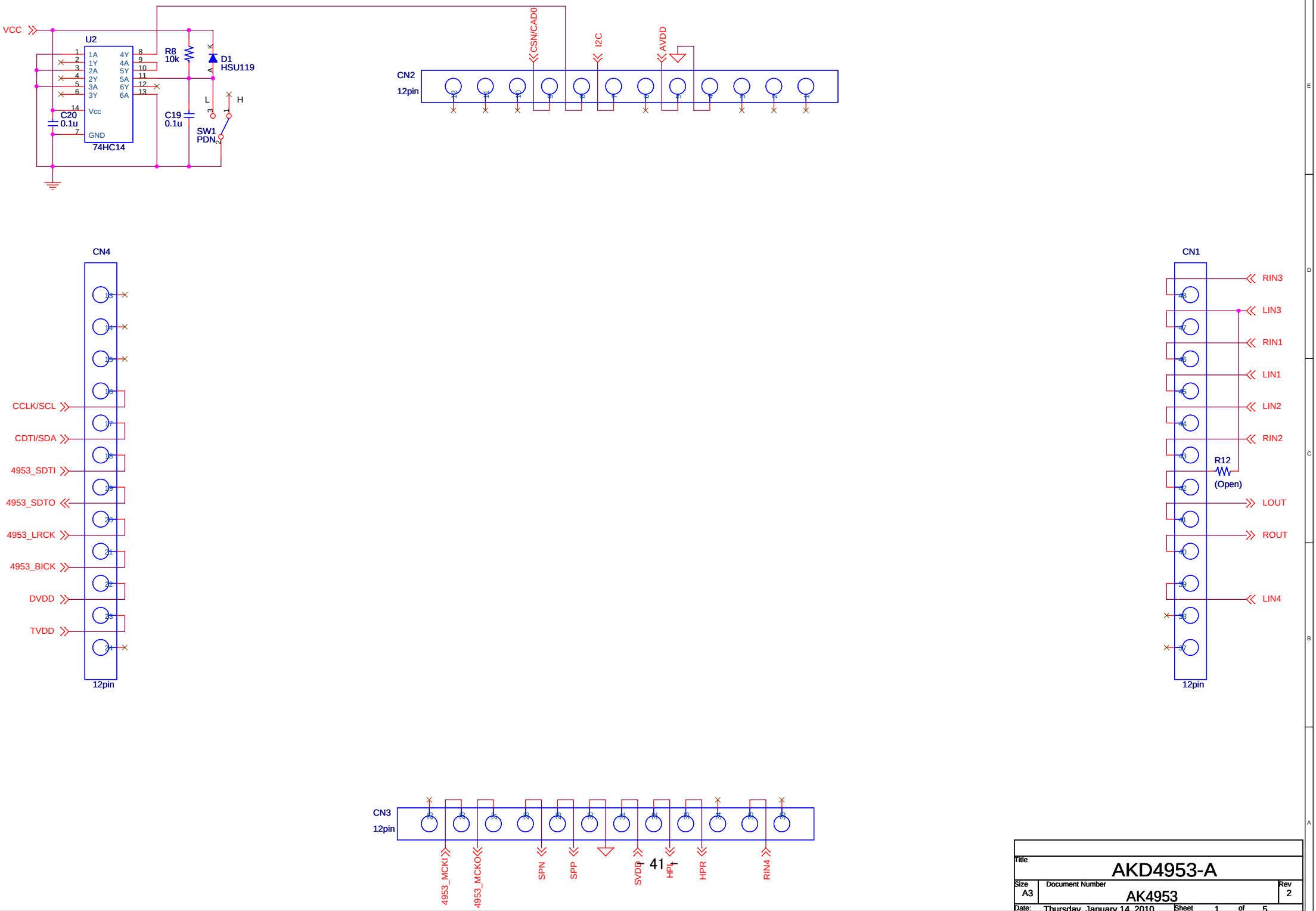
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
10/04/26	KM101802	2	First edition	

IMPORTANT NOTICE

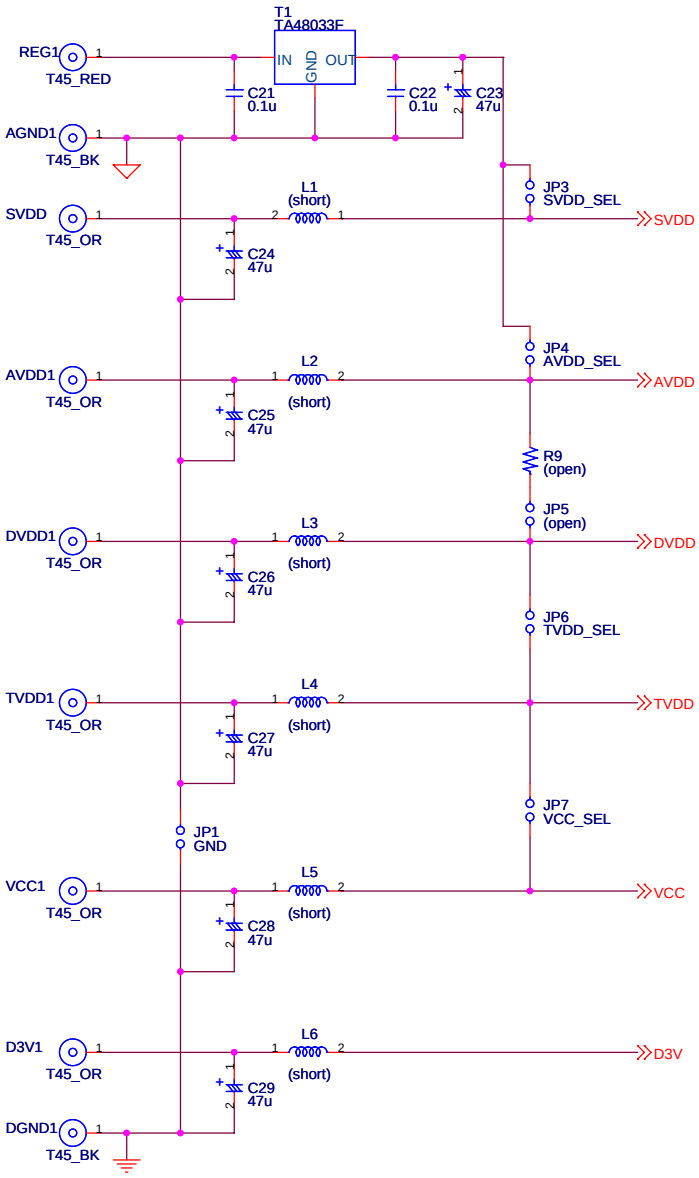
- These products and their specifications are subject to change without notice.
- When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.

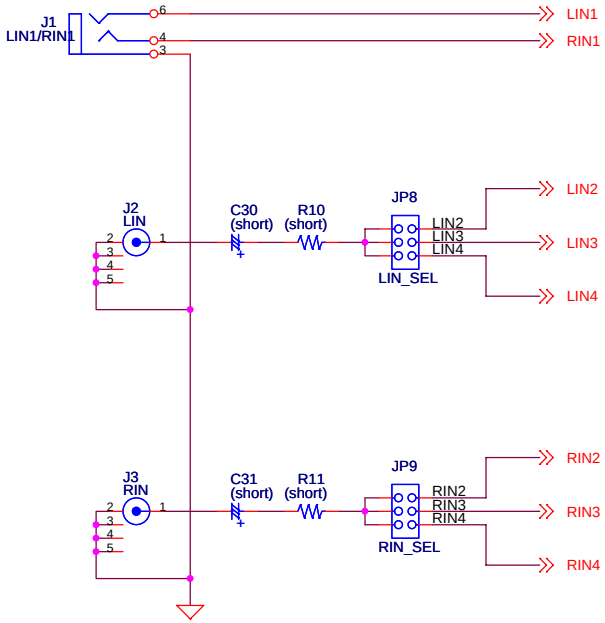


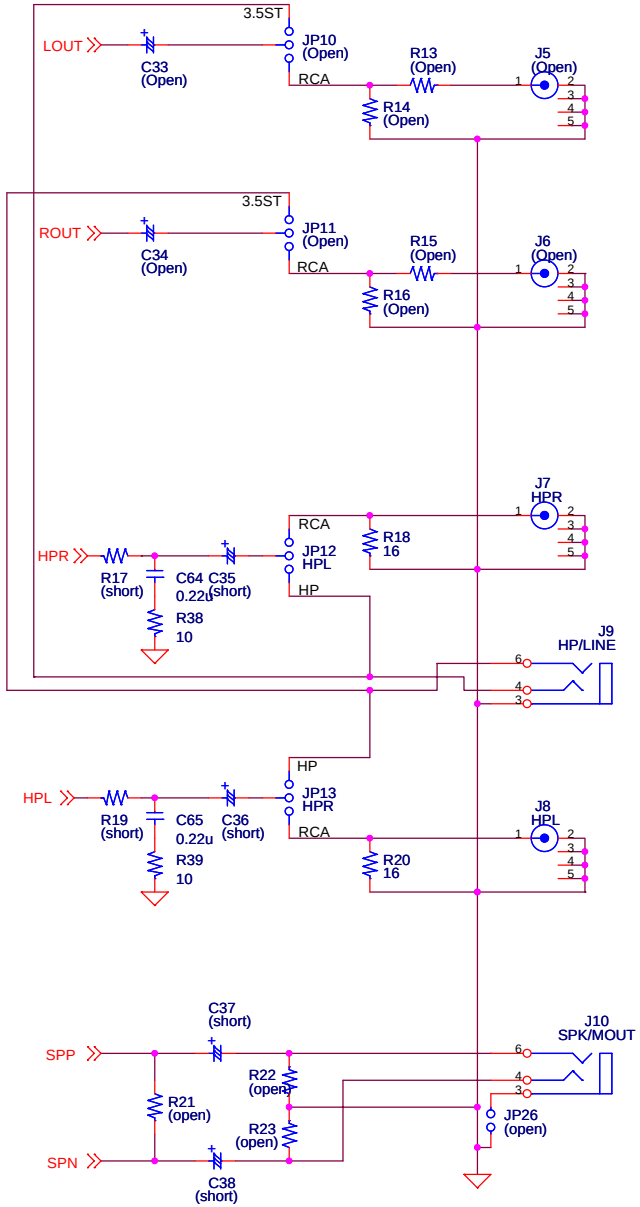
Title	AKD4953-A-36QFN-SUB	
Size A2	Document Number AK4953	Rev 0
Date: Tuesday, April 20, 2010	Sheet 1 of 1	



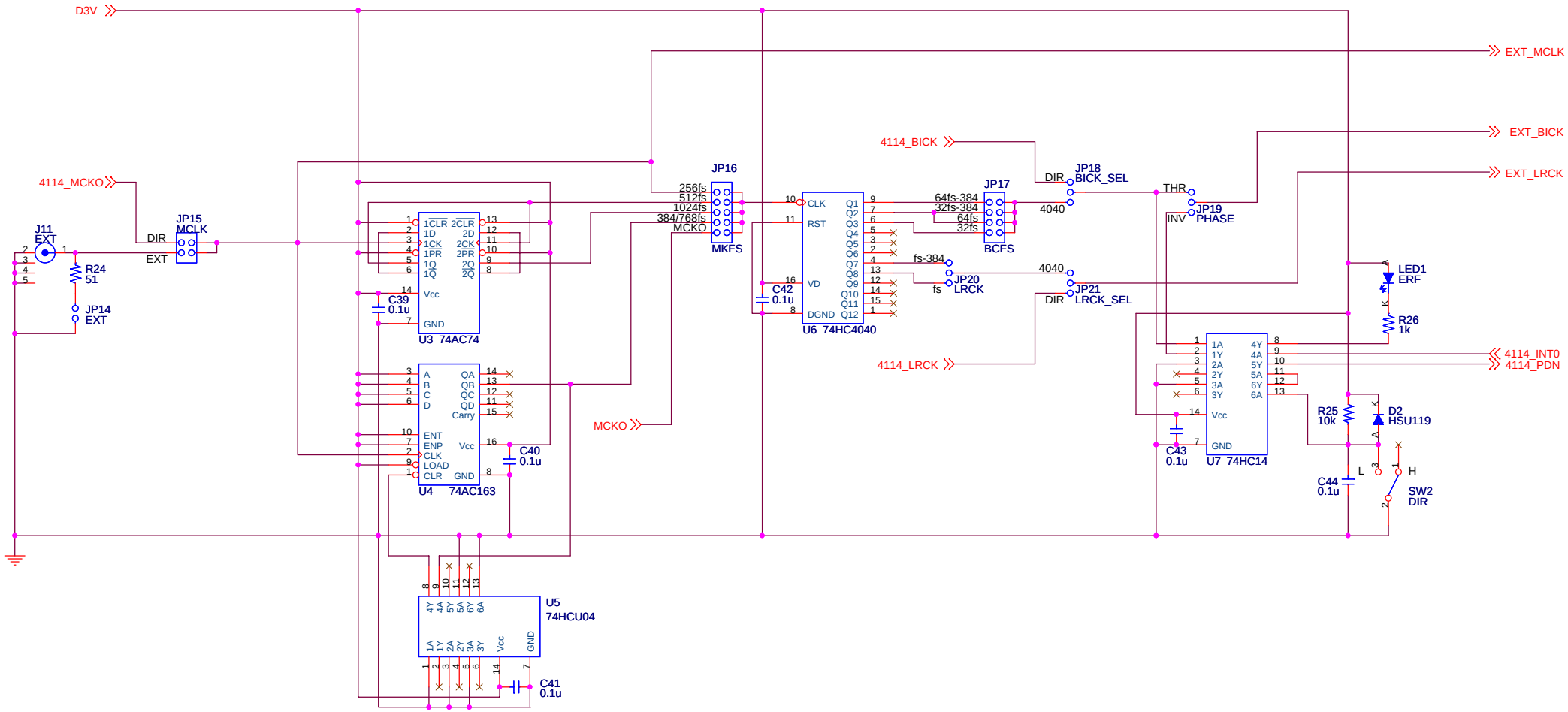
Title	AKD4953-A	
Size A3	Document Number AK4953	Rev 2
Date: Thursday, January 14, 2010	Sheet 1 of 5	



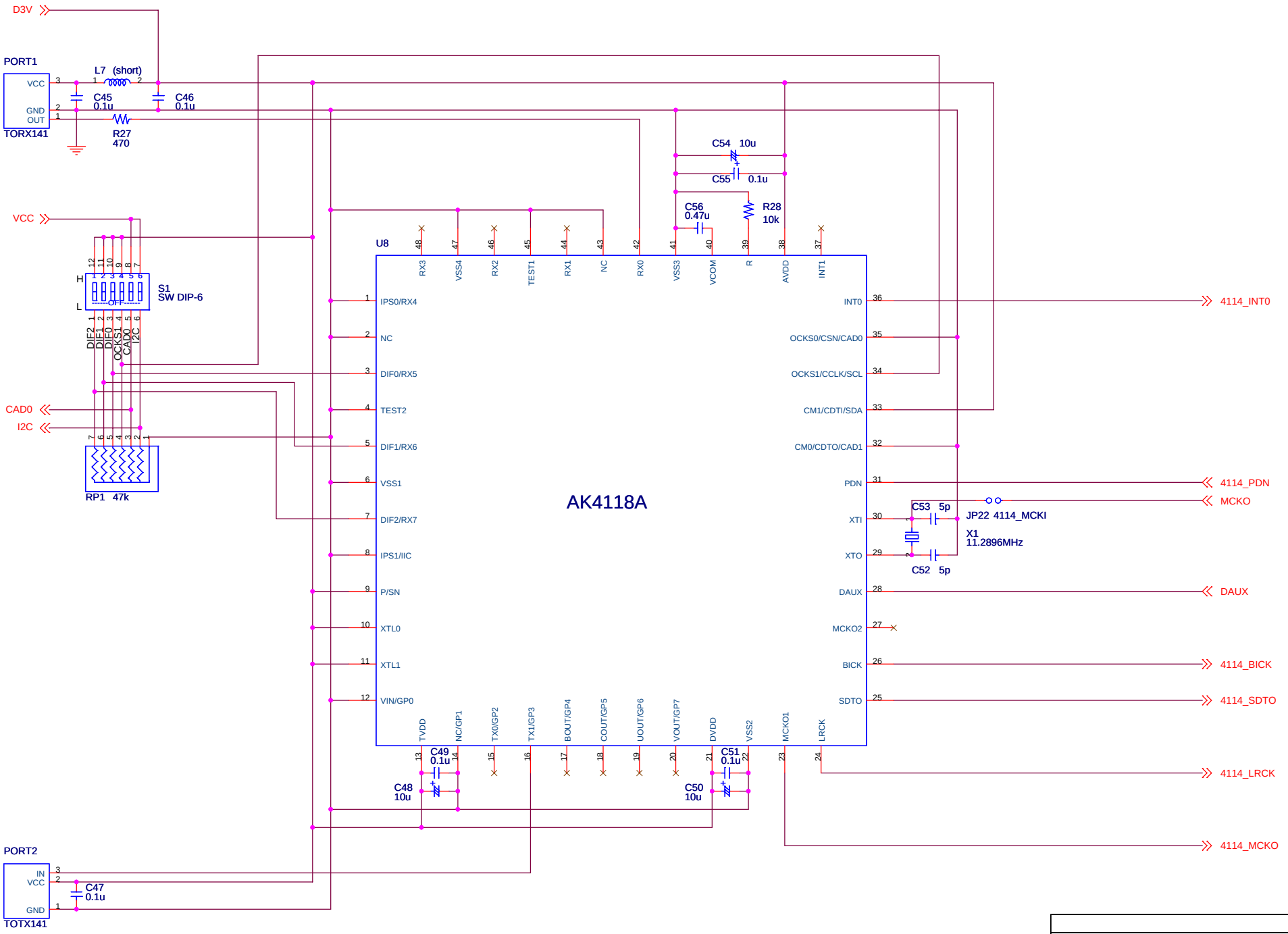




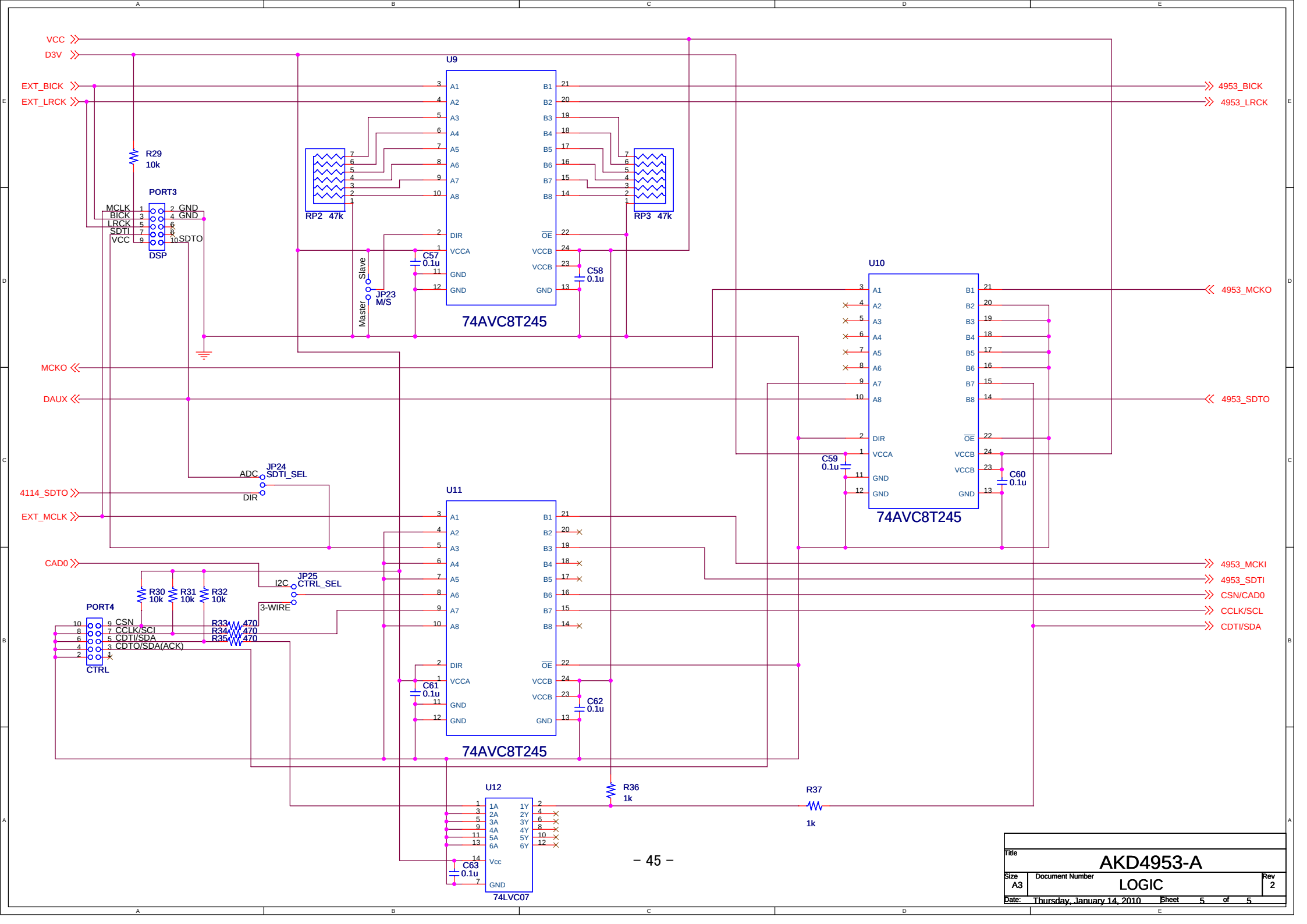
Title	AKD4953-A	
Size: A3	Document Number: Power Supply, I/O	Rev: 2
Date: Thursday, January 14, 2010	Sheet 2 of 5	



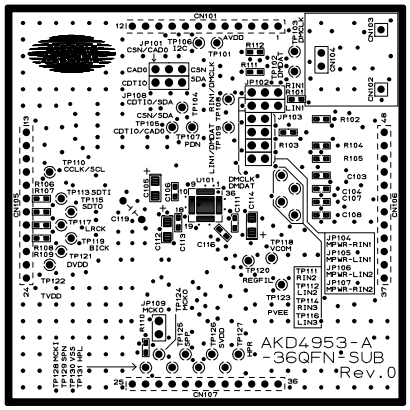
Title	AKD4953-A	
Size: A3	Document Number: CLOCK	Rev: 2
Date: Thursday, January 14, 2010	Sheet 3 of 5	



Title	AKD4953-A	
Size: A3	Document Number: DIR/DIT	Rev: 2
Date: Thursday, January 14, 2010	Sheet 4 of 5	

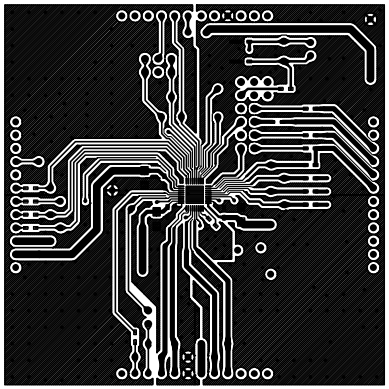


Title	AKD4953-A	
Size: A3	Document Number: LOGIC	Rev: 2
Date: Thursday, January 14, 2010	Sheet 5 of 5	



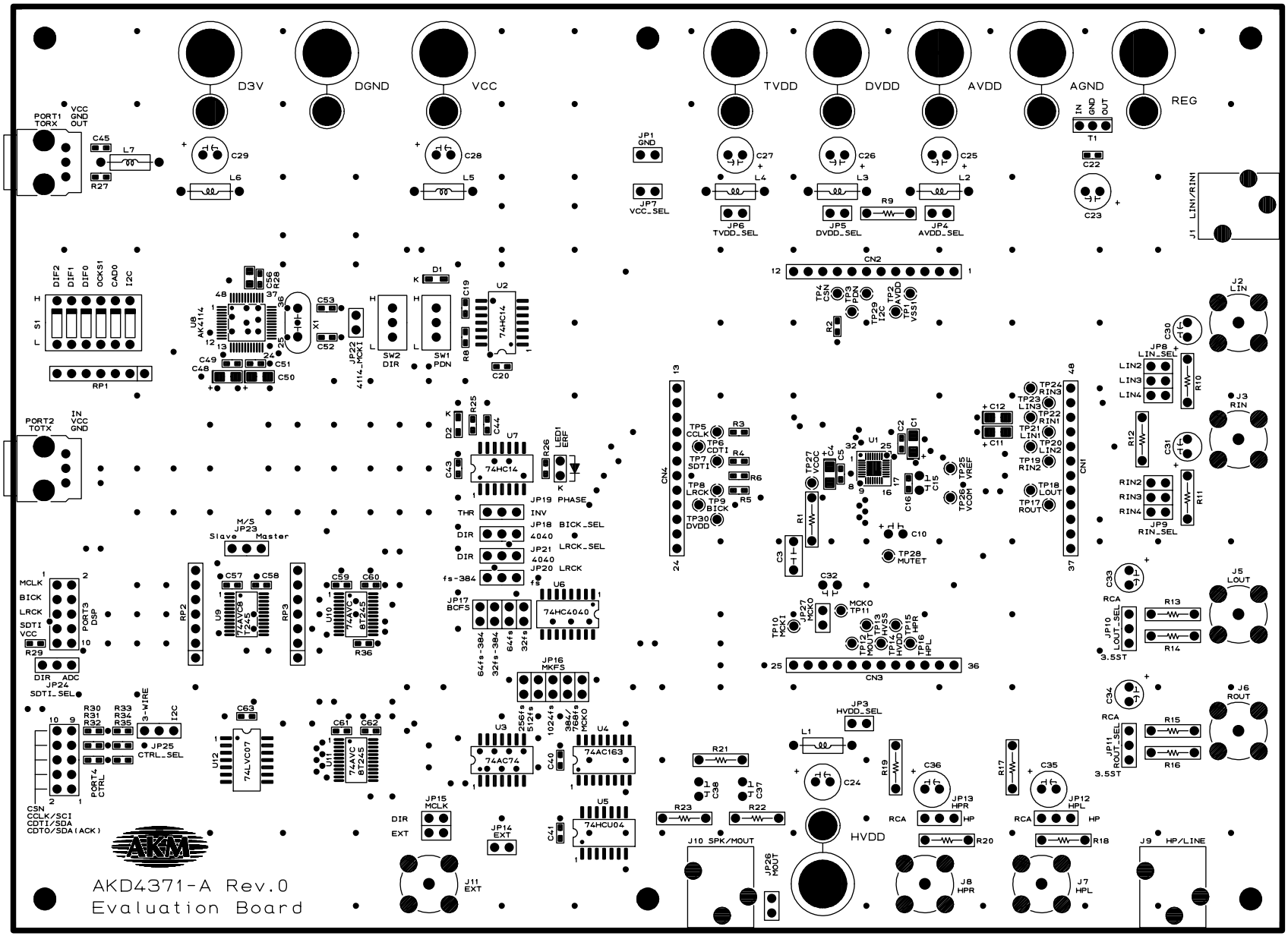
AKD4953-A SUB 36QFN L1 SILK

AKD4353-A SUB 3BOTTOM L2 SILK



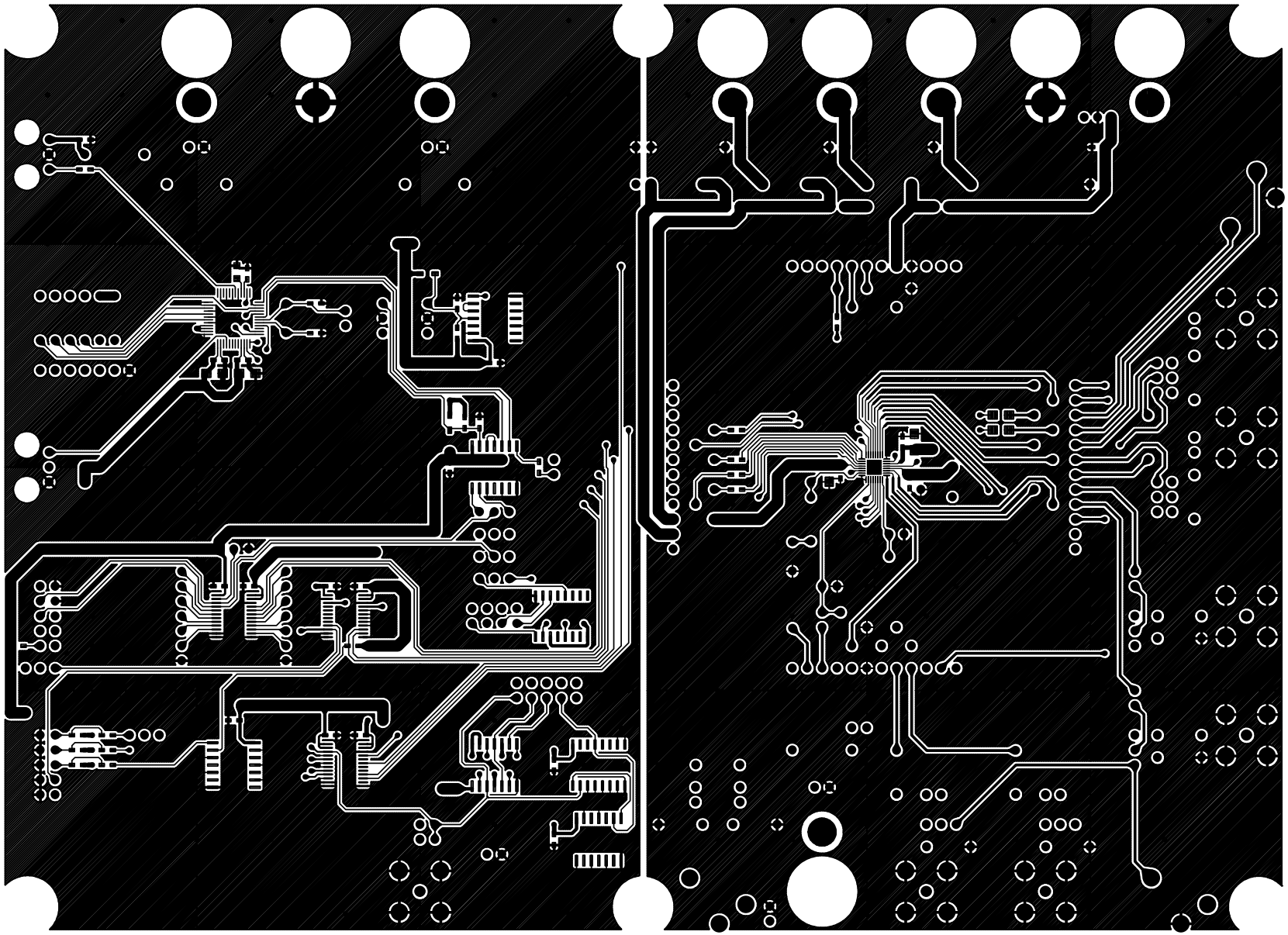
AKD4953-A SUB 36QFN L1

AKD4953-A SUB 36pFN L2



AKD4370-A L1 SILK

AKD6370-A L2 SILK



AKD4370-A L1

AKD6370-A L2