AKD4753-A

AK4753 Evaluation Board Rev.1

GENERAL DESCRIPTION

The AKD4753-A is an evaluation board for AK4753, 2-in, 4-out CODEC with DSP Functions. The AKD4753-A has the Digital Audio I/F and can achieve the interface with digital audio systems via optical connector.

■ Ordering guide

AKD4753-A --- Evaluation Board for AK4753
(Control software and USB cable are packed with this.)

FUNCTION

- **RCA connectors for analog audio input/output**
- **Optical connector for digital audio input**
- **On-board digital audio interface (AK4118A)**
- **Potentiometers for Volume and Bass gain control**
- **USB connector for serial control interface**
- **1k bits EEPROM**

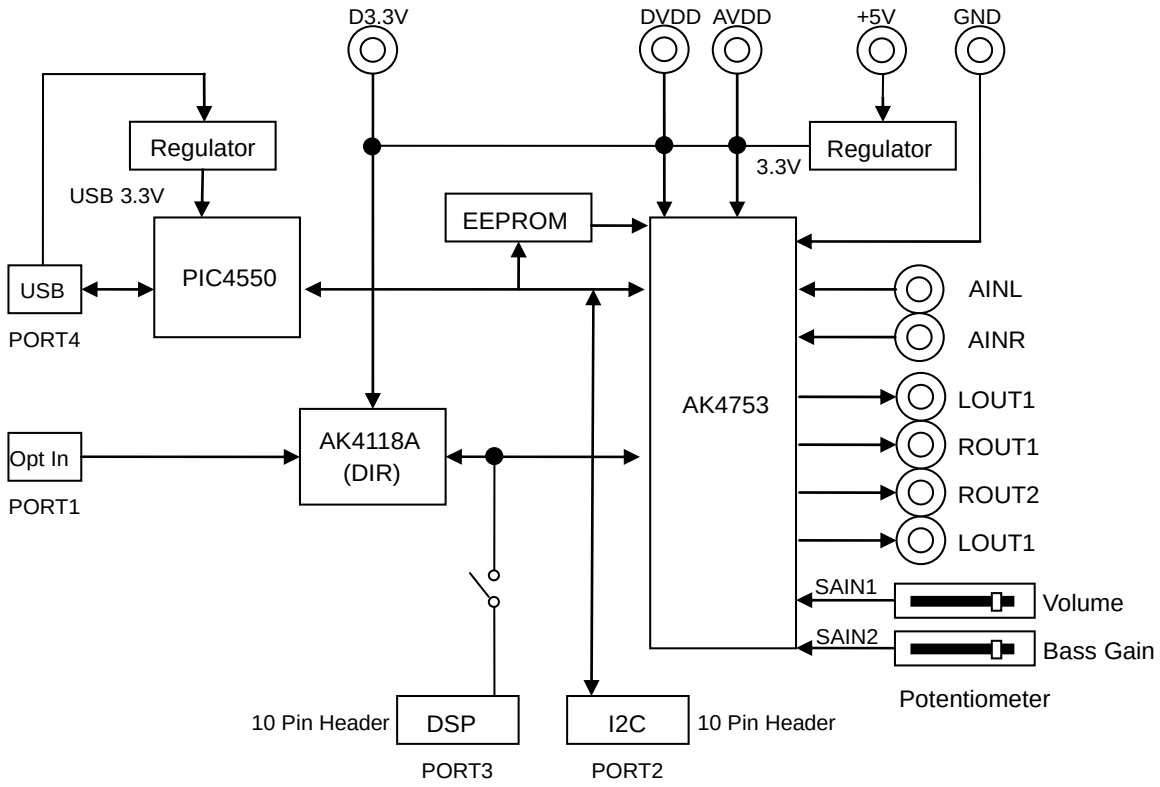


Figure 1. AKD4753-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines

Name of jack	Color of jack	Used for	Open / Connect	Default Setting
+5V	Red	Regulator T2: AVDD, DVDD of AK4753, Digital Logic	Should be always connected When default setting.	+5V
AVDD	Red	AVDD of AK4753	Should be always connected when AVDD of AK4753 is not supplied from regulator T2. In this case "JP13" is set to "Open".	Open
DVDD	Red	DVDD of AK4753	Should be always connected when DVDD of AK4753 is not supplied from regulator T2. In this case "JP14" is set to "Open".	Open
D3.3V	Red	Digital Logic	Should be always connected when Digital Logic is not supplied from regulator T2. In this case "JP15" is set to "Open."	Open
AGND	Black	Analog Ground	Should be always connected.	GND
DGND	Black	Digital Ground	Should be always connected.	GND

Table 1. Set up the power supply lines

Each supply line should be distributed from the power supply unit.

2) Setup the evaluation mode, jumper pins

(2-1) External Slave Mode

(a) Evaluation of using DIR of AK4118A <default>
(b) All interface signals including master clock are fed externally

(2-2) External Master Mode

(a) Evaluation of using DIR of AK4118A

(2-3) PLL Slave Mode

(a) Evaluation of using DIR AK4118A
(b) All interface signals including master clock are fed externally

(2-4) PLL Master Mode

(a) All interface signals including master clock are fed externally

3) Power on

The AK4118A should be reset once bringing S1 (AK4118-PDN) "L" upon power-up.
The AK4753 should be reset once bringing S2 (AK4753-PDN) "L" upon power-up.

■ Evaluation mode

1) External Slave Mode

(a) Evaluation of D/A using DIR of AK4118A. <default>

In case of AK4753 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4753 and AK4118A.Please use AK4118A in the master mode.

PORT1(RX) is used. Nothing should be connected to PORT3(DSP) and J7(MCKI).

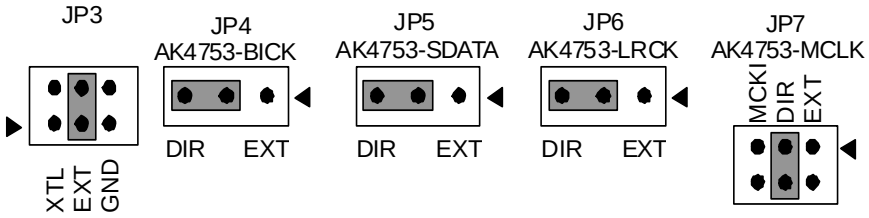


Figure 2. Setting of D/A using DIR of AK4118A

(b) All interface signals including master clock are fed externally.

PORT3(DSP) is used. Nothing should be connected to PORT1(RX) and J7(MCKI).

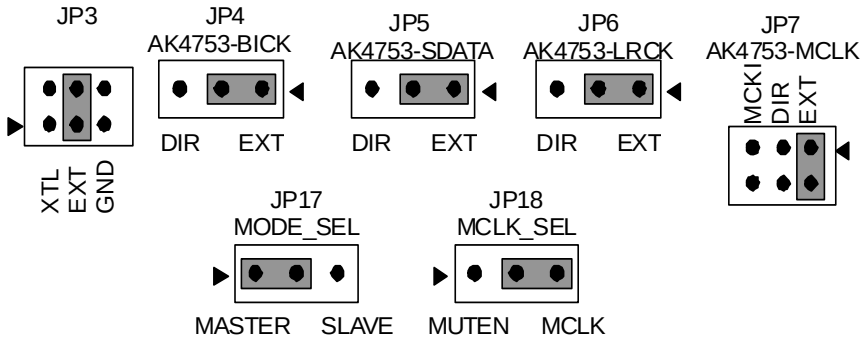


Figure 3. Setting of all interface signals including master clock are fed externally

2) External Master Mode

(a) Evaluation of D/A using DIR of AK4118A.
In case of AK4753 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4753 and AK4118A.Please use AK4118A in the slave mode.

PORT1(RX) is used. Nothing should be connected to PORT3(DSP) and J7(MCKI).

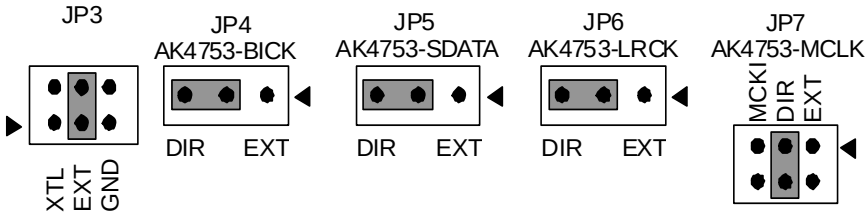


Figure 4. Setting of D/A using DIR of AK4118A

3) PLL Slave Mode

(a) Evaluation of D/A using DIR of AK4118A.
In case of AK4753 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4753 and AK4118A.Please use AK4118A in the master mode.

PORT1(RX) is used. Nothing should be connected to PORT3(DSP) and J7(MCKI).

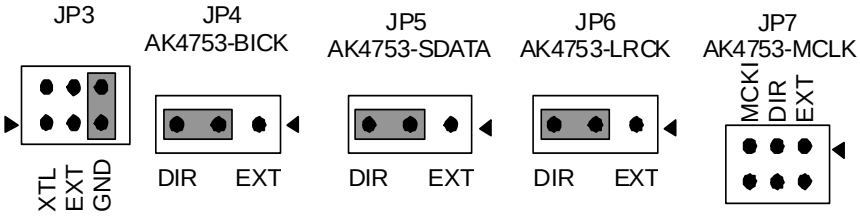


Figure 5. Setting of D/A using DIR of AK4118A

(b) All interface signals including master clock are fed externally.

PORT3(DSP) is used. Nothing should be connected to PORT1(RX) and J7(MCKI).

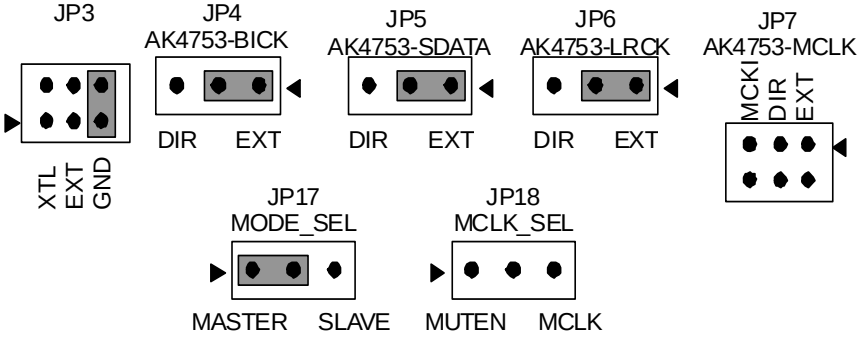


Figure 6. Setting of all interface signals including master clock are fed externally

4) PLL Master Mode

(a) All interface signals including master clock are fed externally.

(a-1) Setup the MCKI.

X1(X'Tal) or J7(MCKI) are used. Nothing should be connected to PORT1(RX).

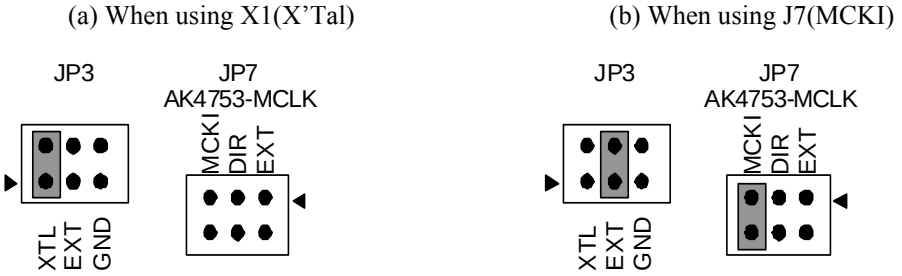


Figure 7. Setup the MCKI

(a-2) Other Setting (BICK, LRCK and SDATA).

PORT3(DSP) is used. Nothing should be connected to PORT1(RX).

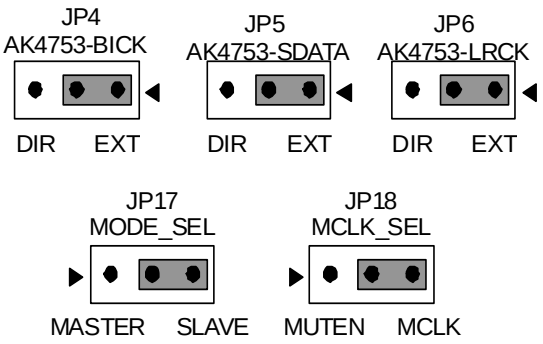


Figure 8. Other Setting (BICK, LRCK and SDATA)

■ EEP-ROM operation setting

1) When you write the setting from Control Soft to EEPROM.
   At this time, please fix the EXTEE switch (See Table 5) to "L".

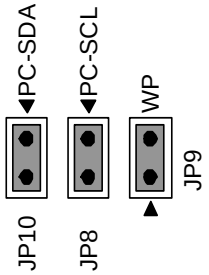


Figure 9. Setting of EEP-ROM operation1

2) When you load the setting from EEPROM to AK4753.
   Please change the EXTEE switch (See Table 5) from "L" to "H" after setting JP8, JP9 and JP10.

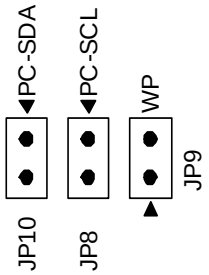


Figure 10. Setting of EEP-ROM operation2

■ Jumper pins setting

[JP1 (SAIN1)]: The selection of connection to SAIN1 pin.
SHORT : Connection. (Default)
OPEN : Unconnection.

[JP2 (SAIN2)]: The selection of connection to SAIN2 pin.
SHORT : Connection. (Default)
OPEN : Unconnection.

[JP8 (PC-SCL)]: The selection of SCL signal.
SHORT : When you write the setting in EEPROM.
OPEN : When you load the setting from EEPROM. (Default)

[JP9 (WP)]: The selection of Write Protect setting of EEPROM.
SHORT : Write protect is Disable.
OPEN : Write protect is Enable. (Default)

[JP10 (PC-SDA)]: The selection of SDA signal.
SHORT : When you write the setting in EEPROM.
OPEN : When you load the setting from EEPROM. (Default)

[JP11]: Not to use.

[JP12 (GND)]: Analog ground and Digital ground.
SHORT : Common. (Default)
OPEN : Separated.

[JP16 (TEST)]: The selection of connection to TEST pin.
SHORT : Connect to VDD.
OPEN : Connect to GND. (Default)

■ Potentiometer setting

[R5]: Volume control
Upper - side: Mute (-∞)
Lower - side: 0dB
[R7]: Bass control
Upper - side: -12dB
Lower - side: +12dB

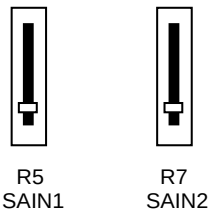


Figure 11. Potentiometers

■ DIR SW Setting

Upper-side is "ON(H)" and lower-side is "OFF(L)".

[S3] (SW DIP-4): Mode setting for AK4118A.

No.	Name	ON ("H")	OFF ("L")	Default
1	OCKS0	AK4118A Master Clock Setting		OFF
2	OCKS1	See Table 3		OFF
3	DIF0	AK4118A Audio Interface Format Setting		ON
4	DIF1	See Table 4		OFF

Table 2. Mode Setting for AK4118A

OCKS1	OCKS0	MCKO1	
L	L	256fs	Default
H	L	512fs	
H	H	Not to use	

Table 3. Setting for AK4118A Master Clock Setting

DIF2	DIF1	DIF0	SDTO	LRCK		BICK		
Fixed "H"	L	L	24bit, Left justified	H/L	O	64fs	O	
	L	H	24bit, I^2S	L/H	O	64fs	O	Default
	H	L	24bit, Left justified	H/L	I	64-128fs	I	
	H	H	24bit, I^2S	L/H	I	64-128fs	I	

Table 4. Setting for AK4118A Audio Interface Format Setting

[S4] (SW DIP-2): Mode setting for AK4753.

No.	Name	ON ("H")	OFF ("L")	Default
1	EXTEE	EEP-ROM Download Mode	Serial Control Mode	OFF
2	BYPASS	DSP Bypass Mode	Normal Operation	OFF

Table 5. Mode Setting for AK4753

■ Function of the Toggle SW

Upper-side is “H” and lower-side is “L”.

[S1] (AK4118-PDN): Resets the AK4118A. Keep “H” during normal operation.
The AK4118A should be resets once bringing “L” upon power-up.

[S2] (AK4753-PDN): Resets the AK4753. Keep “H” during normal operation.
The AK4753 should be resets once bringing “L” upon power-up.

■ Indication for LED

[LED1] (STO): Monitor STO pin of the AK4753.
LED turns on when Read error of EEPROM has occurred to AK4753.

[LED2] (EFR): Monitor INT0 pin of the AK4118A.
LED turns on when some error has occurred to AK4118A.

■ Control Port

It is possible to control AKD4753-A via general USB port. Connect cable with the USB port on board and PC.

Control software is packed with this board. The software operation sequence is included in the evaluation board manual.

■ Analog Input / Output Circuits

1) Analog Inputs

(a) AINL, AINR

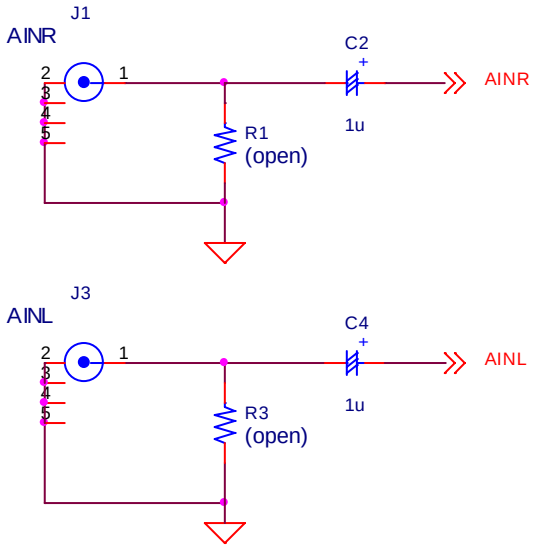


Figure 12. Circuit diagram of AINL and AINR

(b) SAIN1, SAIN2

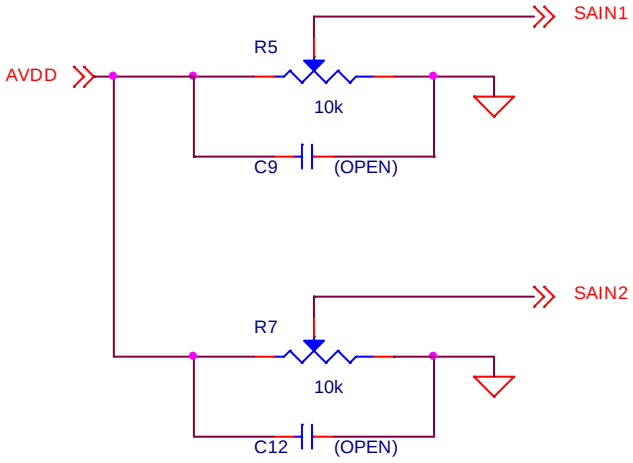


Figure 13. Circuit diagram of SAIN1 and SAIN2

2) Analog Outputs

(a) STEREO Mode (Full-differential)

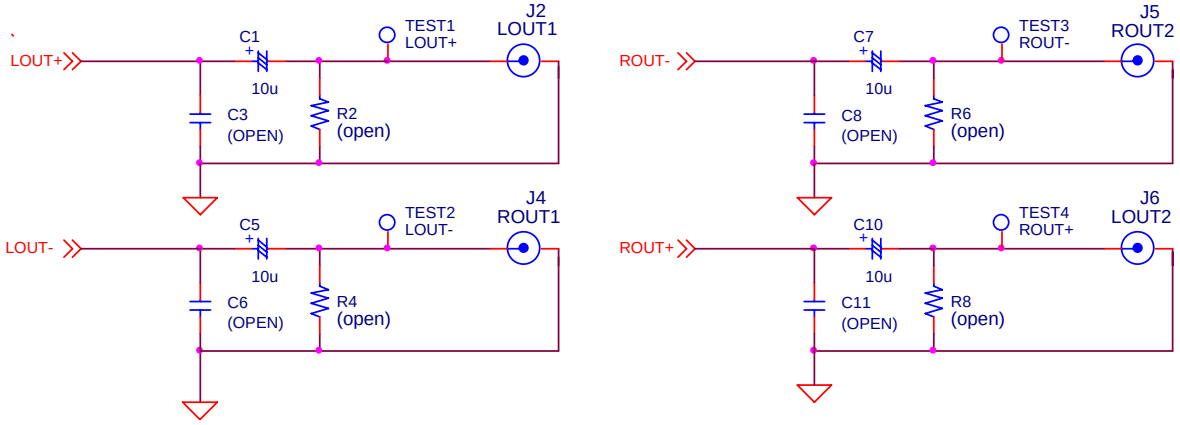


Figure 14. Circuit diagram of STEREO Mode

(b) 2.1-channel Mode

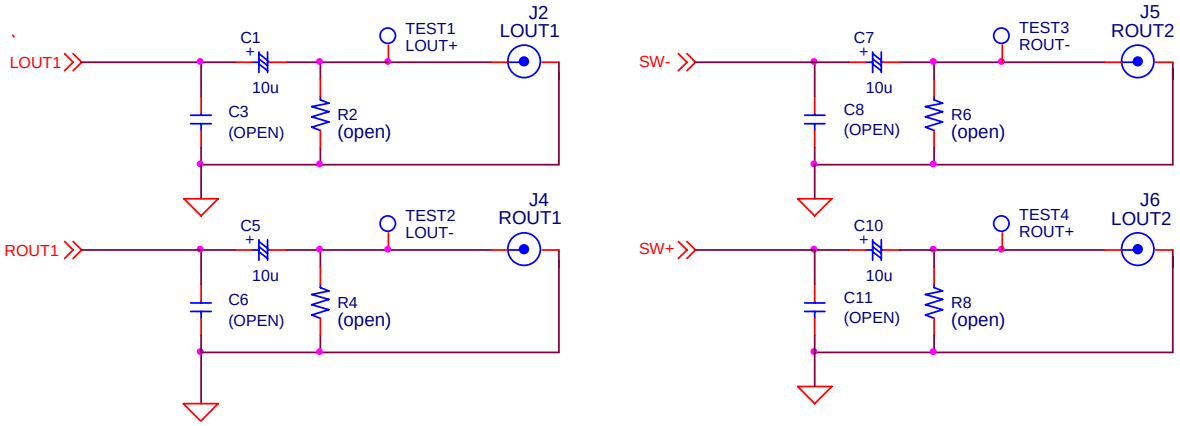


Figure 15. Circuit diagram of 2.1-channel Mode

(c) 4-channel Mode (Single-ended)

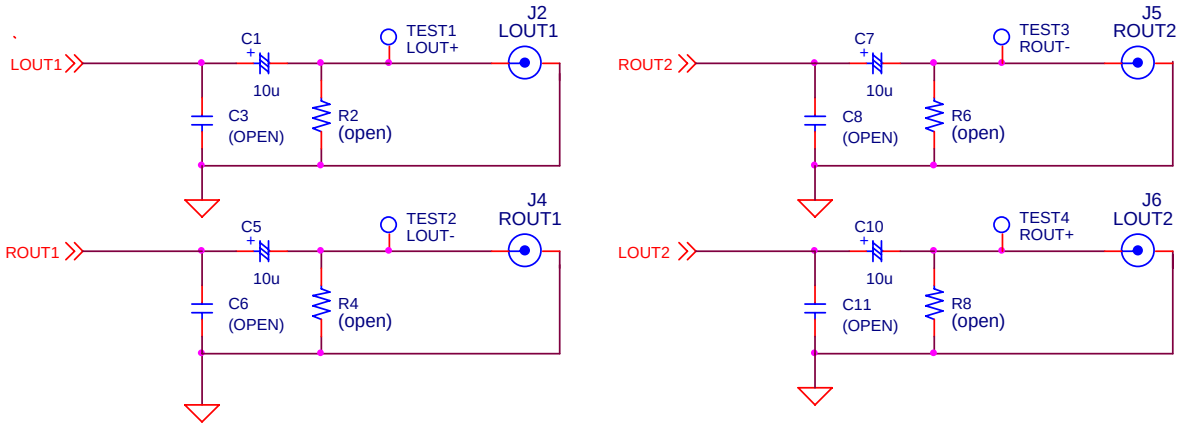


Figure 16. Circuit diagram of 4-channel Mode

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect Evaluation board to PC with USB cable.
   USB control is recognized as HID (Human Interface Device) on the PC.
   When it can not be recognized correctly please Connect Evaluation board to PC with USB cable.
3. Proceed evaluation by following the process below.

■Operation Screen

1. Start up the control program following the process above.
2. After the evaluation board's power is supplied, the AK4753 must be reset once bring S2 (AK4753-PDN) "L" to "H".
3. The operation screen is shown below.

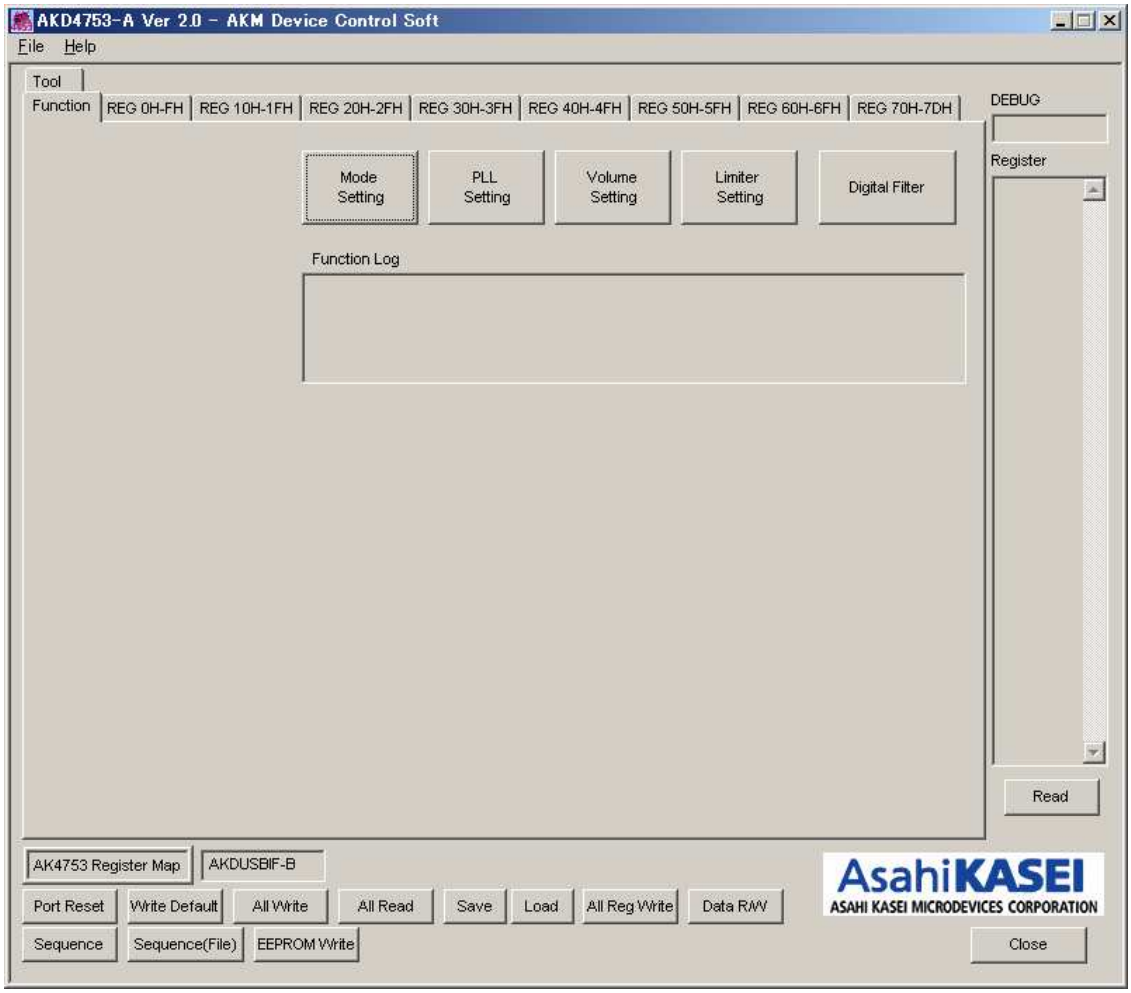


Figure 17. Window of Control Soft

■Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-B)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-B).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [EEPROM Write]: Executing EEPROM write.

12. [Read]: Reading current register settings and display on to the Register area on the right of the main window. This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

■ Tab Functions

1. [Function]: Function control

This tab is for function control.
Each operation is executed by the function buttons on the left side of the screen.

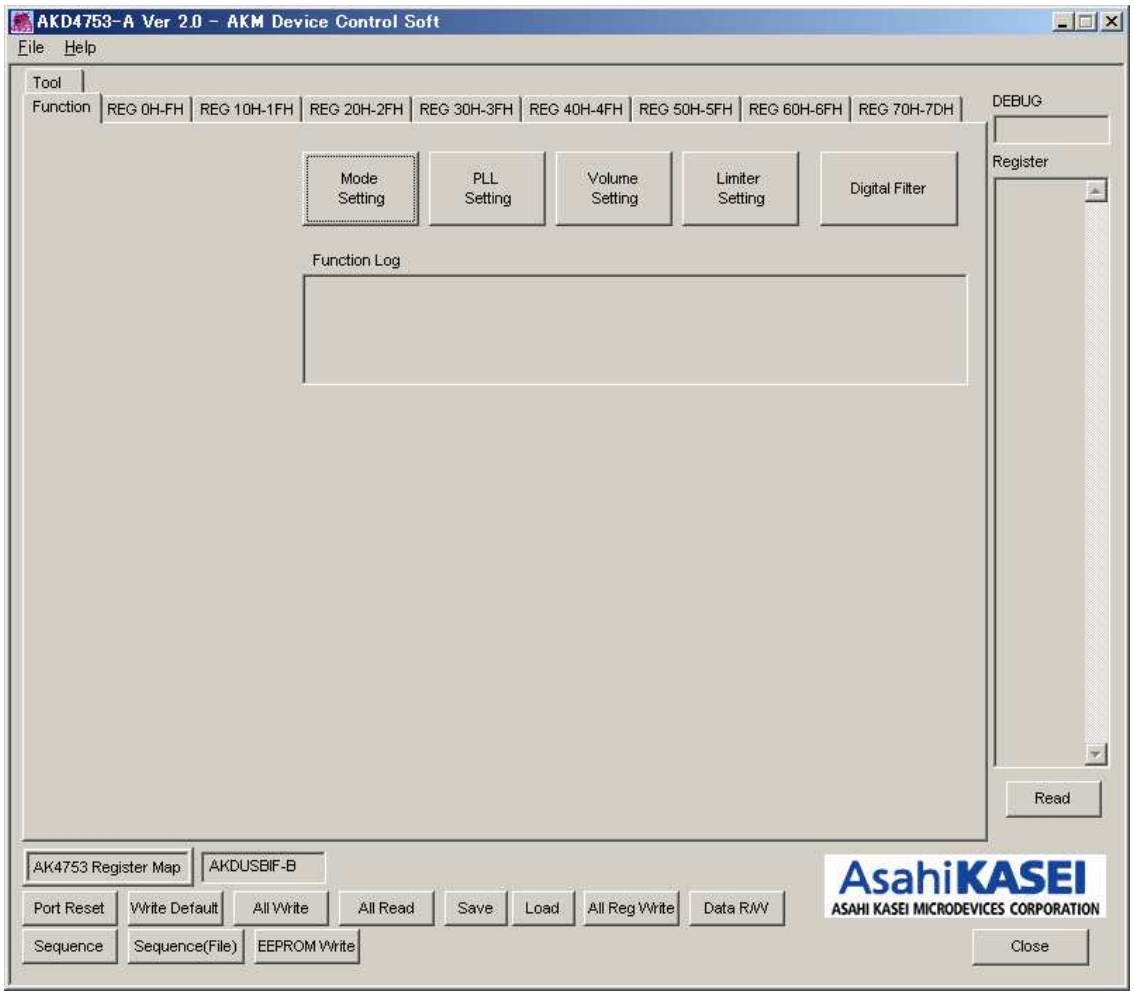


Figure 18.Window of [Function]

1-1. [Mode Setting]: Power Management and Signal Path Setting

When [Mode Setting] button is clicked, the window as shown in opens.
This window is for Power Management and Signal Path Setting.
Refer to the datasheet for register settings of the AK4753.

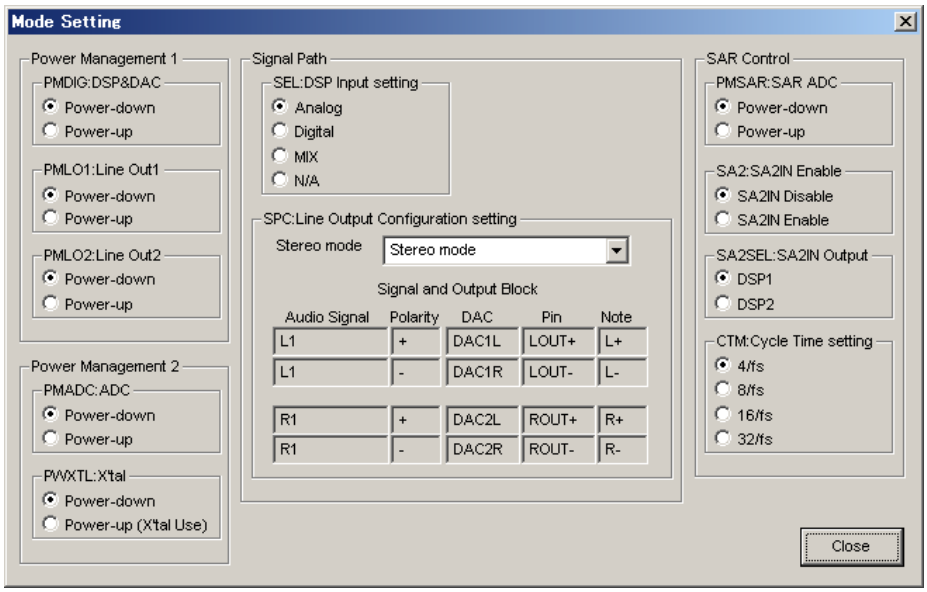


Figure 19. Window of [Mode Setting]

1-2. [PLL Setting]: System Clock and Audio I/F Setting

When [PLL Setting] button is clicked, the window as shown in opens.
This window is for System Clock and Audio I / F Setting.
Refer to the datasheet for register settings of the AK4753.

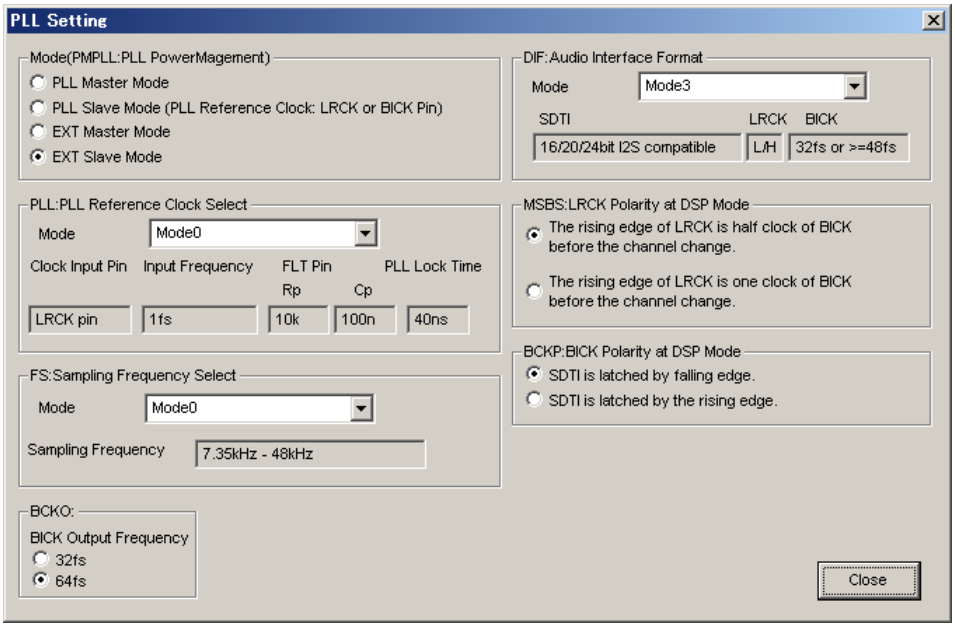


Figure 20. Window of [PLL Setting]

1-3. [DATT Setting]: Volume Setting

When [Volume Setting] button is clicked, the window as shown in opens.
This window is for Volume Setting.
Refer to the datasheet for register settings of the AK4753.

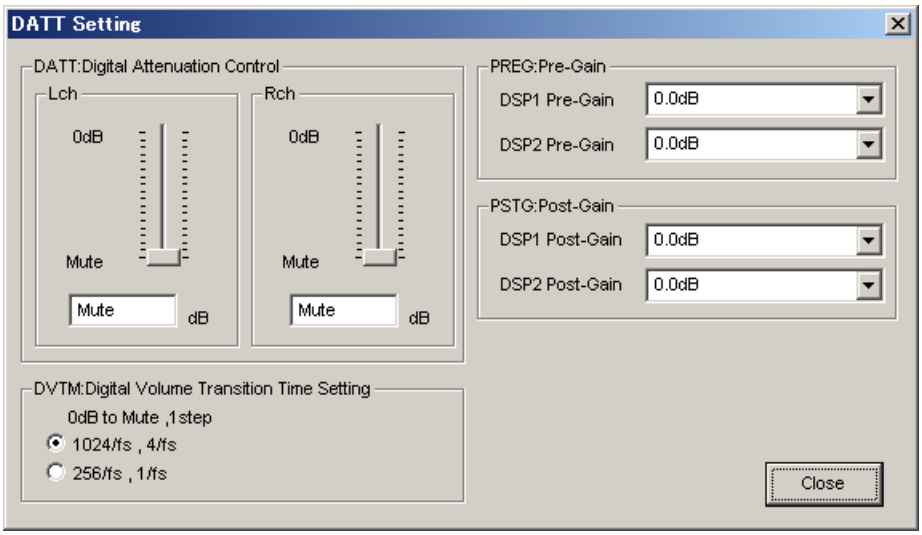


Figure 21. Window of [Volume Setting]

1-3-1. Register map

The volume can be controlled by slide bars.
A register writing is made on every slide bar move.
After the volume slide is moved, it is reflected on to the register map and data writing dialog box.

1-3-2. Volume Control by Slide bar

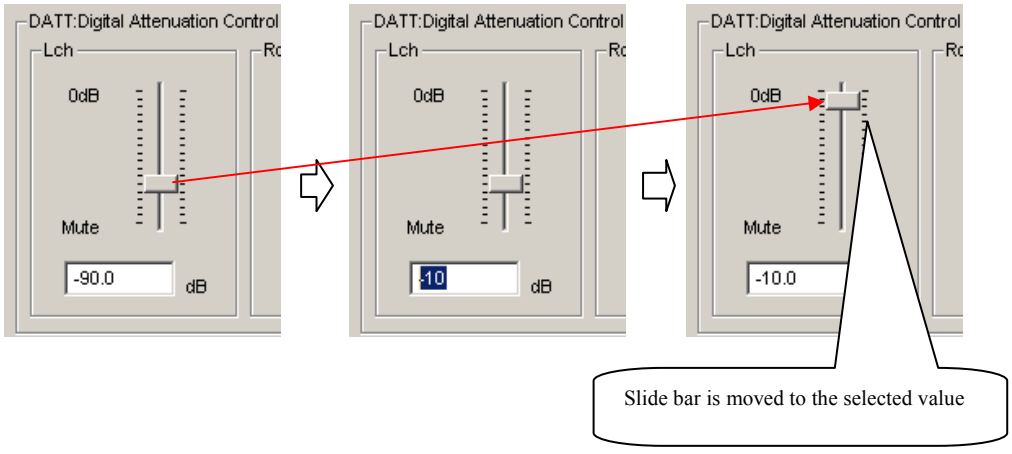


Figure 22. Volume Control by Slide bar

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that written in the dialog box. Use the mouse or arrow keys on the keyboard for small adjustments.

1-4. [Limiter Setting]: Limiter Setting

When [Limiter Setting] button is clicked, the window as shown in opens.
This window is for Limiter Setting.
Refer to the datasheet for register settings of the AK4753.

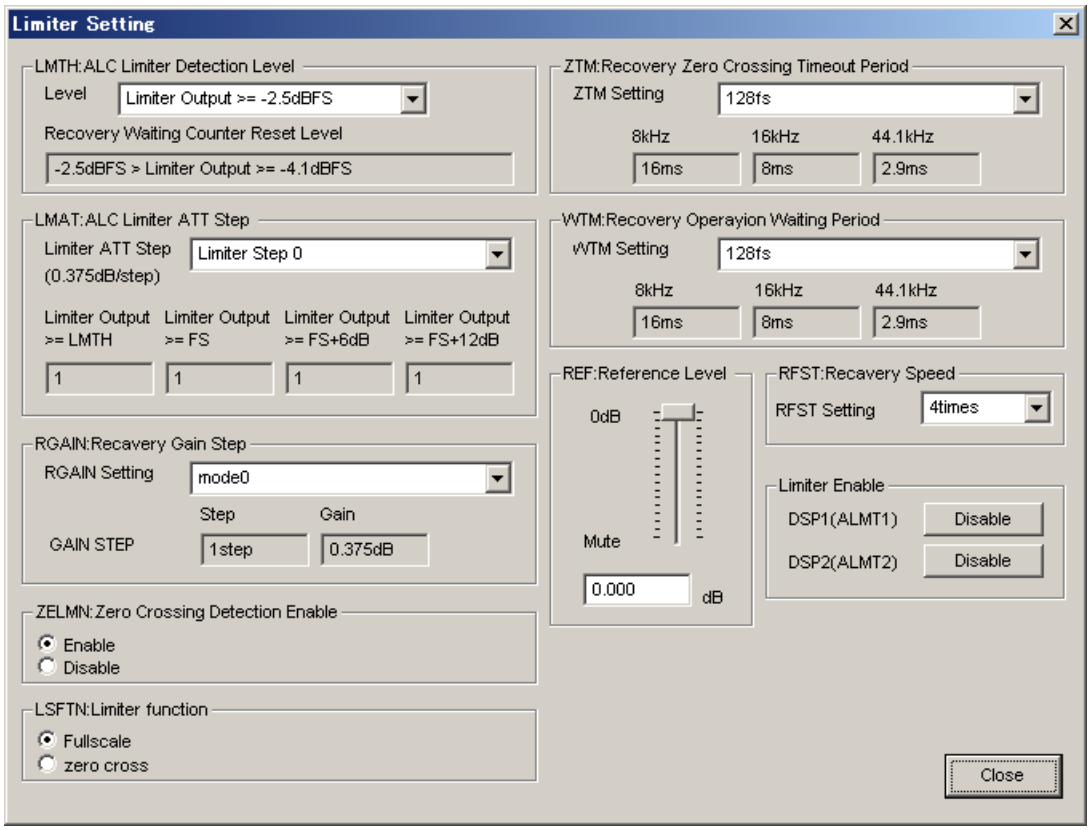


Figure 23. Window of [Limiter Setting]

1-5. [Filter Setting]: Filter Setting

A calculation of a coefficient of Digital Programmable Filters such as HPF / LPF and EQ filters, a register writing and a frequency response checking of HPF / LPF and EQ filters can be made. When [Filter Setting] button is clicked, the window as shown in opens.
Refer to the datasheet for register settings of the AK4753.

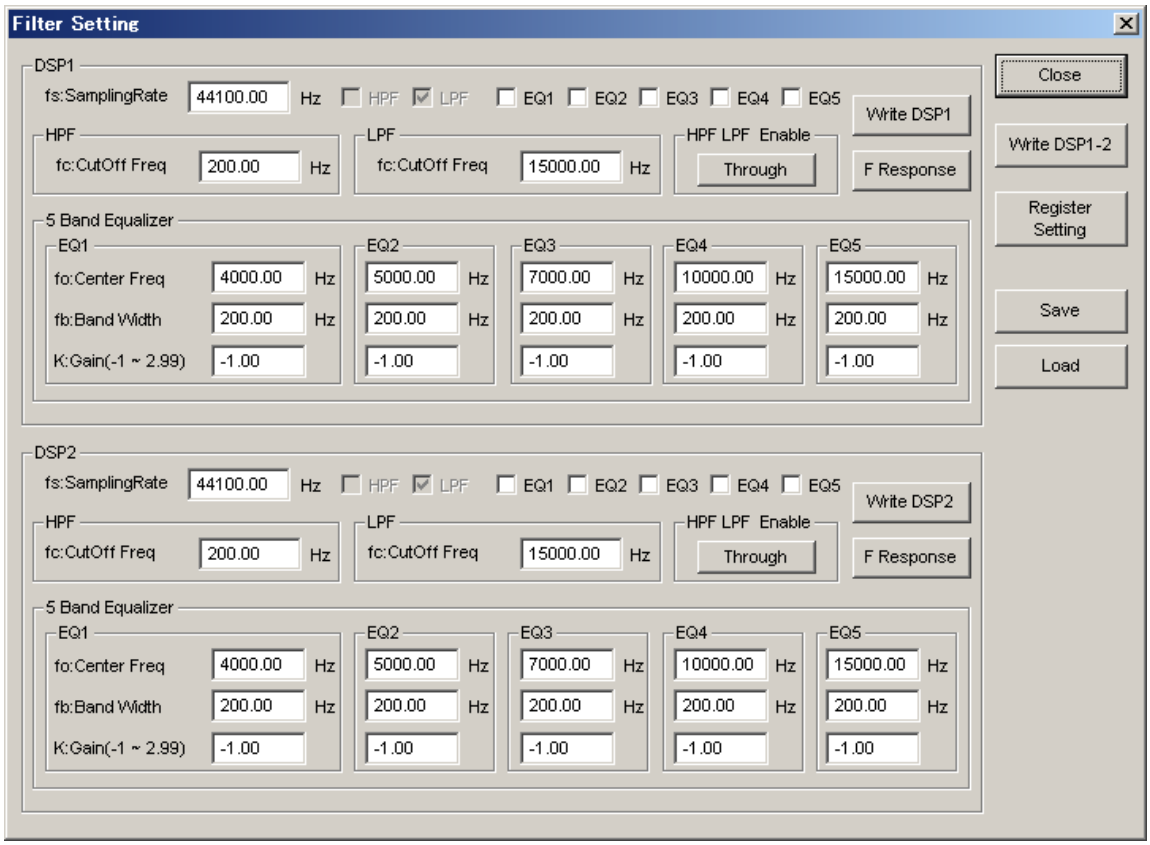


Figure 24. Window of [Filter Setting]

1-5-1. Parameter Setting

(1) Please set a parameter of each Filter.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	$1.042 \times 10^{-3} \leq fc/fs \leq 0.24$
LPF		
Cut Off Frequency	Low pass filter cut off frequency	$5.208 \times 10^{-3} \leq fc/fs \leq 0.24$
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	$3.125 \times 10^{-3} \leq fon/fs < 0.4969$
EQ1-5 Band Width	EQ1-5 Band Width (**Note 1**)	fbn/fs ≤ 0.25
EQ1-5 Gain	EQ1-5 Gain (**Note 2**)	-1≤ Gain < 3

Table 6. Parameter Setting

Note 1. A gain difference is a bandwidth of 3dB from center frequency.
Note 2. When a gain is smaller than 0 , EQ becomes a notch filter.

(2) “HPF LPF Enable” , “HPF” ,”LPF” , “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5”

Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON.
When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed.

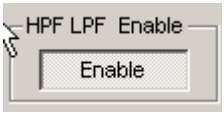


Figure 25. Filter ON/OFF setting button

1-5-2. A calculation of a register

A register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

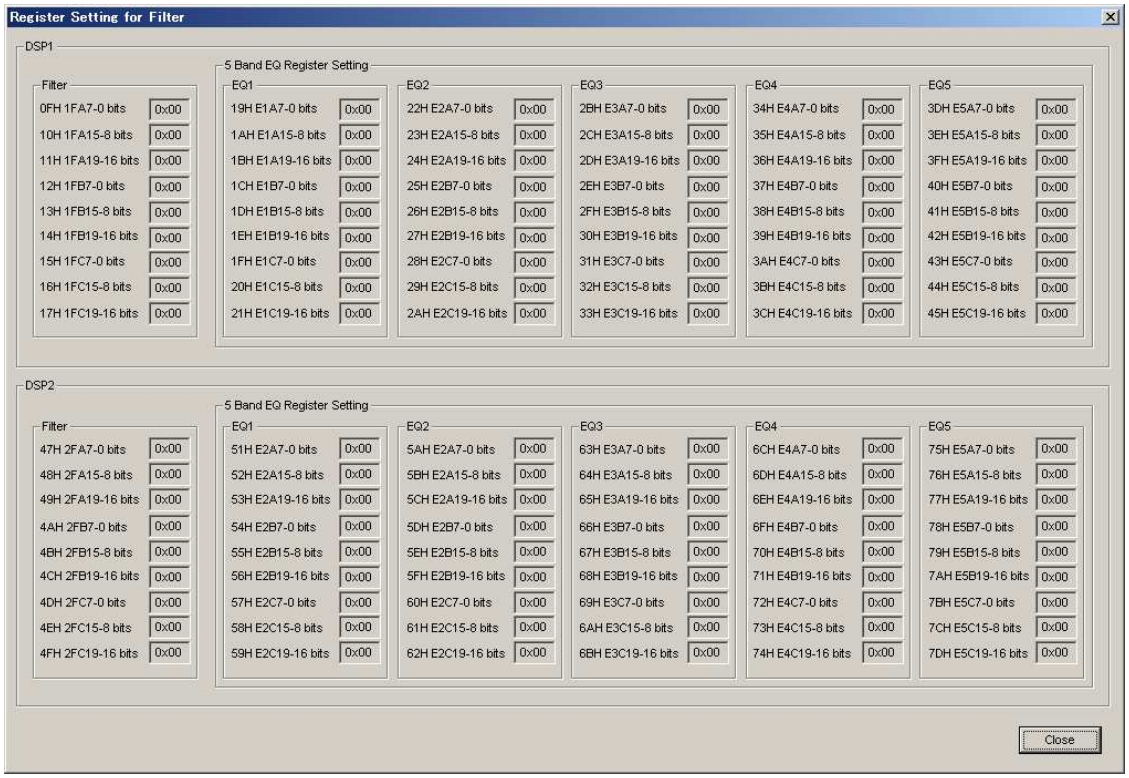


Figure 26. A register setting calculation result

Followings are the cases when a register set value is updated.

(1) When [Register Setting] button was pushed.
(2) When [F Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button "HPF LPF Enable", "HPF" ,"LPF","EQ1", "EQ2", "EQ3", "EQ4", "EQ5"

1-5-3. Indication of a frequency characteristic

A frequency characteristic is displayed when push a [F Response] button. Then, a register set point is also updated.
Change "Frequency Range", and indication of a frequency characteristic is updated when push a [UpDate] button.

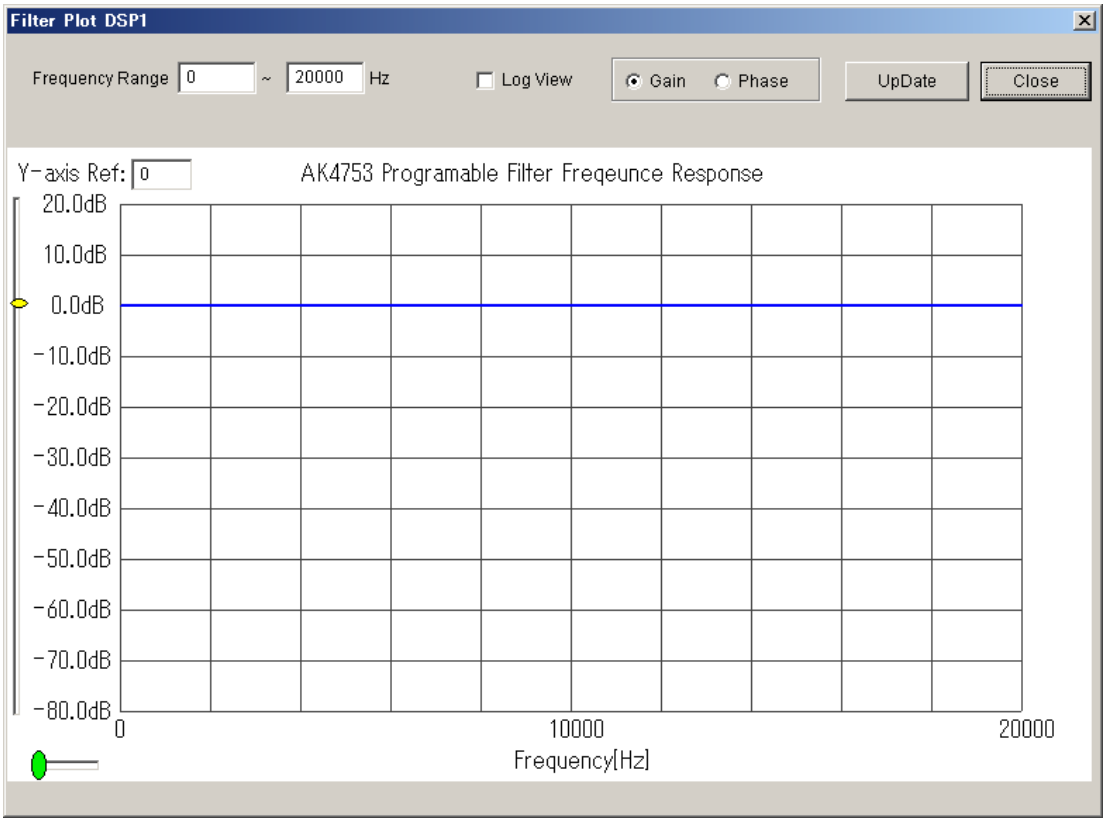


Figure 27. A frequency characteristic indication result

Followings are the cases when a register set value is updated.

(1) When [Register Setting] button was pushed.
(2) When [F Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button "HPF LPF Enable", "HPF" ,"LPF","EQ1", "EQ2", "EQ3", "EQ4", "EQ5"

1-5-4. Filter Setting

The filter setting can be executed by dragging the number to 1-5 in the mouse.
Band Width can be adjusted in the operation of Center Frequency and Gain right-clicking in the operation of the left-click.

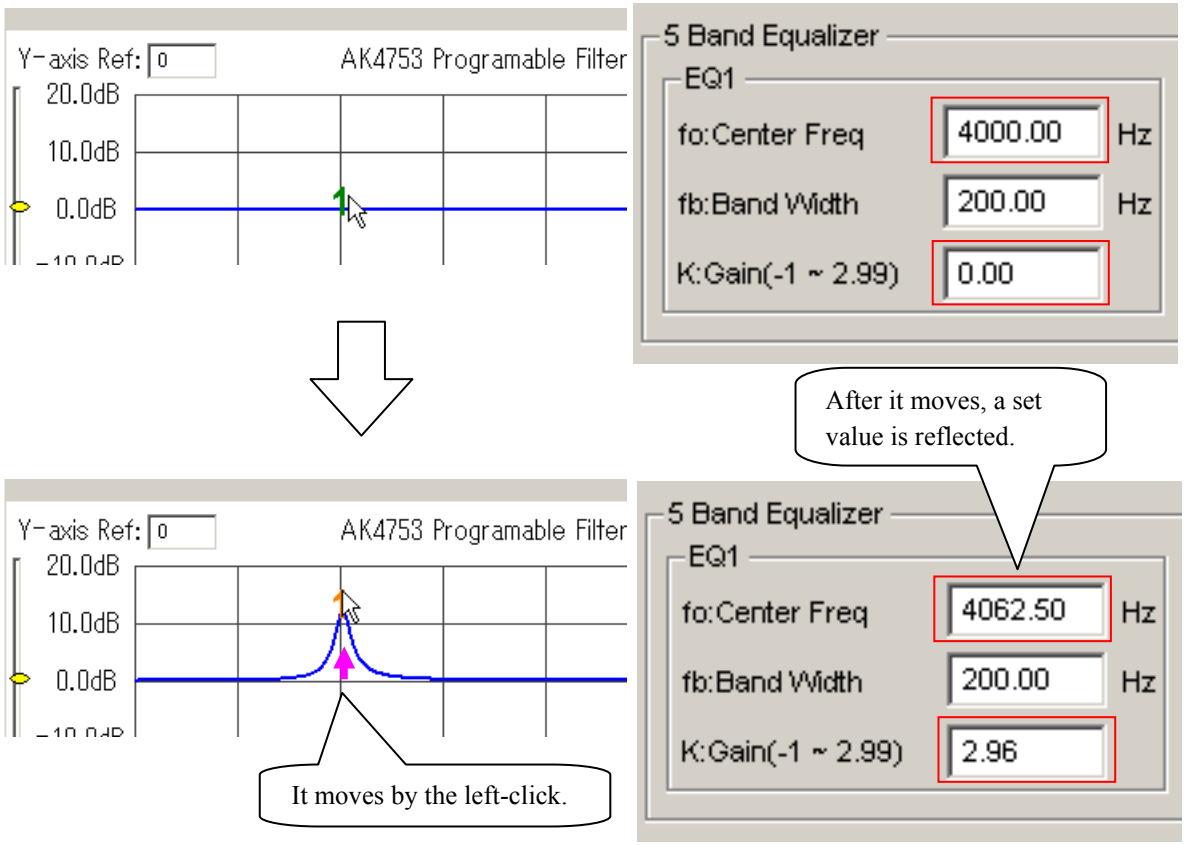


Figure 28. Filter Setting(Left-clicking operation)

Figure 29. Filter Setting(Right-clicking operation)

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

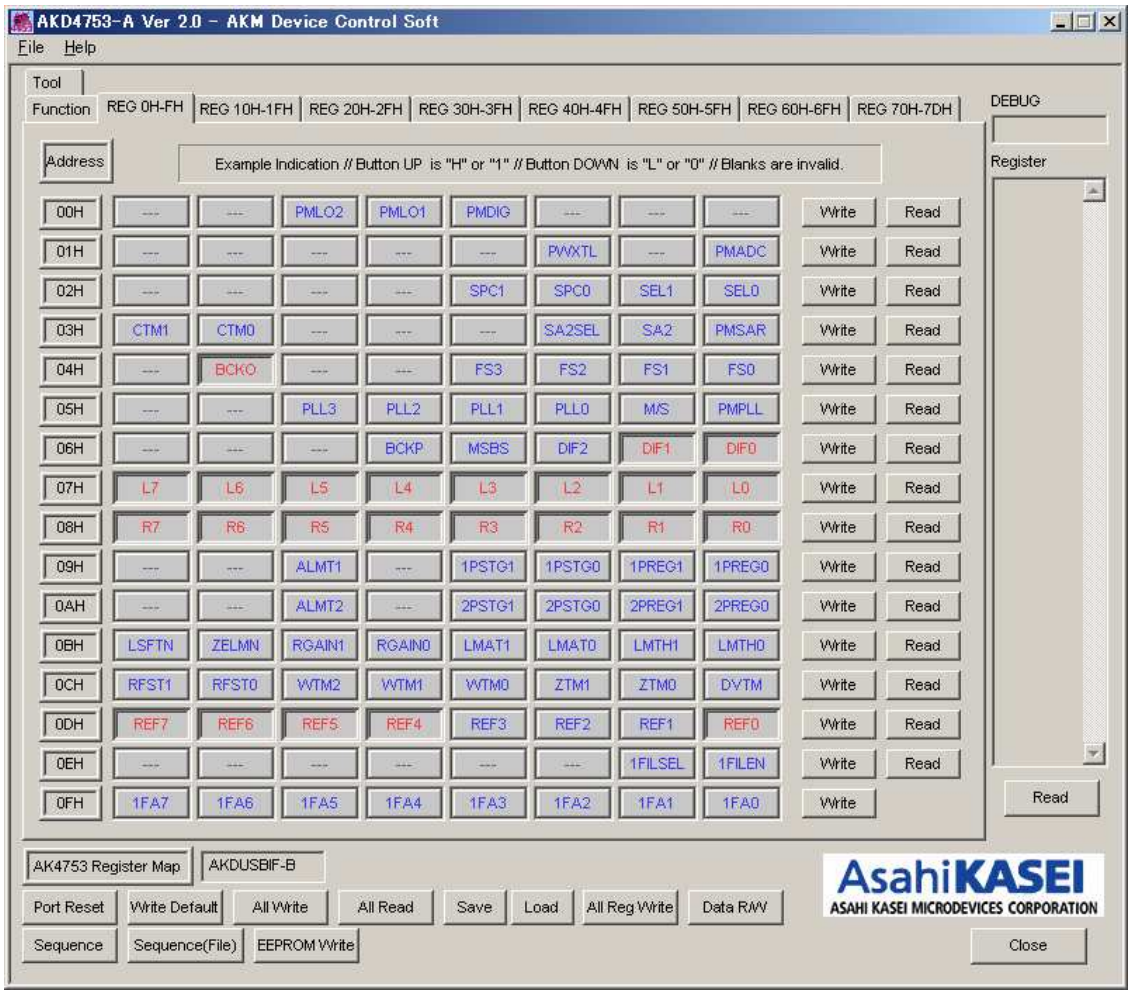


Figure 30. Window of [REG]

2-1. [Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

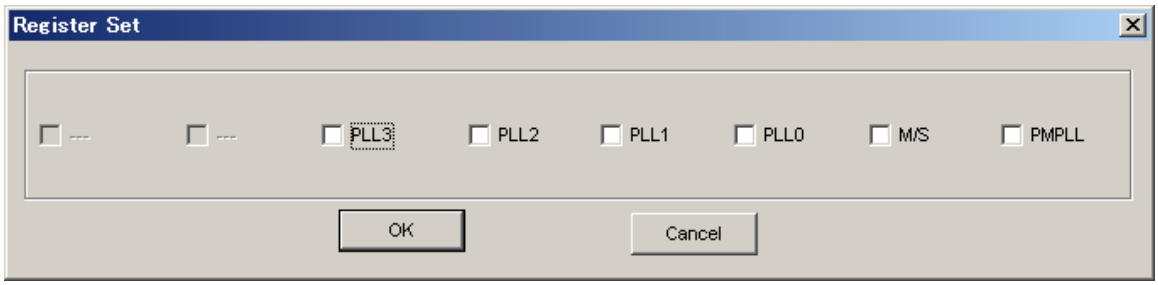


Figure 31. Window of [Register Set]

2-2. [Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

3. [Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

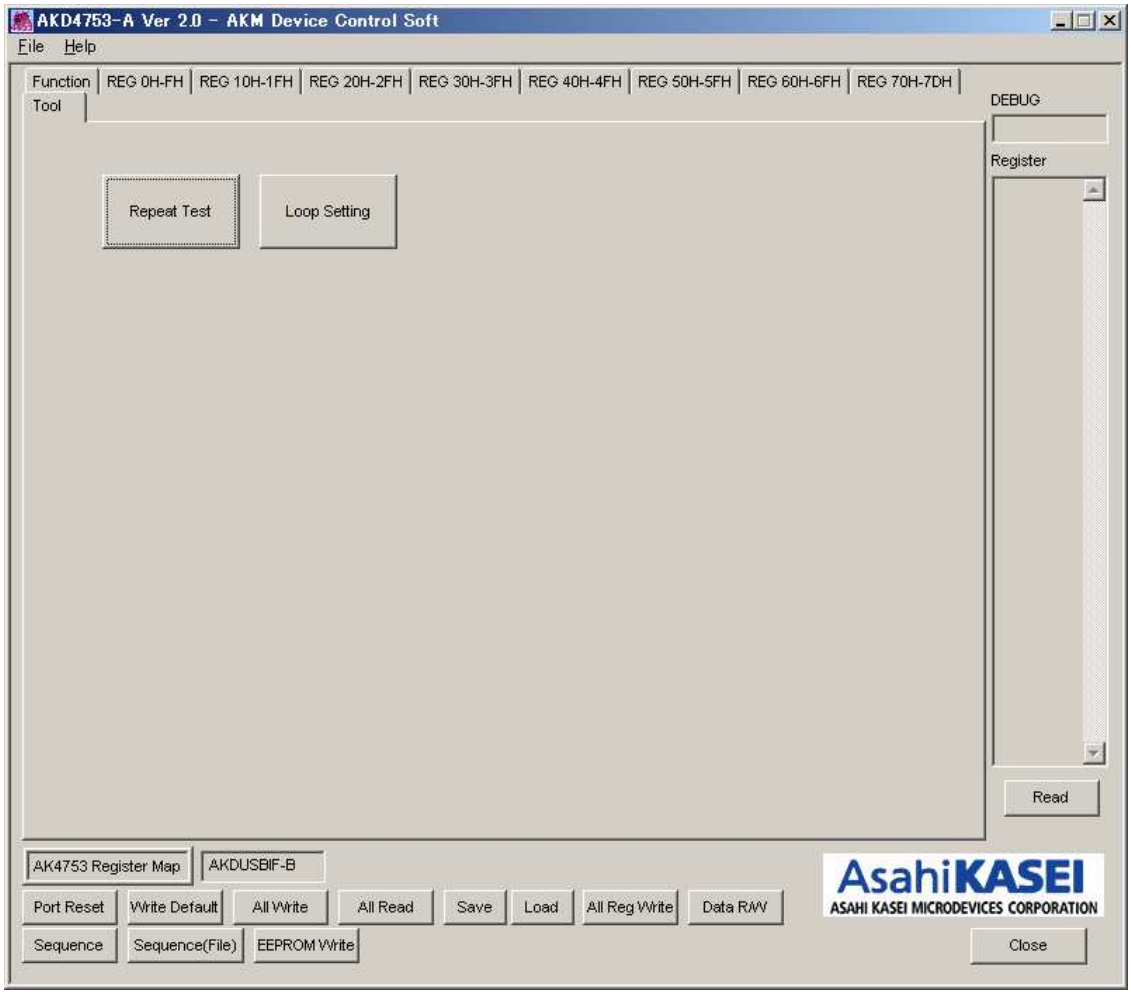


Figure 32. Window of [Tool]

3-1. [Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

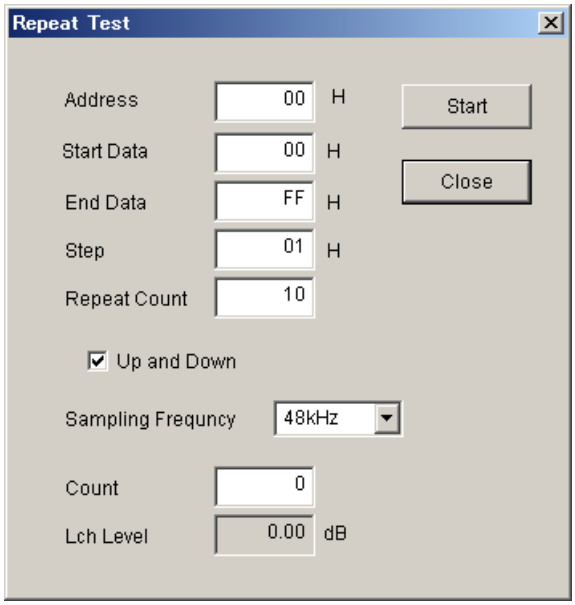


Figure 33. Window of [Repeat Test]

3-2. [Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

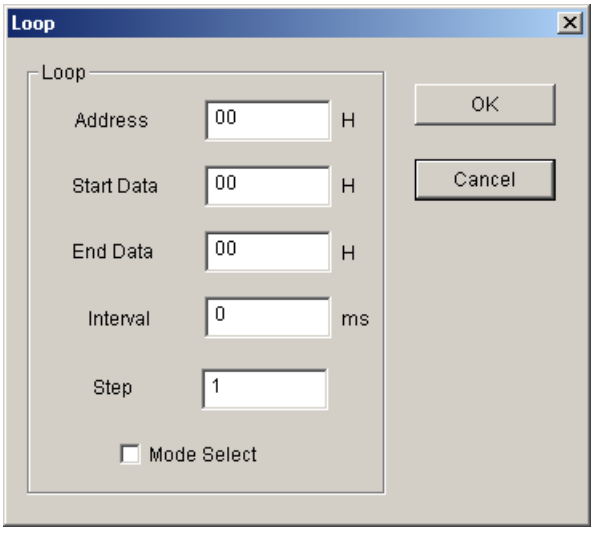


Figure 34. Window of [Loop]

■Dialog Boxes

1. [All Reg Write]: ALL Register Write

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

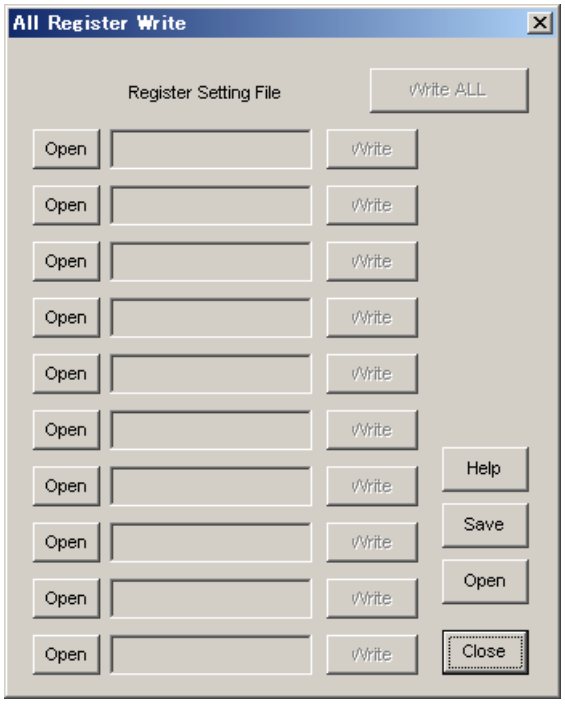


Figure 35. Window of [All Reg Write]

[Open (left)]	: Selecting a register setting file (*.akr).
[Write]	: Executing register writing.
[Write All]	: Executing all register writings. Writings are executed in descending order.
[Help]	: Help window is popped up.
[Save]	: Saving the register setting file assignment. The file name is "*.mar".
[Open (right)]	: Opening a saved register setting file assignment "*. mar".
[Close]	: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.

(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data Read/Write

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

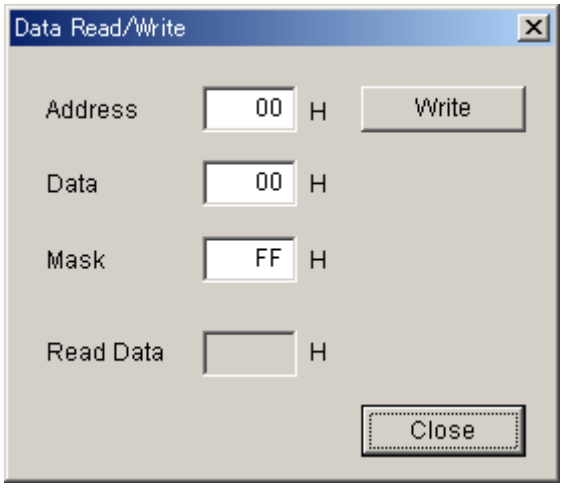


Figure 36. Window of [Data R/W]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is "AND" processed input data.

[Write] : Writing to the address specified by "Address" box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

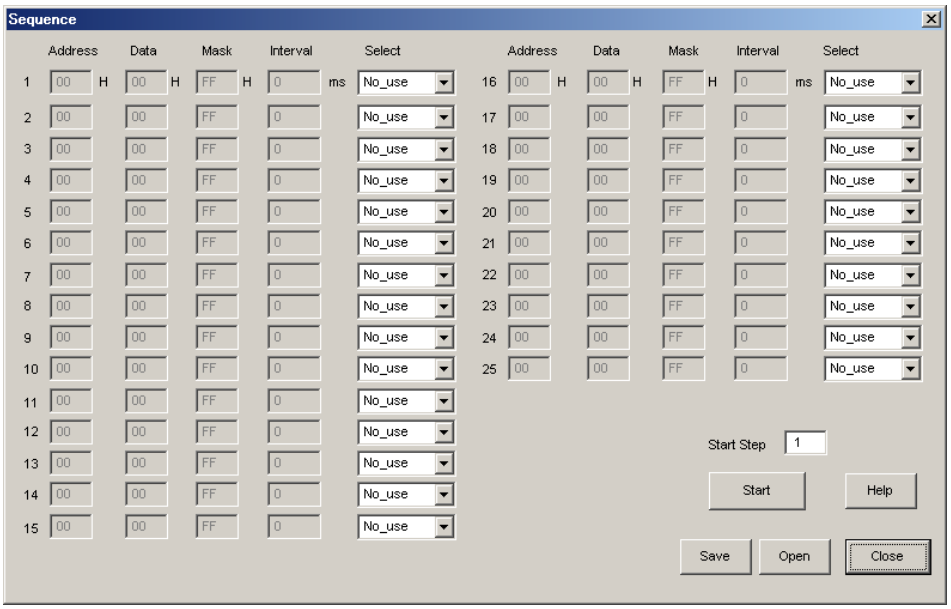


Figure 37. Window of [Sequence]

3-1. Sequence Setting

Set register sequence by following process bellow.

(1)Select a command
Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >

- No_use : Not using this address
- Register : Register writing
- Reg(Mask) : Register writing (Masked)
- Interval : Taking an interval
- Stop : Pausing the sequence
- End : Finishing the sequence

(2)Input sequence

[Address] : Data address
[Data] : Writing data
[Mask] : Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval] : Interval time

Valid boxes for each process command are shown bellow.

· No use : None
· Register : [Address], [Data], [Interval]
· Reg(Mask) : [Address], [Data], [Mask], [Interval]
· Interval : [Interval]
· Stop : None
· End : None

3-2. Control Buttons

The function of Control Button is shown bellow.

[Start] : Executing the sequence
[Help] : Opening a help window
[Save] : Saving sequence settings as a file. The file name is "*.aks".
[Open] : Opening a sequence setting file "*.aks".
[Close] : Closing the dialog box and finish the process.

3-3. Stop of the sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)] : Sequence(File)

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.

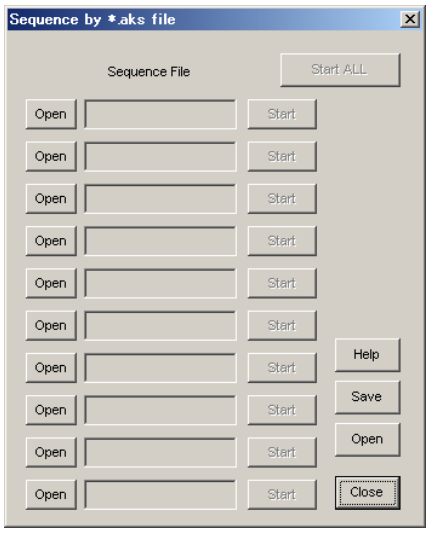


Figure 38. Window of [Sequence(File)]

[Open (left)]	: Opening a sequence setting file (*.aks).
[Start]	: Executing the sequence setting.
[Start All]	: Executing all sequence settings. Sequences are executed in descending order.
[Help]	: Pop up the help window.
[Save]	: Saving sequence setting file assignment. The file name is "*.mas".
[Open(right)]	: Opening a saved sequence setting file assignment "*. mas".
[Close]	: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.

(2) When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.

Figure 39. Window of [Sequence Pause]

5. [EEPROM] : Write

Press the [EEPROM Write] button. Register setting wrings to EEPROM.

The following messages are displayed according to the result of processing.

・Writing failure

Figure 40. Window of [Writing failure]

・Writing success

Figure 41. Window of [Writing success]

Measurement Result

[Measurement condition]

- Measurement Unit : Audio Precession System Two Cascade
- MCLK : 11.2896MHz (DAC)
  12.288MHz (ADC to DAC)
- BICK : 64fs
- fs : 44.1kHz
- Power Supply : AVDD=DVDD=3.3V
- Band Width : 22Hz ~ 22kHz
- Measurement Mode : External Slave Mode (DAC)
  PLL Master Mode (ADC to DAC)
- Temperature : Room Temperature

[Measurement Result]

1. DAC

a). Single-ended, LOUT1/ROUT1, LOUT2/ROUT2 R_L=Open

Parameter	Result Lch1 / Rch1	Result Lch2 / Rch2	Unit
S/(N+D) (0dBFS Input)	88.6 / 88.6	88.7 / 88.7	dB
D-Range (-60dB Input, A-weighted)	98.0 / 98.7	98.7 / 98.3	dB
S/N (No Signal, A-weighted)	98.0 / 98.7	98.9 / 98.4	dB
Output Voltage	2.40 / 2.40	2.40 / 2.40	Vpp

b). Differential, LOUT/ROUT, R_L=Open

Parameter	Result Lch / Rch	Unit
S/(N+D) (0dBFS Input)	92.4 / 92.2	dB
D-Range (-60dB Input, A-weighted)	103.2 / 102.7	dB
S/N (No Signal, A-weighted)	103.6 / 102.6	dB
Output Voltage	±2.40 / ±2.40	Vpp

2. ADC to DAC

a). Single-ended, LOUT1/ROUT1, LOUT2/ROUT2 R_L=Open

Parameter	Result Lch1 / Rch1			Result Lch2 / Rch2			Unit
S/(N+D) (-1dBFS Input)	82.9	/	83.3	82.9	/	83.2	dB
D-Range (-60dB Input, A-weighted)	92.3	/	93.1	92.6	/	93.1	dB
S/N (No Signal, A-weighted)	92.3	/	93.2	92.6	/	93.1	dB

b). Differential, LOUT/ROUT, R_L= Open

Parameter	Result Lch / Rch			Unit
S/(N+D) (-1dBFS Input)	85.4	/	85.3	dB
D-Range (-60dB Input, A-weighted)	96.0	/	95.9	dB
S/N (No Signal, A-weighted)	96.1	/	96.0	dB

PLOT DATA

1-a). DAC Single-ended [LOUT1/ROUT1 pins]

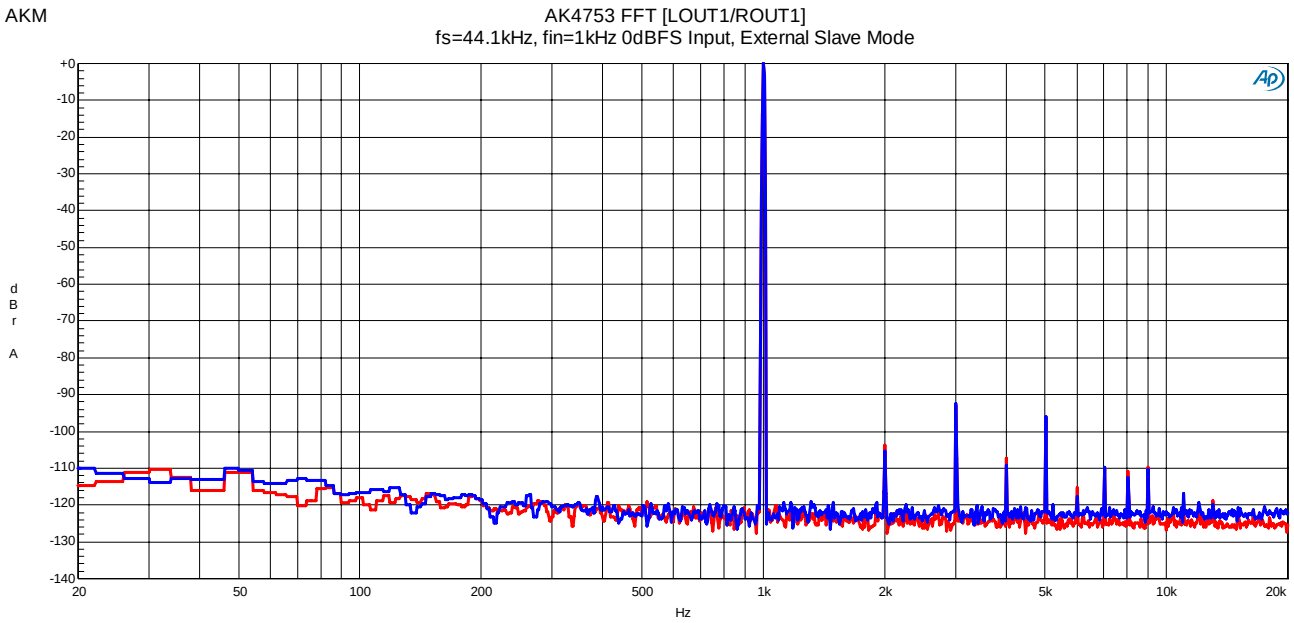


Figure 42. FFT(0dBFS Input)

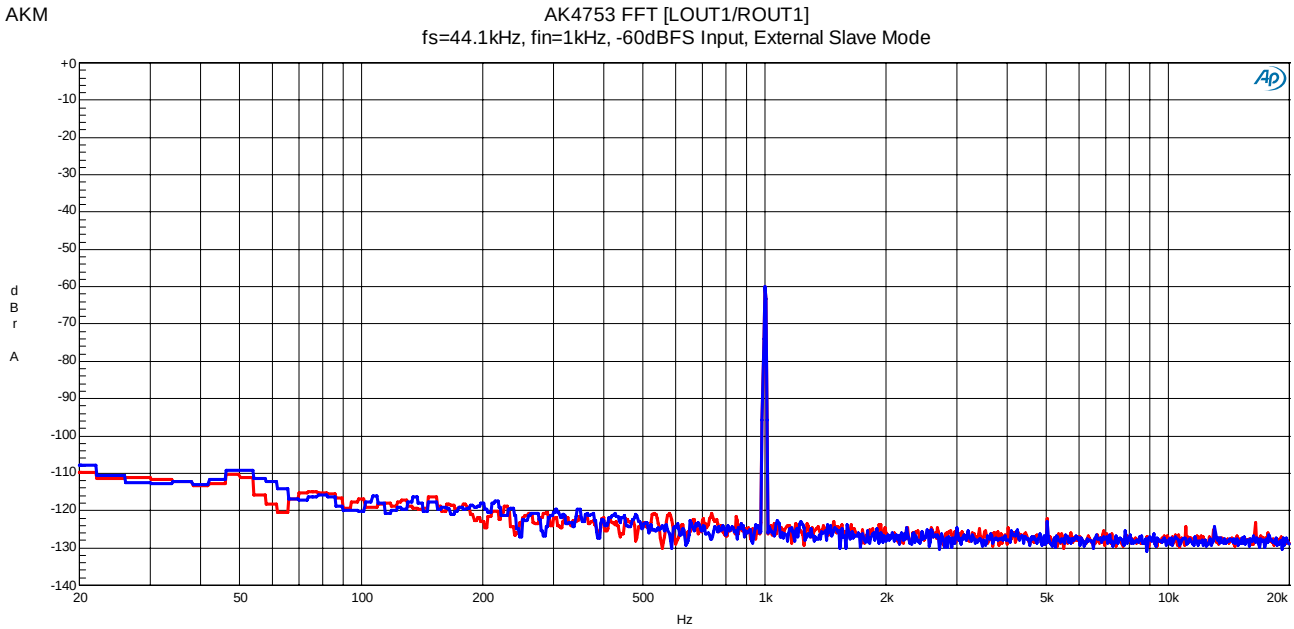


Figure 43. FFT(-60dB Input)

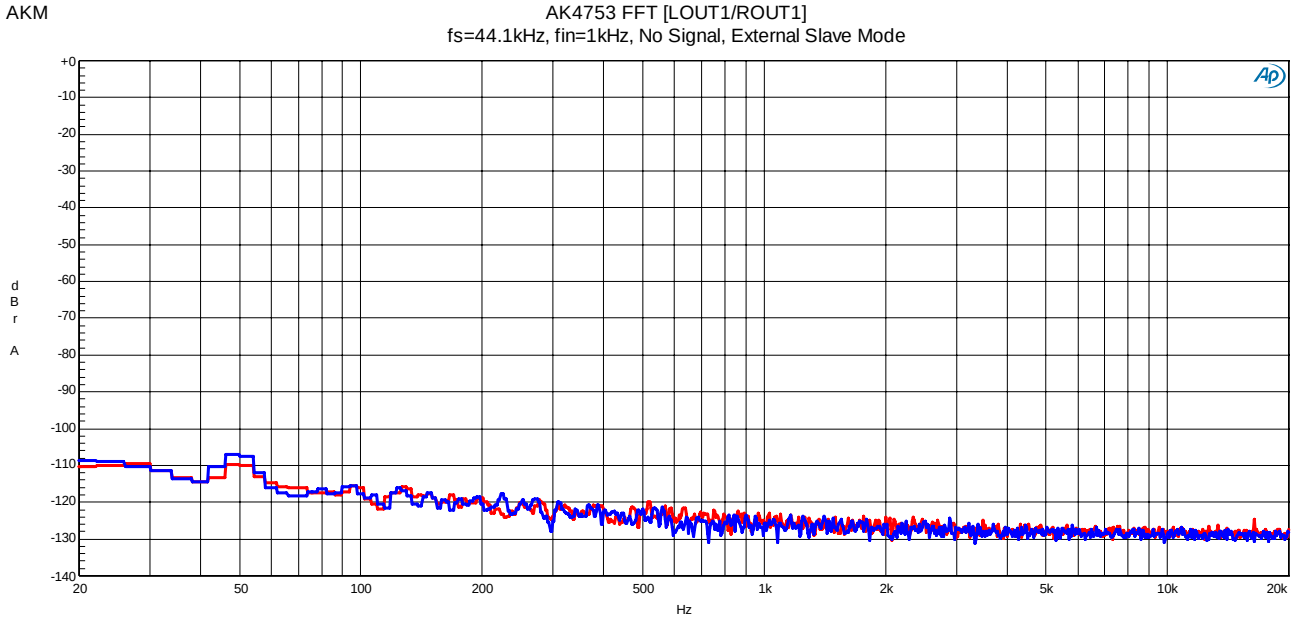


Figure 44. FFT(No Signal)

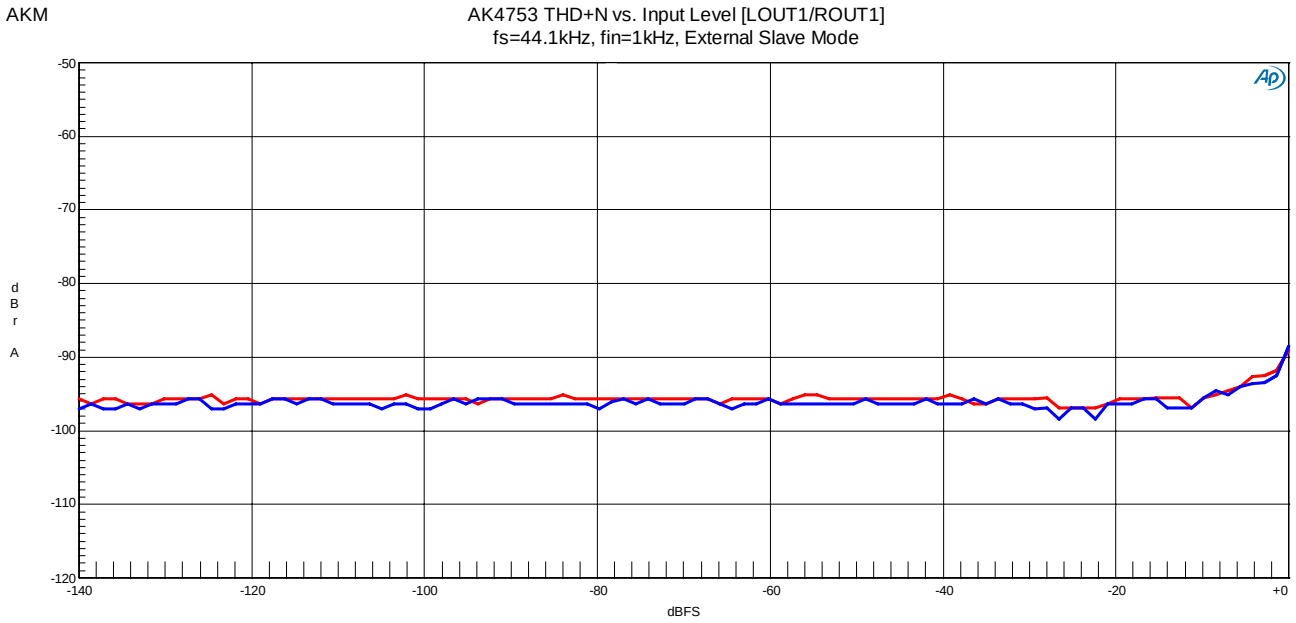


Figure 45. THD+N vs. Input Level

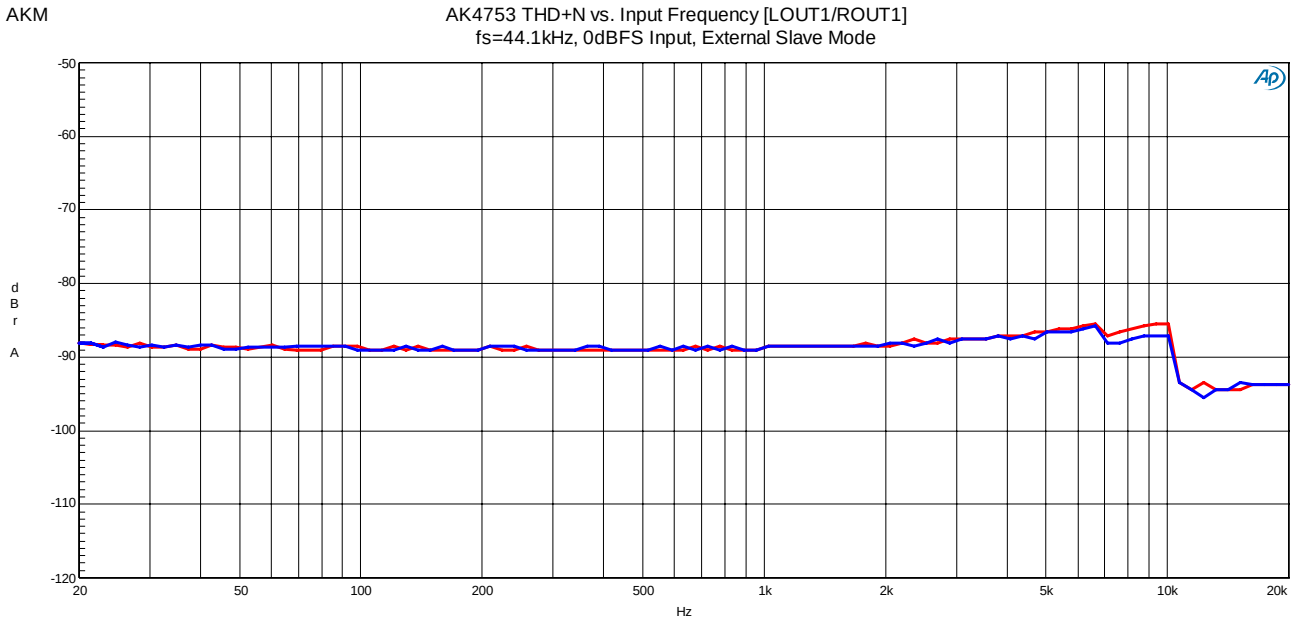


Figure 46. THD+N vs. Input Frequency

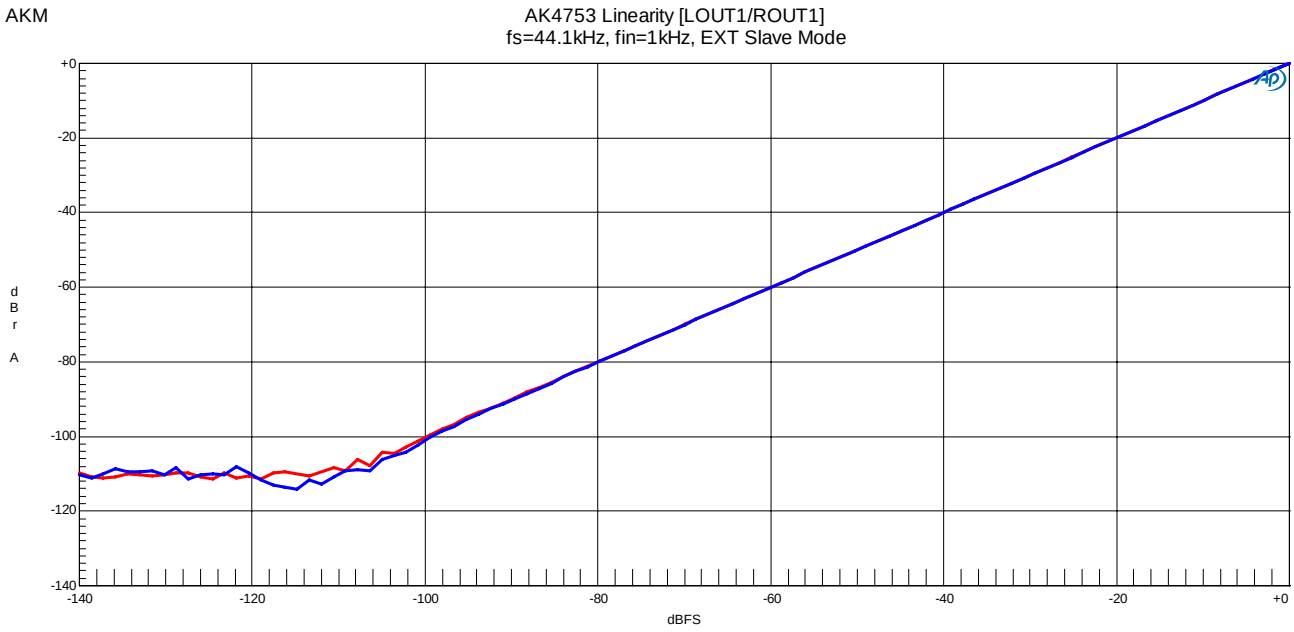


Figure 47. Linearity

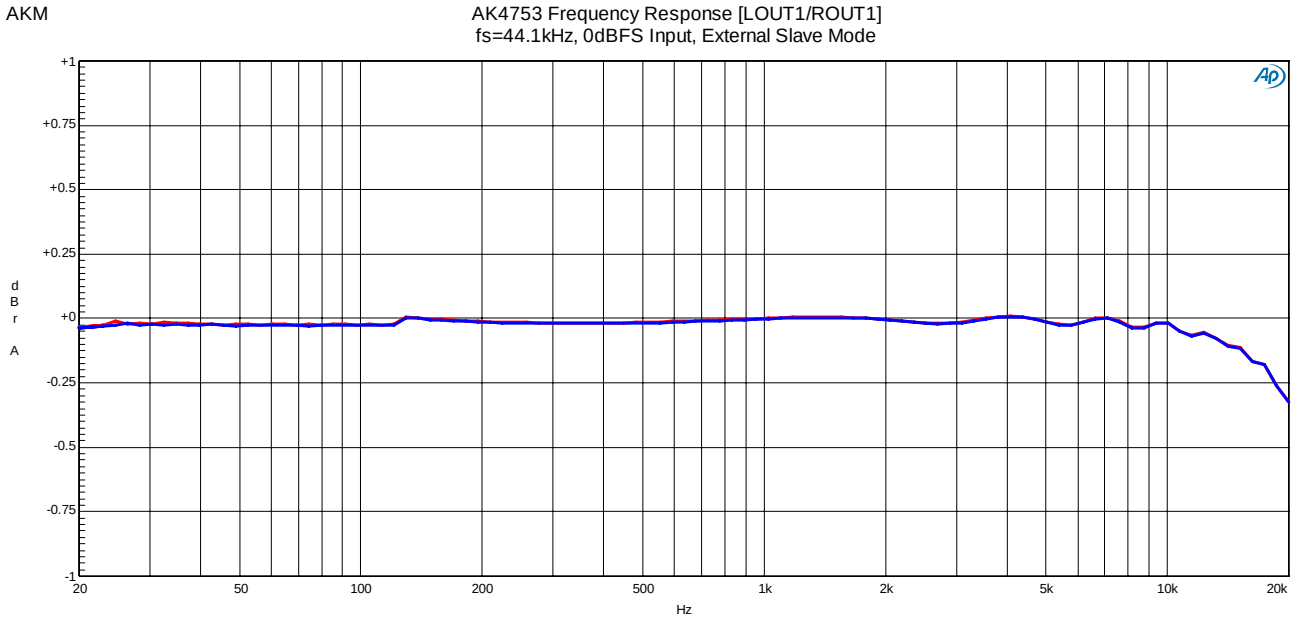


Figure 48. Frequency Response

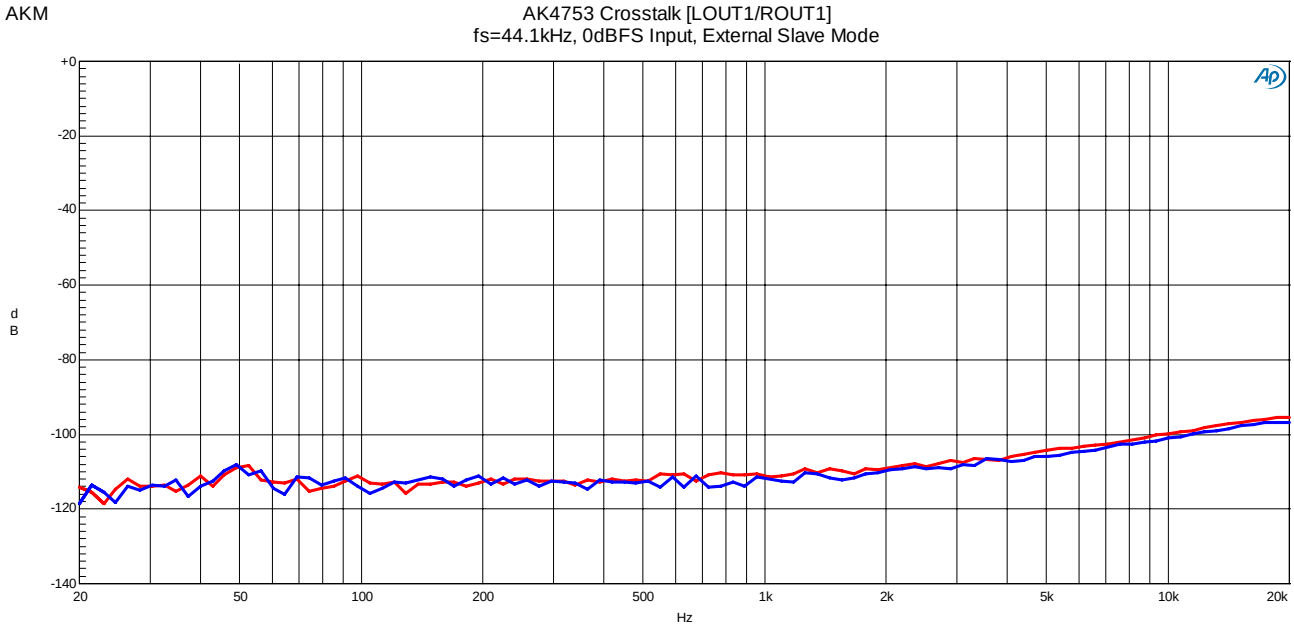


Figure 49. Crosstalk

PLOT DATA

1-b). DAC Differential [LOUT/ROUT pins]

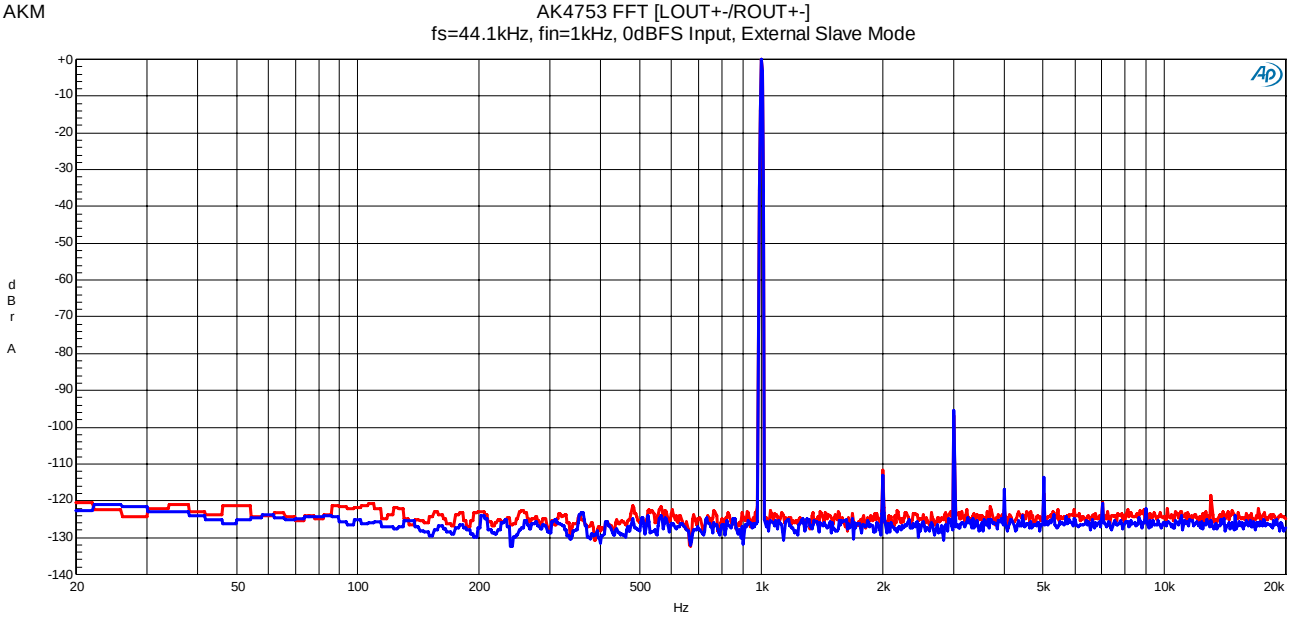


Figure 50. FFT(0dBFS Input)

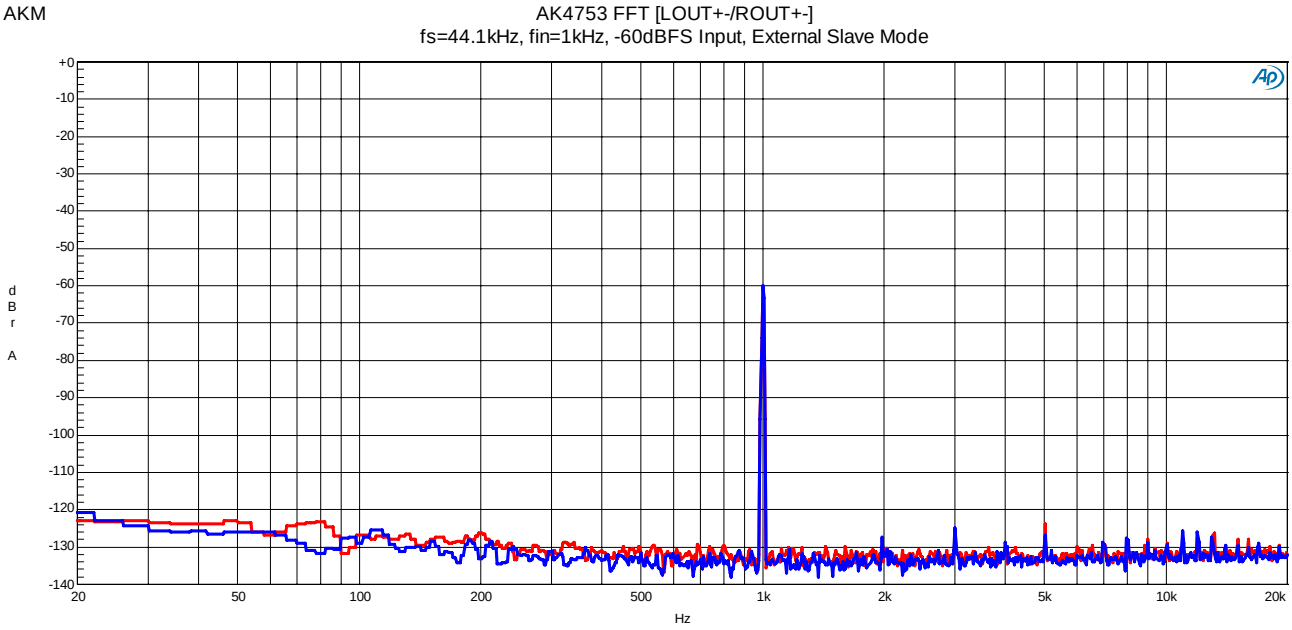


Figure 51. FFT(-60dB Input)

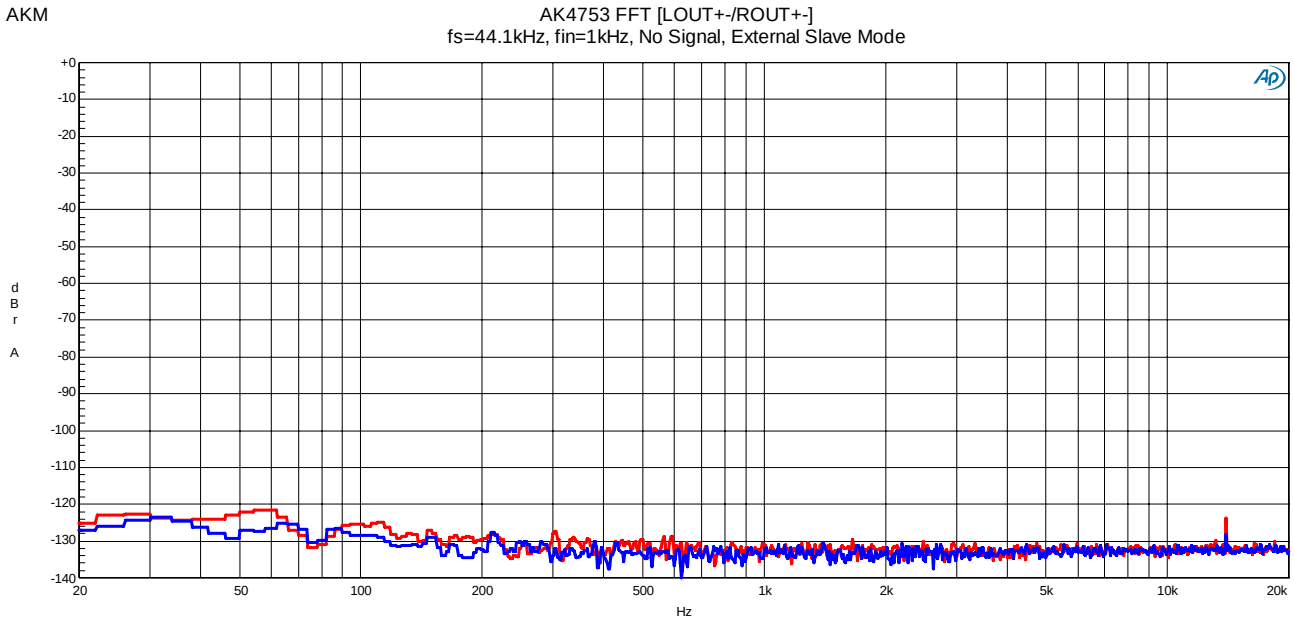


Figure 52. FFT(No Signal)

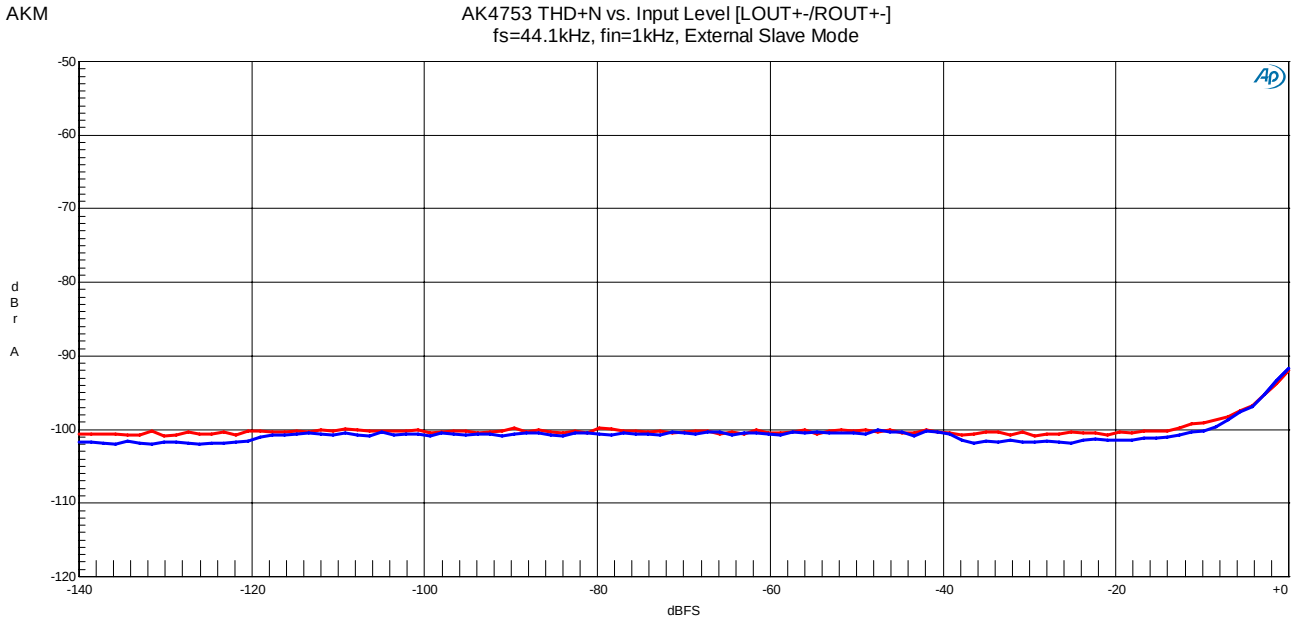


Figure 53. THD+N vs. Input Level

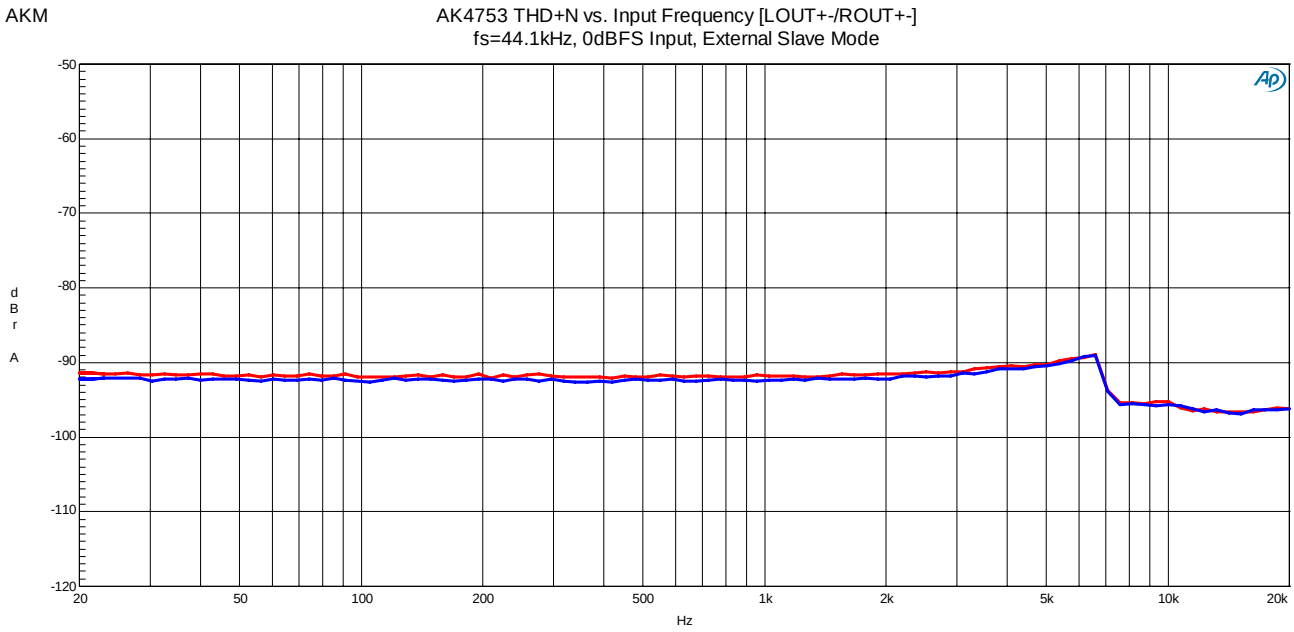


Figure 54. THD+N vs. Input Frequency

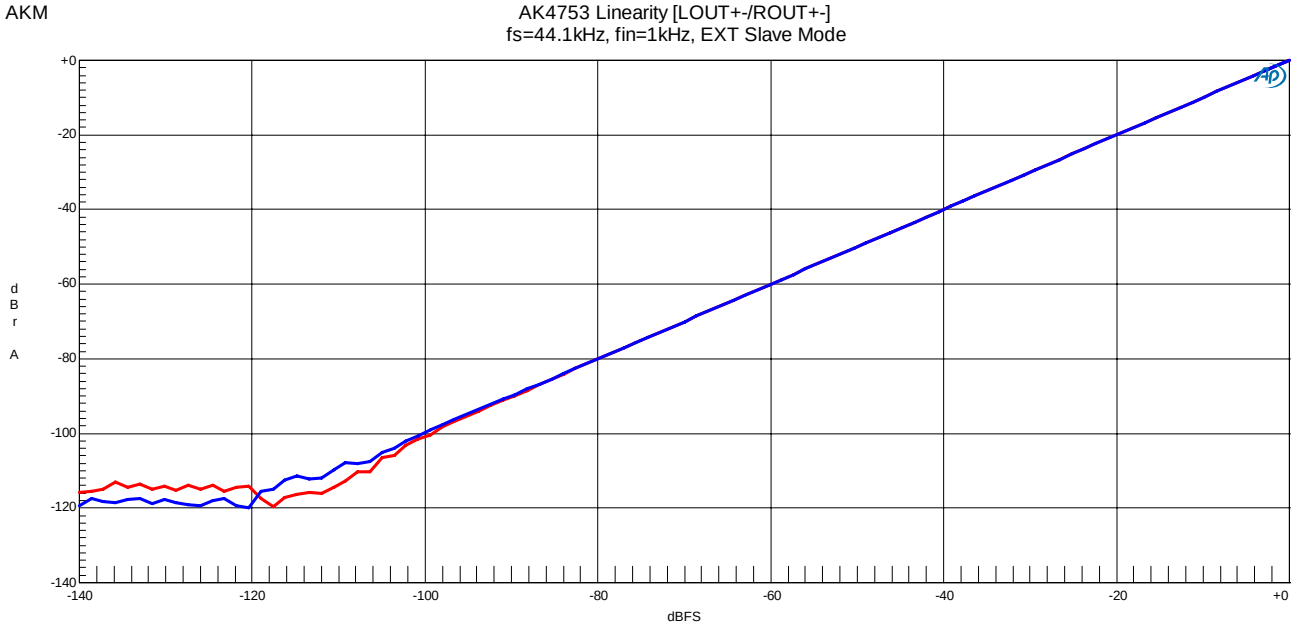


Figure 55. Linearity

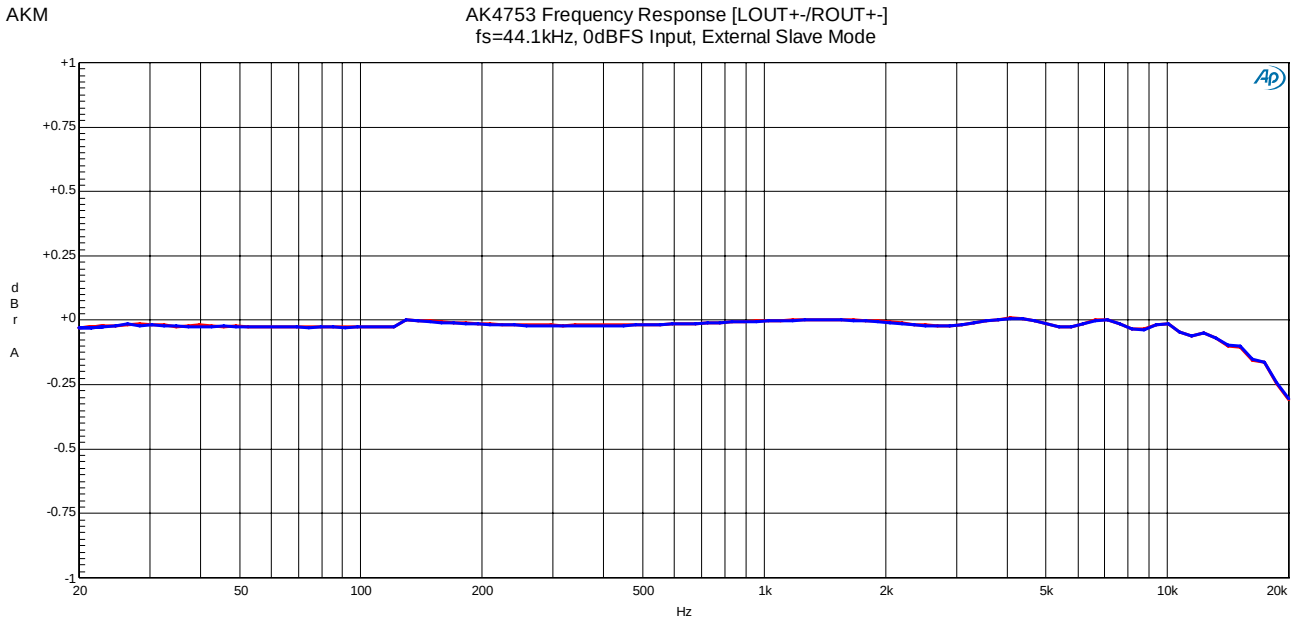


Figure 56. Frequency Response

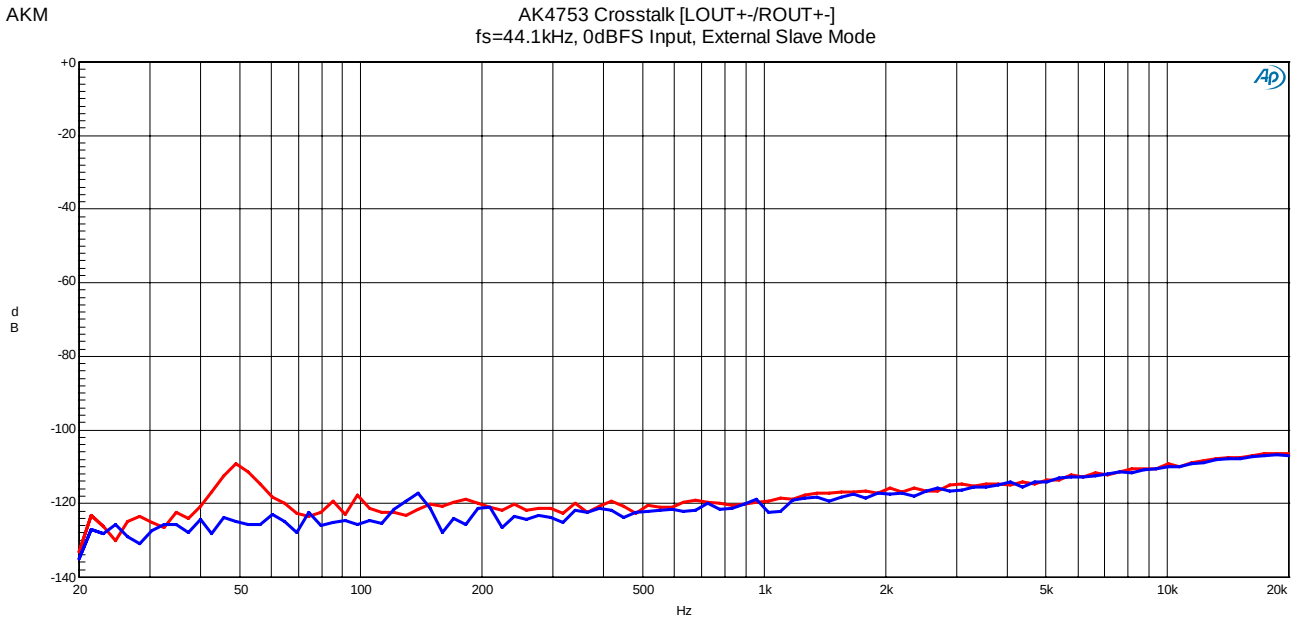


Figure 57. Crosstalk

PLOT DATA

2-a). ADC to DAC Single-ended [LOUT1/ROUT1 pins]

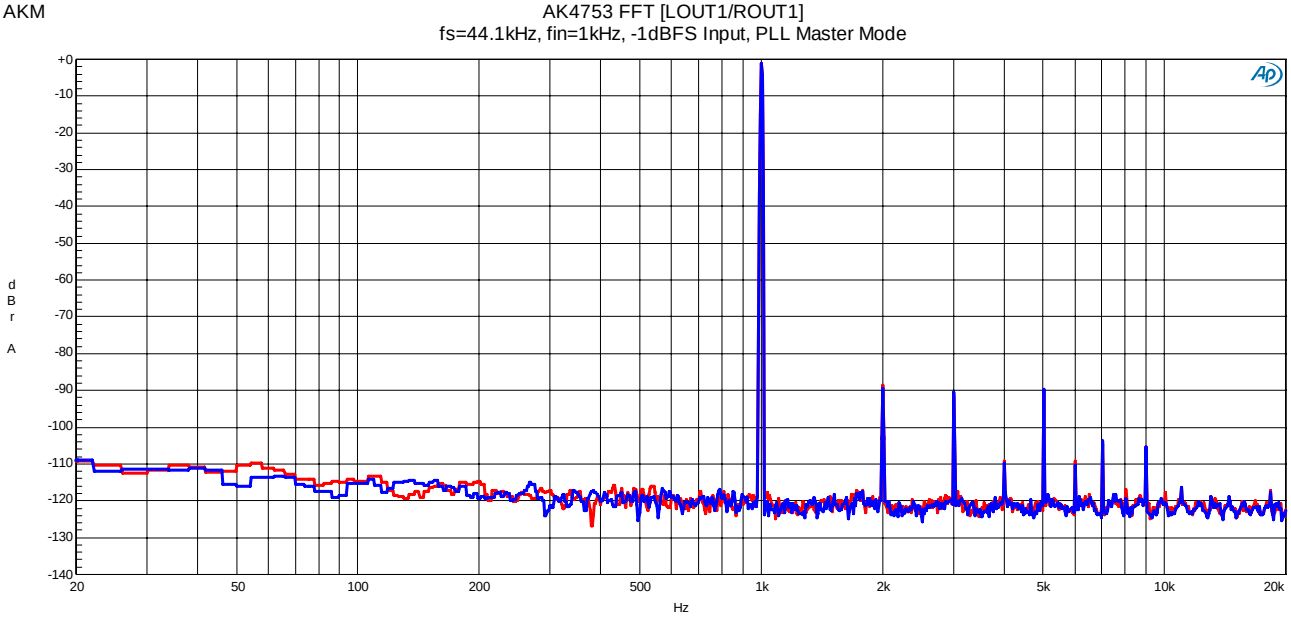


Figure 58. FFT(-1dBFS Input)

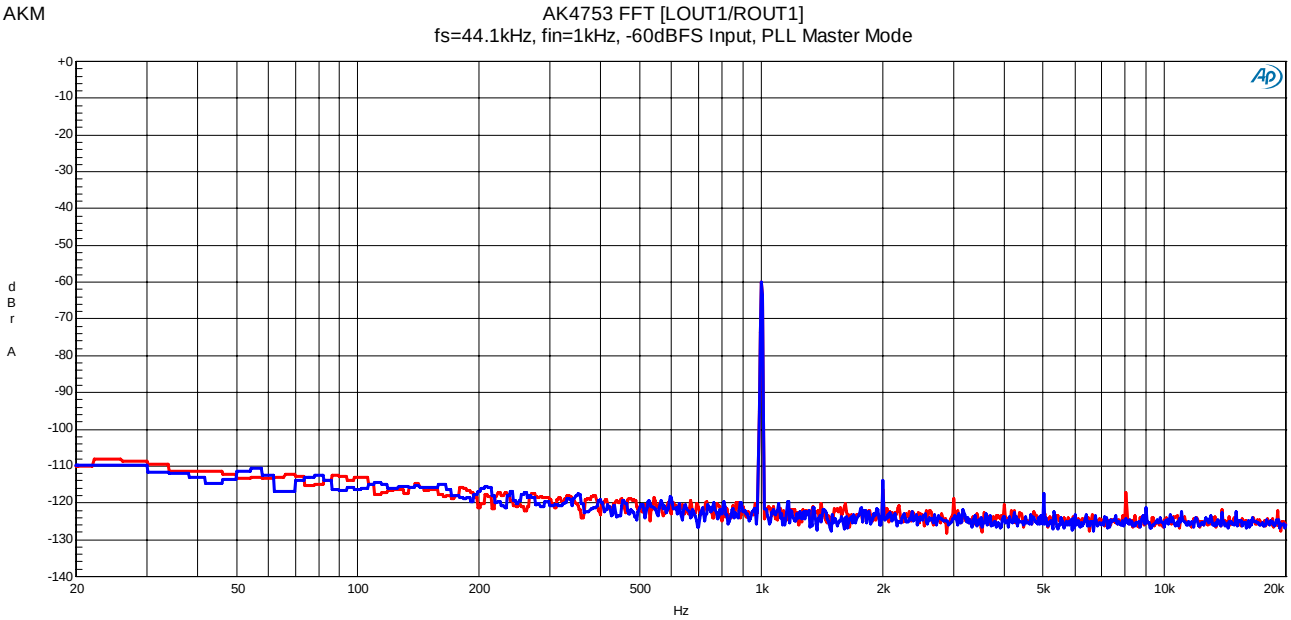


Figure 59. FFT(-60dBFS Input)

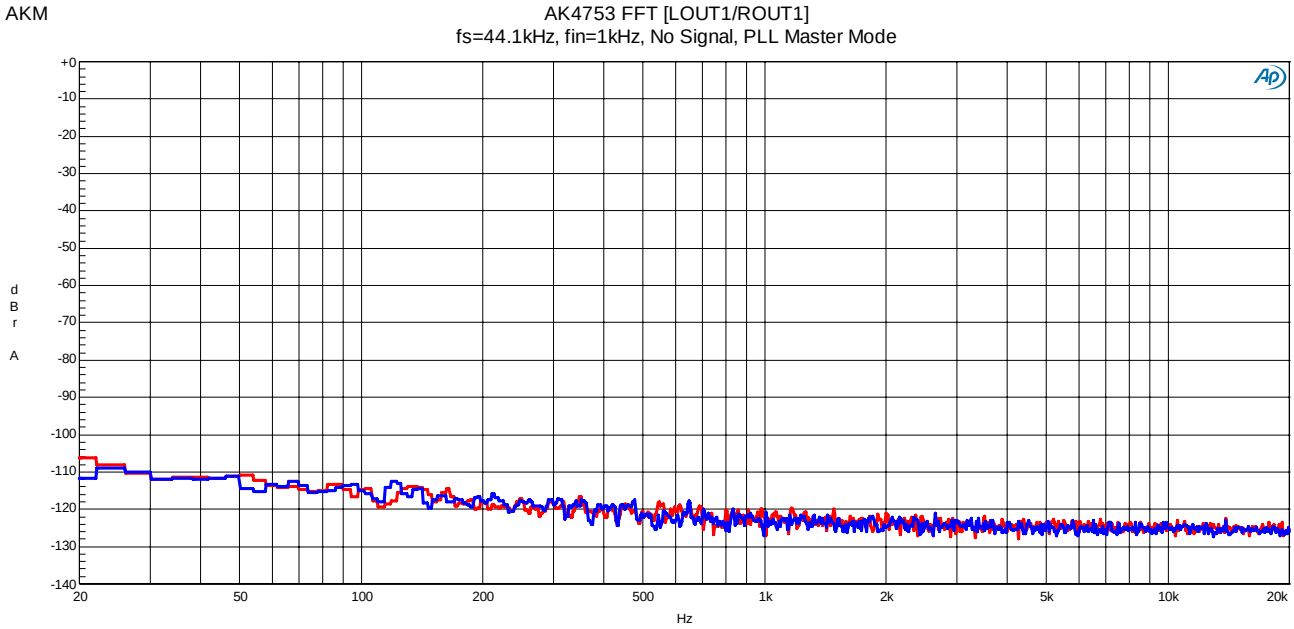


Figure 60. FFT(No Signal)

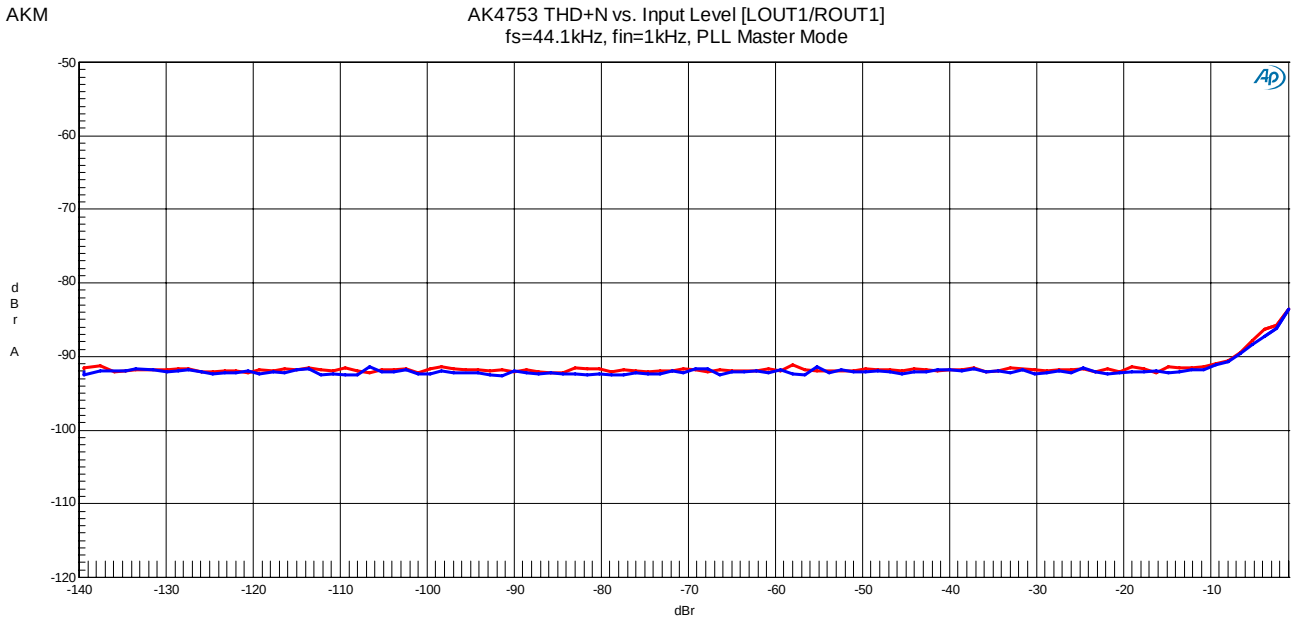


Figure 61. THD+N vs. Input Level

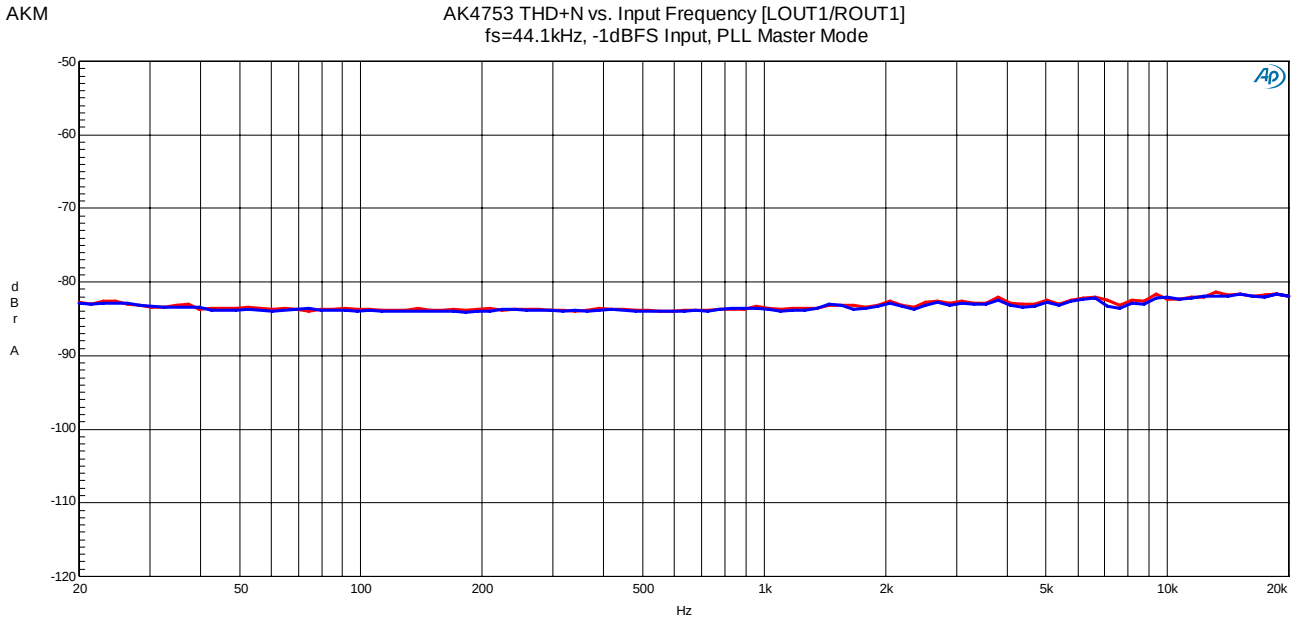


Figure 62. THD+N vs. Input Frequency

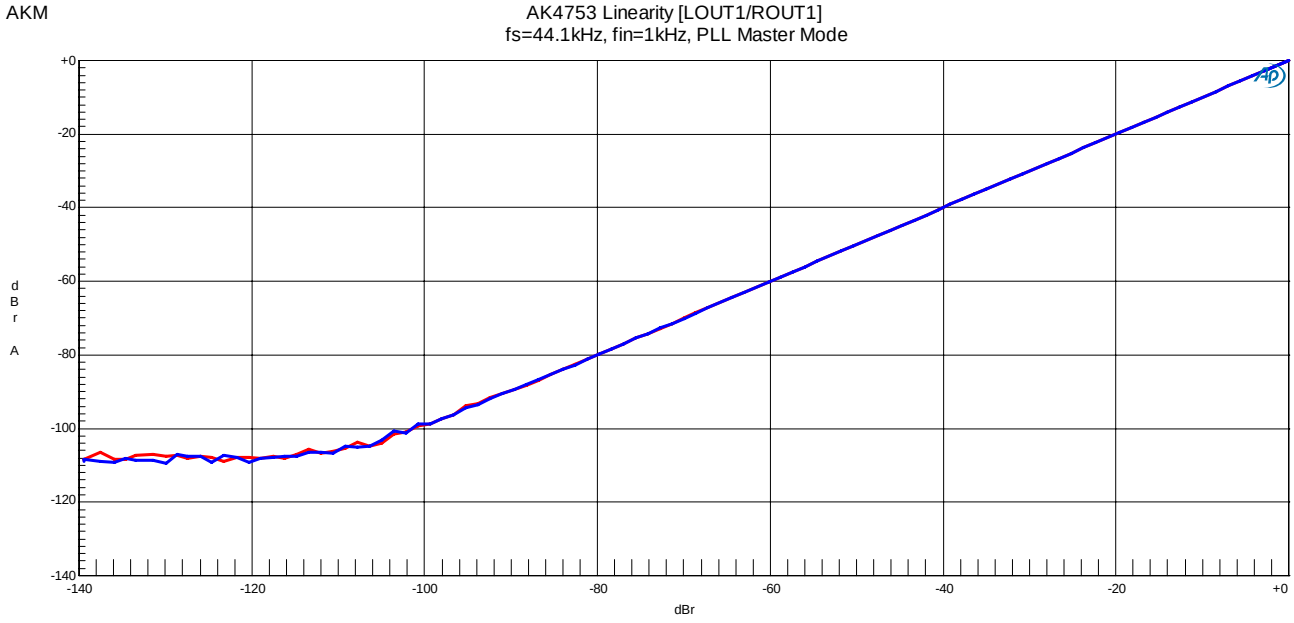


Figure 63. Linearity

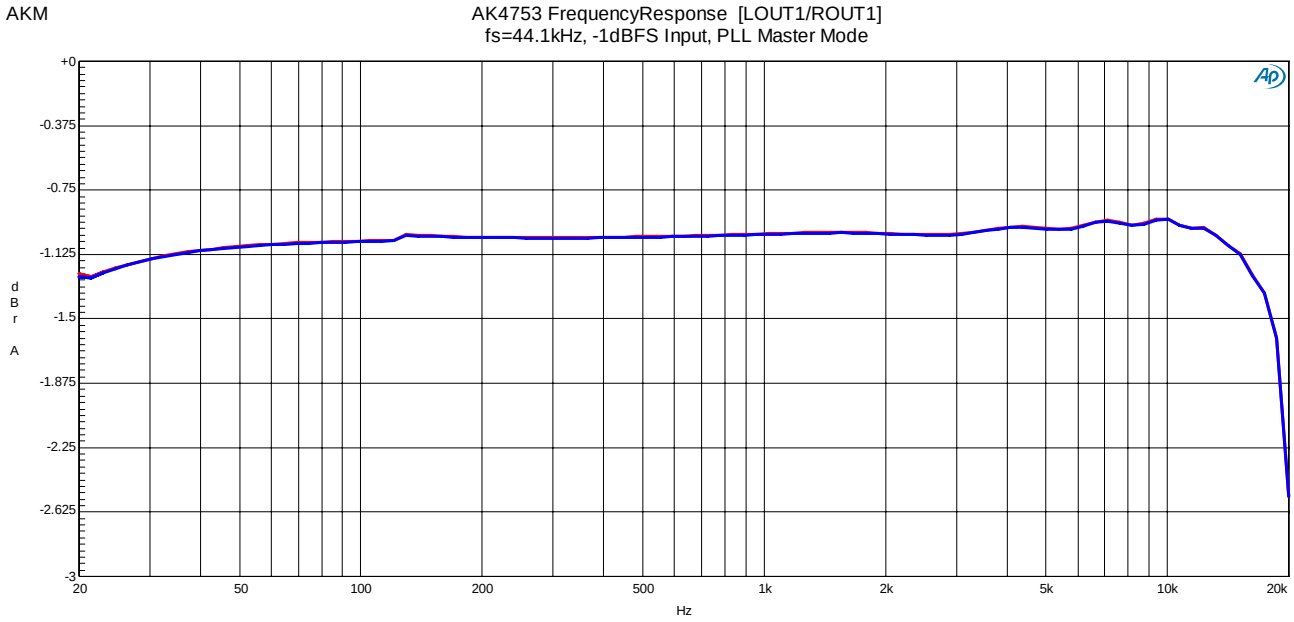


Figure 64. Frequency Response

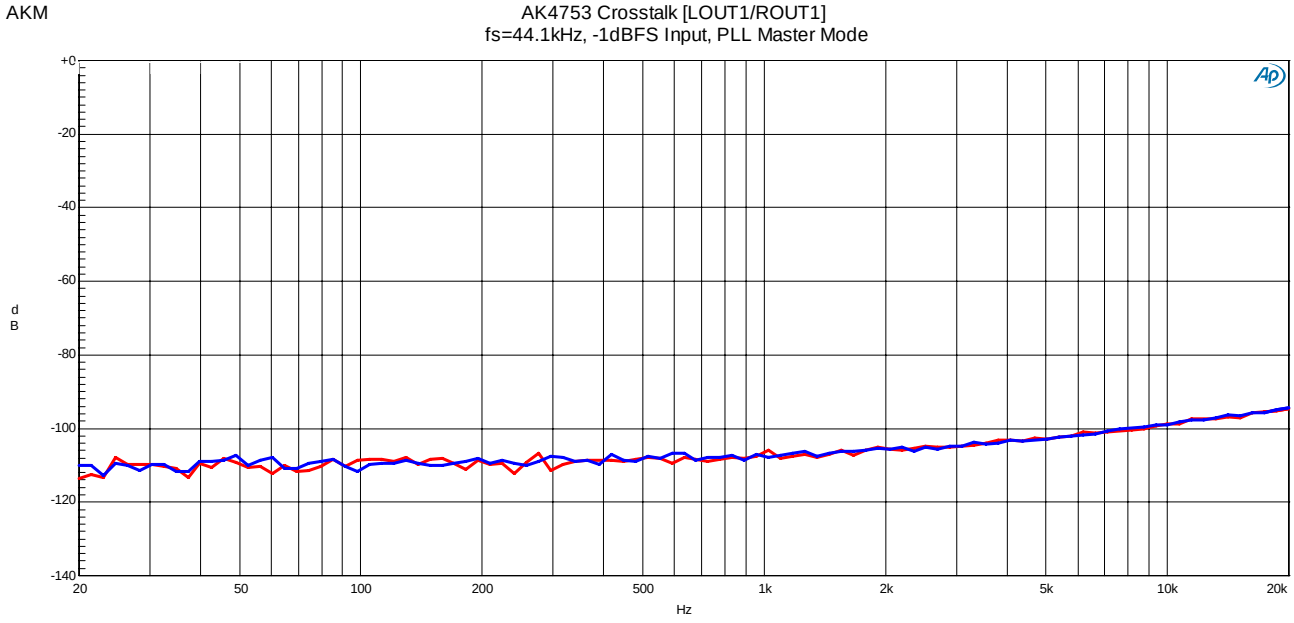


Figure 65. Crosstalk

PLOT DATA

2-b). ADC to DAC Differential [LOUT/ROUT pins]

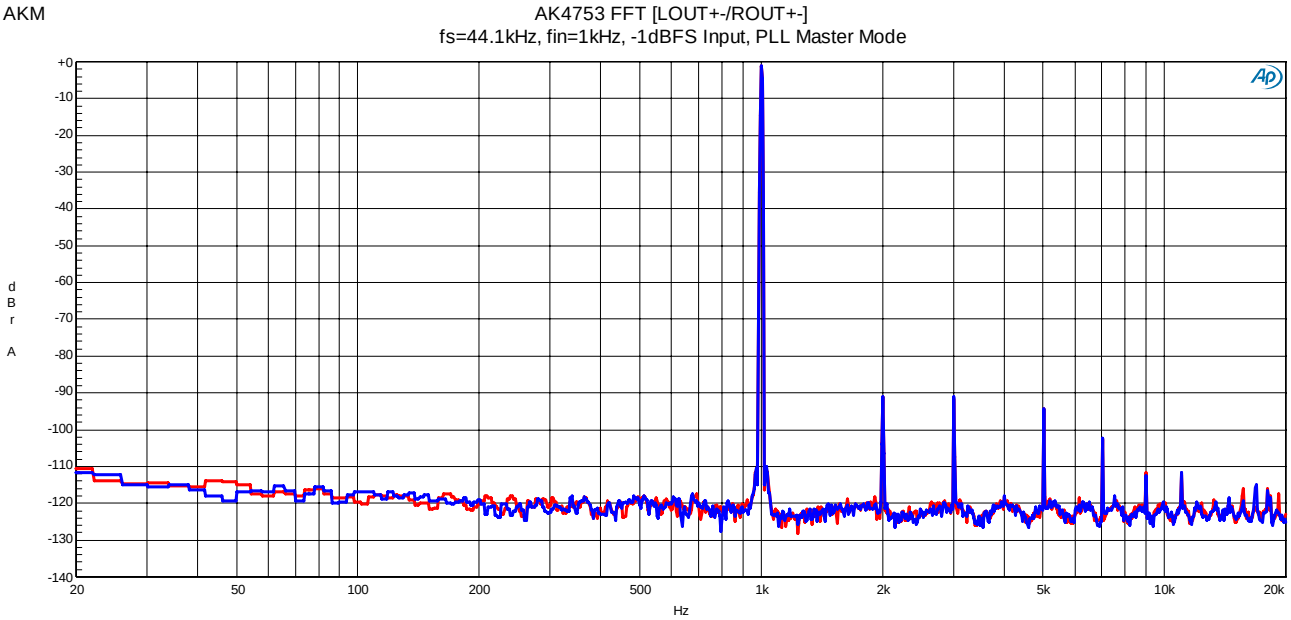


Figure 66. FFT(-1dBFS Input)

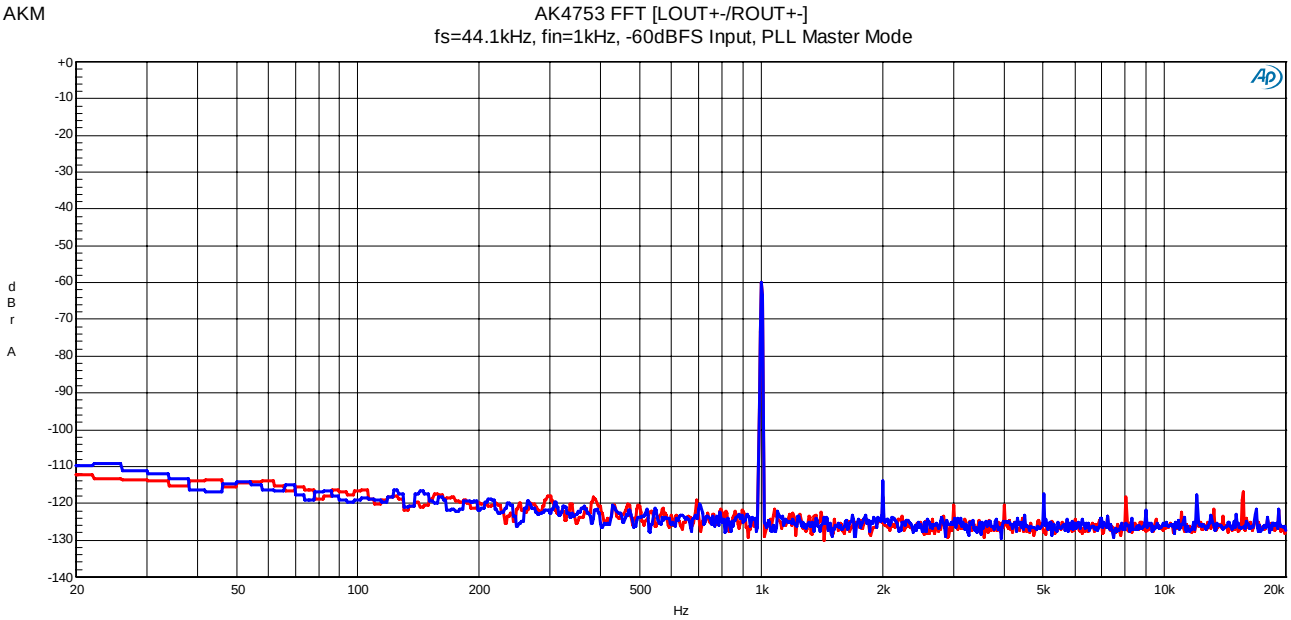


Figure 67. FFT(-60dBFS Input)

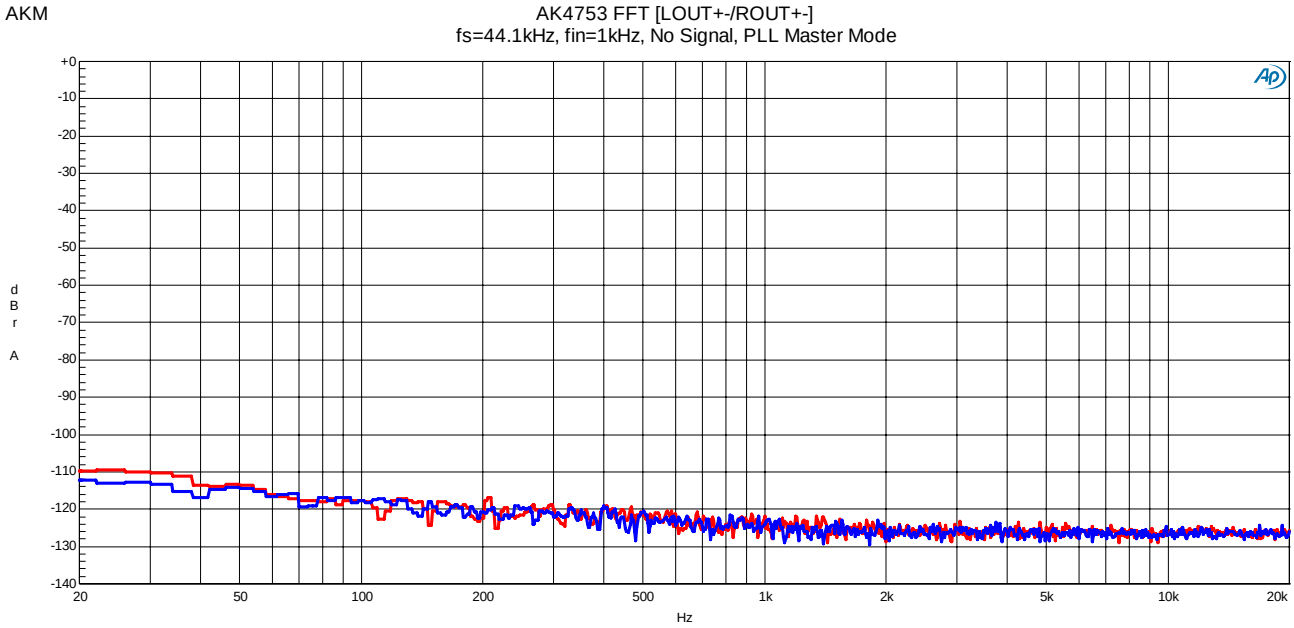


Figure 68. FFT(No Signal)

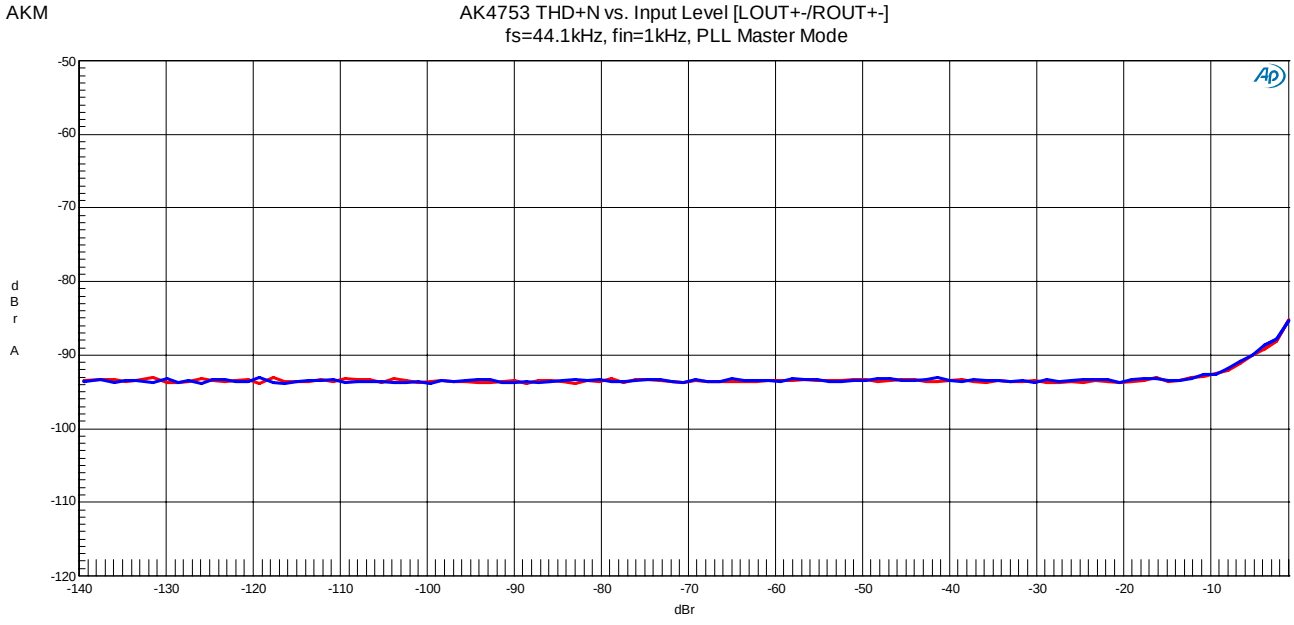


Figure 69. THD+N vs. Input Level

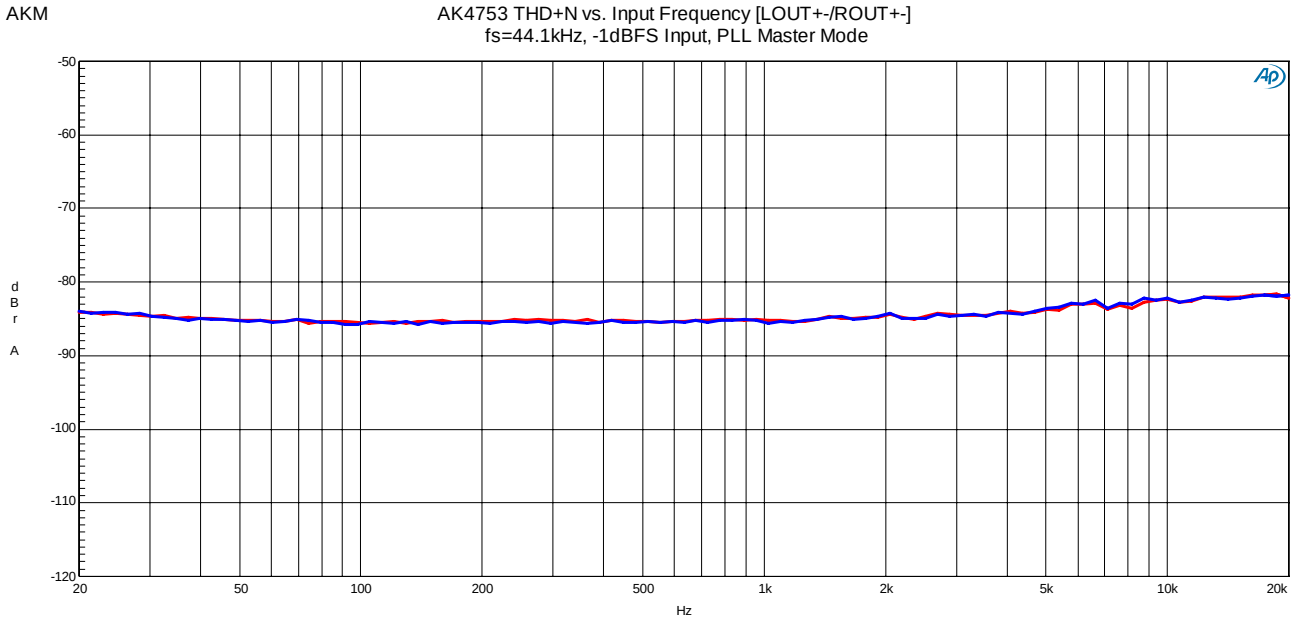


Figure 70. THD+N vs. Input Frequency

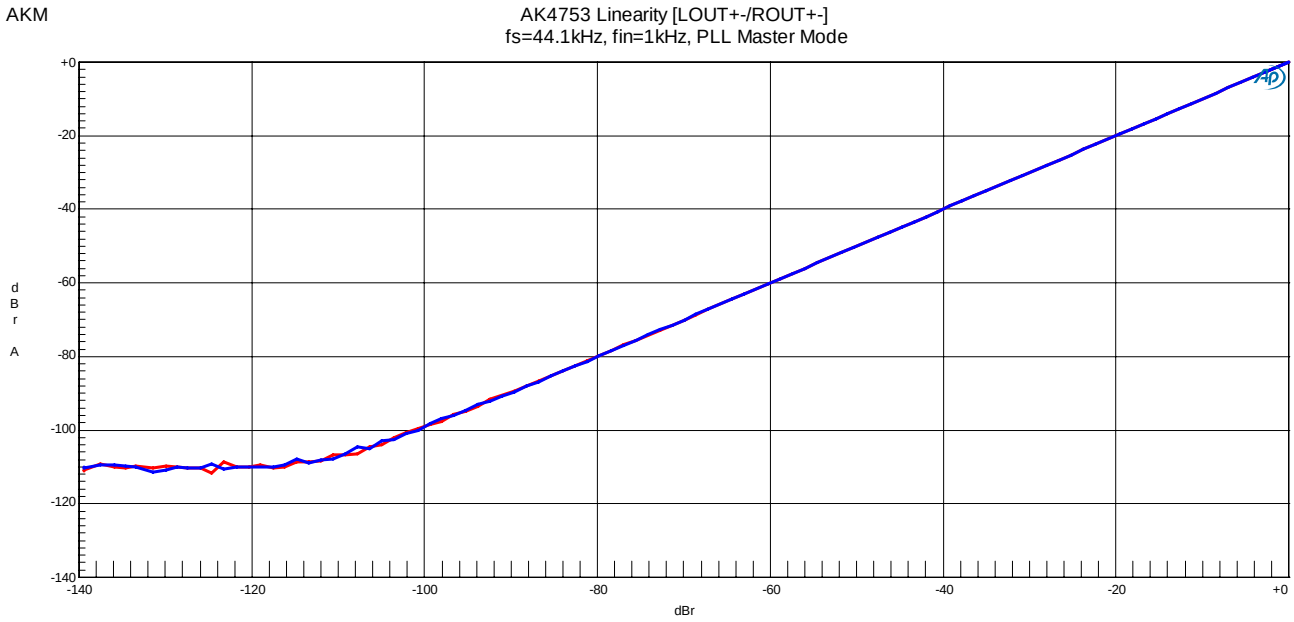


Figure 71. Linearity

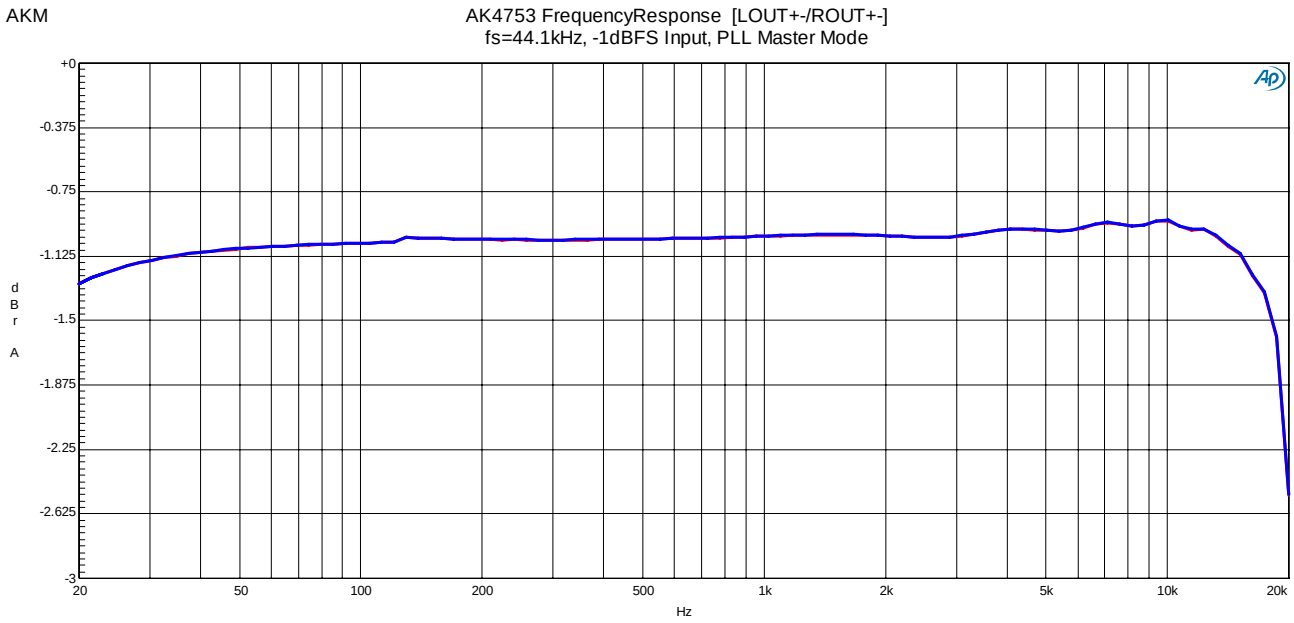


Figure 72. Frequency Response

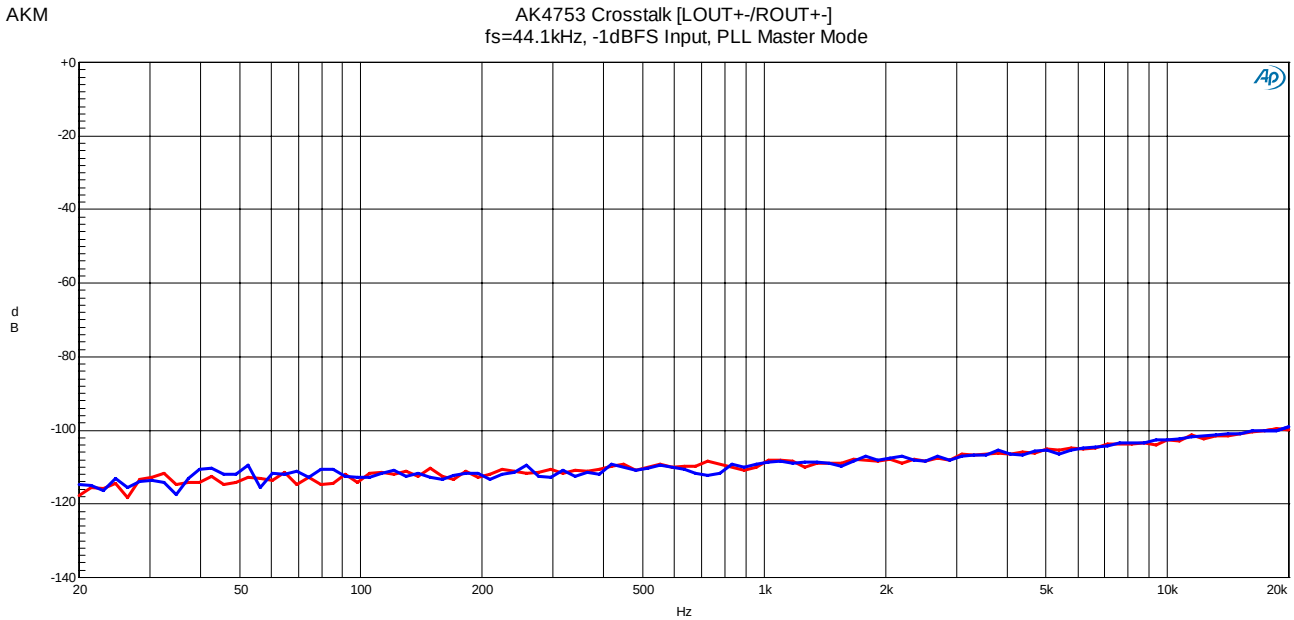
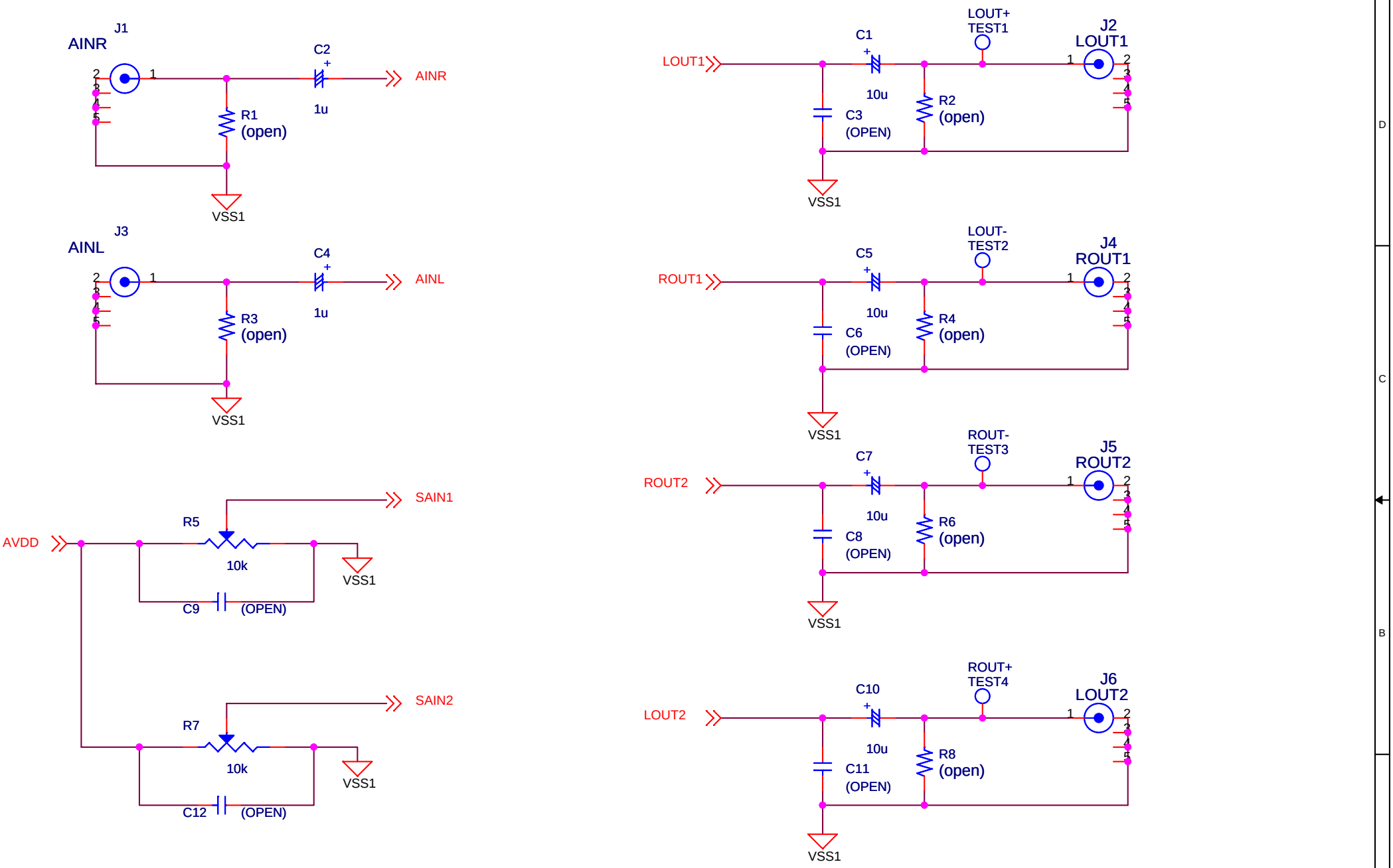


Figure 73. Crosstalk

Revision History

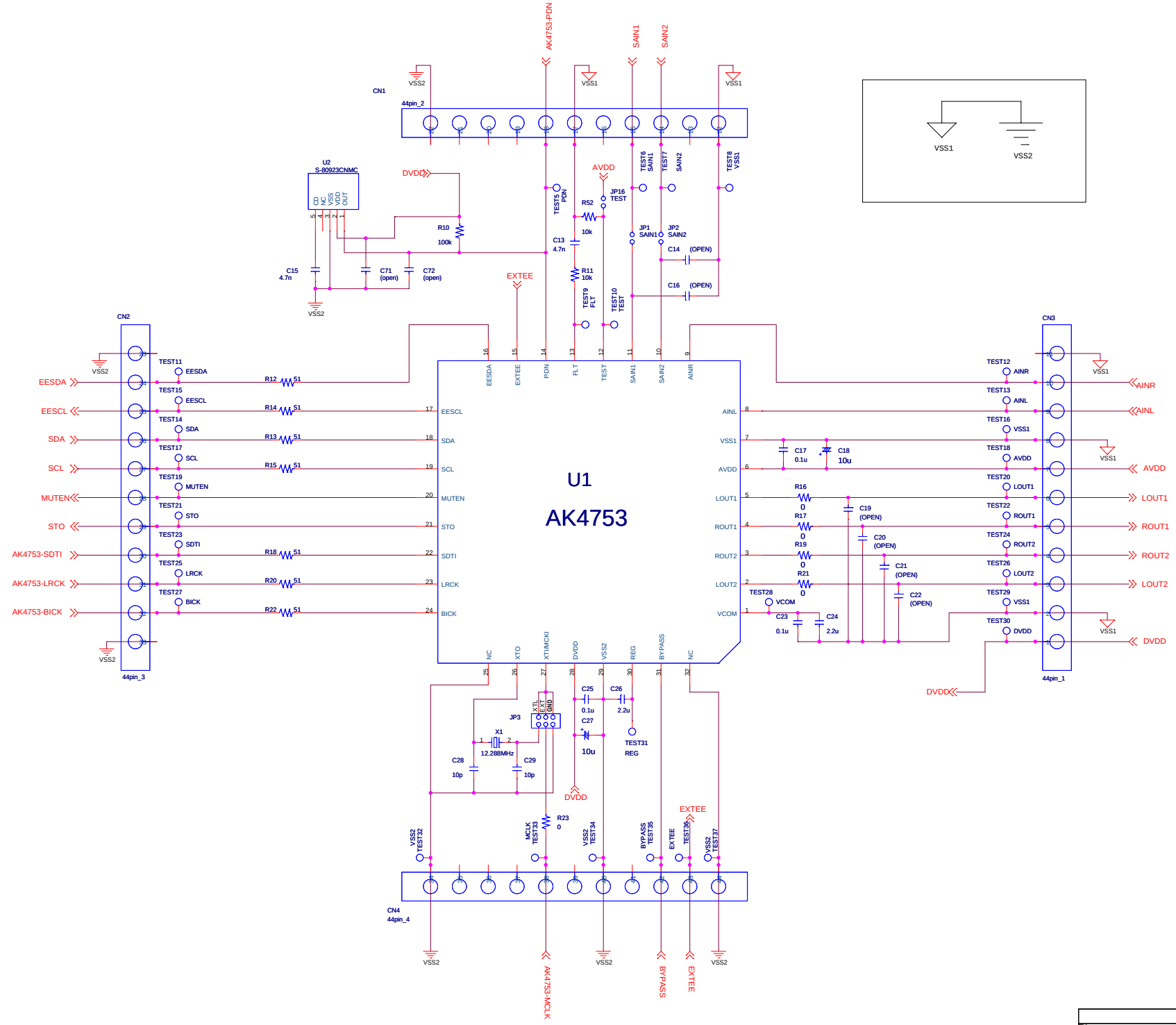
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
10/09/17	KM103900	0	First Edition	
10/09/30	KM103901	1	Description Change	Measurement results ware changed.
			Board Modification	Schematic circuit diagram was changed.



Title: AKD4753-A

Size: A | Document Number: AIN / AOUT | Rev: 1

Date: Wednesday, September 29, 2010 | Sheet 1 of 5



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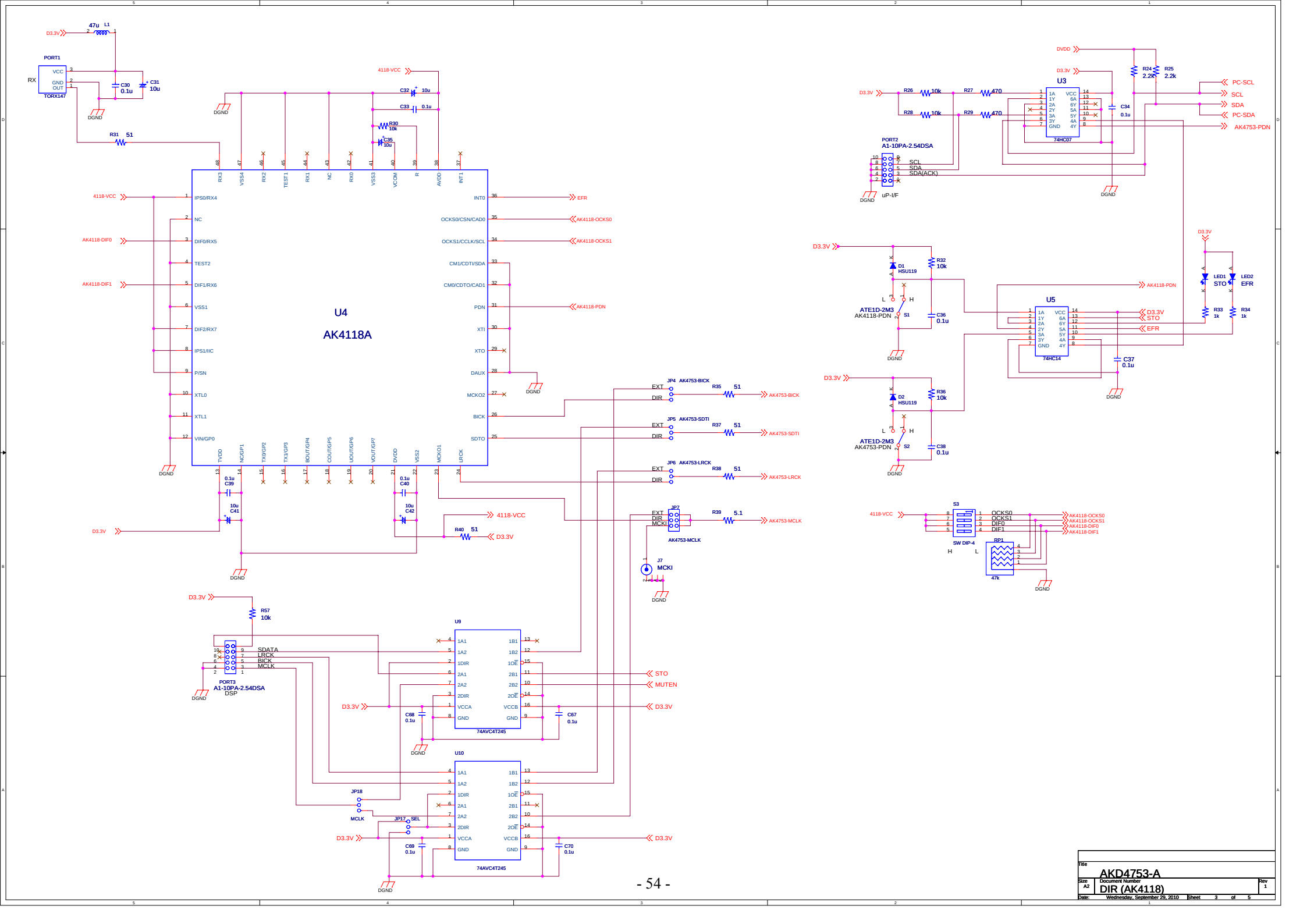
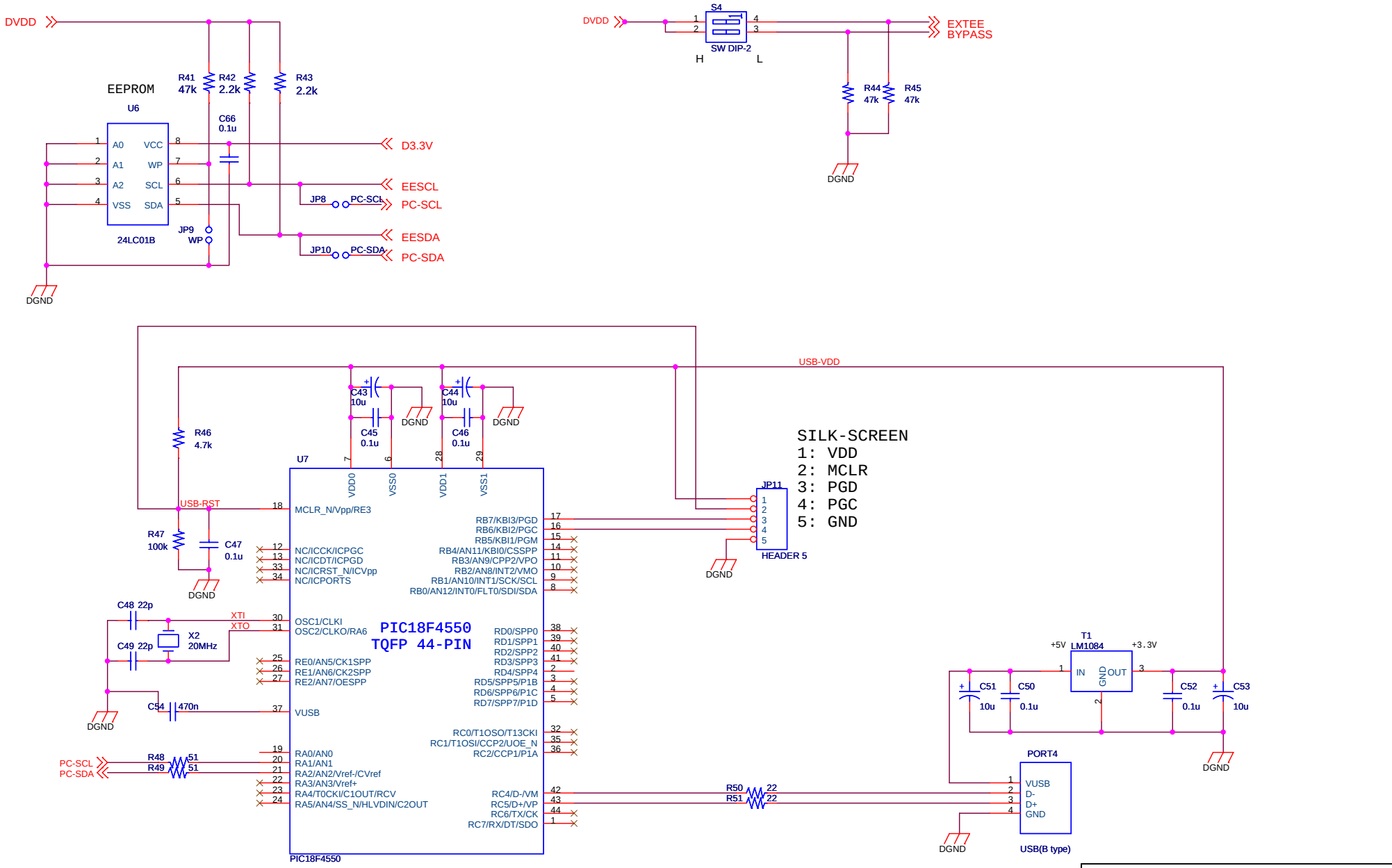
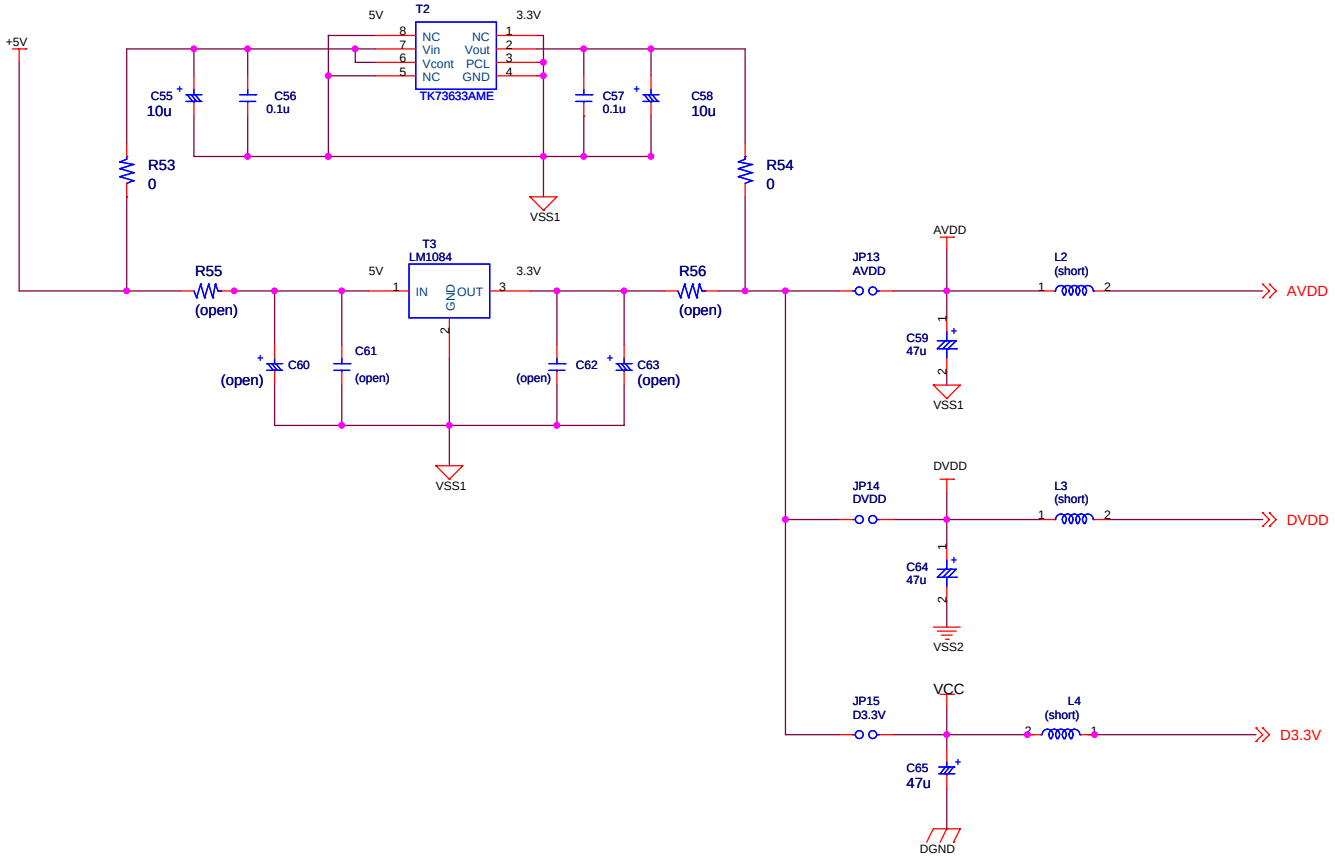
Size C	Document Number AK4753	Rev 1
Date: Wednesday, September 29, 2010	Sheet 2 of 5	

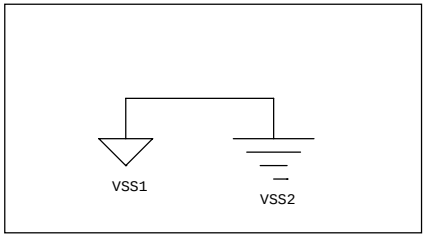


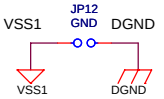
Title	AKD4753-A	
Size A2	Document Number DIR (AK4118)	Rev 1
Date: Wednesday, September 29, 2010	Sheet 3 of 5	

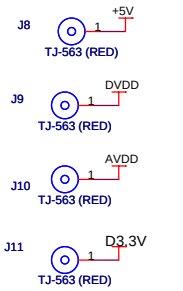


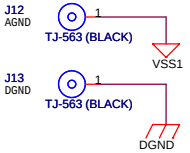
Title	AK4753-A	
Size B	Document Number EEPROM	Rev 1
Date: Wednesday, September 29, 2010	Sheet 4 of 5	











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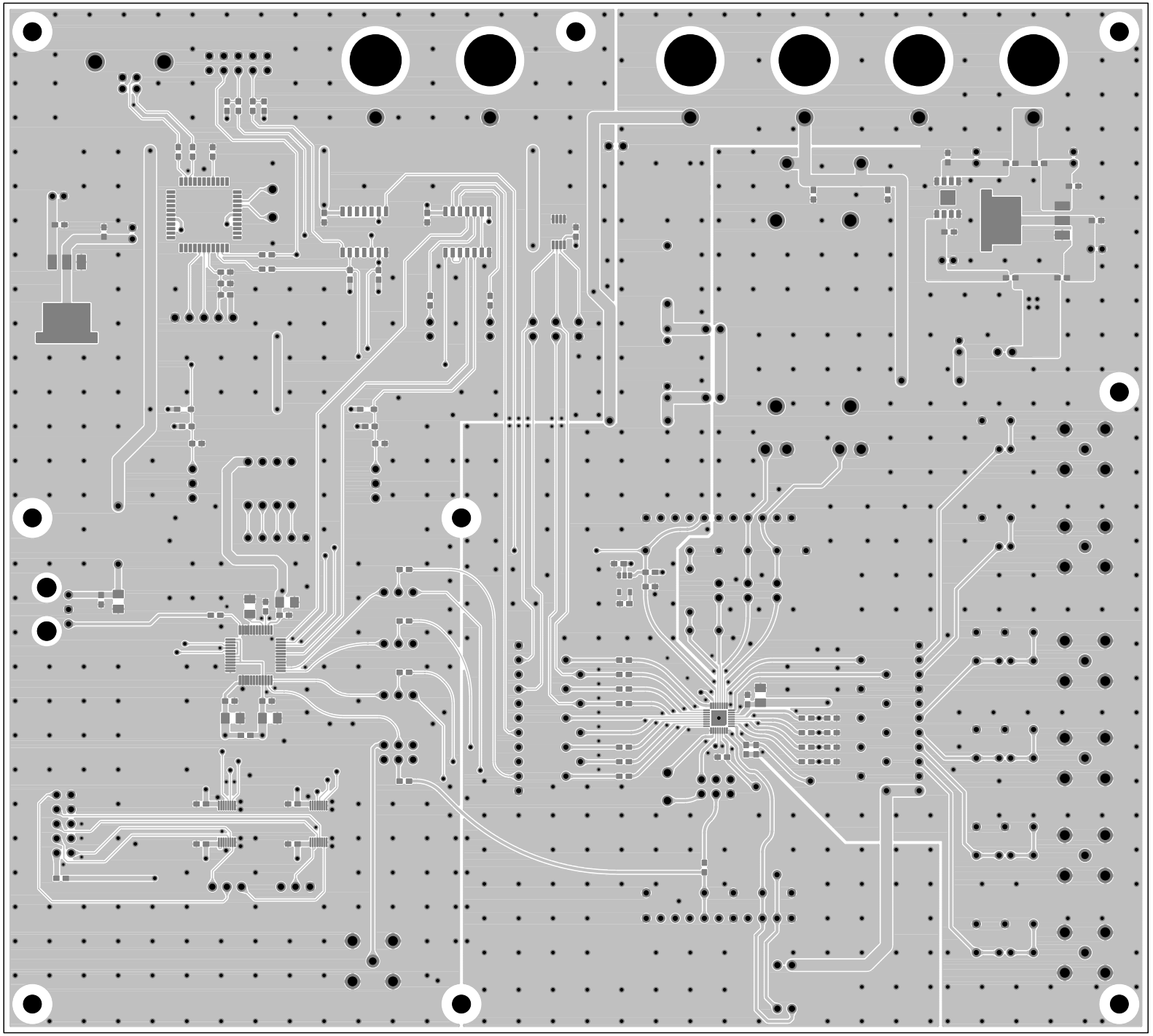
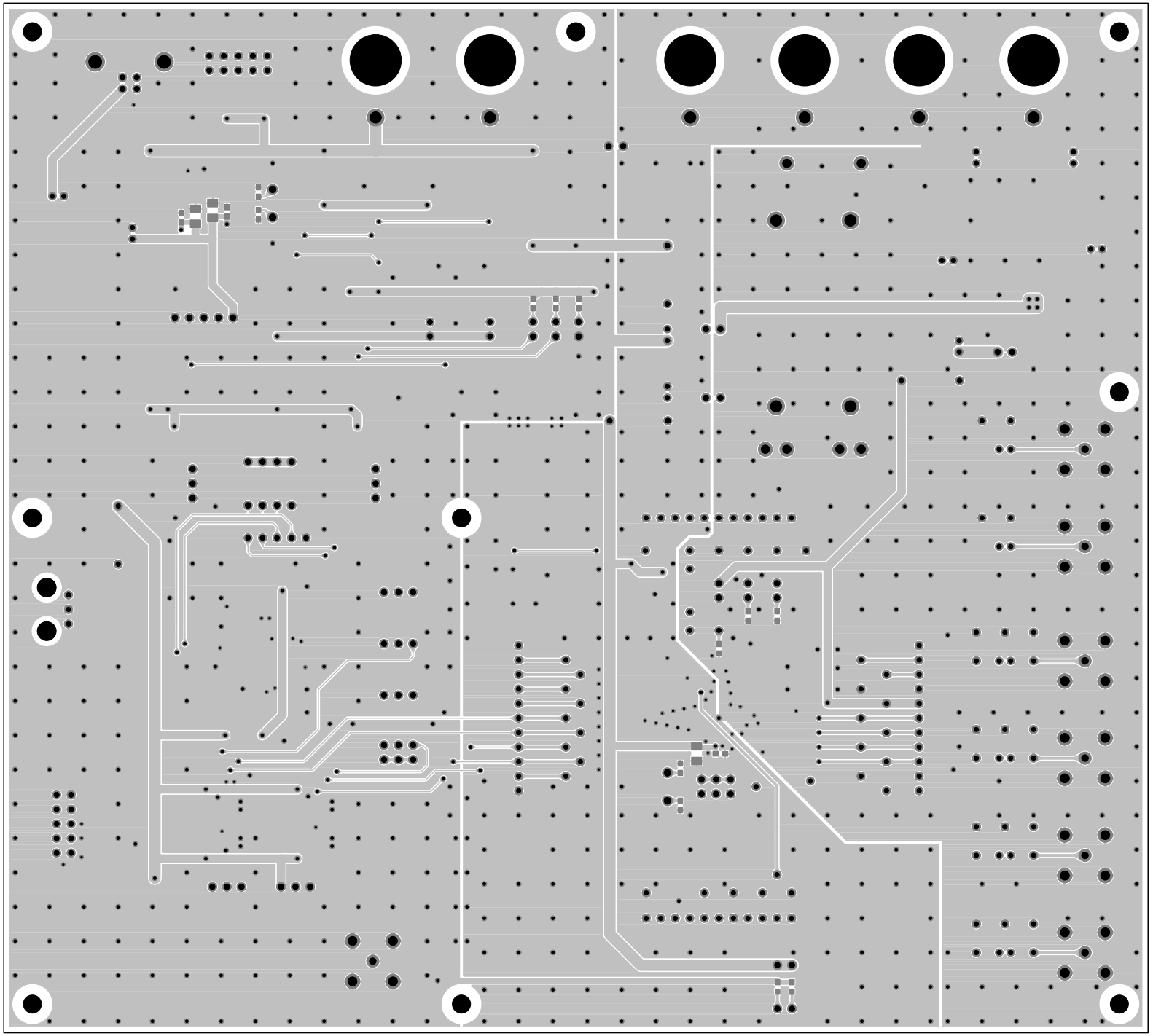
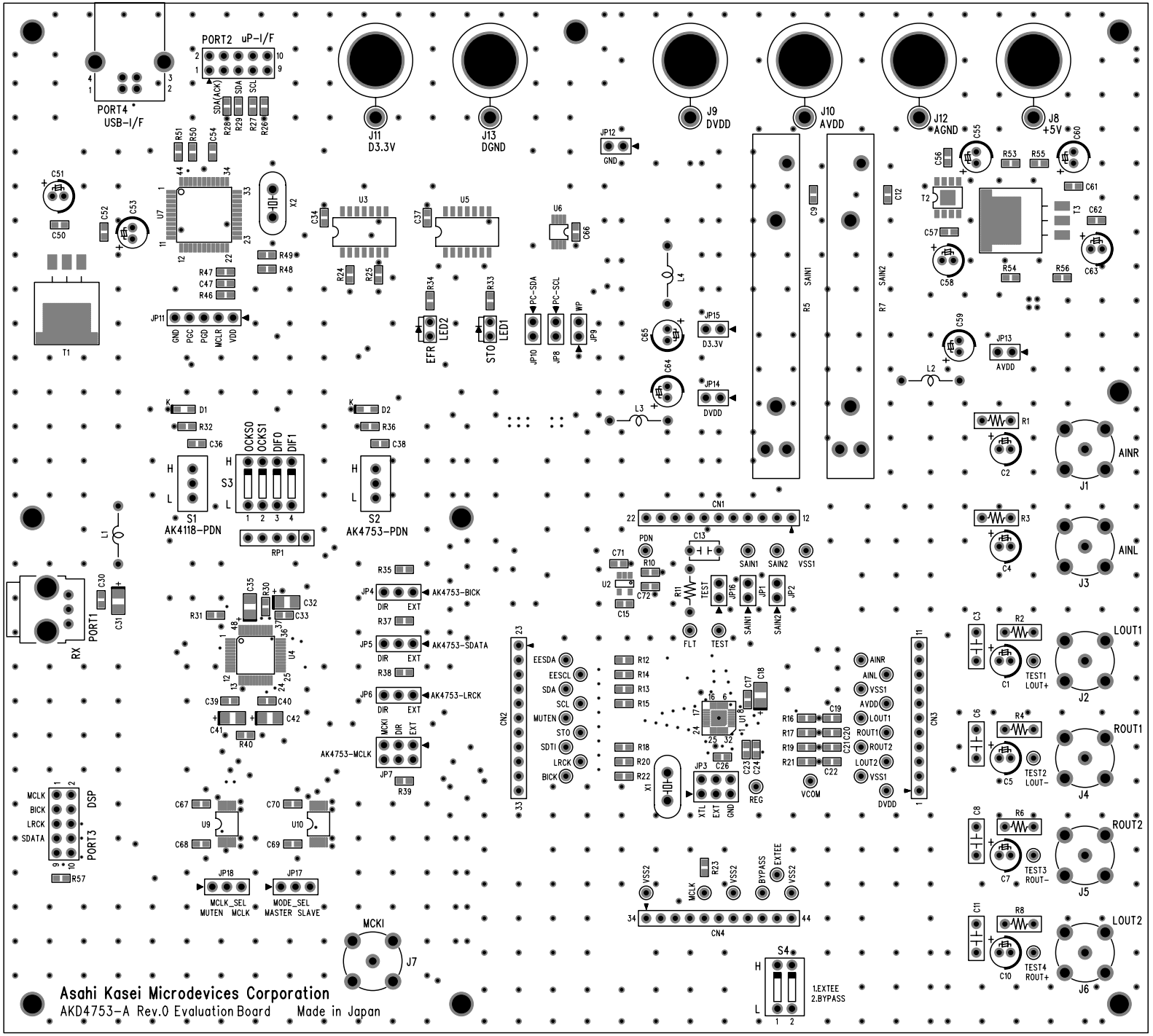
Size A3	Document Number POWER	Rev 1
Date: Wednesday, September 29, 2010	Sheet 5 of 5	



AKD4753-A MAIN Lay1



AKD4753-A MAIN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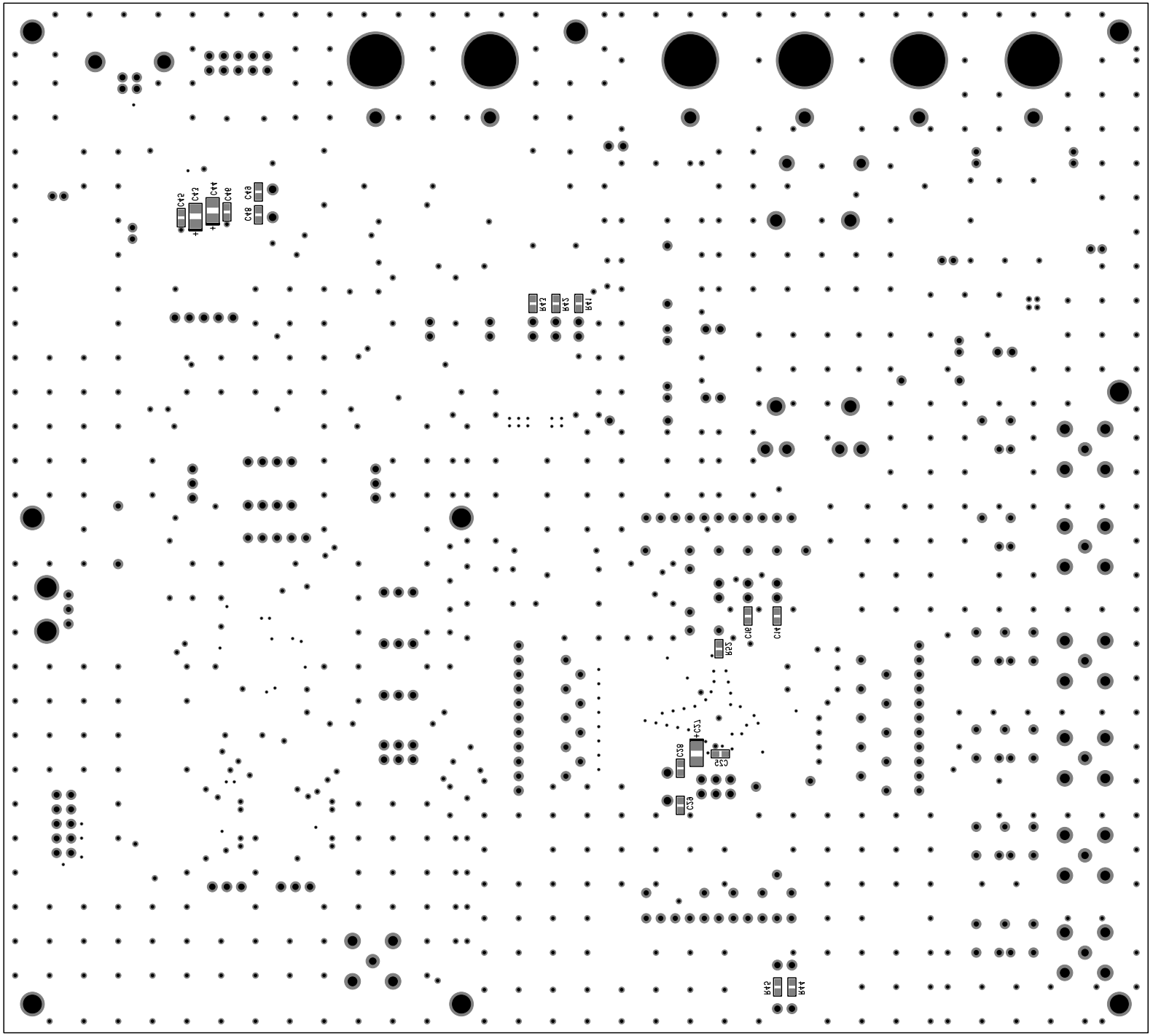
PORT4 USB-I/F
J11 D3.3V
J13 DGND
J9 DVDD
J10 AVDD
J12 AGND
J8 +5V
S1 AK4118-PDN
S2 AK4753-PDN
S3
OCKS0 OCKS1 DIF0 DIF1
RP1
AK4753-BICK
AK4753-SDATA
AK4753-LRCK
AK4753-MCLK
PORT1
PORT3 DSP
MCLK BICK LRCK SDATA
JP18 MCLK_SEL MUTEN MCLK
JP17 MODE_SEL MASTER SLAVE
MCKI J7
CN1
CN2
CN3
CN4
AINR J1
AINL J3
LOUT1 J2
ROUT1 J4
ROUT2 J5
LOUT2 J6
S4 1.EXTEE 2.BYPASS
Asahi Kasei Microdevices Corporation
AKD4753-A Rev.0 Evaluation Board Made in Japan


C42
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R44