Low Power Multiclock Generator with XO
AK8137A

Features

- 25MHz Crystal Input
- One 25MHz-Reference Output
- Selectable Clock out Frequencies:
  - 100, 133, 166, 200MHz
  - 96MHz
  - 100MHz
  - 25MHz
- Low Jitter Performance
  - Cycle to Cycle Jitter:
    85 psec at CPU_C
    125 psec at SATA_C
    250 psec at UBS_C
- Low Current Consumption:
  37mA (Typ.) at 3.3V
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85°C
- Package:
  20-pin SSOP (Lead free, Halogen free)

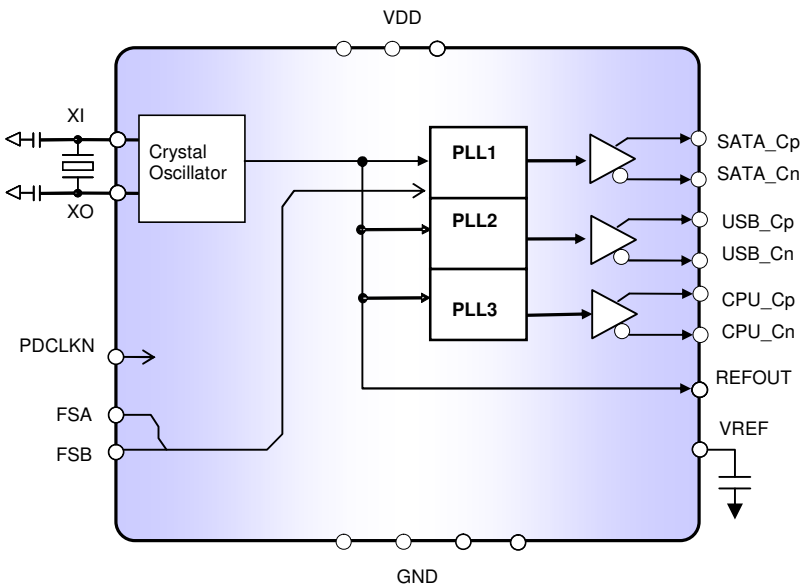
Description

The AK8137A is a member of AKM's low power multi clock generator family designed for a feature rich DTV or STB, requiring a range of system clocks with high performance. The AK8137A generates different frequency clocks from a 25 MHz crystal oscillator and provides them to up to four outputs configured by pin-setting. PLL in AK8137A are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8137A is available in a 20-pin SSOP package.

Applications

- Set-Top-Boxes

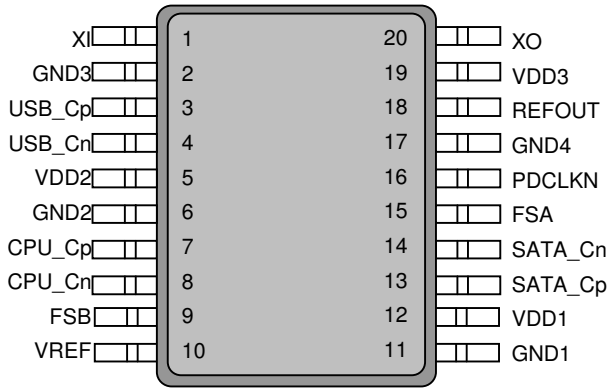
Block Diagram



AK8137A Multi Clock Generator

Pin Descriptions

Package: 20-Pin SSOP(Top View)



Pin No.	Pin Name	Pin Type	Description
1	XI	AI	Crystal connection, Connect to 25.000MHz crystal
2	GND3	PWR	Ground 3
3	USB_Cp	DO	96MHz Clock output for USB
4	USB_Cn	DO	
5	VDD2	PWR	Power Supply 2
6	GND2	PWR	Ground 2
7	CPU_Cp	DO	Clock output for CPU See Table 1 for its selectable frequency
8	CPU_Cn	DO	
9	FSB	DI	CPU Clock select 360kΩ internal pull-up.
10	VREF	AO	VREF Pin. Connect 1uF capacitor.
11	GND1	PWR	Ground 1
12	VDD1	PWR	Power Supply 1
13	SATA_Cp	DO	100MHz Clock output for SATA
14	SATA_Cn	DO	
15	FSA	DI	CPU Clock select 360kΩ internal pull-up.
16	PDCLKN	DI	Clock Output Control H: Power Down Disable, L: Power Down Enable 500kΩ internal pull-up.
17	GND4	PWR	Ground4
18	REFOUT	DO	Reference Clock Output 25.000MHz Crystal
19	VDD3	PWR	Power Supply 3
20	XO	AO	Crystal connection, Connect to 25.000MHz crystal

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8137A	8137A	Tape and Reel	20-pin SSOP	-20 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	± 10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage (1)	VDD	Pin: VDD1,VDD2,VDD3	3.0	3.3	3.6	V
Output Load Capacitance	CL	Pin: Diff CLK pins See Figure.1			2	pF
Output Load Capacitance	Cpl	Pin: REFOUT			25	pF

Note:

(1) Power to VDD1, VDD2 , VDD3 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: FSA,FSB,PDCLKN	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: FSA,FSB,PDCLKN			0.3VDD	V
Input Current	I_L	Pin: FSA,FSB,PDCLKN	-20		+10	μA
High Level Output Voltage	V_{OH}	Pin: REFOUT I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: REFOUT I_{OL}=+4mA			0.2VDD	V
Output impedance		Pin: Diff CLK pins TA=25℃,3.3V	14	20	26	Ω
VREF Voltage	Vref	Pin: VREF	0.72	0.8	0.88	V
Current Consumption 1	I_{DD1}	No load Clock out selection by note (1) VDD=3.3V, Ta=25℃		37		mA
Current Consumption 2	I_{DD2}	On load (2) Clock out selection by note (1) VDD=3.3V, Ta=25℃		51		mA
Current Consumption 3	I_{DDPD}	PDCLKN=”L” Ta=25℃		50	250	μA

(1)CPU_Cp/n:200MHz, USB_Cp/n:96MHz, SATA_Cp/n: 100MHz

(2)Diff CLK pins: Figure1, REFOUT:Cpl=25pF

AC Characteristics

All specifications at VDD: over 3.0 to 3.6V, Ta: over -20 to +85℃, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency	$F_{\_osc}$	Pin: XI,XO		25.000		MHz
Cycle to Cycle Jitter 1	$Jit_{\_cycle\text{-}cycle1}$	Pin: CPU_Cp, CPU_Cn (1)(2)	-85		+85	ps
Cycle to Cycle Jitter 2	$Jit_{\_cycle\text{-}cycle2}$	Pin: USB_Cp, USB_Cn (1)(2)	-250		+250	ps
Cycle to Cycle Jitter 3	$Jit_{\_cycle\text{-}cycle3}$	Pin: SATA_Cp,SATA_Cn (1)(2)	-125		+125	ps
Output Clock Duty Cycle	DtyCyc	Pin: Diff CLK Pins (2) Figure.3	45	50	55	%
		Pin: REFOUT (3)	40	50	60	%
Output Clock Slew Rate	$Slew_{\_rise\_fall}$	Diff CLK Pins(2) Figure3	2.5		8.0	V/ns
Slew rate matching	$Slew_{\_ver}$	Diff CLK Pins(2) Figure.2			20	%
Differential output swing	$V_{\_swing}$	Diff CLK Pins(2) Figure.3	300			mV
Crossing point voltage	$V_{\_cross}$	Diff CLK Pins(2) Figure.2	300		550	mV
Variation of Vcr	$V_{\_cross\_delta}$	Diff CLK Pins(2) Figure.2			140	mV
Maximim output voltage	$V_{\_max}$	Diff CLK Pins(2) Figure.2			1.15	V
Minimum output voltage	$V_{\_min}$	Diff CLK Pins(2) Figure.2	-0.3			V
Output Clock Rise Time	$T_{\_rise}$	Pin: REFOUT (3)		2.5	5.0	ns
Output Clock Fall Time	$T_{\_fall}$	Pin: REFOUT (3)		2.5	5.0	ns
Output disable Time(4)	$T_{\_dis}$	Pin: CLK Pins			300	ms
Power-up Time1(4)	$T_{\_put1}$	Pin: CLK Pins			150	ms
Power-up Time2(5)	$T_{\_put2}$	Pin: CLK Pins			150	ms

(1) 1000 sampling or more

(2) Measured with load condition shown in Figure.1

(3) Measured with load capacitance of 25pF

(4) Refer to Figure.5 on Power down sequence

(5) Refer to Figure.4 on Power On Reset sequence

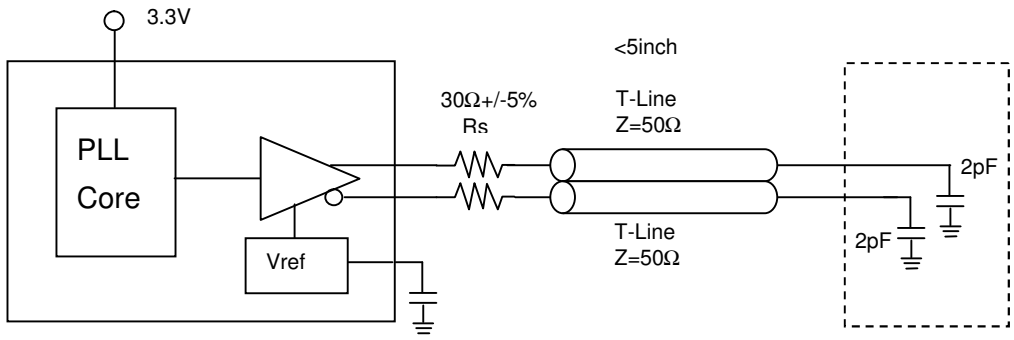


Figure.1 Diff Clocks Load condition

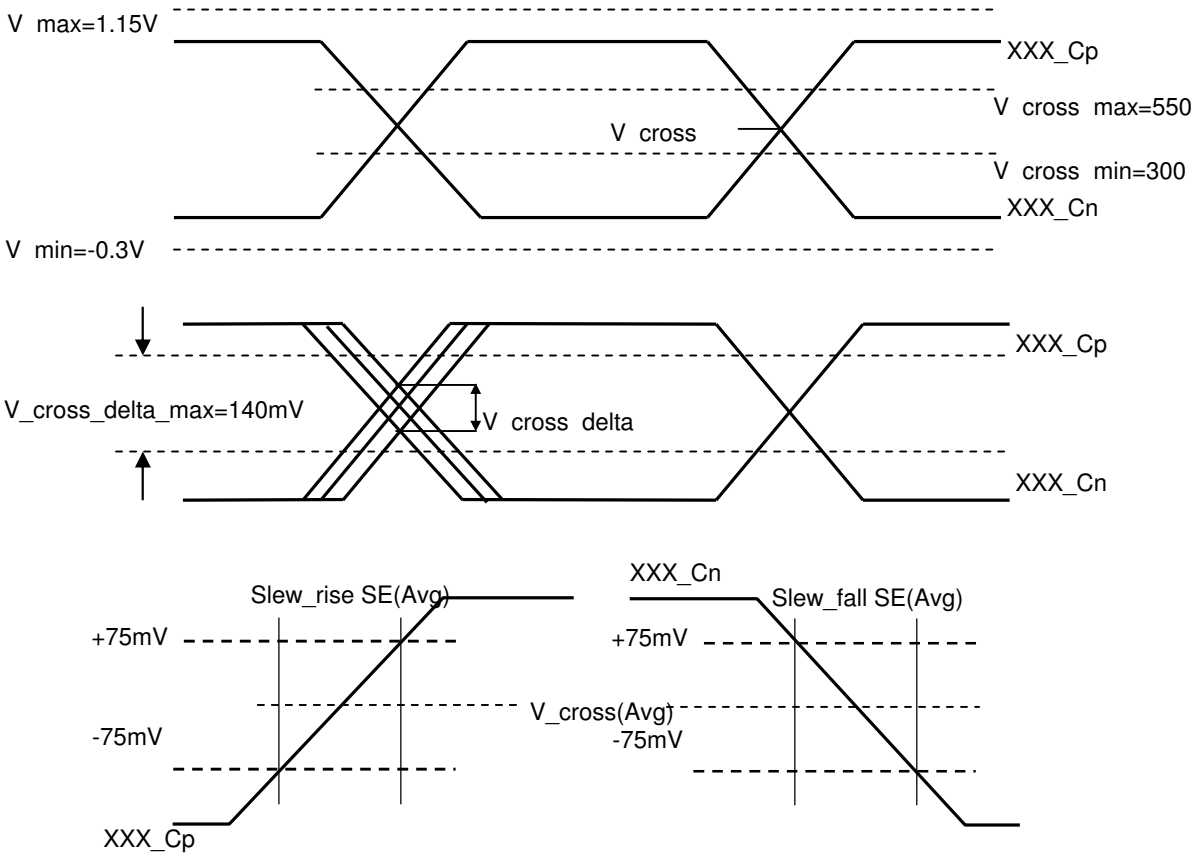


Figure.2 Single ended (SE) measurement waveforms

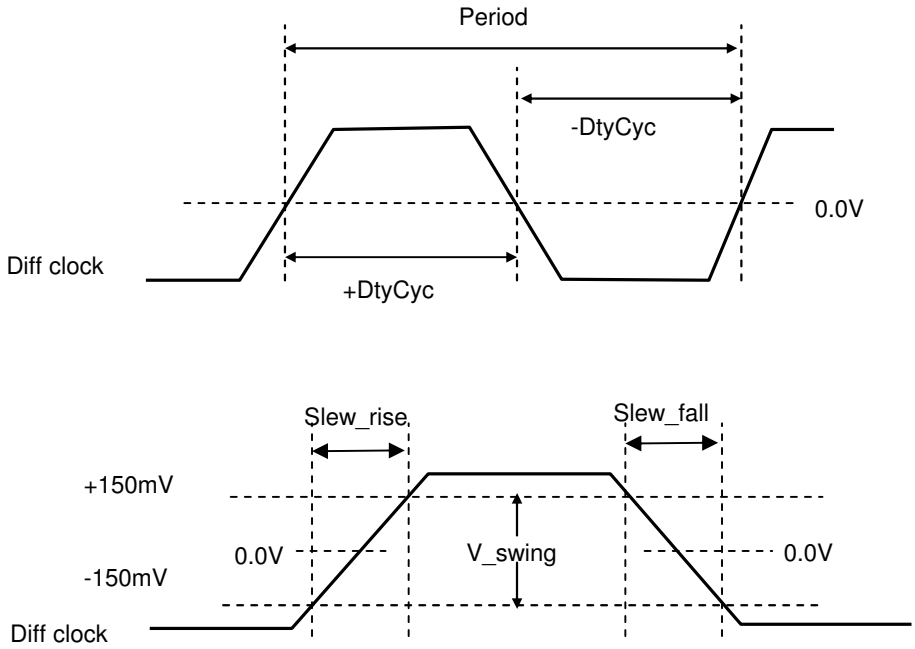


Figure.3 Differential (DIFF) measurement waveforms

Functional Description

Power On Reset

AK8137A has the POR(Power On Reset) circuit. In power up, the POR works and the register is set to the initial value and all clock output becomes enable without glitch.

Note1) The assumption power start time to reach 90 % of VDD is within 20 ms.
Note2) The first register setting should be done after the 150 ms elapse after the power on.

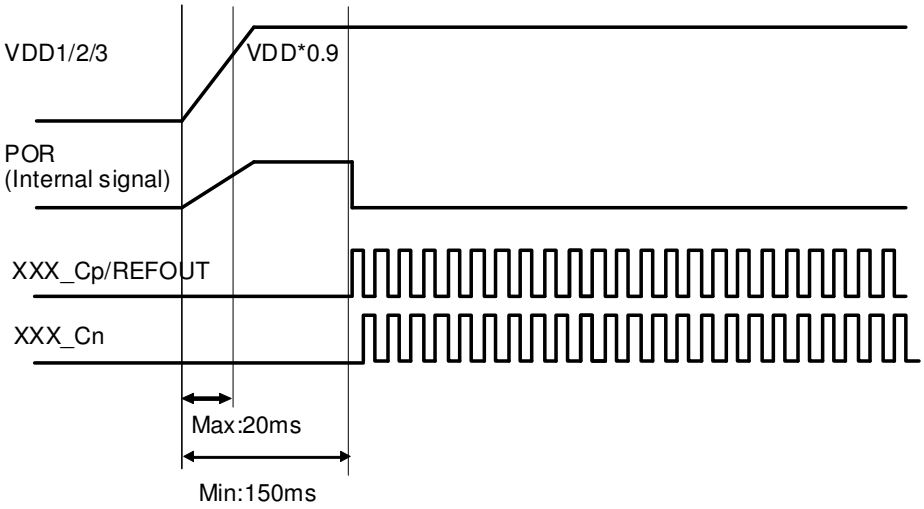


Figure.4 Recommend Power On Reset Sequence

Power down Control

When the PDCLKN is “L”, CPU_Cp/Cn, USB_Cp/Cn and SATA_Cp/Cn clocks are forced to “L”. When it is “H”, they are activated.

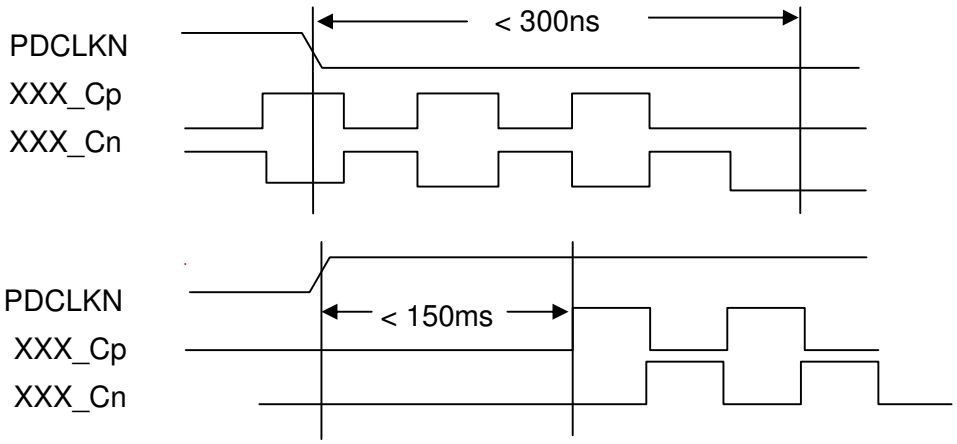


Figure.5 Power Down Sequence

Output clock frequency selection

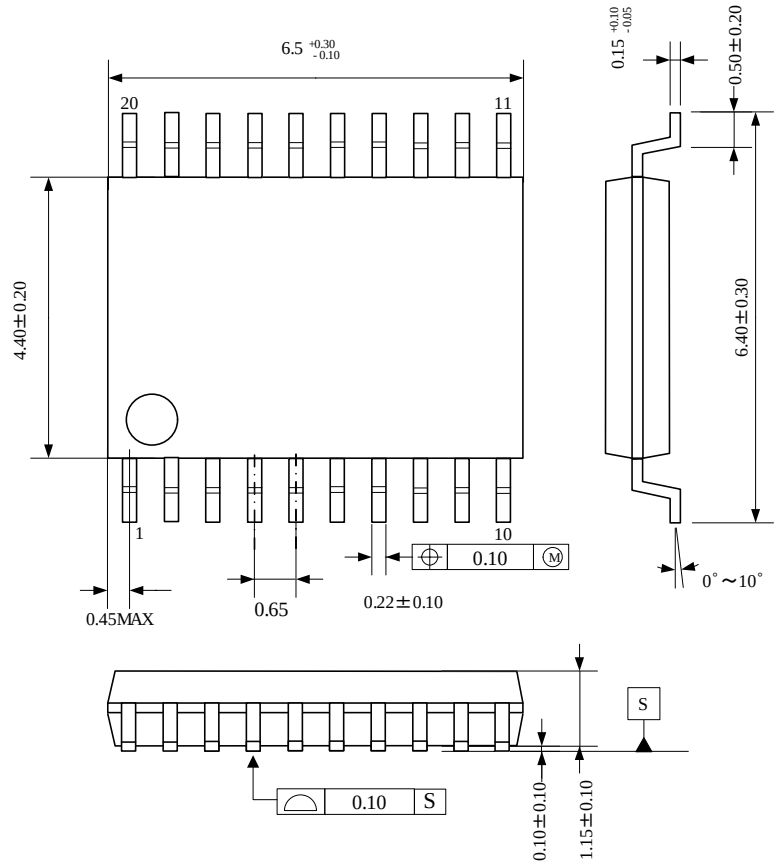
The AK8137A generates a range of low-jitter and hi-accuracy clock frequencies with three built-in PLLs and provides four assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of FSA and FSB.
The selectable frequency is shown in **Table 1**..

Table 1: Clock output Frequency

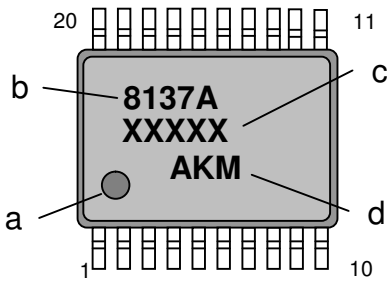
FSB	FSA	CPU_C Frequency (MHz)
L	L	100
L	H	133
H	L	166
H	H	200

Package Information

- **20SSOP Mechanical data**

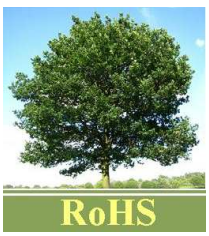


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (5 digits)
d Product Family Logo (1)

- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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It is noted the documents according to this product, which was released before the date of 1st April 2009, shall include the old company name as Asahi Kasei EMD Corporation (AKEMD). These documents will be continuously valid by interpreting the old company