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|  AK4679 |
| 24bit Stereo CODEC with DSP and MIC/RCV/HP/SPK/LINE-AMP |

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| GENERAL DESCRIPTION |
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The AK4679 is a 24bit stereo CODEC and a built-in Microphone-Amplifier, Receiver-Amplifier, Mono Class-D Speaker-Amplifier, Cap-less Class-G Headphone-Amplifier and Line-Amplifier as well as HF/Audio DSP. The AK4679 features AKM DSP core to deal with hands free function for wide band and dual PCM I/F in addition to audio I/F that allows easy interfacing in mobile phone designs with Bluetooth I/F. The playback features also include 5-band Parametric EQ and Dynamic Range Control; therefore the AK4679 can automatically adjust the volume to a comfortable level that has no distortion and provides great flexibility. The AK4679 is available in a 78pin BGA, utilizing less board space than competitive offerings.

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| FEATURES |
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◆ **CODEC&Amp block**

1. Recording Function (Stereo CODEC)

- 4 Stereo Input Selectors
- 4 Stereo Inputs (Single-ended) or 3 Mono Input (Full-differential)
- MIC Amplifier: +24dB ~ -6dB, 3dB step
- 2 Output MIC Power Supplies
- Digital ALC (Automatic Level Control): +36dB ~ -54dB, 0.375dB Step, Mute
- ADC CHARACTERISTICS: S/(N+D): 80dB, DR, S/N: 87dB (MIC-Amp=+18dB)
S/(N+D): 80dB, DR, S/N: 92dB (MIC-Amp=0dB)
- Stereo Digital MIC Interface
- Wind-noise Reduction Filter
- Stereo Separation Emphasis
- 3-band Programmable Notch Filter
- Audio Interface Format: 24/16bit MSB justified, 24/16bit I²S, 16bit DSP Mode

2. Playback Function (Stereo CODEC)

- Digital Volume (+6dB ~ -57.0dB, 0.5dB Step, Mute)
- Digital ALC (Automatic Level Control): +36dB ~ -54dB, 0.375dB Step, Mute
- Stereo Separation Emphasis
- Dynamic Range Control
- 5-band Parametric Equalizer
- Stereo Line Output (Selectable Full-differential / Single-ended)
- Mono Receiver-Amp
 - BTL Output
 - Output Power: 60mW @ 32Ω
 - Analog Volume: +12 ~ -30dB & Mute, 3dB Step
- Cap-less Stereo Class-G Headphone-Amp
 - Output Power: 25mW @ 32Ω, 45mW @ 16Ω
 - Analog Volume: +6 ~ -62dB & Mute, 2dB Step
 - Zero crossing Detection
 - Pop Noise Free at Power-ON/OFF
- Mono Class-D Speaker-Amp
 - BTL Output
 - Short Protection Circuit
 - Output Power: 1.1W @ 8Ω, SVDD=4.2V, THD+N = 10%
0.89W @ 8Ω, SVDD=4.2V, THD+N = 1%
 - Analog Volume: +12 ~ -30dB & Mute, 3dB Step
 - Pop Noise Free at Power-ON/OFF
- Audio Interface Format:
 - 24/16bit MSB justified, 16bit LSB justified, 16/24bit I²S, 16bit DSP Mode

3. Dual PCM I/F for Baseband & Bluetooth Interface
 - Four sample Rate Converters (Up sample: up to x6: Down sample: down to x1/6)
 - Sample Rate:
 - PORTA (Mono): 8 ~ 16kHz
 - PORTB (Stereo): 8 ~ 48kHz
 - Digital Volume
 - Slave Mode
 - Audio Interface Format:
 - 16bit Linear, 8bit A-law, 8bit μ -law
 - Short/Long Frame, I²S, MSB justified
4. Power Management
5. Master Clock(Audio I/F):
 - (1) PLL Mode
 - Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 25MHz, 26MHz, 27MHz (MCKI pin)
32fs or 64fs (BICK pin)
 - (2) External Clock Mode
 - Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
6. Output Master Clock Frequencies(Audio I/F): 32fs/64fs/128fs/256fs
7. Sampling Frequency (Audio I/F)
 - PLL Slave Mode (BICK pin): 8kHz ~ 48kHz
 - PLL Master Mode:
 - 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - EXT Master/Slave Mode:
 - 8kHz ~ 48kHz (256fs), 8kHz ~ 24kHz (512fs), 8kHz ~ 12kHz (1024fs)
8. Audio I/F: Master/Slave mode

◆ **DSP block**

9. Embedded DSP
 - Flexible programming with built-in program and data memories
 - Hardware accelerator
 - Word length: 24bit (Data RAM 24bit floating point)
 - Multiplier 20 x 20 → 40bit (double precision available)
 - Divider 20 / 20 → 20bit
 - ALU: 44bit arithmetic operation (with overflow margin 4bit)
24bit floating point arithmetic and logic operation
 - Program RAM: 4096w x 36bit
 - Coefficient RAM: 2048w x 20bit
 - Data RAM: 2048w x 24bit (24bit floating point)
 - Offset Register: 32w x 15bit
 - Delay RAM: 16384w x 24bit (24bit floating point)
 - 5625 steps at fs16KHz, 1875 steps at fs48KHz
 - Internal clock generator
10. DSP Serial Audio Interface Format
 - 24bit Left justified, I²S,
 - 16/24 bit linear, 8bit A-law, 8bit μ -law PCM
 - Sampling rate 8 KHz ~ 48 KHz
 - Up/Down sampling rate converter for Port#2 (8KHz → 16KHz)
11. Operational, sleep, suspend mode

◆ *General*

12. μ P I/F: I²C Bus (Ver 1.0, 400kHz Fast Mode), SPI (DSP block only)

13. Ta = -30 ~ 85°C

14. Power Supply:

- SVDD (SPK/RCV/LINE-Amp): 3.0 ~ 5.5V
- AVDD (Analog): 1.7 ~ 2.0V
- DVDD (Digital Core): 1.7 ~ 2.0V
- PVDD (HP-Amp & Charge Pump): 1.7 ~ 2.0V
- TVDDA, TVDDE (Digital I/F): 1.6 ~ 3.6V
- VDDE (DSP Core) 1.1 ~ 1.3V

15. Package : 78pin FBGA(4.5 x 4.5 mm, 0.4mm pitch)

■ Block Diagram

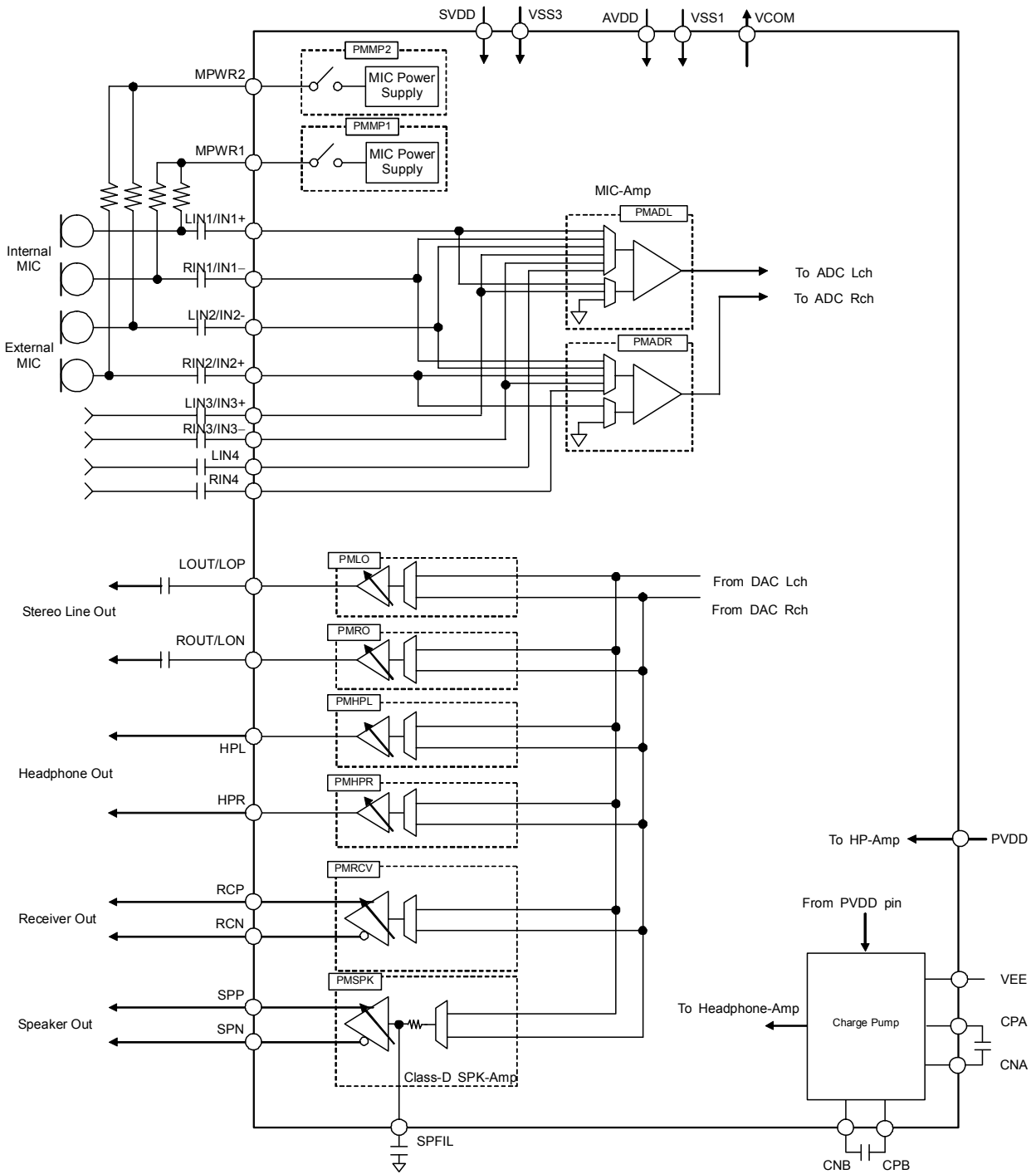


Figure 1. Analog Block Diagram

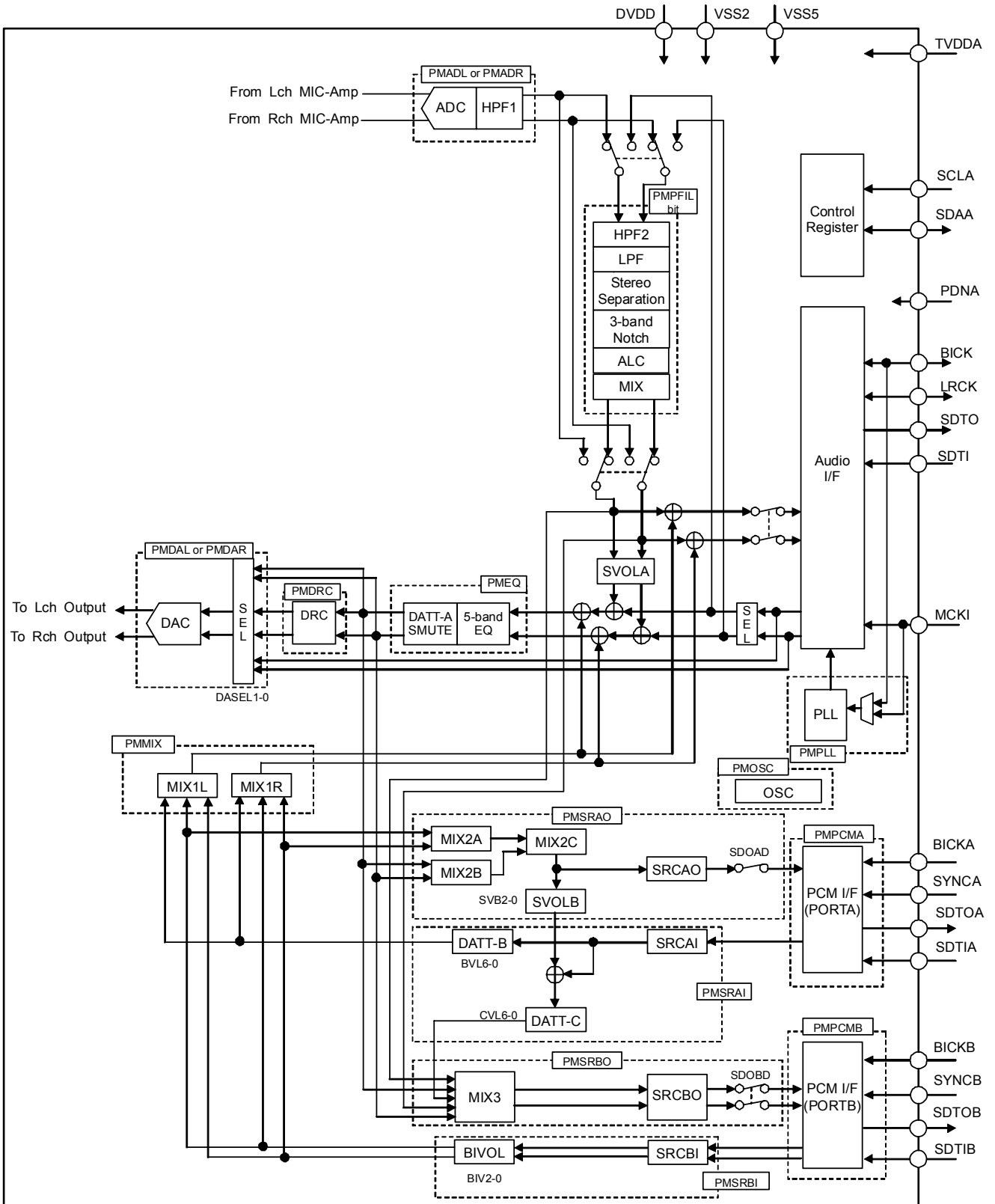


Figure 2. Digital Block Diagram

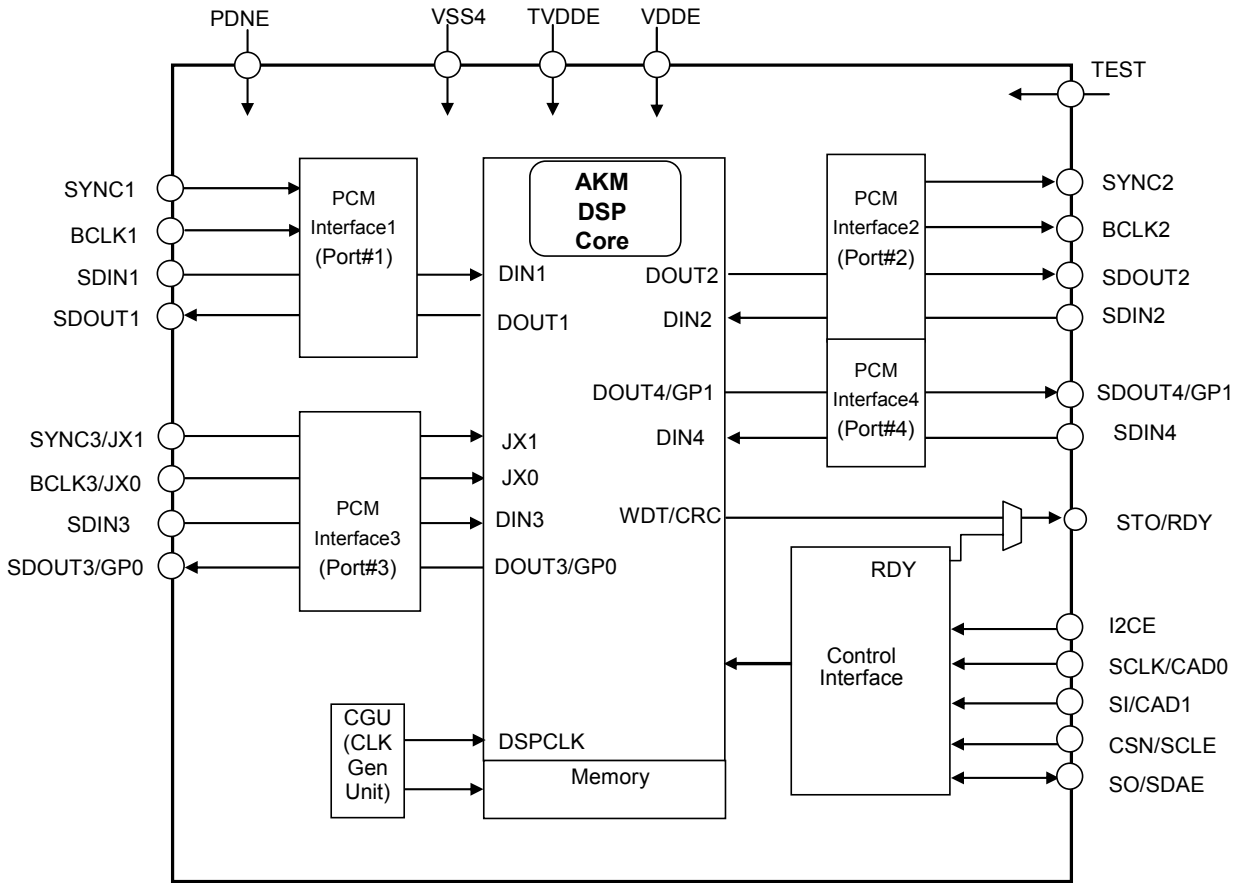


Figure 3. DSP Block Diagram

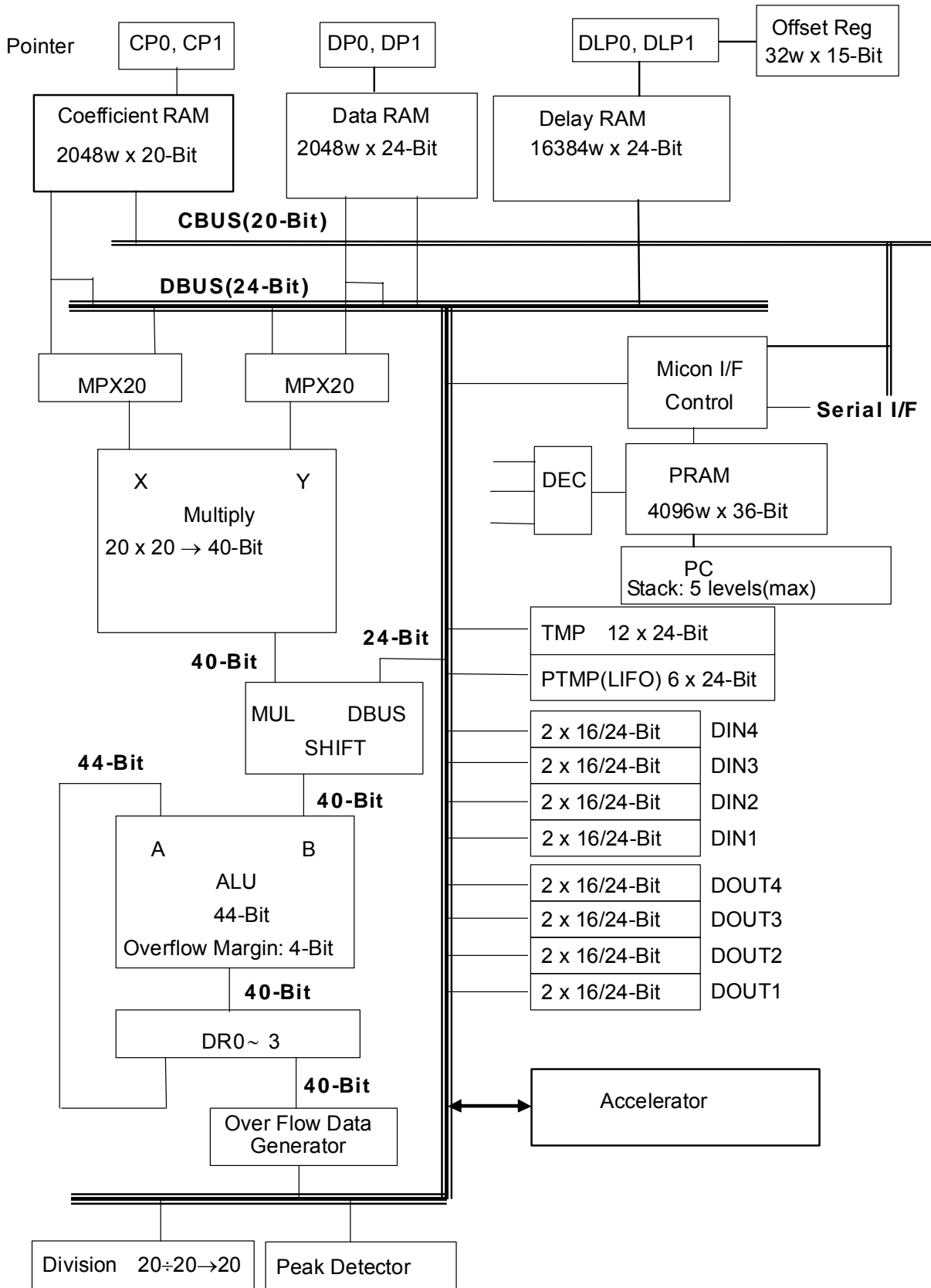


Figure 4. DSP Core

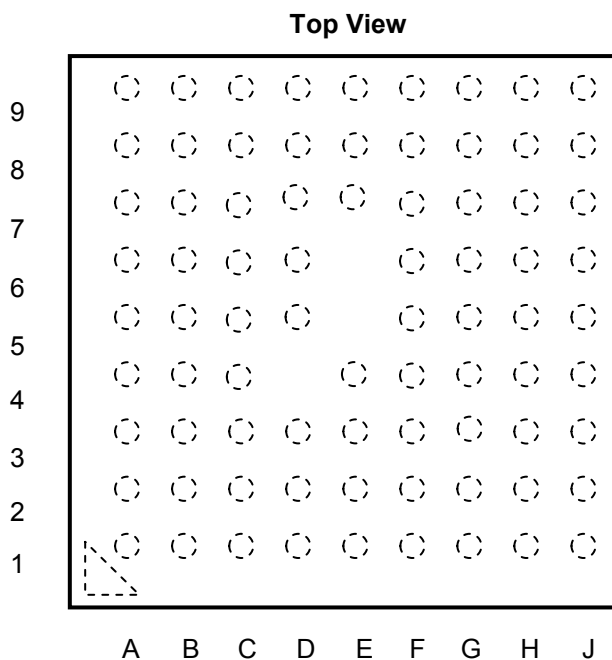
■ Ordering Guide

AK4679EG
AKD4679

-30 ~ +85°C
Evaluation board for AK4679

78pin BGA (0.4mm pitch) Black type

■ Pin Layout Top View



| | | | | | | | | | |
|---|---------------|---------------|-------------------------|----------------|-------|----------------|-------------|--------|-------|
| 9 | LIN2/ IN2- | RIN2/ IN2+ | LIN1/ IN1+/ DMDAT | LIN3/ IN3+ | HPR | PVDD | CNA | VSS5 | CNB |
| 8 | VSS1 | CSN/ SCLE | RIN1/ IN1-/ DMCLK | RIN3/ IN3- | HPL | VEE | VEE | CPA | CPB |
| 7 | VCOM | LOUT/ LOP | SCLK_ CAD0 | PDNE | RIN4 | LIN4 | PDNA | SDAA | VSS2 |
| 6 | AVDD | ROUT/ LON | SI/ CAD1 | SYNC2 | | BCLK1 | SCLA | SDTO | TVDDA |
| 5 | MPWR1 | MPWR2 | SO/ SDAE | JX1/ SYNC3 | | SDIN1 | SYNC1 | LRCK | BICK |
| 4 | RCP | RCN | SDOUT2 | | TEST | SDOUT3 /GP0 | SYNCA | SDTOB | SDTI |
| 3 | SVDD | VSS3 | SDIN4 | SDIN2 | SDIN3 | JX0/ BCLK3 | STO/ RDY | SYNCB | MCKI |
| 2 | SPN | VSS3 | I2CE | SDOUT4 /GP1 | SDTIA | BCLK2 | BICKA | BICKB | SDTOA |
| 1 | SVDD | SPP | SPFIL | TVDE | DVDD | VSS4 | VDDE | SDOUT1 | SDTIB |
| | A | B | C | D | E | F | G | H | J |

Total 78pin

| PIN/FUNCTION | | | |
|------------------------|----------|-----|--|
| No. | Pin Name | I/O | Function |
| Power Supply | | | |
| A6 | AVDD | - | Analog Power Supply Pin, 1.7 ~ 2.0V |
| A7 | VCOM | O | Common Voltage Output Pin |
| A8 | VSS1 | - | Ground 1 Pin |
| E1 | DVDD | - | Digital Core Power Supply Pin, 1.7 ~ 2.0V |
| J6 | TVDDA | - | Digital I/O Power Supply Pin, 1.6 ~ 3.6V |
| J7 | VSS2 | - | Ground 2 Pin |
| A1,A3 | SVDD | - | Analog Amp Power Supply Pin, 3.0 ~ 5.5V |
| B2,B3 | VSS3 | - | Ground 3 Pin |
| F9 | PVDD | - | HP-Amp & Charge Pump Power Supply Pin |
| H9 | VSS5 | - | Ground 5 Pin |
| F8,G8 | VEE | - | Charge Pump Circuit Negative Voltage Output Pin |
| H8 | CPA | O | Positive Charge Pump Capacitor Terminal A Pin |
| G9 | CNA | I | Negative Charge Pump Capacitor Terminal A Pin |
| J8 | CPB | O | Positive Charge Pump Capacitor Terminal B Pin |
| J9 | CNB | I | Negative Charge Pump Capacitor Terminal B Pin |
| A5 | MPWR1 | O | MIC Power Supply 1 Pin |
| B5 | MPWR2 | O | MIC Power Supply 2 Pin |
| Audio Interface | | | |
| J3 | MCKI | I | External Master Clock Input Pin |
| J5 | BICK | I/O | Audio Serial Data Clock Pin |
| H5 | LRCK | I/O | Input / Output Channel Clock Pin |
| J4 | SDTI | I | Audio Serial Data Input Pin |
| H6 | SDTO | O | Audio Serial Data Output Pin |
| PCM Interface | | | |
| G2 | BICKA | I | Serial Data Clock A Pin |
| G4 | SYNCA | I | Sync Signal A Pin |
| E2 | SDTIA | I | Serial Data Input A Pin |
| J2 | SDTOA | O | Serial Data Output A Pin |
| H2 | BICKB | I | Serial Data Clock B Pin |
| H3 | SYNCB | I | Sync Signal B Pin |
| J1 | SDTIB | I | Serial Data Input B Pin |
| H4 | SDTOB | O | Serial Data Output B Pin |
| Analog Input | | | |
| C9 | LIN1 | I | Lch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input, DMIC bit = "0") |
| | IN1+ | I | Positive Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input, DMIC bit = "0") |
| | DMDAT | I | Digital Microphone Data Input Pin (DMIC bit = "1") |
| C8 | RIN1 | I | Rch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input, DMIC bit = "0") |
| | IN1- | I | Negative Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input, DMIC bit = "0") |
| | DMCLK | O | Digital Microphone Clock Pin (DMIC bit = "1") |
| A9 | LIN2 | I | Lch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2- | I | Negative Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| B9 | RIN2 | I | Rch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2+ | I | Positive Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| D9 | LIN3 | I | Lch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input) |
| | IN3+ | I | Positive Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input) |
| D8 | RIN3 | I | Rch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input) |
| | IN3- | I | Negative Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input) |
| F7 | LIN4 | I | Lch Analog Input 4 Pin |
| E7 | RIN4 | I | Rch Analog Input 4 Pin |

PIN/FUNCTION (Cont.)

| No. | Pin Name | I/O | Function |
|--|----------|-----|--|
| Analog Output | | | |
| B6 | ROUT | O | Rch Stereo Line Output Pin (LODIF bit = "0": Stereo Line Output) |
| | LON | O | Negative Line Output Pin (LODIF bit = "1": Full-differential Mono Output) |
| B7 | LOUT | O | Lch Stereo Line Output Pin (LODIF bit = "0": Stereo Line Output) |
| | LOP | O | Positive Line Output Pin (LODIF bit = "1": Full-differential Mono Output) |
| A4 | RCP | O | Receiver-Amp Positive Output Pin |
| B4 | RCN | O | Receiver-Amp Negative Output Pin |
| E8 | HPL | O | Lch Headphone-Amp Output Pin |
| E9 | HPR | O | Rch Headphone-Amp Output Pin |
| B1 | SPP | O | Speaker-Amp Positive Output Pin |
| A2 | SPN | O | Speaker-Amp Negative Output Pin |
| C1 | SPFIL | O | Speaker-Amp Filter Pin Connect 2.2nF between SPFIL pin and VSS1. |
| Control Interface for Audio Block | | | |
| G6 | SCLA | I | Control Data Clock Pin |
| H7 | SDAA | I/O | Control Data Input Pin |
| G7 | PDNA | I | Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register. |

Note 1. All input pins except analog input pins (LIN1/IN1+, RIN1/IN1-, LIN2/IN2-, RIN2/IN2+, LIN3/IN3+, RIN3/IN3-, LIN4, RIN4) must not be allowed to float.
I/O pins (LRCK, BICK and SDAA pins) should be processed appropriately.

| NO | Pin Name | I/O | Function |
|----------------|----------|-----|--|
| DSP I/O | | | |
| G1 | VDDE | - | Core Power Supply Pin 1.2V |
| D1 | TVDDE | - | I/O power Supply Pin 1.6~3.6V |
| F1 | VSS4 | - | Ground pin 0V |
| D7 | PDNE | I | Power-Down Mode Pin "H": Power-up, "L": Power-down, reset the control register. The AK4679 DSP must be reset once upon power-up. |
| G3 | STO | O | Status Output Pin (STRDY bit = "0") |
| | RDY | | Data Write Ready output pin for control I/F (STRDY bit = "1") |
| G5 | SYNC1 | I | Frame Sync 1 pin |
| F6 | BCLK1 | I | Serial Data Clock 1 Pin AK4679 DSP goes into stanby state when BCLK1 is not present. |
| F5 | SDIN1 | I | Serial Data Input 1 Pin |
| H1 | SDOUT1 | O | Serial Data Output 1 Pin |
| D6 | SYNC2 | O | Frame Sync 1 pin |
| F2 | BCLK2 | O | Serial Data Clock 2 Pin |
| D3 | SDIN2 | I | Serial Data Input 2 Pin |
| C4 | SDOUT2 | O | Serial Data Output 2 Pin |
| D5 | SYNC3 | I | Frame Sync 3 pin (SELPT bit = "1") |
| | JX1 | | Conditional Jump 1 Pin (SELPT bit = "0") |
| F3 | BCLK3 | I | Serial Data Clock 3 Pin (SELPT bit = "1") |
| | JX0 | | Conditional Jump 0 Pin (SELPT bit = "0") |
| E3 | SDIN3 | I | Serial Data Input 3 Pin |
| F4 | SDOUT3 | O | Serial Data Output 3 Pin (SELDO3 bit = "0") |
| | GP0 | | DSP Programmable output 0 Pin (SELDO3 bit = "1") |
| C3 | SDIN4 | I | Serial Data Input 4 Pin |

| | | | | |
|----|--------|---|--|----------------------|
| D2 | SDOUT4 | O | Serial Data Output 4 Pin | (SELDO4 bit = "0") |
| | GP1 | | DSP Programmable output 1 Pin | (SELDO4 bit = "1") |
| C2 | I2CE | I | Control Interface Mode Select Pin for DSP Block | "H": I2CE, "L": SPI |
| C7 | SCLK | I | Serial Clock Input pin | SPI (I2CE pin = "L") |
| | CAD0 | | Slave Address 0 Input pin | I2C (I2CE pin = "H") |
| B8 | CSN | I | Chip select pin | SPI (I2CE pin = "L") |
| | SCLE | | Control Interface clock input pin | I2C (I2CE pin = "H") |
| C5 | SO | O | Serial data output pin | SPI (I2CE pin = "L") |
| | SDAE | | Control Interface input/output acknowledge pin | I2C (I2CE pin = "H") |
| C6 | SI | I | Serial data input pin | SPI (I2CE pin = "L") |
| | CAD1 | | Slave Address 1 Input pin | I2C(I2CE pin = "H") |
| E4 | TEST | I | Test pin (pull-down resistor) must be connected to VSS4. | |

Note 2. All input pins must not be allowed to float.

Note 3. I2CE and CAD0/1 pins must be fixed to "L" (VSS4) or "H" (TVDD).

■ Handling of Unused Pin on the System

The unused input and output pins on the system should be processed appropriately as below.

| Classification | Pin Name | Setting |
|----------------|---|--|
| Analog | MPWR1, MPWR2, SPP, SPN, RCP, RCN, HPL, HPR, ROUT/LON, LOU/LOP, RIN4, LIN4, RIN3/IN3-, LIN3/IN3+, RIN2/IN2+, LIN2/IN2-, RIN1/IN1-, LIN1/IN1+, CPA, CNA, CPB, CNB, VEE, SPFIL | These pins should be open. |
| Digital | SDTO, SDTOA, SDTOB STO/RDY, SDOUT3/GPO, SDOUT4/GP1 | These pins should be open. |
| | MCKI, SDTI, SDTIA, SDTIB, BICKA, SYNCA, BICKB, SYNCB | These pins should be connected to VSS2. |
| | LRCK, BICK | These pins should be connected to VSS2 and M/S bit should be set to "0". |
| | SYNC1, BCLK1, SDIN3, SDIN4, SYNC3/JX1, BCLK3/JX0, TEST | These pins should be connected to VSS4 |

■ Pin States in DSP Power-down Mode

The table below shows pin states when the PDNE pin = "L".

| NO | Pin Name | I/O | Pin state |
|----|----------|-----|---------------------------------|
| G3 | STO | O | Low |
| | RDY | | |
| H1 | SDOUT1 | O | SDIN2 data output |
| D6 | SYNC2 | O | SYNC1 data output |
| F2 | BCLK2 | O | BCLK1 data output |
| C4 | SDOUT2 | O | SDIN1 data output |
| F4 | SDOUT3 | O | SDIN4 data output |
| | GP0 | | |
| D2 | SDOUT4 | O | SDIN3 data output |
| | GP1 | | |
| C5 | SO | O | Low level (I2CE pin = "L": SPI) |
| | SDAE | I/O | Hi-z (I2CE pin = "H": I2C) |

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|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(VSS1=VSS2=VSS3=VSS4=VSS5=0V; Note 4, Note 5)

| Parameter | | Symbol | min | max | Unit |
|--|----------------------|--------|------|-------------|------|
| Power Supplies: | Analog | AVDD | -0.3 | 2.5 | V |
| | SPK/RCV/LINE-Amp | SVDD | -0.3 | 6.0 | V |
| | HP-Amp & Charge Pump | PVDD | -0.3 | 2.5 | V |
| | Digital Core | DVDD | -0.3 | 2.5 | V |
| | Digital I/O (Codec) | TVDDA | -0.3 | 6.0 | V |
| | DSP Core | VDDE | -0.3 | 1.6 | V |
| | Digital I/O (DSP) | TVDDE | -0.3 | 4.1 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage (Note 6) | | VINA | -0.3 | AVDD + 0.3 | V |
| Digital Input Voltage (Note 8) | | VIND1 | -0.3 | TVDD + 0.3 | V |
| Digital Input Voltage (Note 7) | | VINDE | -0.3 | TVDDE + 0.3 | V |
| Ambient Temperature (powered applied) | | Ta | -30 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |
| Maximum Power Dissipation | | Pd | - | 1 | W |

Note 4. All voltages with respect to ground.

Note 5. VSS1 to VSS5 must be connected to the same analog ground plane.

Note 6. RIN4, LIN4, RIN3/IN3-, LIN3/IN3+, RIN2/IN2+, LIN2/IN2-, RIN1/IN1-, LIN1/IN1+ pins

Note 7. SDTI, LRCK, BICK, MCKI, PDNA, BICKA, SYNCA, SDITA, BICKB, SYNCB, SDTIB, SCLA and SDAA pins. Pull-up resistors at SDAA and SCLA pins should be connected to (TVDDA+0.3)V or less voltage.

Note 8. SYNC1/2/3, BCLK1/2/3, SDIN1-4, SDOUT1-4, I2CE, STO/RDY, SCLK/CAD, SI/CAD0, CSN/SCLE and SO/SDAE. Pull-up resistors at SDAE and SCLE pins should be connected to (TVDDE+0.3)V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

| |
|---|
| RECOMMENDED OPERATING CONDITIONS |
|---|

(VSS1=VSS2=VSS3=VSS4=VSS5=0V; Note 4)

| Parameter | | Symbol | min | typ | max | Unit | |
|----------------------------|----------------------|-------------|-------------|------|-----|------|---|
| Power Supplies (Note 9) | Analog | AVDD | 1.7 | 1.8 | 2.0 | V | |
| | SPK/RCV/LINE-Amp | SVDD | 3.0 | 4.2 | 5.5 | V | |
| | HP-Amp & Charge Pump | PVDD | 1.7 | 1.8 | 2.0 | V | |
| | Digital Core | DVDD | 1.7 | 1.8 | 2.0 | V | |
| | Digital I/O (Codec) | TVDDA | 1.6 | 1.8 | 3.6 | V | |
| | DSP Core | VDDE | 1.1 | 1.2 | 1.3 | V | |
| | Digital I/O (DSP) | TVDDE | 1.6 | 1.8 | 3.6 | V | |
| | Difference | | AVDD – PVDD | -0.2 | – | 0.2 | V |
| | | | AVDD – DVDD | -0.2 | – | 0.2 | V |
| | | PVDD – DVDD | -0.2 | – | 0.2 | V | |

Note 4. All voltages with respect to ground.

Note 9. The power-up sequence between supplies (AVDD, SVDD, PVDD, DVDD or TVDD) is not critical. The PDNA pin should be held “L” when power supplies are tuning on. The PDNA pin is allowed to be “H” after all power supplies are applied and settled. The AK4679 should be operated along the recommended power-up/down sequence shown in “System Design (Grounding and Power Supply Decoupling)” to avoid pop noise at speaker output, receiver output, headphone outputs and line outputs.

*** AVDD, PVDD, DVDD, VDDE, TVDDE and TVDDA can be powered OFF (Power is not applied) when SVDD is powered ON (Power is applied) with both PDNA and PDNE pin “L”. When turning on AVDD, PVDD, DVDD, VDDE, TVDDE and TVDDA again in this case, the PDNA pin must be “L” until all other power supplies are powered ON. Also, when turning off AVDD, PVDD, DVDD, VDDE, TVDDE and TVDDA both the PDNA and PDNE pin must be “L” before other power supplies start to turn off.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=PVDD= DVDD=TVDDA= TVDDE=1.8V, SVDD=4.2V, VDDE=1.2V;
VSS1=VSS2=VSS3=VSS4 =VSS5 =0V; Signal Frequency=1kHz; 24bit Data; fs=44.1kHz, BICK=64fs; Measurement
Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

| Parameter | min | typ | max | Unit | |
|---|-----------|-------|-------|-------|-----------------|
| MIC Amplifier: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins | | | | | |
| Input Resistance | 17 | 25 | 38 | kΩ | |
| Gain (Note 10) | | | | | |
| Gain Setting | -6 | - | +24 | dB | |
| Step Width | - | 3 | - | dB | |
| MIC Power Supply: MPWR1, MPWR2 pin | | | | | |
| Output Voltage (Note 11) | 2.3 | 2.5 | 2.7 | V | |
| Load Resistance | 1.0 | - | - | kΩ | |
| Load Capacitance | - | - | 30 | pF | |
| Output Noise Level (A-weighted) | - | -107 | - | dBV | |
| PSRR (Note 12) | | | | | |
| 217Hz | - | 100 | - | dB | |
| 1kHz | - | 100 | - | dB | |
| Stereo ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins(Single-ended Input) → Stereo ADC → Programmable Filter (IVOL=0dB, EQ=ALC=OFF) → SDTO | | | | | |
| Resolution | - | - | 24 | Bits | |
| Input Voltage (Note 13) | (Note 14) | 0.204 | 0.227 | 0.250 | V _{pp} |
| | (Note 15) | 1.62 | 1.8 | 1.98 | V _{pp} |
| S/(N+D) (-1dBFS) | (Note 14) | 69 | 80 | - | dB |
| | (Note 15) | - | 80 | - | dB |
| D-Range (-60dBFS, A-weighted) | (Note 14) | 76 | 87 | - | dB |
| | (Note 15) | - | 92 | - | dB |
| S/N (A-weighted) | (Note 14) | 76 | 87 | - | dB |
| | (Note 15) | - | 92 | - | dB |
| Interchannel Isolation (Note 16) | (Note 14) | 75 | 90 | - | dB |
| | (Note 15) | - | 100 | - | dB |
| Interchannel Gain Mismatch (Note 16) | (Note 14) | - | 0 | 0.8 | dB |
| | (Note 15) | - | 0 | 0.8 | dB |

Note 10. In case of full-differential input, MGAIN (min)=-3dB

Note 11. In case of M1CL1 bit or M1CL2 bit = "0". Output voltage is proportional to AVDD (typ. 1.39 x AVDD V).
M1CL1 bit or M1CL2 bit = "1": typ. 1.56 x AVDD V

Note 12. PSRR is referred to SVDD with 500mV_{pp} sine wave.

Note 13. Input voltage which means ADC full-scale voltage is proportional to AVDD voltage.

Single-ended Input: $V_{in} = 1.0 \times AVDD \text{ V}_{pp}(\text{typ})$.

Full-Differential Input: $V_{in} = (IN+) - (IN-) = 1.0 \times AVDD \text{ V}_{pp}(\text{typ})$.

$IN+ = 0.5 \times AVDD(\text{typ})$, $IN- = 0.5 \times AVDD(\text{typ})$

Pseudo-Differential Input: $V_{in} = (IN+) - (IN-) = 1.0 \times AVDD \text{ V}_{pp}(\text{typ})$.

$IN+ = 1.0 \times AVDD(\text{typ})$, $IN- = 0V$ ($IN-$ pin should be connected to VSS1.)

Note 14. MG1L3=0=MG1R3=0 bits = "BH" (+18dB).

In case of Full-differential, S/(N+D) =75dB, DR=S/N=81dB

Note 15. MG1L3=0=MG1R3=0 bits = "5H" (0dB).

In case of Full-differential, S/(N+D) =79dB, DR=S/N=91dB

Note 16. This is a value between Lch and Rch of each input.

| Parameter | min | typ | max | Unit |
|--|------|------|------|-----------------|
| Stereo DAC Characteristics: | | | | |
| Resolution | - | - | 24 | Bits |
| Stereo Line Output Characteristics: Stereo DAC → LOUT/ROUT pins, ALC=OFF, IVOL=0dB, OVOL=0dB, LVL=0dB, $R_L=10k\Omega$; unless otherwise specified. | | | | |
| Output Voltage (Note 17) | 1.62 | 1.8 | 1.98 | V _{pp} |
| S/(N+D) (0dBFS) | 70 | 80 | - | dB |
| S/N (A-weighted) | 82 | 92 | - | dB |
| Interchannel Isolation | 85 | 95 | - | dB |
| Interchannel Gain Mismatch | - | 0 | 0.8 | dB |
| Load Resistance | 10 | - | - | k Ω |
| Load Capacitance | - | - | 30 | pF |
| PSRR (Note 18) | | | | |
| 217Hz | - | 75 | - | dB |
| 1kHz | - | 75 | - | dB |
| Mono Line Output Characteristics: Stereo DAC → LOP/LON pins, ALC=OFF, IVOL=0dB, OVOL=0dB, LVL=0dB, LODIF bit = "1", $R_L=10k\Omega$ for each pin (Full-differential) | | | | |
| Output Voltage (Note 19) | 3.24 | 3.6 | 3.96 | V _{pp} |
| S/(N+D) (0dBFS) | - | 73 | - | dB |
| S/N (A-weighted) | - | 95 | - | dB |
| Load Resistance (LOP/LON pins, respectively) (Note 20) | 10 | - | - | k Ω |
| Load Capacitance (LOP/LON pins, respectively) (Note 21) | - | - | 30 | pF |
| PSRR (Note 18) | | | | |
| 217Hz | - | 70 | - | dB |
| 1kHz | - | 70 | - | dB |
| Mono Receiver-Amp Output Characteristics: DAC(Stereo, Note 22) → RCP/RCN pins, ALC=OFF, IVOL=0dB, OVOL=0dB, RCVG=-6dB, $R_L=32\Omega$, BTL; unless otherwise specified. | | | | |
| Output Voltage (Note 23) | | | | |
| 0dBFS | 1.76 | 1.96 | 2.16 | V _{pp} |
| 0dBFS, RCVG=0dB | - | 3.91 | - | V _{pp} |
| S/(N+D) | | | | |
| 0dBFS | 40 | 59 | - | dB |
| 0dBFS, RCVG=0dB | - | 55 | - | dB |
| S/N (A-weighted) (DAC → RCP/RCN pins) | 84 | 94 | - | dB |
| Output Noise Level (A-weighted, RCVG = -9dB) | - | -100 | - | dBV |
| Load Resistance | 32 | - | - | Ω |
| Load Capacitance (Note 21) | - | - | 30 | pF |
| PSRR (Note 18) | | | | |
| 217Hz | - | 75 | - | dB |
| 1kHz | - | 75 | - | dB |

Note 17. Output voltage is proportional to AVDD voltage. $V_{out} = 1.0 \times AVDD \text{ Vpp}(\text{typ})$

Note 18. PSRR is referred to SVDD with 200mV_{pp} sine wave.

Note 19. Output voltage is proportional to AVDD voltage. $V_{out} = (LOP) - (LON) = 2.0 \times AVDD \text{ Vpp}(\text{typ})$

Note 20. This is a resistance value between output pin and VSS1. When a resistor is connected between output pins, load resistance for each output pin is half. Therefore, it is necessary to decide load resistance in consideration of these.

Note 21. This is a capacitance value between output pin and VSS1. When a capacitor is connected between output pins, load capacitance for each output pin doubles. Therefore, it is necessary to decide load capacitance in consideration of these.

Note 22. Input signal of left and right channels is same phase and level.

Note 23. Output voltage is proportional to AVDD voltage. $V_{out} = (RCP) - (RCN) = 2.17 \times AVDD \text{ Vpp}(\text{typ})$

$P_o = 15\text{mW} @ 32\Omega, V_{out} = 1.96\text{Vpp}$. $P_o = 60\text{mW} @ 32\Omega, V_{out} = 3.91\text{Vpp}$.

| Parameter | min | typ | max | Unit |
|---|------|------|------|------------------|
| Headphone-Amp Characteristics: DAC(Stereo, Note 22) → HPL/HPR pins, ALC=OFF, IVOL=0dB, OVOL=0dB, HPG=0dB, $R_L=32\Omega$ | | | | |
| Output Voltage (Note 24) | | | | |
| 0dBFS, $R_L = 32\Omega$, HPG=-4dB | 1.44 | 1.6 | 1.76 | V _{pp} |
| 0dBFS, $R_L = 16\Omega$, HPG=-4dB | - | 1.6 | - | V _{pp} |
| 0dBFS, $R_L = 32\Omega$, HPG=0dB | - | 2.5 | - | V _{pp} |
| 0dBFS, $R_L = 16\Omega$, HPG=0dB | - | 0.85 | - | V _{rms} |
| S/(N+D) | | | | |
| 0dBFS, $R_L = 32\Omega$, HPG=-4dB | 50 | 73 | - | dB |
| 0dBFS, $R_L = 16\Omega$, HPG=-4dB | - | 67 | - | dB |
| 0dBFS, $R_L = 32\Omega$, HPG=0dB | - | 73 | - | dB |
| 0dBFS, $R_L = 16\Omega$, HPG=0dB | - | 20 | - | dB |
| S/N (A-weighted) | 85 | 95 | - | dB |
| Output Noise Level (A-weighted, HPG=-14dB) | - | -106 | - | dBV |
| Interchannel Isolation | 60 | 80 | - | dB |
| Interchannel Gain Mismatch | - | 0 | 0.8 | dB |
| Load Resistance | 16 | 32 | - | Ω |
| Load Capacitance (Note 25) | - | - | 300 | pF |
| PSRR (Note 26) | | | | |
| 217Hz | - | 70 | - | dB |
| 1kHz | - | 60 | - | dB |
| DC-offset (HPG ≤ -4dB) | -1 | 0 | 1 | mV |
| Speaker-Amp Characteristics: DAC(stereo, Note 27) → SPP/SPN pins, ALC=OFF, IVOL=0dB, OVOL=0dB, SPKG=-6dB, $R_L=8\Omega + 10\mu\text{H}$ | | | | |
| Output Power | | | | |
| SVDD=5.0V, THD+N = 10% | - | 1.57 | - | W |
| SVDD=4.2V, THD+N = 10% | - | 1.1 | - | W |
| SVDD=4.2V, THD+N = 1% | - | 0.89 | - | W |
| SVDD=3.7V, THD+N = 1% | - | 0.69 | - | W |
| Output Voltage (-3dBFS) (Note 28) | 5.0 | 5.4 | 6.2 | V _{pp} |
| S/(N+D) (SVDD=3.7V, Po=0.35W) | 40 | 59 | - | dB |
| Output Noise Level (A-weighted) (Note 29) | - | -82 | -73 | dBV |
| Load Resistance | 8 | - | - | Ω |
| Load Capacitance (Note 25) | - | - | 300 | pF |
| PSRR (Note 30) | | | | |
| 217Hz | - | 63 | - | dB |
| 1kHz | - | 63 | - | dB |
| DC-offset | -10 | 0 | 10 | mV |
| Current Limit (Note 31) | - | 40 | 80 | mA |

Note 24. The Output voltage is proportional to AVDD voltage. $V_{out} = 1.4 \times AVDD$ V_{pp}(typ).

Po = 10mW @ 32 Ω , Vout = 1.6V_{pp}. Po = 25mW @ 32 Ω , Vout = 2.5V_{pp}.

Po = 20mW @ 16 Ω , Vout = 1.6V_{pp}. Po = 45mW @ 16 Ω , Vout = 0.85V_{rms}.

Note 25. Load Capacitance for VSS1.

Note 26. PSRR is referred to PVDD with 200mV_{pp} sine wave.

Note 27. Input signal of left and right channels is same phase and level.

Note 28. Output voltage is proportional to AVDD voltage. $V_{out} = (SPP) - (SPN) = 3.0 \times AVDD$ V_{pp}(typ).

Note 29. In case of mono signal input (e.g. Lch only) and SPKG=0dB, output noise level is -84dBV.

Note 30. PSRR is referred to SVDD with 200mV_{pp} sine wave.

Note 31. The average current between SVDD and VSS3 when the SPP and SPN pins are shorted and output power is 890mW.

| Parameter | | min | typ | max | Unit |
|---|-------------------|-----|-----|-----|------|
| Stereo Line Output Volume Characteristics: | | | | | |
| Gain Setting | | -9 | - | +6 | dB |
| Step Width | | 1 | 3 | 5 | dB |
| Headphone Output Volume Characteristics: | | | | | |
| Gain Setting | | -62 | - | +6 | dB |
| Step Width | Gain: +6 ~ -40dB | 1 | 2 | 3 | dB |
| | Gain: -40 ~ -62dB | - | 2 | - | dB |
| Speaker Output Volume Characteristics: | | | | | |
| Gain Setting | | -30 | - | +12 | dB |
| Step Width | | 1 | 3 | 5 | dB |
| Receiver Output Volume Characteristics: | | | | | |
| Gain Setting | | -30 | - | +12 | dB |
| Step Width | | 1 | 3 | 5 | dB |

| Parameter | | min | typ | max | Unit |
|---|-----------|-----|-----|-----|------|
| Power Supply Current: | | | | | |
| Power Up (PDNE and PDNA pin = "H", All Circuits Power-up) | | | | | |
| AVDD + DVDD + PVDD + TVDDA + TVDDE | (Note 32) | - | 6.2 | - | mA |
| SVDD (No Load) | (Note 33) | - | 3.5 | - | mA |
| VDDE | (Note 36) | - | 3.1 | 6.3 | mA |
| Power Down (PDNA pin = PDNE pin = "L") (Note 34) | | | | | |
| AVDD + PVDD + DVDD + TVDDA + TVDDE + SVDD | | - | 1 | 10 | μA |
| SVDD (Note 35) | | - | 0 | 10 | μA |
| VDDE | | | 2.4 | 8 | μA |

Note 32. EXT Slave Mode, fs=44.1kHz, No input, No load, PMADL = PMADR = PMDAL = PMDAR = PMPFIL = PMEQ = PMDRC = PMLO = PMRO = PMHPL = PMHPR = PMSPK = PMRCV = PMVCM bits = "1", PMPLL = PMMP1 = PMMP2 = M/S = PMOSC = PMMIX = PMSRAI = PMSRAO = PMSRBI = PMSRBO = PMPCMA = PMPCMB bits = "0".

AVDD= 3.9mA (typ), DVDD= 1.4mA (typ), PVDD= 0.75mA (typ), SVDD=3.5mA (typ), TVDD = 0.1mA (typ).

Note 33. PLL Master Mode, Audio I/F sampling frequency =44.1kHz, PCM I/F A sampling frequency =16kHz, PCM I/F B sampling frequency = 8kHz, No input, No load, PMADL = PMADR = PMDAL = PMDAR = PMPFIL = PMEQ = PMDRC = PMLO = PMRO = PMHPL = PMHPR = PMSPK = PMRCV = PMVCM = PMPLL = PMMP1 = PMMP2 = M/S = PMOSC = PMMIX = PMSRAI = PMSRAO = PMSRBI = PMSRBO = PMPCMA = PMPCMB bits = "1". PLL Reference Clock = MCKI = 11.2896MHz. In this case, output current of the MPWR1 and MPWR2 pins are 0mA.

AVDD= 4.6mA (typ), DVDD= 4.0mA (typ), PVDD= 0.78mA (typ), SVDD=4.2mA (typ), TVDD = 0.2mA (typ)

Note 34. All digital input pins are fixed to each supply pin TVDDA, TVDDE or VSS2, VSS4.

Note 35. AVDD, DVDD, PVDD, TVDDA, VDDE and TVDDE are powered OFF.

Note 36. fs=8 kHz 16 bit (FSD bits=0h, LAW bits = 0h, DIFD bit = 3h, TESTC bits = 1h, DSP running with programmed connecting DIN1 with DOUT2 and DIN2 with DOUT1.

■ Power Consumption for Each Operation Mode

Condition: Ta=25°C; AVDD=DVDD=PVDD=TVDD =1.8V, SVDD=4.2V; VDEE=1.2V,

VSS1=VSS2=VSS3=VSS4=VSS5=0V; fs=44.1kHz; fs2=16kHz, fs3=8kHz, External Slave Mode,

BICK=64fs; No data input, Receiver / Speaker / Headphone = No Load.

| Mode | AVDD [mA] | DVDD+PVDD [mA] | TVDD [mA] | SVDD [mA] | Total Power [mW] |
|--|--------------|-------------------|--------------|--------------|---------------------|
| LIN1/RIN1 → ADC (Note 37) | 1.93 | 0.74 | 0.1 | 0.003 | 5.0 |
| DAC → Lineout (Note 38) | 1.27 | 0.46 | 0.02 | 0.9 | 6.9 |
| DAC → HP (Note 39) | 0.82 | 1.21 | 0.02 | 0.003 | 3.7 |
| DAC → RCV (Note 40) | 1.22 | 0.44 | 0.02 | 1.3 | 8.5 |
| DAC → SPK (Note 41) | 1.75 | 0.44 | 0.02 | 1.35 | 9.4 |
| PCM I/F A → PCM I/F B & PCM I/F B → PCM I/F A (Note 42) | 0.21 | 1.19 | 0.1 | 0.003 | 2.7 |

Note 37. PMVCM = PMADL = PMADR bits = "1", PFSDO bit = "0"

Note 38. PMVCM = PMDAL = PMDAR = PMLO = PMRO bits = "1", DASEL1-0 bits = "10"

Note 39. PMVCM = PMDAL = PMDAR = PMHPL = PMHPR bits = "1", DASEL1-0 bits = "10"

Note 40. PMVCM = PMDAL = PMDAR = PMRCV bits = "1", DASEL1-0 bits = "10"

Note 41. PMVCM = PMDAL = PMDAR = PMSPK bits = "1", DASEL1-0 bits = "10"

Note 42. PMVCM = PMOSC = PMPCMA = PMSRAI = PMSRAO = PMPCMB = PMSRBI = PMSRBO bits = "1"

Table 1. Power Consumption for Each Operation Mode (typ)

| |
|----------------------------|
| SRC CHARACTERISTICS |
|----------------------------|

(Ta=25°C; AVDD=PVDD= DVDD=TVDDA=TVVDE =1.8V, SVDD=4.2V, VDDE=1.2V;
VSS1=VSS2=VSS3=VSS4 =VSS5 =0V; Signal Frequency=1kHz; 16bit Data; Measurement Bandwidth=20Hz ~
FSO/2kHz; unless otherwise specified)

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|-----|------------|-----|----------|
| SRC Characteristics (SRCAI): SDTIA → SRCAI → SDTO | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Sample Rate | FSI | 8 | - | 16 | kHz |
| Output Sample Rate | FSO | 8 | - | 48 | kHz |
| THD+N (Input = 1kHz, -1dBFS, Note 43) FSO/FSI = 44.1kHz/8kHz | | - | -88 | - | dB |
| Dynamic Range (Input = 1kHz, -60dBFS, Note 43) FSO/FSI = 44.1kHz/8kHz | | - | 98 | - | dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 1/2 | | 6 | - |
| SRC Characteristics (SRCAO): SDTI → SRCAO → SDTOA | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Sample Rate | FSI | 8 | - | 48 | kHz |
| Output Sample Rate | FSO | 8 | - | 16 | kHz |
| THD+N (Input = 1kHz, -1dBFS, Note 43) FSO/FSI = 8kHz/44.1kHz FSO/FSI = 16kHz /8kHz | | - | -75 -88 | - | dB dB |
| Dynamic Range (Input = 1kHz, -60dBFS, Note 43) FSO/FSI = 8kHz/44.1kHz FSO/FSI = 16kHz /8kHz | | - | 100 99 | - | dB dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 1/6 | | 2 | - |
| SRC Characteristics (SRCBI, SRCBO): SDTI → SRCBO → SDTOB, SDTIB → SRCBI → SDTO | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Sample Rate | FSI | 8 | - | 48 | kHz |
| Output Sample Rate | FSO | 8 | - | 48 | kHz |
| THD+N (Input = 1kHz, -1dBFS, Note 43) FSO/FSI = 8kHz/44.1kHz FSO/FSI = 44.1kHz/8kHz | | - | -75 -88 | - | dB dB |
| Dynamic Range (Input = 1kHz, -60dBFS, Note 43) FSO/FSI = 8kHz/44.1kHz FSO/FSI = 44.1kHz/8kHz | | - | 100 99 | - | dB dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 1/6 | | 6 | - |

Note 43. Measured by Audio Precision System Two Cascade.

| FILTER CHARACTERISTICS (CODEC) | | | | | | |
|---|---------|------|------|-------|------|------|
| (Ta=25°C; AVDD = PVDD =DVDD=1.7 ~ 2.0V; SVDD=3.0 ~ 5.5V, TVDDA=TVDDDE=1.6 ~ 3.6V, VDDE=1.1~1.3V; fs=44.1kHz; Programmable Filter=OFF) | | | | | | |
| Parameter | Symbol | min | typ | max | Unit | |
| ADC Digital Filter (Decimation LPF): | | | | | | |
| Passband (Note 44) | ±0.16dB | PB | 0 | - | 17.3 | kHz |
| | -0.66dB | | - | 19.4 | - | kHz |
| | -1.1dB | | - | 19.9 | - | kHz |
| | -6.9dB | | - | 22.1 | - | kHz |
| Stopband (Note 44) | SB | 26.1 | - | - | - | kHz |
| Passband Ripple | PR | - | - | ±0.16 | - | dB |
| Stopband Attenuation | SA | 73 | - | - | - | dB |
| Group Delay (Note 45) | GD | - | 20 | - | - | 1/fs |
| Group Delay Distortion | ΔGD | - | 0 | - | - | μs |
| ADC Digital Filter (HPF): HPFC1-0 bits = "00" | | | | | | |
| Frequency Response | -3.0dB | FR | - | 3.4 | - | Hz |
| | -0.5dB | | - | 10 | - | Hz |
| | -0.1dB | | - | 22 | - | Hz |
| DAC Digital Filter (LPF): | | | | | | |
| Passband (Note 44) | ±0.05dB | PB | 0 | - | 20.0 | kHz |
| | -6.0dB | | - | 22.05 | - | kHz |
| Stopband (Note 44) | SB | 24.1 | - | - | - | kHz |
| Passband Ripple | PR | - | - | ±0.05 | - | dB |
| Stopband Attenuation | SA | 54 | - | - | - | dB |
| Group Delay (Note 45) | GD | - | 25 | - | - | 1/fs |
| DAC Digital Filter (LPF) + SCF + SMF: | | | | | | |
| Frequency Response: 0 ~ 20.0kHz | FR | - | ±1.0 | - | - | dB |

Note 44. The passband and stopband frequencies scale with fs (system sampling rate).

For example, DAC is PB=0.454 x fs (@±0.05dB). Each response refers to that of 1kHz.

Note 45. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes group delay of the HPF and Programmable filter. For the DAC, this time is from setting the 24-bit data of both channels from the input register to the output of analog signal and includes selector block (SDMIN, PFMXL/R and SRMXL/R), DRC, 5-band EQ and DATT-A. For the signal through the programmable filters, group delay is increased 4/fs at Playback Mode from the value above if there is no phase changed by the IIR filter.

| |
|-------------------------------------|
| FILTER CHARACTERISTICS (SRC) |
|-------------------------------------|

(Ta=25°C; AVDD = PVDD =DVDD=1.7 ~ 2.0V; SVDD=3.0 ~ 5.5V, TVDDA=TVVDE=1.6 ~ 3.6V, VDDE=1.1~1.3V; Programmable Filter=OFF)

| Parameter | | Symbol | min | typ | max | Unit | |
|---|--------------------------------------|--|-----------|---|-----------|-----------|-----|
| Digital Filter | | | | | | | |
| Passband | -0.23dB | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | PB | 0 | - | 0.4583FSI | kHz |
| | -0.20dB | $0.905 \leq \text{FSO/FSI} < 0.985$ | PB | 0 | - | 0.4167FSI | kHz |
| | -0.13dB | $0.714 \leq \text{FSO/FSI} < 0.905$ | PB | 0 | - | 0.3104FSI | kHz |
| | -0.11dB | $0.656 \leq \text{FSO/FSI} < 0.714$ | PB | 0 | - | 0.2813FSI | kHz |
| | -0.10dB | $0.492 \leq \text{FSO/FSI} < 0.656$ | PB | 0 | - | 0.2167FSI | kHz |
| | -0.09dB | $0.452 \leq \text{FSO/FSI} < 0.492$ | PB | 0 | - | 0.1948FSI | kHz |
| | -0.07dB | $0.357 \leq \text{FSO/FSI} < 0.452$ | PB | 0 | - | 0.1458FSI | kHz |
| | -0.07dB | $0.324 \leq \text{FSO/FSI} < 0.357$ | PB | 0 | - | 0.1271FSI | kHz |
| | -0.06dB | $0.226 \leq \text{FSO/FSI} < 0.324$ | PB | 0 | - | 0.0729FSI | kHz |
| -0.17dB | $0.1667 \leq \text{FSO/FSI} < 0.226$ | PB | 0 | - | 0.0625FSI | kHz | |
| Stopband | | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | SB | 0.5417FSI | - | - | kHz |
| | | $0.905 \leq \text{FSO/FSI} < 0.985$ | SB | 0.5021FSI | - | - | kHz |
| | | $0.714 \leq \text{FSO/FSI} < 0.905$ | SB | 0.3958FSI | - | - | kHz |
| | | $0.656 \leq \text{FSO/FSI} < 0.714$ | SB | 0.3667FSI | - | - | kHz |
| | | $0.492 \leq \text{FSO/FSI} < 0.656$ | SB | 0.3021FSI | - | - | kHz |
| | | $0.452 \leq \text{FSO/FSI} < 0.492$ | SB | 0.2802FSI | - | - | kHz |
| | | $0.357 \leq \text{FSO/FSI} < 0.452$ | SB | 0.2313FSI | - | - | kHz |
| | | $0.324 \leq \text{FSO/FSI} < 0.357$ | SB | 0.2125FSI | - | - | kHz |
| | | $0.226 \leq \text{FSO/FSI} < 0.324$ | SB | 0.1583FSI | - | - | kHz |
| | $0.1667 \leq \text{FSO/FSI} < 0.226$ | SB | 0.1271FSI | - | - | kHz | |
| Stopband Attenuation | | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | SA | 87.0 | - | - | dB |
| | | $0.905 \leq \text{FSO/FSI} < 0.985$ | SA | 88.0 | - | - | dB |
| | | $0.714 \leq \text{FSO/FSI} < 0.905$ | SA | 87.5 | - | - | dB |
| | | $0.656 \leq \text{FSO/FSI} < 0.714$ | SA | 86.8 | - | - | dB |
| | | $0.492 \leq \text{FSO/FSI} < 0.656$ | SA | 86.4 | - | - | dB |
| | | $0.452 \leq \text{FSO/FSI} < 0.492$ | SA | 86.0 | - | - | dB |
| | | $0.357 \leq \text{FSO/FSI} < 0.452$ | SA | 86.6 | - | - | dB |
| | | $0.324 \leq \text{FSO/FSI} < 0.357$ | SA | 86.1 | - | - | dB |
| | | $0.226 \leq \text{FSO/FSI} < 0.324$ | SA | 85.7 | - | - | dB |
| | $0.1667 \leq \text{FSO/FSI} < 0.226$ | SA | 72.8 | - | - | dB | |
| Group Delay (Note 46) | | | | | | | |
| PCM I/F A → PCM I/F B | (PMMIX bit="0") | GD | - | $30/\text{fs}2+10.5/\text{fs}3$ | - | s | |
| | (PMMIX bit="1") | GD | - | $29.5/\text{fs}2+37.5/\text{fs}3+9.5/\text{fs}$ | - | s | |
| PCM I/F B → PCM I/F A | (PMMIX bit="0") | GD | - | $30/\text{fs}2+10.5/\text{fs}3$ | - | s | |
| | (PMMIX bit="1") | GD | - | $29.5/\text{fs}2+37.5/\text{fs}3+9.5/\text{fs}$ | - | s | |
| PCM I/F A → SDTO | | GD | - | $29.5/\text{fs}2+11.5/\text{fs}$ | - | s | |
| PCM I/F B → SDTO | | GD | - | $29.5/\text{fs}2+12.5/\text{fs}$ | - | s | |
| PCM I/F A → 5-band EQ → DATT-A → DRC → DAC Digital Output (Note 47) | | GD | - | $29.5/\text{fs}2+32.5/\text{fs}$ | - | s | |
| PCM I/F B → 5-band EQ → DATT-A → DRC → DAC Digital Output (Note 47) | | GD | - | $29.5/\text{fs}2+33.5/\text{fs}$ | - | s | |

Note 46. This value is the time from the rising edge of LRCK, SYNCA or SYNCB after data is input to rising edge of LRCK after data is output, when LRCK, SYNCA or SYNCB for Output data corresponds with SYNCA or SYNCB for Input.

fs: LRCK Frequency, fs2: SYNCA Frequency, fs3: SYNCB Frequency.

Note 47. This value includes group delay of DAC digital filter.

DC CHARACTERISTICS

(Ta=25°C; AVDD = PVDD =DVDD=1.7 ~ 2.0V, VDDE=1.2V; SVDD=3.0 ~ 5.5V, TVDDA =TVDDE=1.6 ~ 3.6V)

| Parameter | | Symbol | min | typ | max | Unit |
|---|-----------------|--------|-----------|-----|----------|------|
| High-Level Input Voltage (Note 48) | 2.2V≤TVDDA≤3.6V | VIH1 | 70%TVDDA | - | - | V |
| | 1.6V≤TVDDA<2.2V | VIH1 | 80%TVDDA | - | - | V |
| Low-Level Input Voltage (Note 48) | 2.2V≤TVDDA≤3.6V | VIL1 | - | - | 30%TVDDA | V |
| | 1.6V≤TVDDA<2.2V | VIL1 | - | - | 20%TVDDA | V |
| High-Level Output Voltage (Note 49)(Iout=-200μA) | | VOH1 | TVDDA-0.2 | - | - | V |
| Low-Level Output Voltage (Note 49)(Iout=200μA) (SDAA pin, 2.0V≤TVDDA≤3.6V: Iout=3mA) (SDAA pin, 1.6V≤TVDDA<2.0V: Iout=3mA) | | VOL1 | - | - | 0.2 | V |
| | | VOL2 | - | - | 0.4 | V |
| | | VOL2 | - | - | 20%TVDDA | V |
| | | VOL2 | - | - | 20%TVDDA | V |
| Input Leakage Current (Note 50) | | Iind | - | - | ±2 | μA |
| Digital MIC Interface (DMDAT pin Input; DMIC bit = "1") | | | | | | |
| High-Level Input Voltage | | VIH3 | 65%AVDD | - | - | V |
| Low-Level Input Voltage | | VIL3 | - | - | 35%AVDD | V |
| Digital MIC Interface (DMCLK pin Output; DMIC bit = "1") | | | | | | |
| High-Level Output Voltage (Iout=-80μA) | | VOH3 | AVDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout= 80μA) | | VOL3 | - | - | 0.4 | V |
| Input Leakage Current (Note 50) | | Iin | - | - | ±10 | μA |

Note 48. BICK, LRCK, SDTI, MCKI, PDNA, BICKA, SYNCA, SDTIA, BICKB, SYNCB, SDTIB, SCLA and SDAA pins.

Note 49. BICK, LRCK SDTO, SDTOA and SDTOB pins

Note 50. SYNCB, BICKB, SDTIB, SDTI, LRCK, MCKI, BICK, SCLA, SDAA, SDTIA, BICKA and SYNCA pins.
I/O pins (LRCK, BICK and SDAA pins) are at the time of Input state.

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----------|-----|----------|------|
| High level input voltage | VIH | 70%TVDDE | - | - | V |
| Low level input voltage | VIL | - | - | 30%TVDDE | V |
| High level output voltage Iout=-200μA (Note 51) | VOH | TVDDE-0.2 | - | - | V |
| Low level output voltage Iout= 200μA (Note 51) | VOL | - | - | 0.2 | V |
| Low-level Output Voltage (SDAE pin, TVDDE ≥ 2.0V: Iout=3mA) (SDAE pin, TVDDE < 2.0V: Iout=3mA) | VOL | - | - | 0.4 | V |
| | VOL | - | - | 20%TVDDE | V |
| Input leakage current | Iin | - | - | ±10 | μA |

Note 51. Except for the SDAE pin.

| |
|----------------------------------|
| SWITCHING CHARACTERISTICS |
|----------------------------------|

(Ta=25°C; AVDD=DVDD=PVDD=1.7 ~ 2.0V, VDDE=1.1~1.3V, TVDDA=TVDDE=1.6 ~3 .6V, SVDD=3.0 ~ 5.5V; CL=20pF or 400pF (SDAA, SDAE pin); unless otherwise specified)

| Parameter | Symbol | min | typ | max | Unit |
|---|----------------------|------------|------|-------------|------|
| PLL Master Mode (PLL Reference Clock = MCKI pin) | | | | | |
| MCKI Input Timing | | | | | |
| Frequency | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns |
| LRCK Output Timing | | | | | |
| Frequency | fs | 8 | - | 48 | kHz |
| DSP Mode: Pulse Width High | tLRCKH | - | tBCK | - | ns |
| Except DSP Mode: Duty Cycle | Duty | - | 50 | - | % |
| BICK Output Timing | | | | | |
| Period | BCKO bit = "0" | tBCK | - | 1/(32fs) | ns |
| | BCKO bit = "1" | tBCK | - | 1/(64fs) | ns |
| Duty Cycle | dBCK | - | 50 | - | % |
| PLL Slave Mode (PLL Reference Clock = BICK pin) | | | | | |
| LRCK Input Timing | | | | | |
| Frequency | fs | 8 | - | 48 | kHz |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | ns |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % |
| BICK Input Timing | | | | | |
| Period | PLL3-0 bits = "0010" | tBCK | - | 1/(32fs) | ns |
| | PLL3-0 bits = "0011" | tBCK | - | 1/(64fs) | ns |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns |

| Parameter | Symbol | min | typ | max | Unit | |
|-----------------------------|----------------|----------|-------|-------------|--------|-----|
| External Slave Mode | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | 256fs | fCLK | 2.048 | - | 12.288 | MHz |
| | 512fs | fCLK | 4.096 | - | 12.288 | MHz |
| | 1024fs | fCLK | 8.192 | - | 12.288 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns | |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns | |
| LRCK Input Timing | | | | | | |
| Frequency | 256fs | fs | 8 | - | 48 | kHz |
| | 512fs | fs | 8 | - | 24 | kHz |
| | 1024fs | fs | 8 | - | 12 | kHz |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | ns | |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % | |
| BICK Input Timing | | | | | | |
| Period | tBCK | 312.5 | - | - | ns | |
| Pulse Width Low | tBCKL | 130 | - | - | ns | |
| Pulse Width High | tBCKH | 130 | - | - | ns | |
| External Master Mode | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | 256fs | fCLK | 2.048 | - | 12.288 | MHz |
| | 512fs | fCLK | 4.096 | - | 12.288 | MHz |
| | 1024fs | fCLK | 8.192 | - | 12.288 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns | |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns | |
| LRCK Output Timing | | | | | | |
| Frequency | fs | 8 | - | 48 | kHz | |
| DSP Mode: Pulse Width High | tLRCKH | - | tBCK | - | ns | |
| Except DSP Mode: Duty Cycle | Duty | - | 50 | - | % | |
| BICK Output Timing | | | | | | |
| Period | BCKO bit = "0" | tBCK | - | 1/(32fs) | ns | |
| | BCKO bit = "1" | tBCK | - | 1/(64fs) | ns | |
| Duty Cycle | dBCK | - | 50 | - | % | |

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----------------|------------|-----------------|------|
| Audio Interface Timing (DSP Mode) | | | | | |
| Master Mode | | | | | |
| LRCK “↑” to BICK “↑” (Note 52) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| LRCK “↑” to BICK “↓” (Note 53) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| BICK “↑” to SDTO (BCKP bit = “0”) | tBSD | –70 | - | 70 | ns |
| BICK “↓” to SDTO (BCKP bit = “1”) | tBSD | –70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Slave Mode | | | | | |
| LRCK “↑” to BICK “↑” (Note 52) | tLRB | 0.4 x tBCK | - | - | ns |
| LRCK “↑” to BICK “↓” (Note 53) | tLRB | 0.4 x tBCK | - | - | ns |
| BICK “↑” to LRCK “↑” (Note 52) | tBLR | 0.4 x tBCK | - | - | ns |
| BICK “↓” to LRCK “↑” (Note 53) | tBLR | 0.4 x tBCK | - | - | ns |
| BICK “↑” to SDTO (BCKP bit = “0”) | tBSD | - | - | 80 | ns |
| BICK “↓” to SDTO (BCKP bit = “1”) | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Audio Interface Timing (Right/Left justified & I²S) | | | | | |
| Master Mode | | | | | |
| BICK “↓” to LRCK Edge (Note 54) | tMBLR | –40 | - | 40 | ns |
| LRCK Edge to SDTO (MSB) (Except I ² S mode) | tLRD | –70 | - | 70 | ns |
| BICK “↓” to SDTO | tBSD | –70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Slave Mode | | | | | |
| LRCK Edge to BICK “↑” (Note 54) | tLRB | 50 | - | - | ns |
| BICK “↑” to LRCK Edge (Note 54) | tBLR | 50 | - | - | ns |
| LRCK Edge to SDTO (MSB) (Except I ² S mode) | tLRD | - | - | 80 | ns |
| BICK “↓” to SDTO | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

Note 52. MSBS, BCKP bits = “00” or “11”.

Note 53. MSBS, BCKP bits = “01” or “10”.

Note 54. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-------------|-----|------|------|
| PCM Interface Timing (BICKA, SYNCA, SDTIA, SDTOA pins): | | | | | |
| SYNCA Timing | | | | | |
| Frequency | fs2 | 8 | - | 16 | kHz |
| Serial Interface Timing at Short/long Frame Sync | | | | | |
| BICKA Frequency | fBCK2 | 128 | - | 4096 | kHz |
| BICKA Period | tBCK2 | 244 | - | - | ns |
| BICKA Pulse Width Low | tBCKL2 | 100 | - | - | ns |
| Pulse Width High | tBCKH2 | 100 | - | - | ns |
| SYNCA Edge to BICKA “↓” (Note 55) | tSYB2 | 40 | - | - | ns |
| SYNCA Edge to BICKA “↑” (Note 56) | tSYB2 | 40 | - | - | ns |
| BICKA “↓” to SYNCA Edge (Note 55) | tBSY2 | 40 | - | - | ns |
| BICKA “↑” to SYNCA Edge (Note 56) | tBSY2 | 40 | - | - | ns |
| SYNCA to SDTOA (MSB) (Except Short Frame) | tSYD2 | - | - | 60 | ns |
| BICKA “↑” to SDTOA (BCKPA bit = “0”) | tBSD2 | - | - | 60 | ns |
| BICKA “↓” to SDTOA (BCKPA bit = “1”) | tBSD2 | - | - | 60 | ns |
| SDTIA Hold Time | tSDH2 | 25 | - | - | ns |
| SDTIA Setup Time | tSDS2 | 25 | - | - | ns |
| SYNCA Pulse Width Low | tSYL2 | 0.8 x tBCK2 | - | - | ns |
| Pulse Width High | tSYH2 | 0.8 x tBCK2 | - | - | ns |
| Serial Interface Timing at MSB justified and I²S | | | | | |
| BICKA Frequency | fBCK2 | 256 | - | 3072 | kHz |
| BICKA Period | tBCK2 | 312.5 | - | - | ns |
| BICKA Pulse Width Low | tBCKL2 | 130 | - | - | ns |
| Pulse Width High | tBCKH2 | 130 | - | - | ns |
| SYNCA Edge to BICKA “↑” | tSYB2 | 50 | - | - | ns |
| BICKA “↑” to SYNCA Edge | tBSY2 | 50 | - | - | ns |
| SYNCA to SDTOA (MSB) (Except I ² S mode) | tSYD2 | - | - | 80 | ns |
| BICKA “↓” to SDTOA | tBSD2 | - | - | 80 | ns |
| SDTIA Hold Time | tSDH2 | 50 | - | - | ns |
| SDTIA Setup Time | tSDS2 | 50 | - | - | ns |
| SYNCA Duty Cycle | dSYC2 | 45 | 50 | 55 | % |

Note 55. MSBSA, BCKPA bits = “00” or “11”.

Note 56. MSBSA, BCKPA bits = “01” or “10”.

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-------------|-----|------|------|
| PCM Interface Timing (BICKB, SYNCB, SDTIB, SDTOB pins): | | | | | |
| SYNCB Timing | | | | | |
| Frequency | fs3 | 8 | - | 48 | kHz |
| Serial Interface Timing at Short/long Frame Sync | | | | | |
| BICKB Frequency | fBCK3 | 128 | - | 4096 | kHz |
| BICKB Period | tBCK3 | 244 | - | - | ns |
| BICKB Pulse Width Low | tBCKL3 | 100 | - | - | ns |
| Pulse Width High | tBCKH3 | 100 | - | - | ns |
| SYNCB Edge to BICKB “↓” (Note 57) | tSYB3 | 40 | - | - | ns |
| SYNCB Edge to BICKB “↑” (Note 58) | tSYB3 | 40 | - | - | ns |
| BICKB “↓” to SYNCB Edge (Note 57) | tBSY3 | 40 | - | - | ns |
| BICKB “↑” to SYNCB Edge (Note 58) | tBSY3 | 40 | - | - | ns |
| SYNCB to SDTOB (MSB) (Except Short Frame) | tSYD3 | - | - | 60 | ns |
| BICKB “↑” to SDTOB (BCKPB bit = “0”) | tBSD3 | - | - | 60 | ns |
| BICKB “↓” to SDTOB (BCKPB bit = “1”) | tBSD3 | - | - | 60 | ns |
| SDTIB Hold Time | tSDH3 | 25 | - | - | ns |
| SDTIB Setup Time | tSDS3 | 25 | - | - | ns |
| SYNCB Pulse Width Low | tSYL3 | 0.8 x tBCK3 | - | - | ns |
| Pulse Width High | tSYH3 | 0.8 x tBCK3 | - | - | ns |
| Serial Interface Timing at MSB justified and I²S | | | | | |
| BICKB Frequency | fBCK3 | 256 | - | 3072 | kHz |
| BICKB Period | tBCK3 | 312.5 | - | - | ns |
| BICKB Pulse Width Low | tBCKL3 | 130 | - | - | ns |
| Pulse Width High | tBCKH3 | 130 | - | - | ns |
| SYNCB Edge to BICKB “↑” | tSYB3 | 50 | - | - | ns |
| BICKB “↑” to SYNCB Edge | tBSY3 | 50 | - | - | ns |
| SYNCB to SDTOB (MSB) (Except I ² S mode) | tSYD3 | - | - | 80 | ns |
| BICKB “↓” to SDTOB | tBSD3 | - | - | 80 | ns |
| SDTIB Hold Time | tSDH3 | 50 | - | - | ns |
| SDTIB Setup Time | tSDS3 | 50 | - | - | ns |
| SYNCB Duty Cycle | dSYC3 | 45 | 50 | 55 | % |

Note 57. MSBSB, BCKPB bits = “00” or “11”.

Note 58. MSBSB, BCKPB bits = “01” or “10”.

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-------------|-----|------|------|
| SYNC1/3, BCLK1/BCLK3 Input Timing | | | | | |
| SYNC1/3 Input Timing | | | | | |
| SYNC1/3 frequency | fs | 8 | | 48 | kHz |
| BCLK1 Input Timing (Note 59, Note 60) | fBCLK | 64 | | 3072 | kHz |
| Pulse width Low | tBCKL1 | 0.4 x tBCLK | | | ns |
| Pulse width High | tBCKH1 | 0.4x tBCLK | | | ns |

Note 59. SYNC1 and BCLK1 or SYNC3 and BCLK3 should be synchronized and their sampling rates (fs) should be stable

Note 60. $fBCLK \geq 4 \times N \times fs$ (N=1, 2, 3....)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| SDIN1, SDIN3, SDIN4, SDOUT1, SDOUT3, SDOUT4 | | | | | |
| Delay Time from BICK1 “↑” to SYNC1 “↑” (Note 61) | tBSYD | 20 | | | ns |
| Delay Time from SYNC1 “↓” to BICK1 “↑” (Note 61) | tSYBD | 100 | | | ns |
| Serial Data Input Latch Setup Time | tB1IDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tB1IDH | 40 | | | ns |
| Delay Time from SYNC1 to Serial Data Output | tSY1OD | | | 40 | ns |
| Delay Time from BICK1 “↓” to Serial Data Output (Note 62) | tB1OD | | | 40 | ns |
| SDIN2, SDOUT2 | | | | | |
| SYNC2 Duty cycle | | | 50 | | % |
| Serial Data Input Latch Setup Time | tB2IDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tB2IDH | 40 | | | ns |
| Delay Time from SYNC2 to Serial Data Outputs | tSY2OD | | | 40 | ns |
| Delay Time from BCLK2 “↓” to Serial Data Output (Note 63) | tB2OD | | | 40 | ns |
| SDINn → SDOUTn (n=1, 2, 3, 4) | | | | | |
| Delay time from SDINn to SDOUTn Output | tIOD | | | 60 | ns |

Note 61. BICK1 edge must not occur at the same time as SYNC1 edge.

Note 62. When the polarity of BICK1 is inverted, delay time is from BICK1 “↑”.

Note 63. When the polarity of BICK2 is inverted, delay time is from BICK2 “↑”

| Parameter | Symbol | min | typ | max | Unit |
|---|---------|-----|----------|-----|-------|
| Control Interface Timing (I²C Bus mode): (Note 64, Note 65) | | | | | |
| SCL Clock Frequency | fSCL | 30 | - | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | - | - | μs |
| Clock Low Time | tLOW | 1.3 | - | - | μs |
| Clock High Time | tHIGH | 0.6 | - | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | μs |
| SDA Hold Time from SCL Falling (Note 66) | tHD:DAT | 0 | - | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | - | - | μs |
| Capacitive Load on Bus | Cb | - | - | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | - | 50 | ns |
| Digital Audio Interface Timing: C_L=100pF | | | | | |
| DMCLK Output Timing | | | | | |
| Period | tSCK | - | 1/(64fs) | - | ns |
| Rising Time | tSRise | - | - | 10 | ns |
| Falling Time | tSfall | - | - | 10 | ns |
| Duty Cycle | dSCK | 45 | 50 | 55 | % |
| Audio Interface Timing | | | | | |
| DMDAT Setup Time | tDMS | 50 | - | - | ns |
| DMDAT Hold Time | tDMH | 0 | - | - | ns |
| Power-down & Reset Timing | | | | | |
| PDNA Accept Pulse Width (Note 67) | tAPDA | 1.5 | - | - | μs |
| PDNE Accept Pulse Width (Note 67) | tAPDE | 0.6 | - | - | μs |
| PDN Reject Pulse Width (Note 67) | tRPD | - | - | 50 | ns |
| PMADL or PMADR “↑” to SDTO valid (Note 68) | | | | | |
| ADRST bit = “0” | tPDV | - | 1059 | - | 1/fs |
| ADRST bit = “1” | tPDV | - | 267 | - | 1/fs |
| PMDML or PMDMR “↑” to SDTO valid (Note 69) | | | | | |
| ADRST bit = “0” | tPDV | - | 1059 | - | 1/fs |
| ADRST bit = “1” | tPDV | - | 267 | - | 1/fs |
| PMSRAO “↑” to SDTOA valid (Note 70) | tPDV2 | - | 164 | - | 1/fs2 |
| PMSRBO “↑” to SDTOB valid (Note 71) | tPDV3 | - | 164 | - | 1/fs3 |

Note 64. SDA means both SDAA and SDAE pins. SCL means both SCLA and SCLE pins.

Note 65. I²C-bus is a registered trademark of NXP B.V.

Note 66. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 67. The audio block of AK4679 can be reset by bringing PDNA pin = “L” to “H” only upon power up. The PDNA pin must held “L” for more than 1.5μs for a certain reset. The DSP block can be reset by bringing PDNE pin = “L” to “H” only upon power up. The PDNE pin must held “L” for more than 0.6μs for a certain reset. The AK4679 is not reset by the “L” pulse less than 50ns.

Note 68. This is the count of LRCK “↑” from the PMADL or PMADR bit = “1”.

Note 69. This is the count of LRCK “↑” from the PMDML or PMDMR bit = “1”.

Note 70. This is the count of SYNCA “↑” from the PMSRAO bit = “1”.

Note 71. This is the count of SYNCB “↑” from the PMSRBO bit = “1”.

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Control Interface Timing (SPI mode) | | | | | |
| SCLK Fall Time | tSF | | | 30 | ns |
| SCLK Rise Time | tSR | | | 30 | ns |
| SCLK Frequency | fSCLK | | | 4.0 | MHz |
| SCLK Low Level Width | tSCLKL | 120 | | | ns |
| SCLK High Level Width | tSCLKH | 120 | | | ns |
| CSN High Level Width | tWRQH | 500 | | | ns |
| From CSN “↑” to PDN “↑” | tRST1 | 600 | | | ns |
| From PDN “↑” to CSN “↓” | tIRRQ | 100 | | | μs |
| From SCLK “↑” to CSN “↑” | tWSC | 500 | | | ns |
| From SCLK “↑” to CSN “↑” | tSCW | 800 | | | ns |
| SI Latch Setup Time | tSIS | 100 | | | ns |
| SI Latch Hold Time | tSIH | 100 | | | ns |
| Delay Time from SCLK “↓” to SO Output | tSOS | | | 100 | ns |
| Hold Time from SCLK “↑” to SO Output (Note 72) | tSOH | 100 | | | ns |

Note 72. Except when input the eighth bit of the command code.

■ Timing Diagram

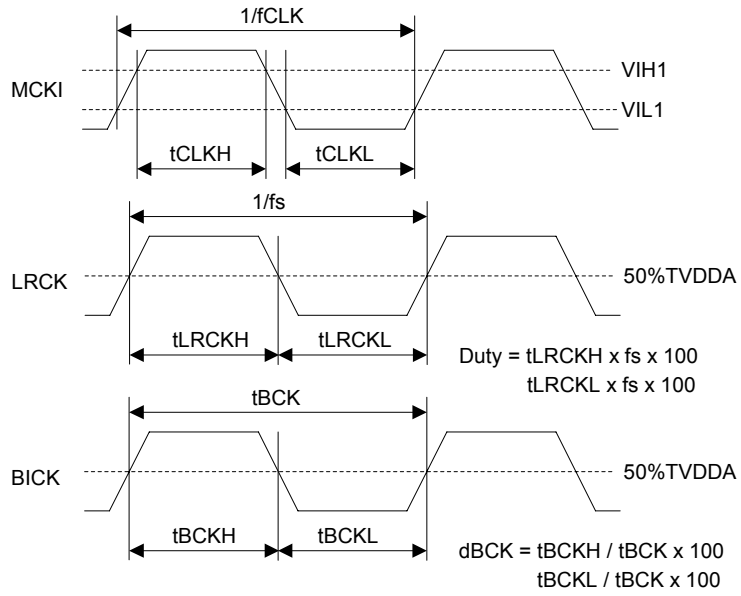


Figure 5. Clock Timing (PLL/EXT Master mode)

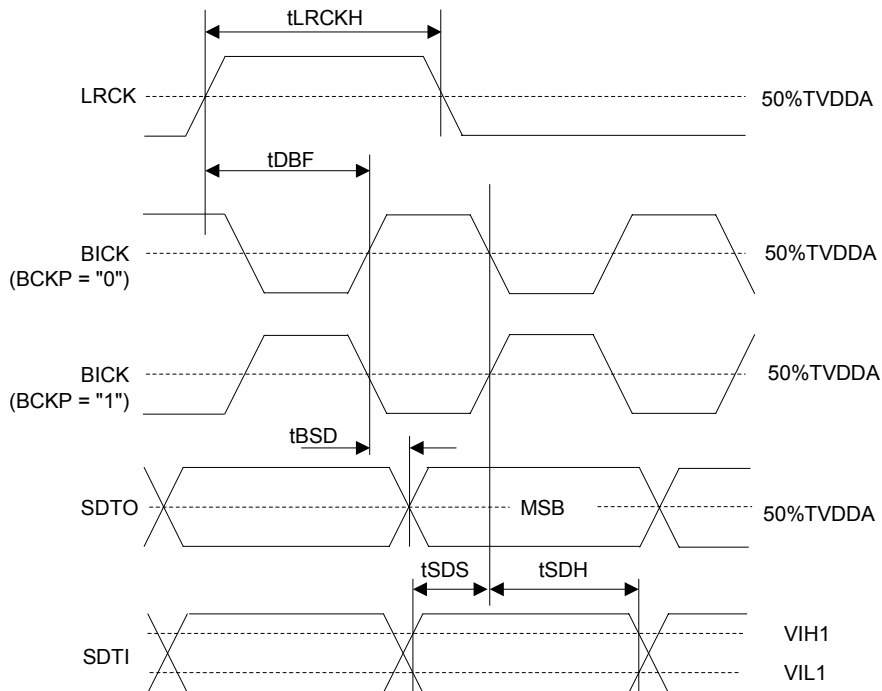


Figure 6. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= "0")

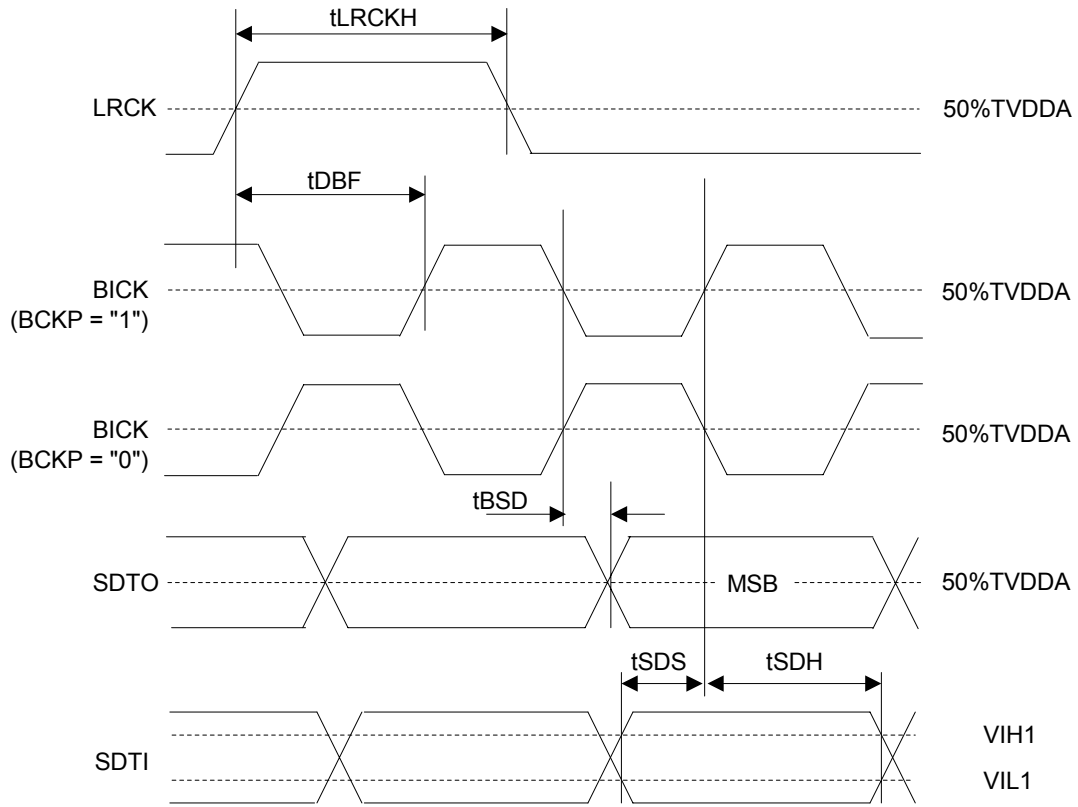


Figure 7. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= “1”)

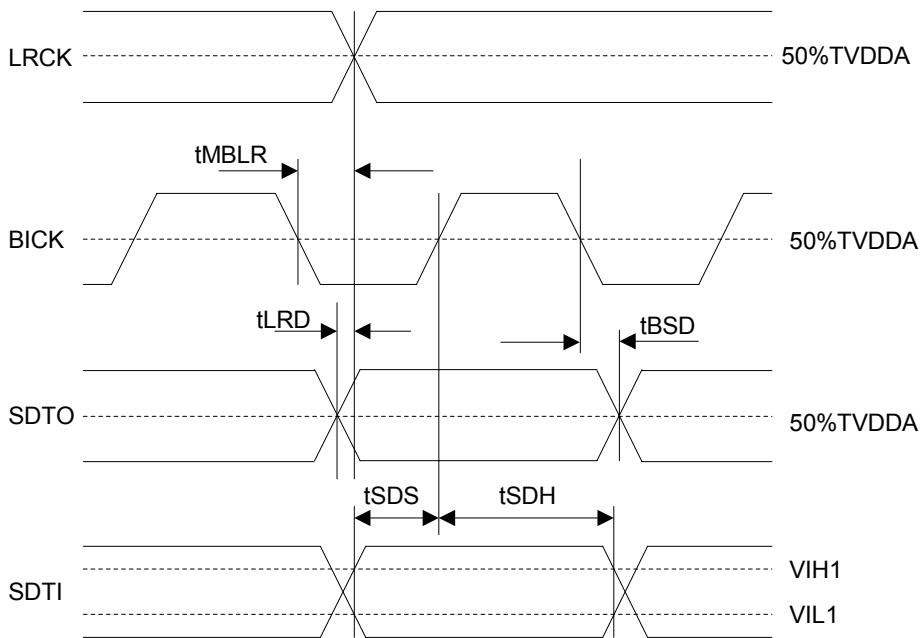


Figure 8. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

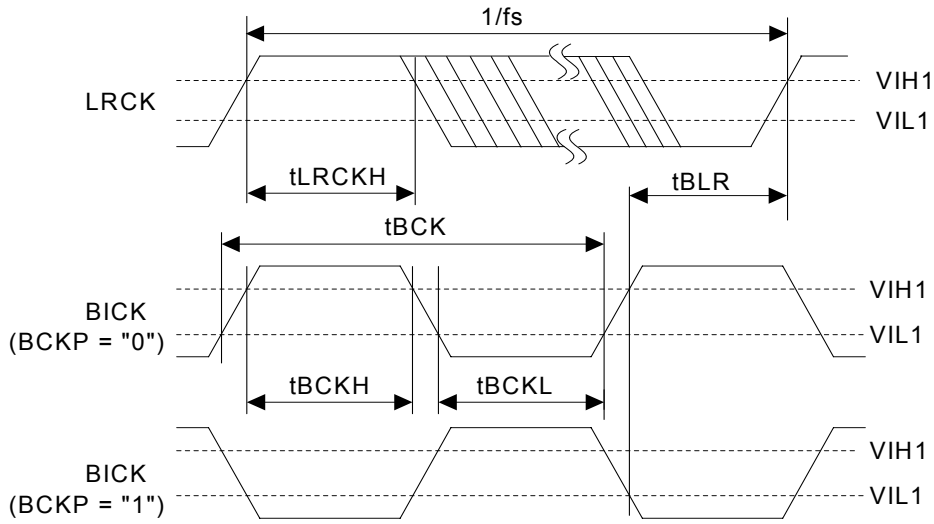


Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = BICK pin, DSP mode, MSBS bit= "0")

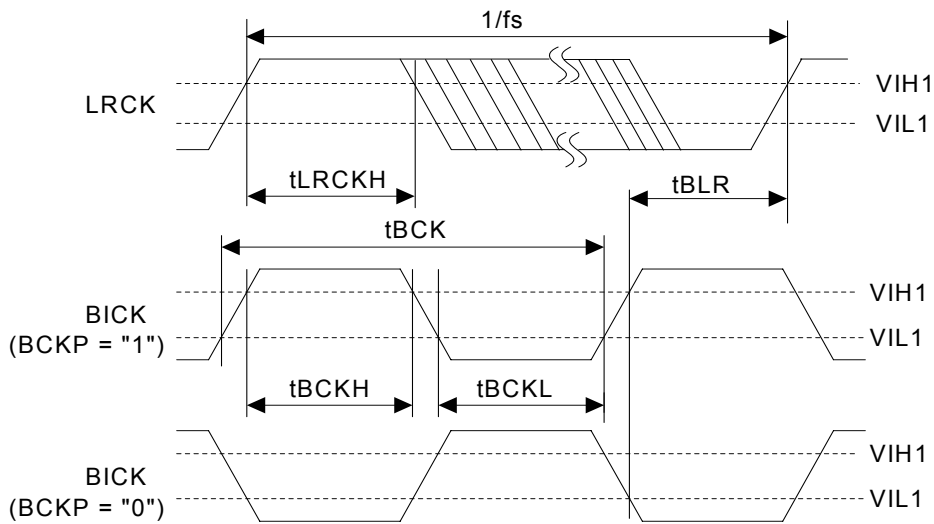


Figure 10. Clock Timing (PLL Slave mode; PLL Reference Clock = BICK pin, DSP mode, MSBS bit= "1")

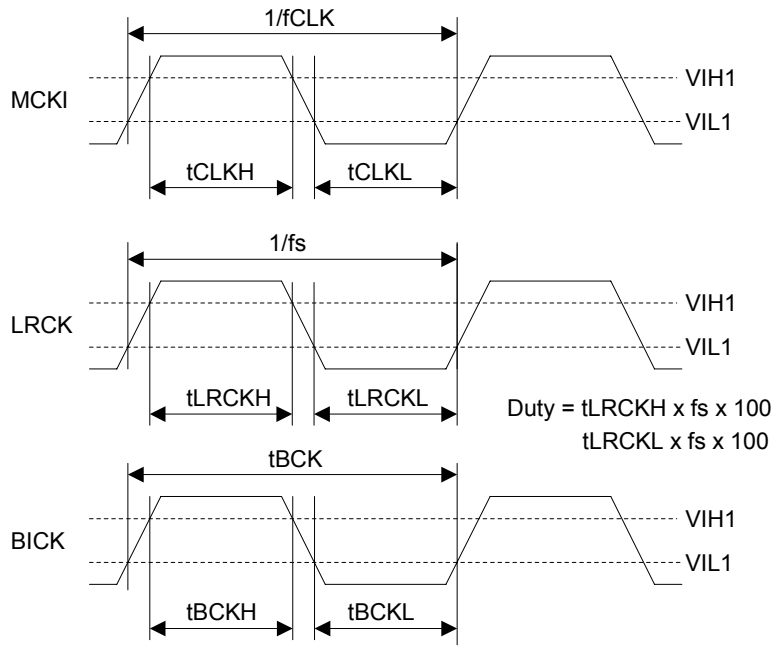


Figure 11. Clock Timing (PLL Slave mode; Except DSP mode)

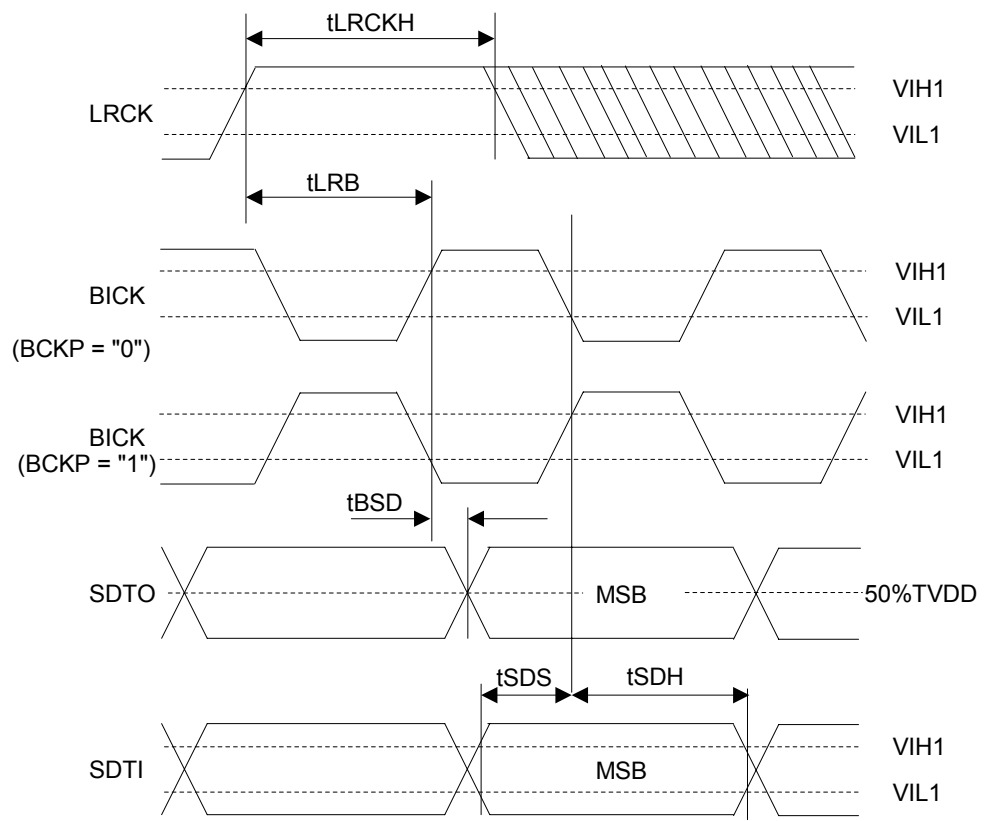


Figure 12. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS bit= "0")

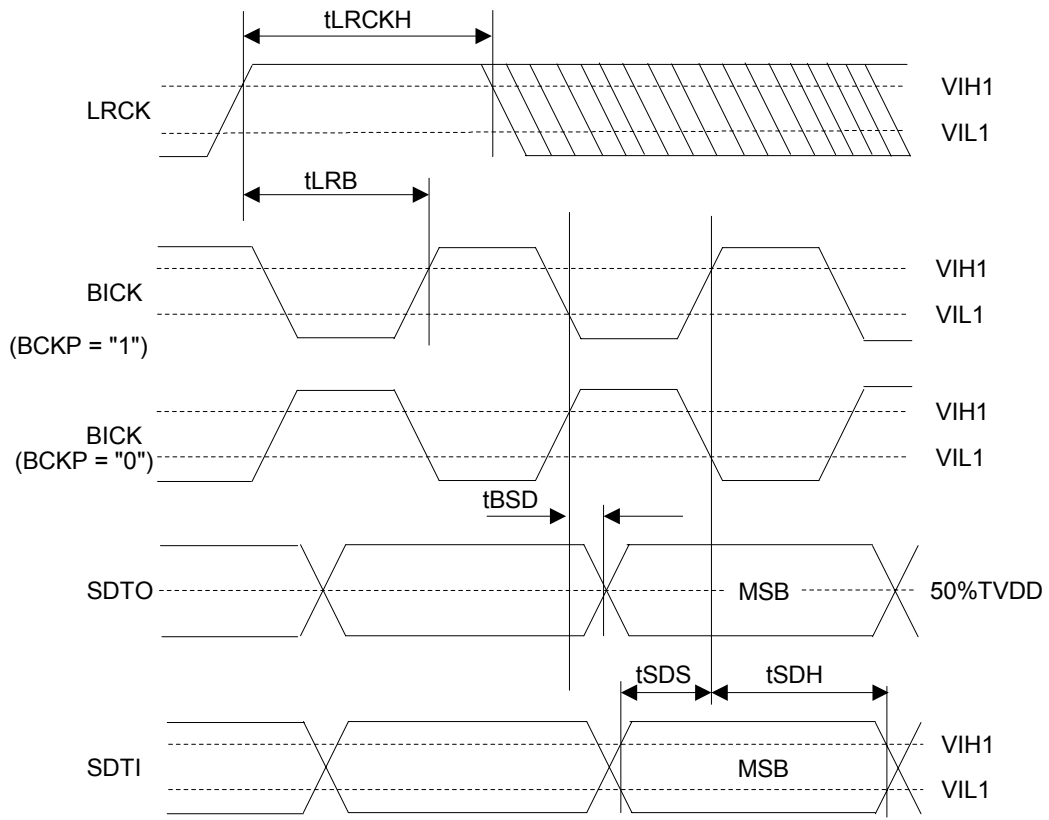


Figure 13. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS bit= "1")

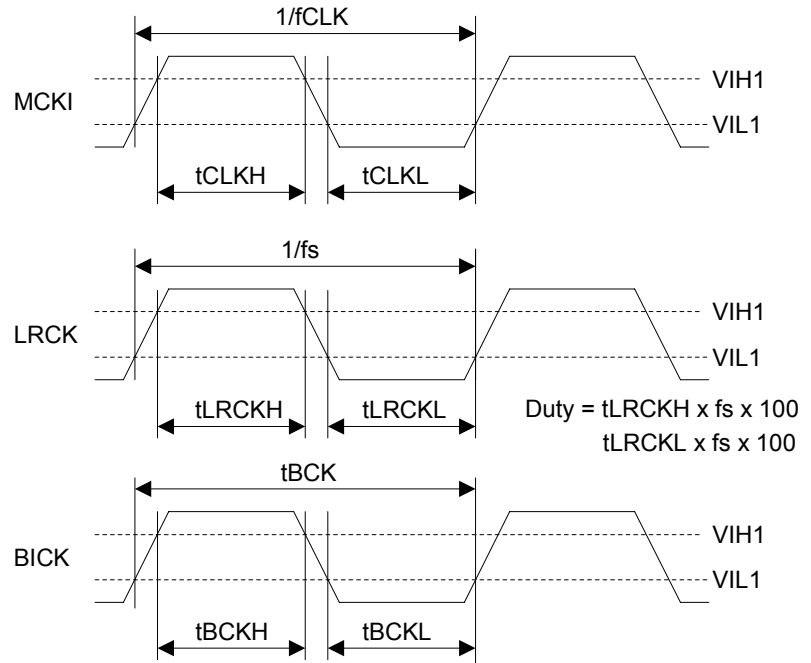


Figure 14. Clock Timing (EXT Slave mode)

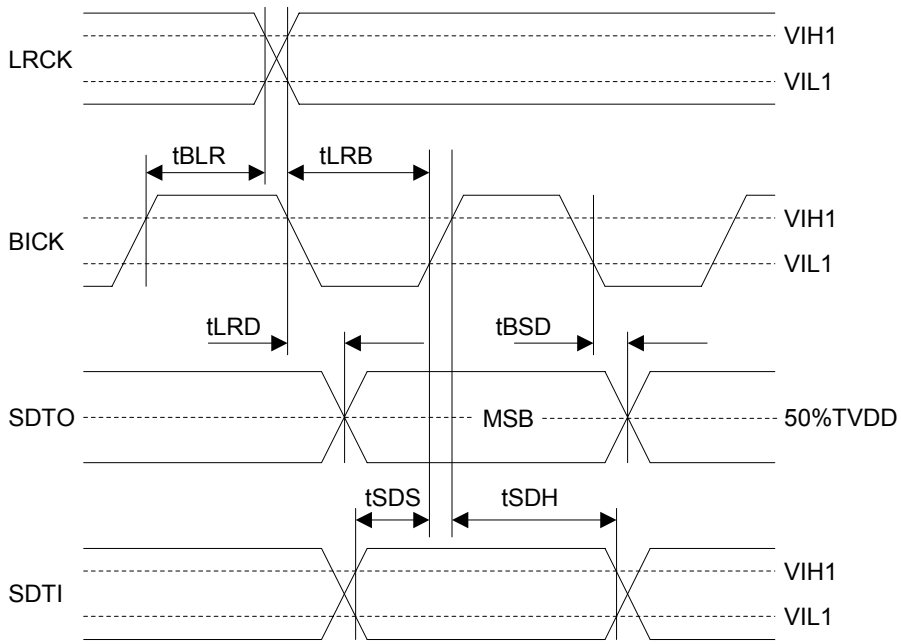


Figure 15. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

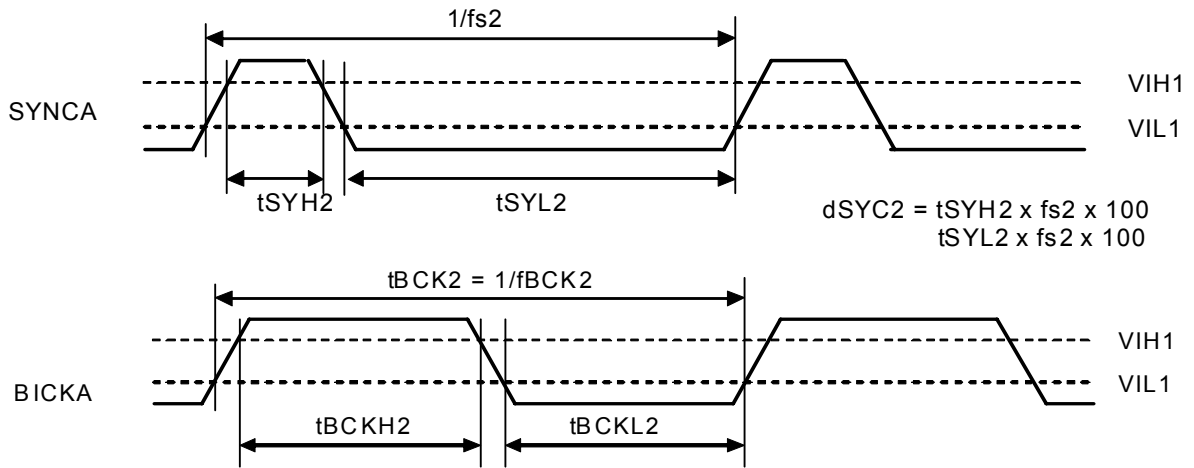


Figure 16. Clock Timing of PCM I/F A

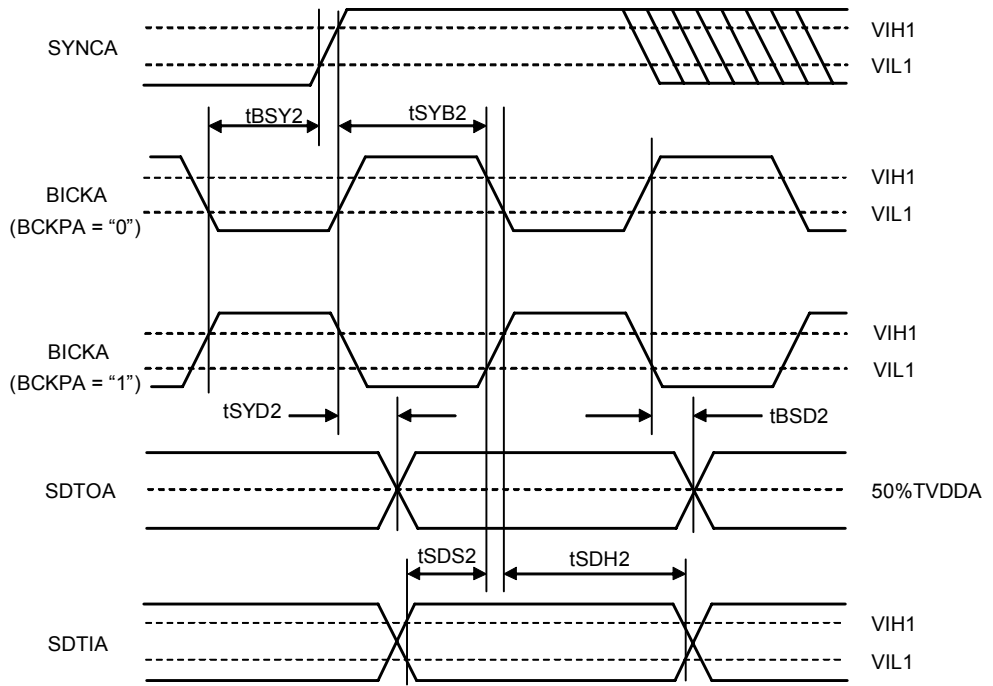


Figure 17. PCM I/F A Timing at short and long frame sync (MSBSA bit="0")

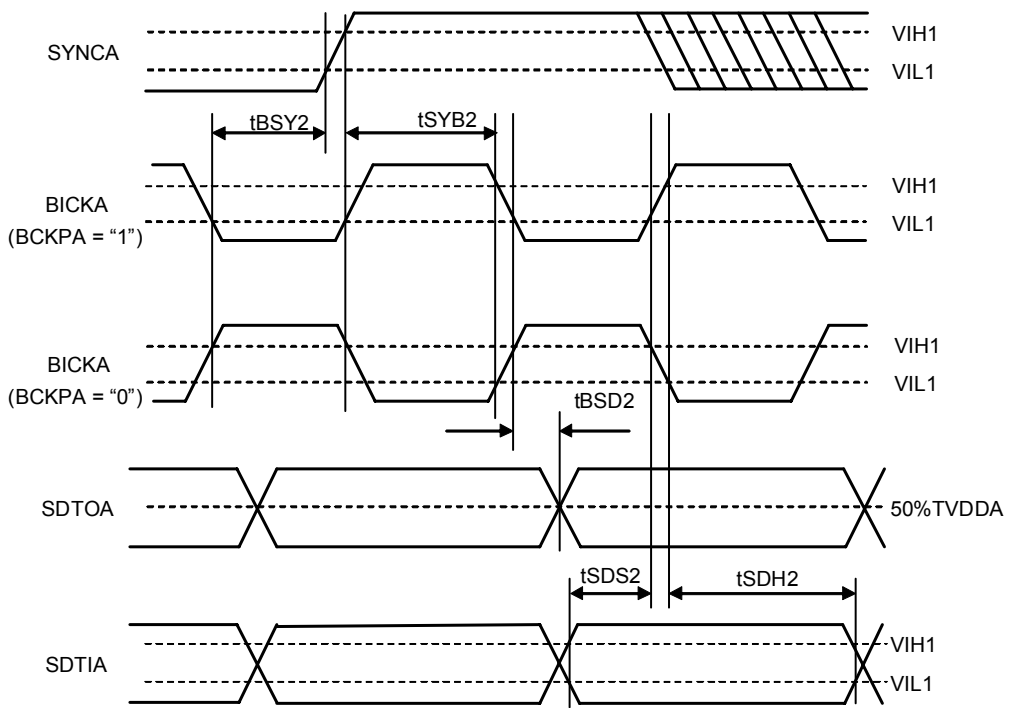


Figure 18. PCM I/F A Timing at short and long frame sync (MSBSA bit="1")

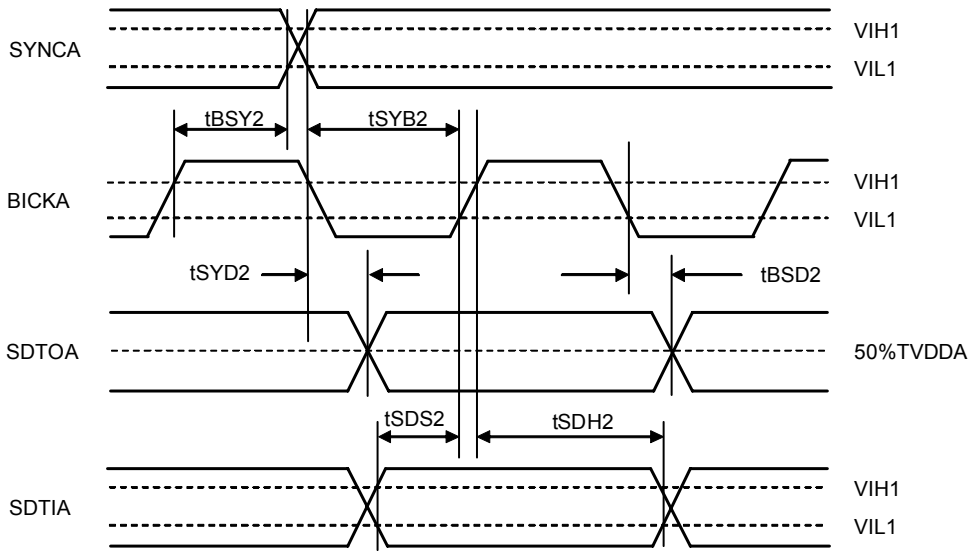


Figure 19. PCM I/F A Timing at MSB justified and I²S

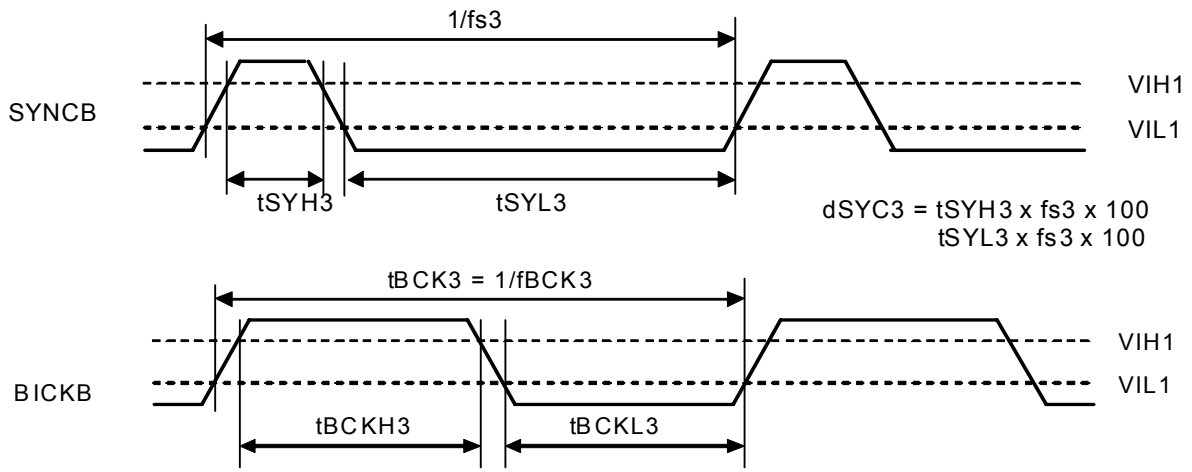


Figure 20. Clock Timing of PCM I/F B

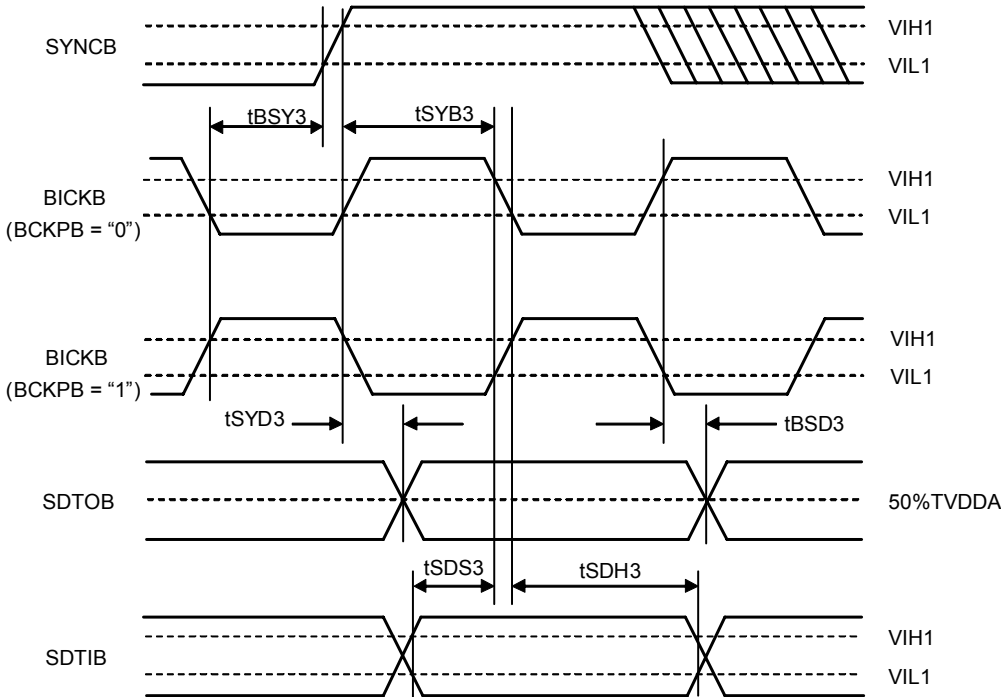


Figure 21. PCM I/F B Timing at short and long frame sync (MSBSB bit= "0")

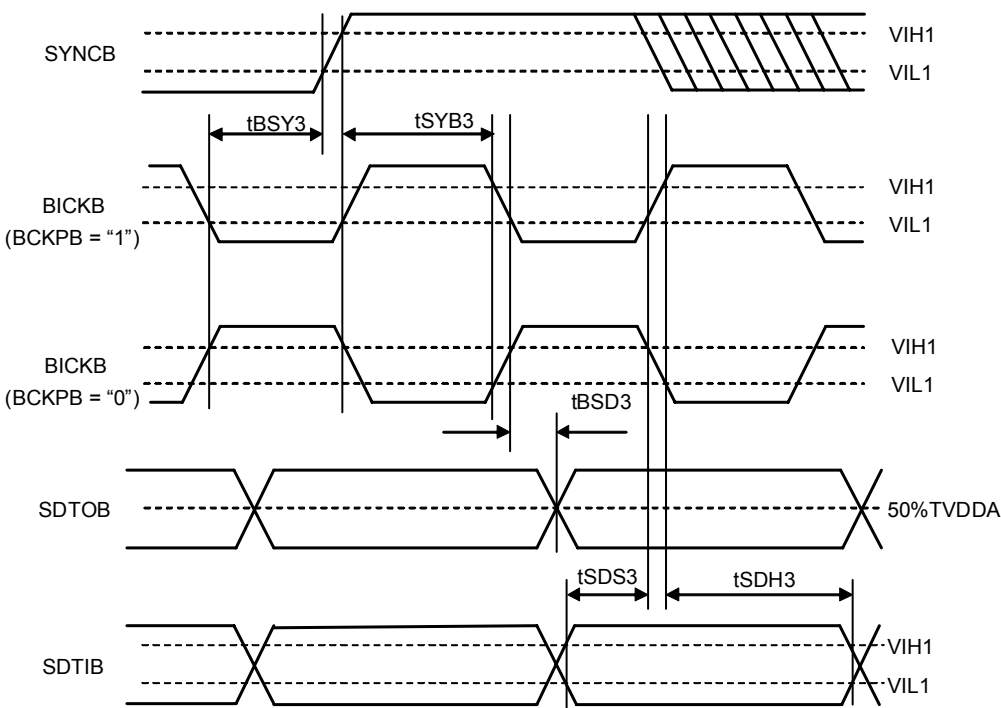


Figure 22. PCM I/F B Timing at short and long frame sync (MSBSB bit= "1")

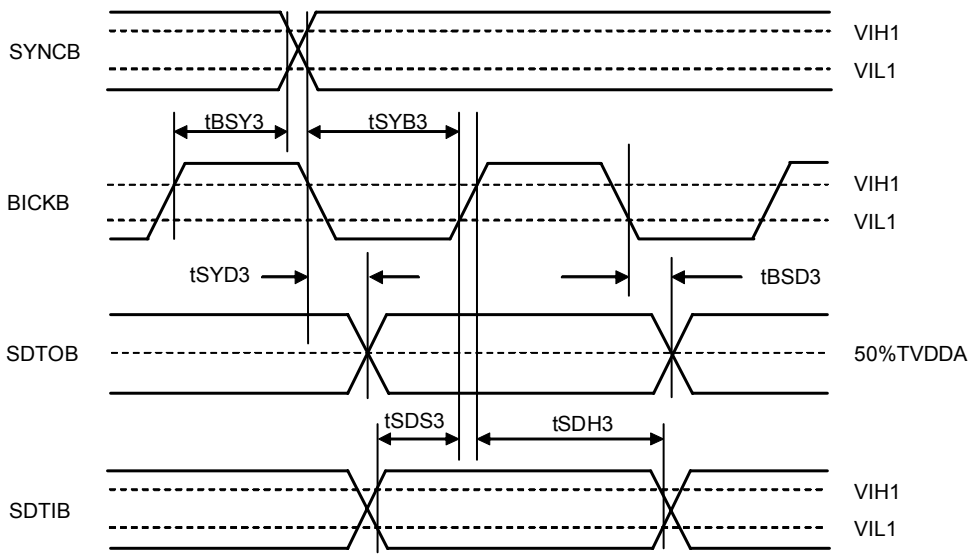


Figure 23. PCM I/F B Timing at MSB justified and I²S

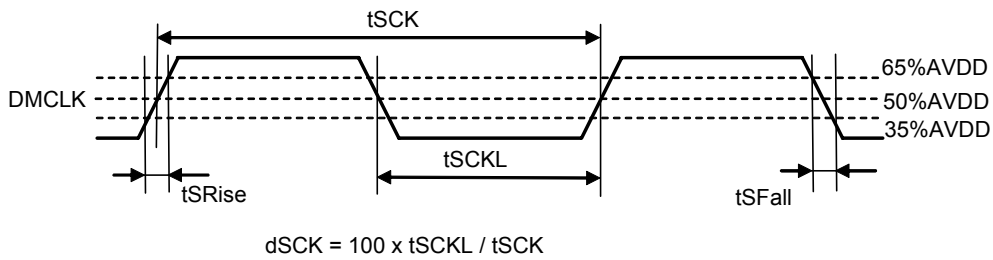


Figure 24. DMCLK Clock Timing

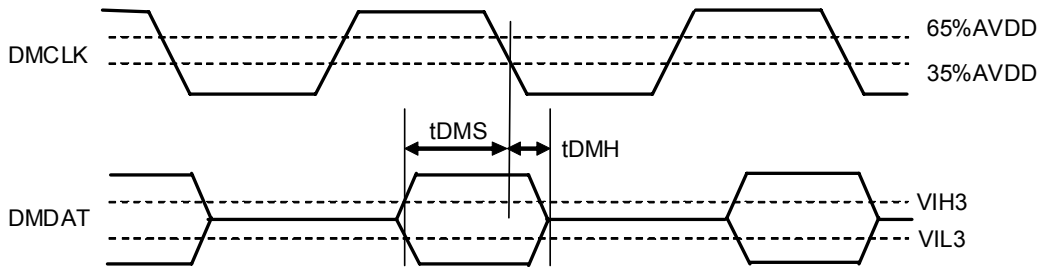


Figure 25. Audio Interface Timing (DCLKP bit = "1")

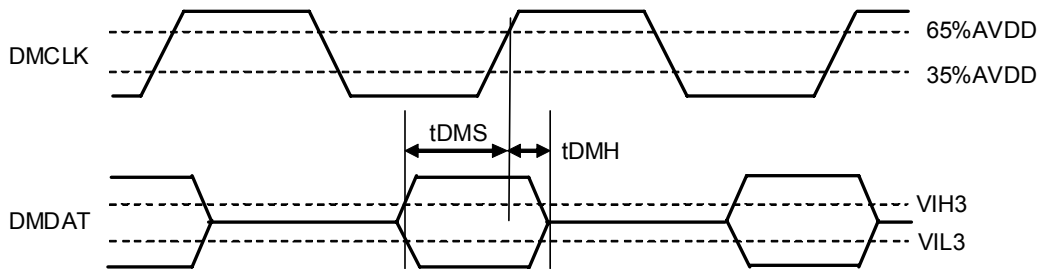


Figure 26. Audio Interface Timing (DCLKP bit = "0")

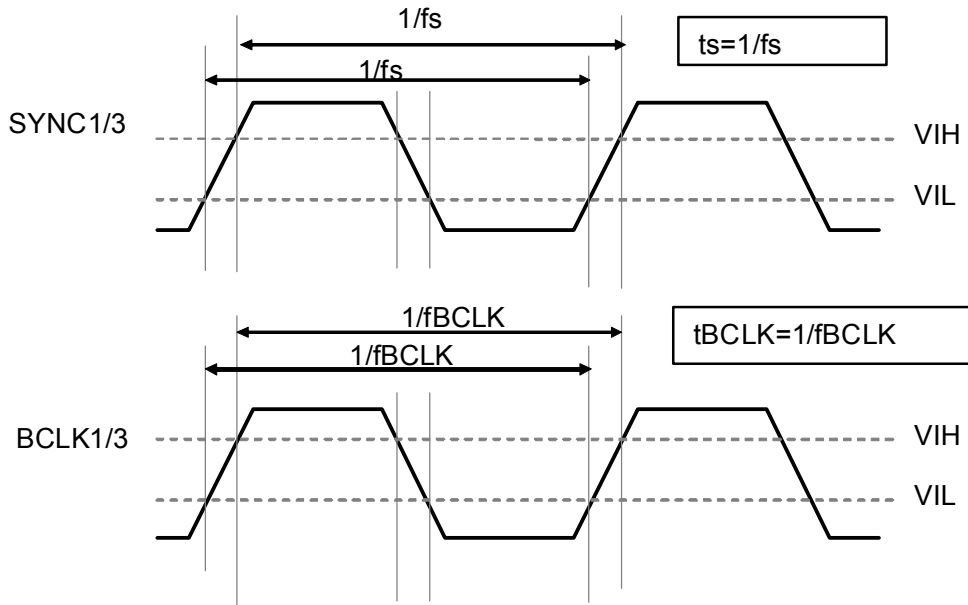


Figure 27. System Clock

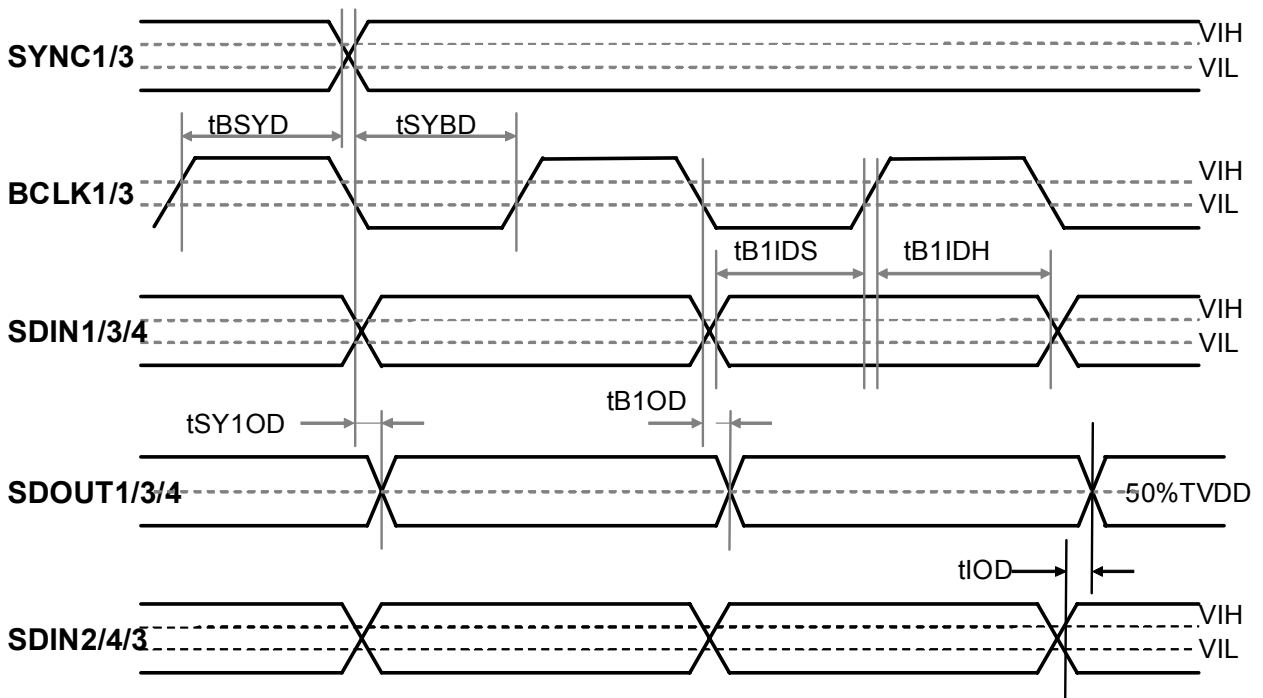


Figure 28. Serial Data Interface (Port#1, 3, 4)

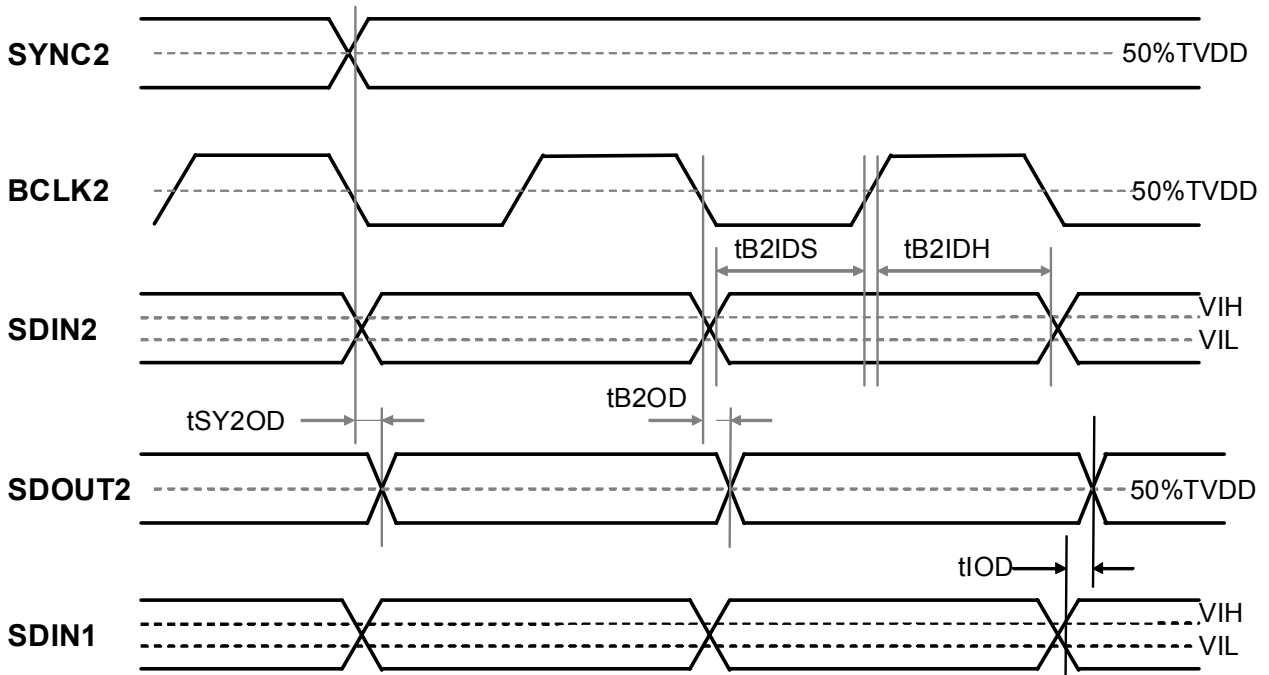


Figure 29. Serial Data Interface (Port#2)

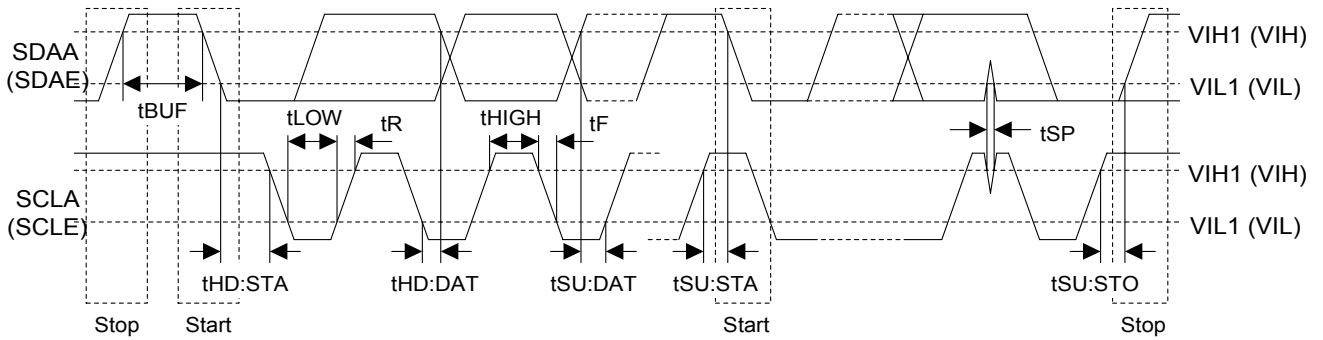


Figure 30. I²C Bus Mode Timing

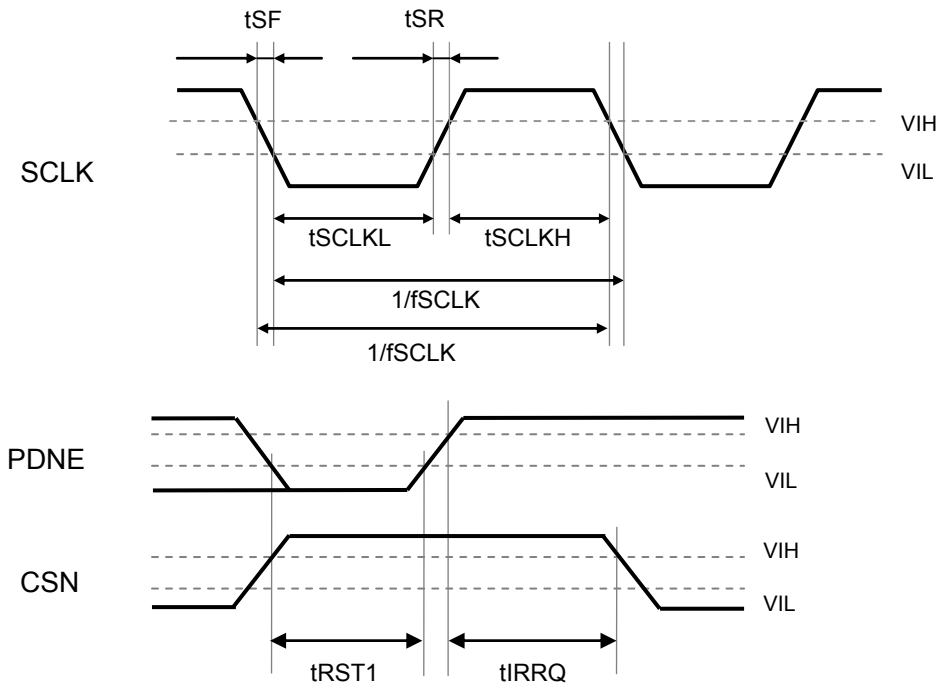


Figure 31. μ P Interface 1 (SPI)

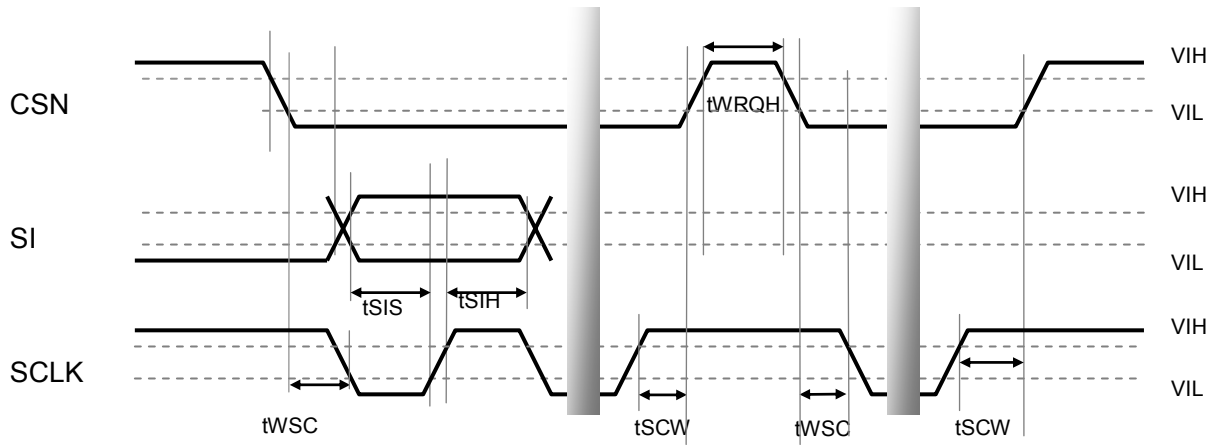


Figure 32. μ P Interface 2 (SPI)

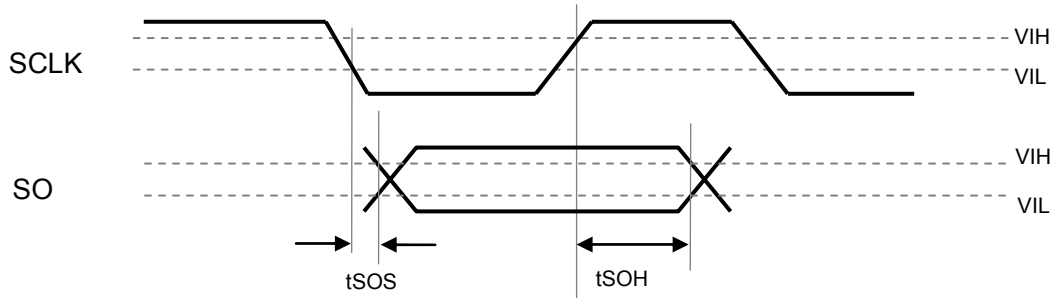


Figure 33. μ P Interface 3 (SPI)

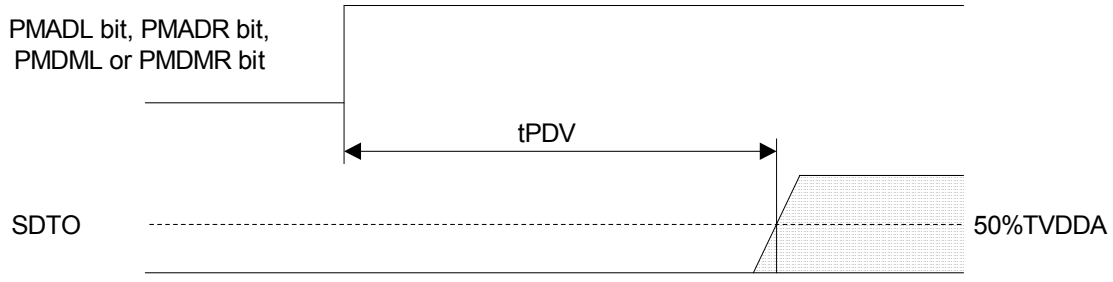


Figure 34. Power Down & Reset Timing 1

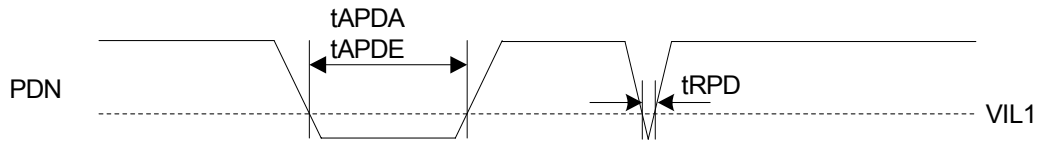


Figure 35. Power Down & Reset Timing 2

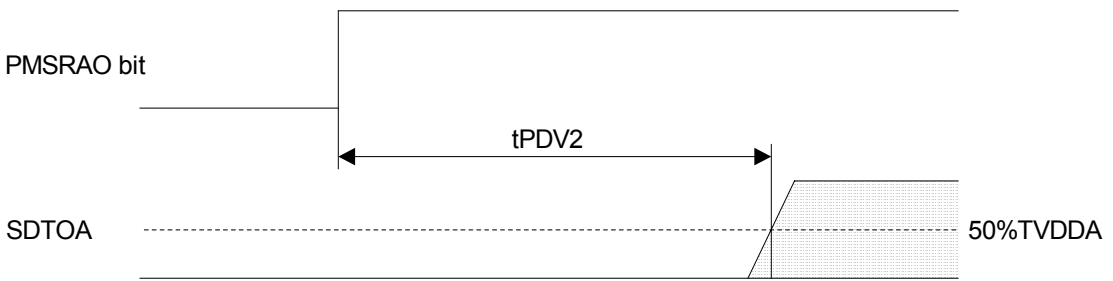


Figure 36. Power Down & Reset Timing 3

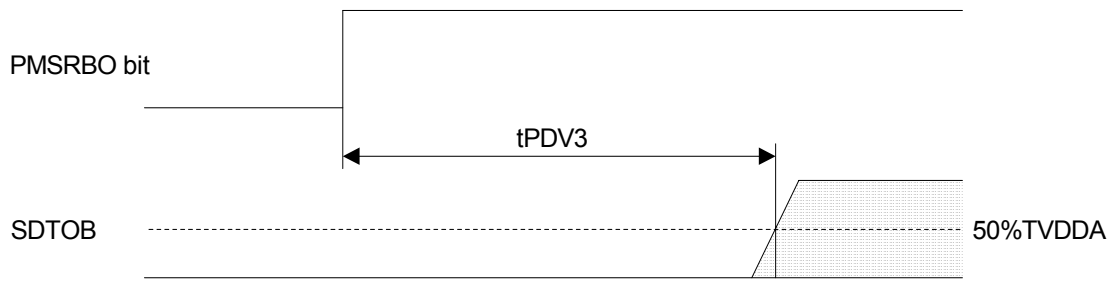


Figure 37. Power Down & Reset Timing 4

OPERATION OVERVIEW

The figure shown below is one the connection example with aAudio Processor, Base-band processor, BT module and AK4679. Since the clock control block (CGU) provides DSP master clock, stable clock from Audio Processor or Base-band must be supplied to the AK4679 during an operation.

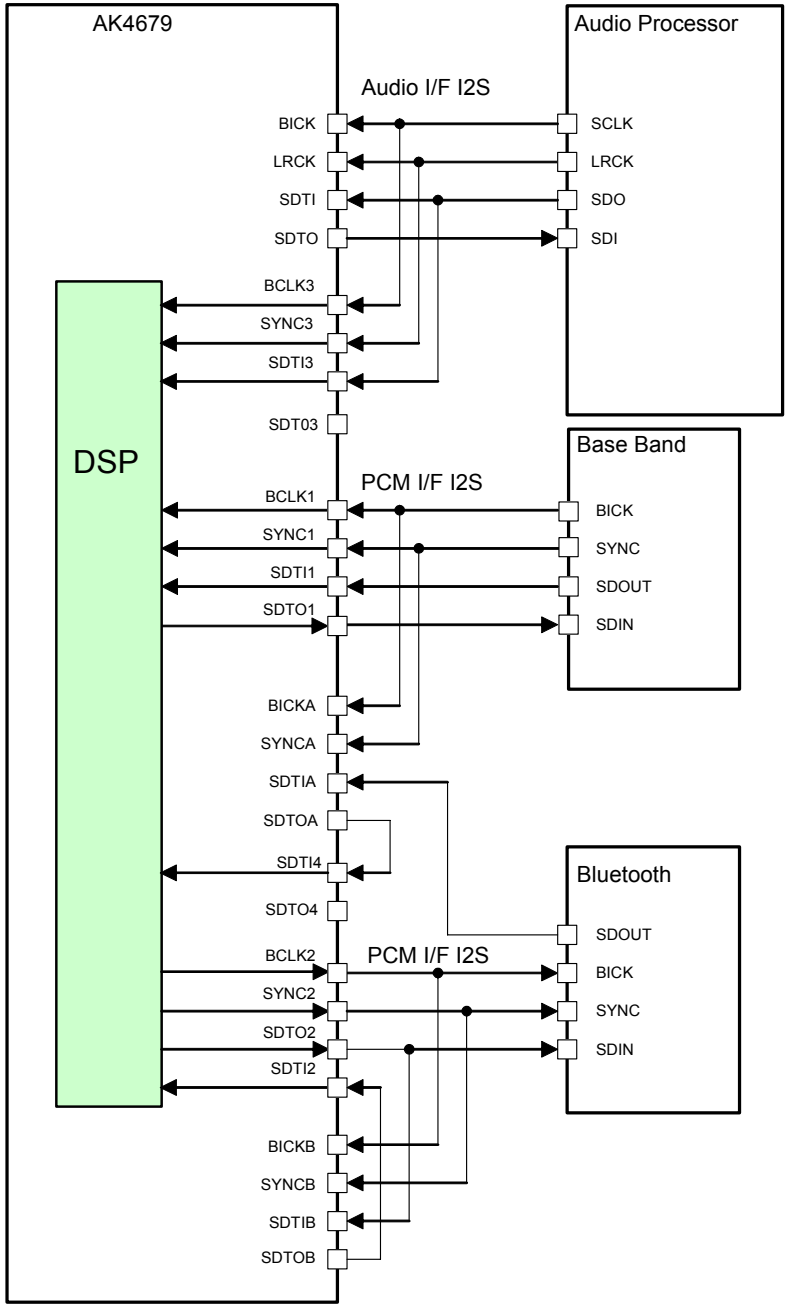


Figure 38. Connection Diagram Example

■ CODEC System Clock (Audio I/F)

There are the following four clock modes to interface with external devices. (Table 2 and Table 3)

| Mode | PMPLL bit | M/S bit | PLL3-0 bits | Figure |
|---|-----------|---------|-------------|-----------|
| PLL Master Mode | 1 | 1 | Table 5 | Figure 39 |
| PLL Slave Mode (PLL Reference Clock: BICK pin) | 1 | 0 | Table 5 | Figure 40 |
| EXT Slave Mode | 0 | 0 | x | Figure 41 |
| EXT Master Mode | 0 | 1 | x | Figure 42 |

Table 2. Clock Mode Setting (x: Don't care)

| Mode | MCKI pin | BICK pin | LRCK pin |
|---|-------------------------|------------------------------------|-----------------|
| PLL Master Mode | Selected by PLL3-0 bits | Output (Selected by BCKO bit) | Output (1fs) |
| PLL Slave Mode (PLL Reference Clock: BICK pin) | GND | Input (Selected by PLL3-0 bits) | Input (1fs) |
| EXT Slave Mode | Selected by FS1-0 bits | Input (≥ 32fs) | Input (1fs) |
| EXT Master Mode | Selected by FS1-0 bits | Output (Selected by BCKO bit) | Output (1fs) |

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode (Audio I/F)

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. The audio I/F is in slave mode until the M/S bit is changed to "1" after the PDNA pin changes from "L" to "H". The AK4679 goes to master mode by changing M/S bit = "1".

When the audio I/F is used in master mode, LRCK and BICK pins are Hi-Z state until M/S bit becomes "1". LRCK and BICK pins of the audio I/F should be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid floating state.

| M/S bit | Mode |
|---------|-------------|
| 0 | Slave Mode |
| 1 | Master Mode |

(default)

Table 4. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = “1”) (Audio I/F)

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) generates clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 5. This lock time is when the audio I/F is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or when the sampling frequency changes.

1) Setting of PLL Mode

| Mode | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | PLL Lock Time (max) |
|--------|----------|----------|----------|----------|-------------------------------|-----------------|---------------------|
| 2 | 0 | 0 | 1 | 0 | BICK pin | 32fs | 2ms |
| 3 | 0 | 0 | 1 | 1 | BICK pin | 64fs | 2ms |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10ms |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10ms |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10ms |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10ms |
| 8 | 1 | 0 | 0 | 0 | MCKI pin | 19.2MHz | 10ms |
| 10 | 1 | 0 | 1 | 0 | MCKI pin | 13MHz | 10ms |
| 11 | 1 | 0 | 1 | 1 | MCKI pin | 26MHz | 10ms |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10ms |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10ms |
| 14 | 1 | 1 | 1 | 0 | MCKI pin | 25MHz | 10ms |
| Others | Others | | | | N/A | | |

Table 5. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI and BICK pins, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 8kHz |
| 1 | 0 | 0 | 0 | 1 | 12kHz |
| 2 | 0 | 0 | 1 | 0 | 16kHz |
| 3 | 0 | 0 | 1 | 1 | 24kHz |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz |
| 10 | 1 | 0 | 1 | 0 | 32kHz |
| 11 | 1 | 0 | 1 | 1 | 48kHz |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz |
| Others | Others | | | | N/A |

Table 6. Setting of Sampling Frequency at PMPLL bit = “1” (N/A: Not available)

■ PLL Unlock State (Audio I/F)

1) PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

In this mode, LRCK and BICK pins output “L” before the PLL goes to lock state after PMPLL bit = “0” → “1” (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to “L” by setting PMPLL bit “0”.

| PLL State | BICK pin | LRCK pin |
|--------------------------------|------------|------------|
| After that PMPLL bit “0” → “1” | “L” Output | “L” Output |
| PLL Unlock (except above case) | Invalid | Invalid |
| PLL Lock | Table 8 | 1fs Output |

Table 7. Clock Operation in PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”) (Audio I/F)

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 25MHz, 26MHz or 27MHz) is input to the MCKI pin, the BICK and LRCK clocks are generated by an internal PLL circuit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 8).

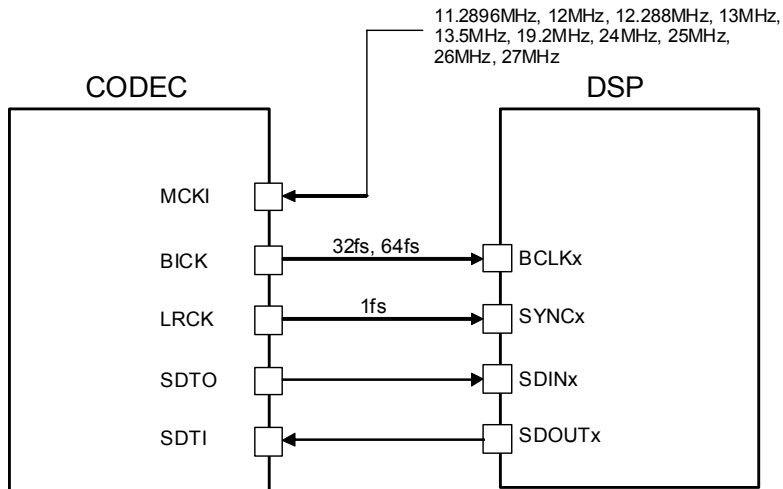


Figure 39. PLL Master Mode (x=1 to 4)

| BCKO bit | BICK Output Frequency |
|----------|-----------------------|
| 0 | 32fs |
| 1 | 64fs |

(default)

Table 8. BICK Output Frequency in Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”) (Audio I/F)

A reference clock of PLL is selected among the input clocks to BICK pin. The required clock to the CODEC is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

BICK input should be synchronized to LRCK input. Sampling frequency can be selected by FS3-0 bits (Table 6).

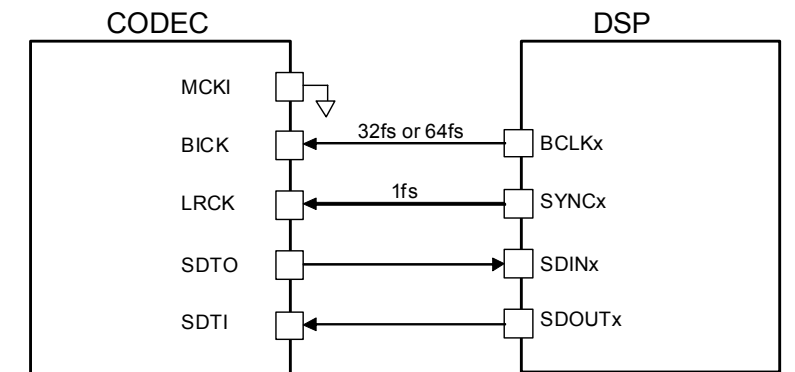


Figure 40. PLL Slave Mode (PLL Reference Clock: BICK pin) (x=1 to 4)

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”) (Audio I/F)

When PMPLL bit is “0”, the audio I/F becomes EXT mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate the CODEC are MCKI (256fs, 512fs, or 1024fs), LRCK (fs) and BICK ($\geq 32fs$). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by CM1-0 bits (Table 9) and sampling frequency is selected by FS3-0 bits (Table 10).

In case that the CODEC is used without Audio I/F (like phone call), the CODEC can be operated by MCKI only. In this case, BICK and LRCK can be stopped.

| Mode | CM1 bit | CM0 bit | MCKI Input Frequency | Sampling Frequency Range |
|------|---------|---------|----------------------|--------------------------|
| 0 | 0 | 0 | 256fs | 24kHz ~ 48kHz |
| 1 | 0 | 1 | 512fs | 8kHz ~ 24kHz |
| 2 | 1 | 0 | 1024fs | 8kHz ~ 12kHz |
| 3 | 1 | 1 | 256fs | 8kHz ~ 24kHz |

(default)

Table 9. MCKI Frequency in EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 8kHz |
| 1 | 0 | 0 | 0 | 1 | 12kHz |
| 2 | 0 | 0 | 1 | 0 | 16kHz |
| 3 | 0 | 0 | 1 | 1 | 24kHz |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz |
| 10 | 1 | 0 | 1 | 0 | 32kHz |
| 11 | 1 | 0 | 1 | 1 | 48kHz |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz |
| Others | Others | | | | N/A |

(default)

Table 10. Setting of Sampling Frequency (N/A: Not available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 11.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|--------|---|
| 256fs | 82dB |
| 512fs | 82dB |
| 1024fs | 92dB |

Table 11. Relationship between MCKI and S/N of LOUT/ROUT pins

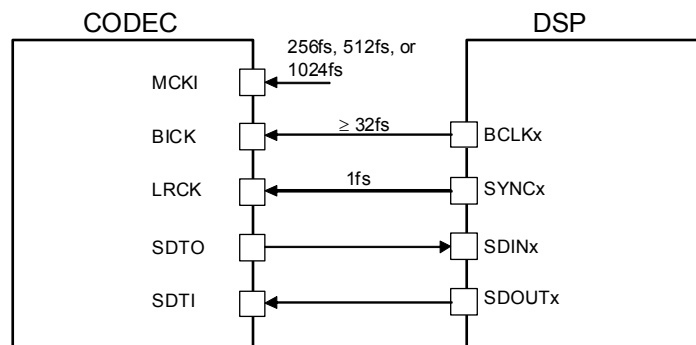


Figure 41. EXT Slave Mode (x=1 to 4)

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”) (Audio I/F)

The audio I/F becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs, or 1024fs). The input frequency of MCKI is selected by CM1-0 bits (Table 12) and sampling frequency is selected by FS3-0 bits (Table 13).

| Mode | CM1 bit | CM0 bit | MCKI Input Frequency | Sampling Frequency Range |
|------|---------|---------|----------------------|--------------------------|
| 0 | 0 | 0 | 256fs | 24kHz ~ 48kHz |
| 1 | 0 | 1 | 512fs | 8kHz ~ 24kHz |
| 2 | 1 | 0 | 1024fs | 8kHz ~ 12kHz |
| 3 | 1 | 1 | 256fs | 8kHz ~ 24kHz |

(default)

Table 12. MCKI Frequency in EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 8kHz |
| 1 | 0 | 0 | 0 | 1 | 12kHz |
| 2 | 0 | 0 | 1 | 0 | 16kHz |
| 3 | 0 | 0 | 1 | 1 | 24kHz |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz |
| 10 | 1 | 0 | 1 | 0 | 32kHz |
| 11 | 1 | 0 | 1 | 1 | 48kHz |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz |
| Others | Others | | | | N/A |

(default)

Table 13. Setting of Sampling Frequency (N/A: Not available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 14.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|--------|---|
| 256fs | 82dB |
| 512fs | 82dB |
| 1024fs | 92dB |

Table 14. Relationship between MCKI and S/N of LOUT/ROUT pins

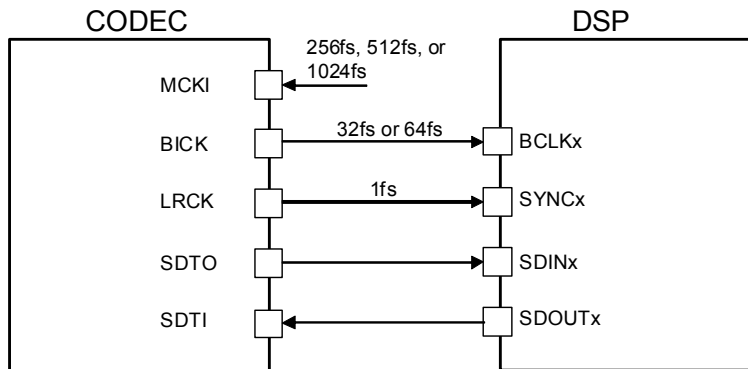


Figure 42. EXT Master Mode (x=1 to 4)

| BCKO bit | BICK Output Frequency |
|----------|-----------------------|
| 0 | 32fs |
| 1 | 64fs |

(default)

Table 15. BICK Output Frequency in Master Mode

■ System Reset

Upon power-up, the PDNA and PDNE pins must be “L” and changed to “H” after all power supplies are supplied. The period of “L” time more than 1.5μs is needed to reset the whole block of AK4679. All internal registers reset to their initial values.

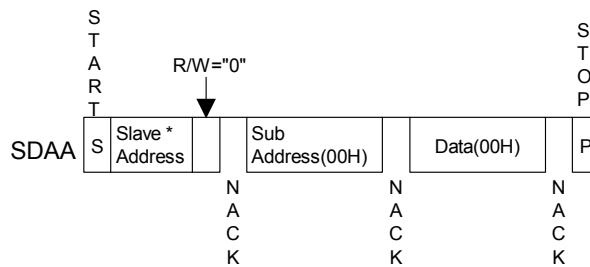
The ADC enters an initialization cycle when the PMADL or PMADR bit is changed from “0” to “1”. The initialization cycle time is set by ADRST bit (Table 16). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC's.

Note 73. The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST bit = “0” or do not use the initial data of ADC.

| ADRST bit | Digital Initialization Cycle | | | (default) |
|-----------|------------------------------|------------|--------------|-----------|
| | fs = 8kHz | fs = 16kHz | fs = 44.1kHz | |
| 0 | 1059/fs | 132.4ms | 66.2ms | 24ms |
| 1 | 267/fs | 33.4ms | 16.7ms | 6.1ms |

Table 16. ADC Digital Initialization Cycle

Audio block's reset is released when the dummy command (Actually, the rising edge of 16th SCL) is input after PDNA pins = “H”. Dummy command is executed by writing all “0” to the register address 00H.



(*: Refer to Figure 124)

Figure 43. Dummy Command for Audio Block

The system reset for DSP block are released when both PWSW bit and MRSTN bit are set after PDNE pins = “H”

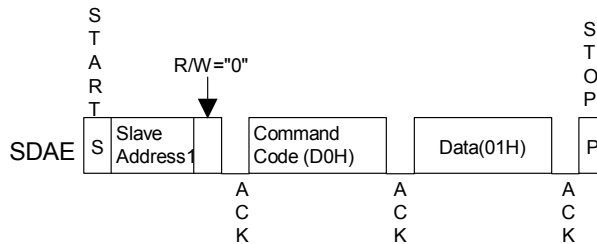
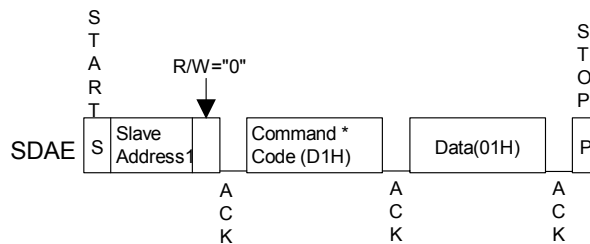


Figure 44. PWSW bit setting for DSP block



(*: Refer to Figure 125)

Figure 45. MRSTN bit setting for DSP block

■ Audio Interface Format

Four types of data formats are available and can be selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the audio I/F in master mode, but must be input to the audio I/F in slave mode.

| Mode | DIF1 bit | DIF0 bit | SDTO (ADC) | SDTI (DAC) | BICK | Figure |
|------|----------|----------|---------------------------------------|--------------------------------------|----------------------------|---------------------|
| 0 | 0 | 0 | 16bit DSP Mode | 16bit DSP Mode | $\geq 32\text{fs}$ | Table 18 |
| 1 | 0 | 1 | 24bit MSB justified | 16bit LSB justified | $\geq 32\text{fs}$ | Figure 50 |
| 2 | 1 | 0 | 24bit MSB justified | 24bit MSB justified | $\geq 48\text{fs}$ | Figure 51 (default) |
| 3 | 1 | 1 | 24/16 bit I ² S compatible | 24/16bit I ² S compatible | 32fs or $\geq 48\text{fs}$ | Figure 52 |

Table 17. Audio Interface Format

If 24-bit(16-bit) data that ADC outputs is converted to 8-bit data by removing LSB 16-bit(8-bit), “-1” at 24bit(16bit) data is converted to “-1” at 8-bit data. And when the DAC playbacks this 8-bit data, “-1” at 8-bit data will be converted to “-65536” at 24-bit (“-256” at 16-bit) data which is a large offset. This offset can be removed by adding the offset of “32768” at 24-bit (“128” at 16bit) to 24-bit(16-bit) data before converting to 8-bit data.

In Mode 1, 2 and 3, the SDTO is clocked out on the falling edge (“↓”) of BICK and the SDTI is latched on the rising edge (“↑”).

In Mode 0 (16bit DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 18).

| DIF1 bit | DIF0 bit | MSBS bit | BCKP bit | Audio Interface Format | Figure |
|----------|----------|----------|----------|--|---------------------|
| 0 | 0 | 0 | 0 | MSB of SDTO is output by the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO's MSB. | Figure 46 (default) |
| | | 0 | 1 | MSB of SDTO is output by the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO's MSB. | Figure 47 |
| | | 1 | 0 | MSB of SDTO is output by next rising edge (“↑”) of the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO's MSB. | Figure 48 |
| | | 1 | 1 | MSB of SDTO is output by next falling edge (“↓”) of the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO's MSB. | Figure 49 |

Table 18. Audio Interface Format in Mode 0

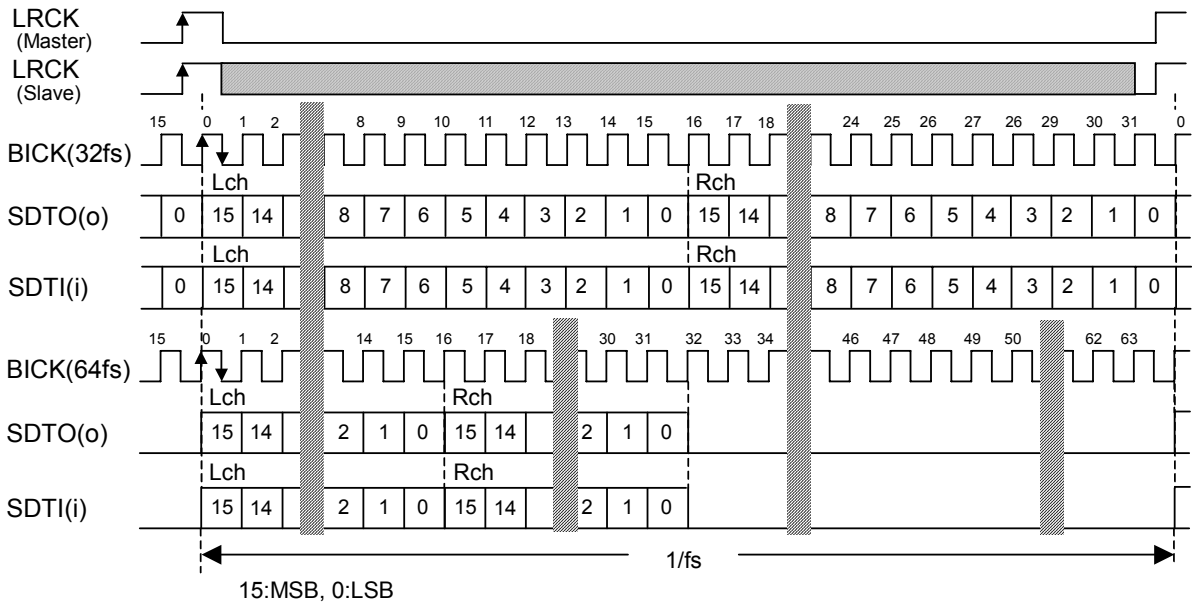


Figure 46. Mode 0 Timing (BCKP bit = "0", MSBS bit = "0")

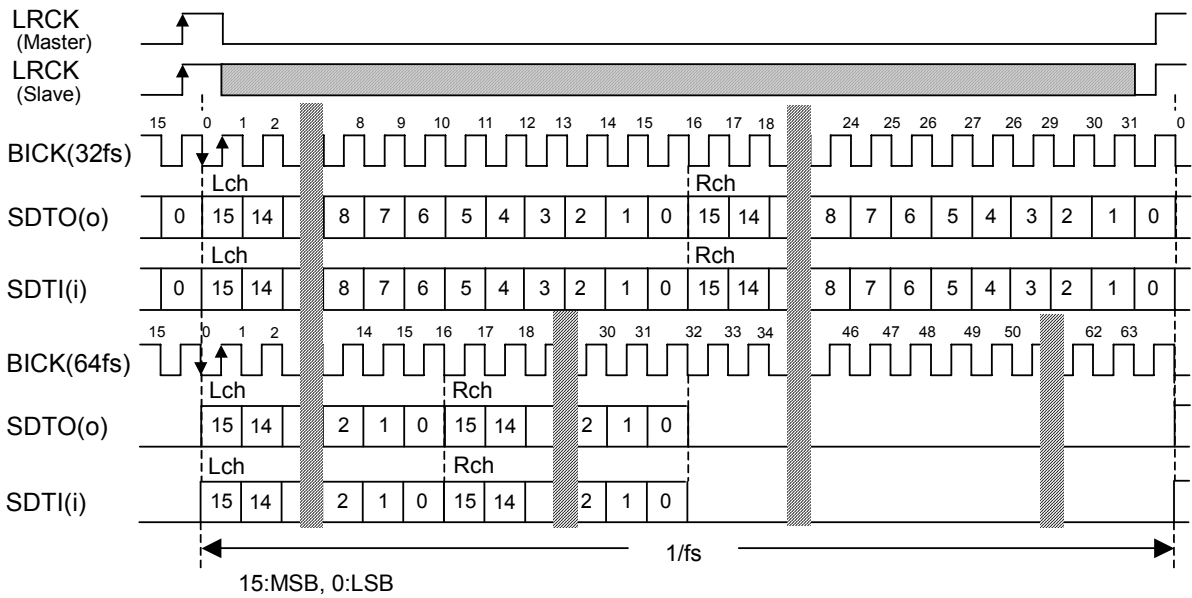


Figure 47. Mode 0 Timing (BCKP bit = "1", MSBS bit = "0")

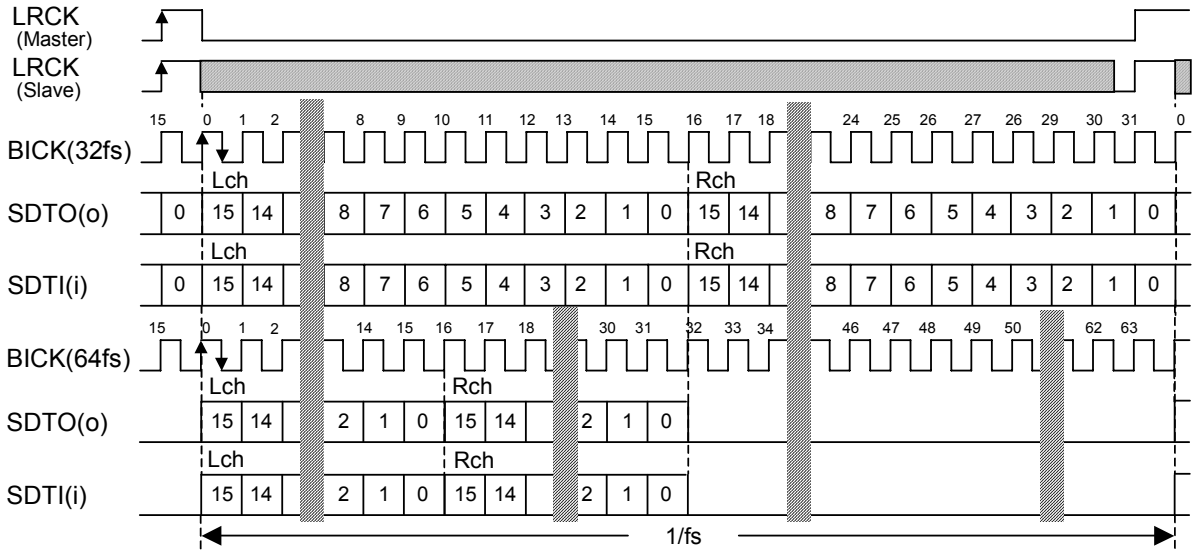


Figure 48. Mode 0 Timing (BCKP bit = "0", MSBS bit = "1")

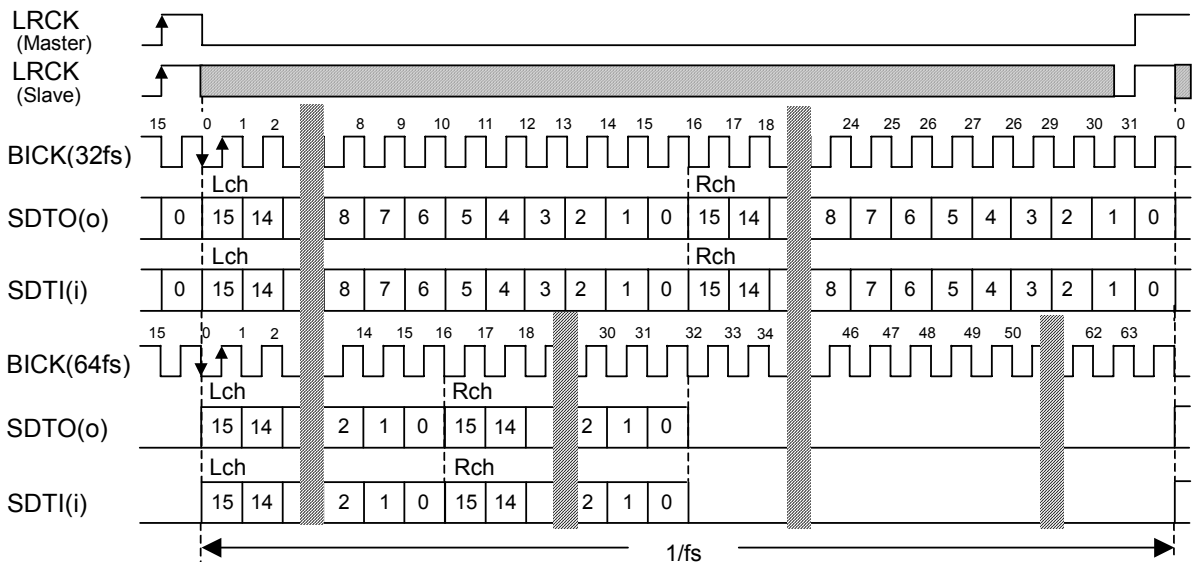


Figure 49. Mode 0 Timing (BCKP bit = "1", MSBS bit = "1")

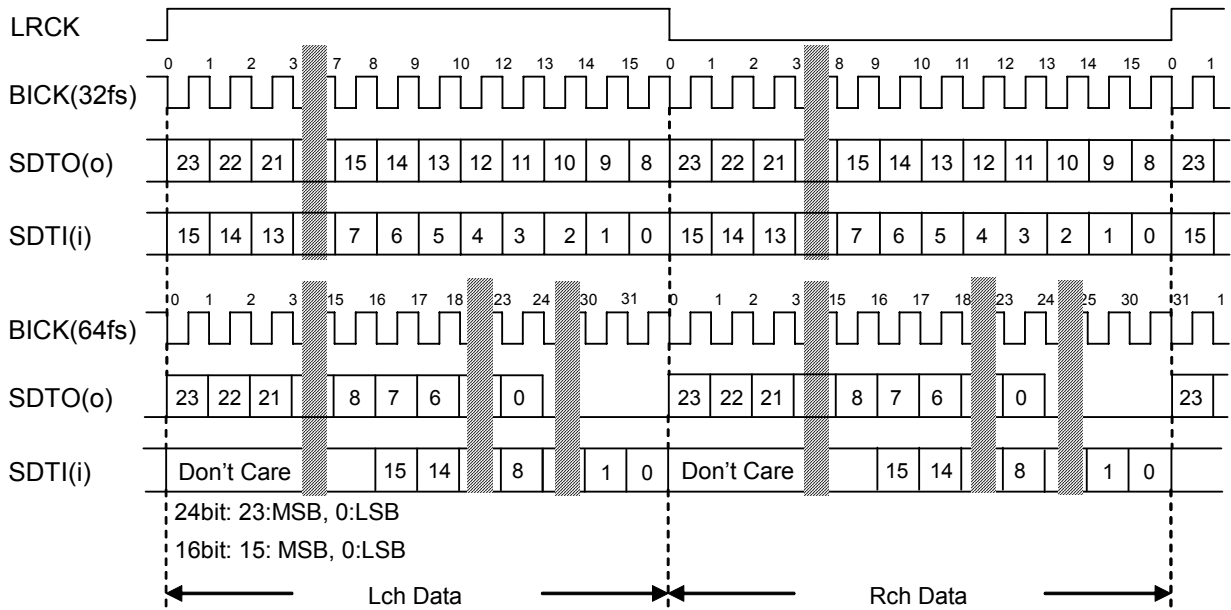


Figure 50. Mode 1 Timing

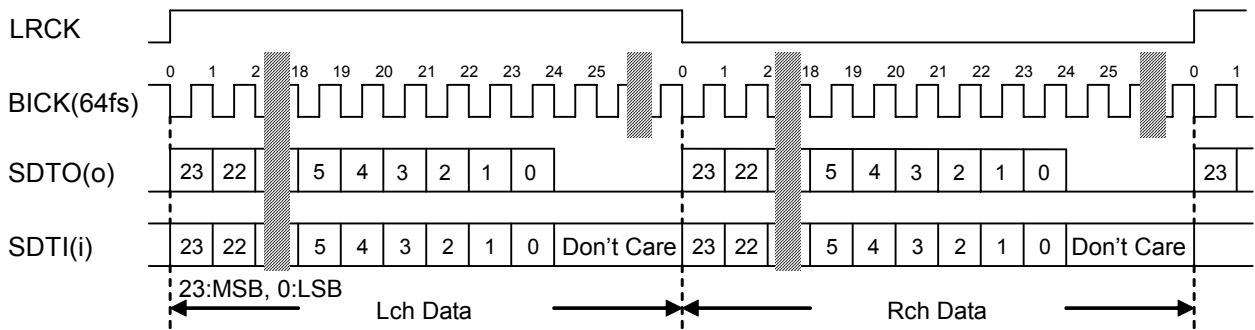


Figure 51. Mode 2 Timing

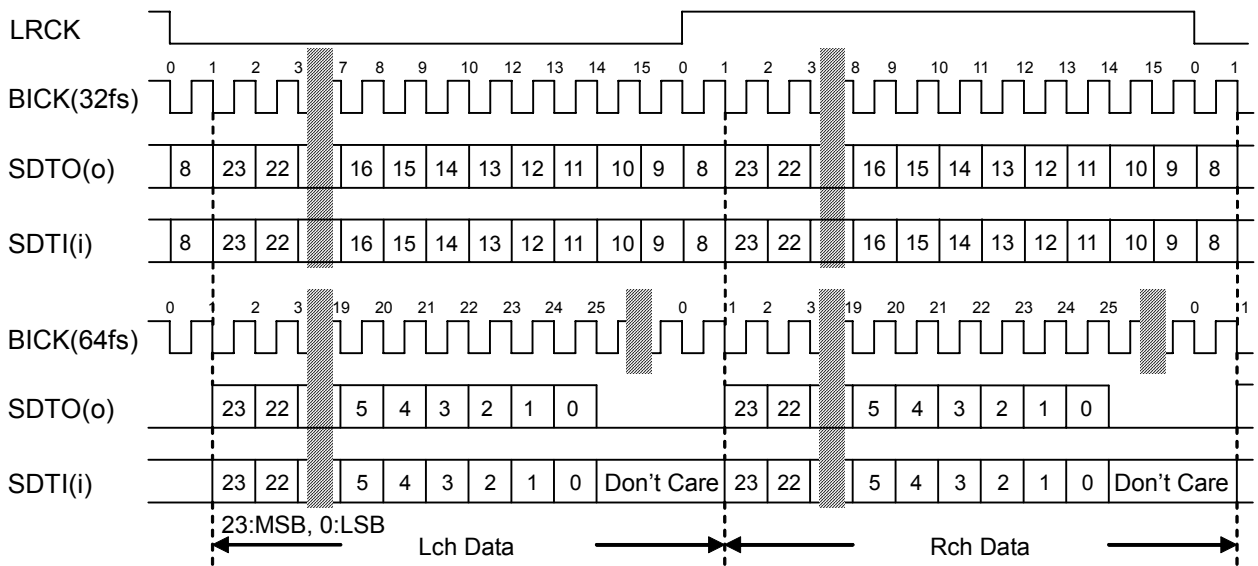


Figure 52. Mode 3 Timing

■ MIC/LINE Input Selector

The AK4679 has input selector. When MDIF1, MDIF2 and MDIF3 bits are “0”, INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3/LIN4 and RIN1/RIN2/RIN3/RIN4, respectively. When MDIF1, MDIF2 and MDIF3 bits are “1”, LIN1/RIN1, LIN2/RIN2 and LIN3/RIN3 pins become IN1+/-, IN2-/+ and IN3+/- pins, respectively. In this case, full-differential input is available (Figure 54). Digital microphone input is selected when DMIC bit = “1”.

| MDIF1 bit | MDIF2 bit | MDIF3 bit | INL1 bit | INL0 bit | INR1 bit | INR0 bit | Lch | Rch | |
|-----------|-----------|-----------|----------|----------|----------|----------|--------|--------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LIN1 | RIN1 | (default) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | LIN1 | RIN2 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | LIN1 | RIN3 | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | LIN1 | RIN4 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | LIN2 | RIN1 | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | LIN2 | RIN2 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | LIN2 | RIN3 | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | LIN2 | RIN4 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | LIN3 | RIN1 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | LIN3 | RIN2 | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | LIN3 | RIN3 | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | LIN3 | RIN4 | |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | LIN4 | RIN1 | |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | LIN4 | RIN2 | |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | LIN4 | RIN3 | |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | LIN4 | RIN4 | |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | IN3+/- | RIN1 | |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | IN3+/- | RIN2 | |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | IN3+/- | RIN4 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | LIN1 | IN2+/- | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | LIN3 | IN2+/- | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | LIN4 | IN2+/- | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | IN3+/- | IN2+/- | |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | IN1+/- | RIN2 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | IN1+/- | RIN3 | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | IN1+/- | RIN4 | |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | IN1+/- | IN2+/- | |
| Others | | | | | | | N/A | | |

Table 19. MIC-Amp Input Signal at DMIC bit = “0” (N/A: Not available)

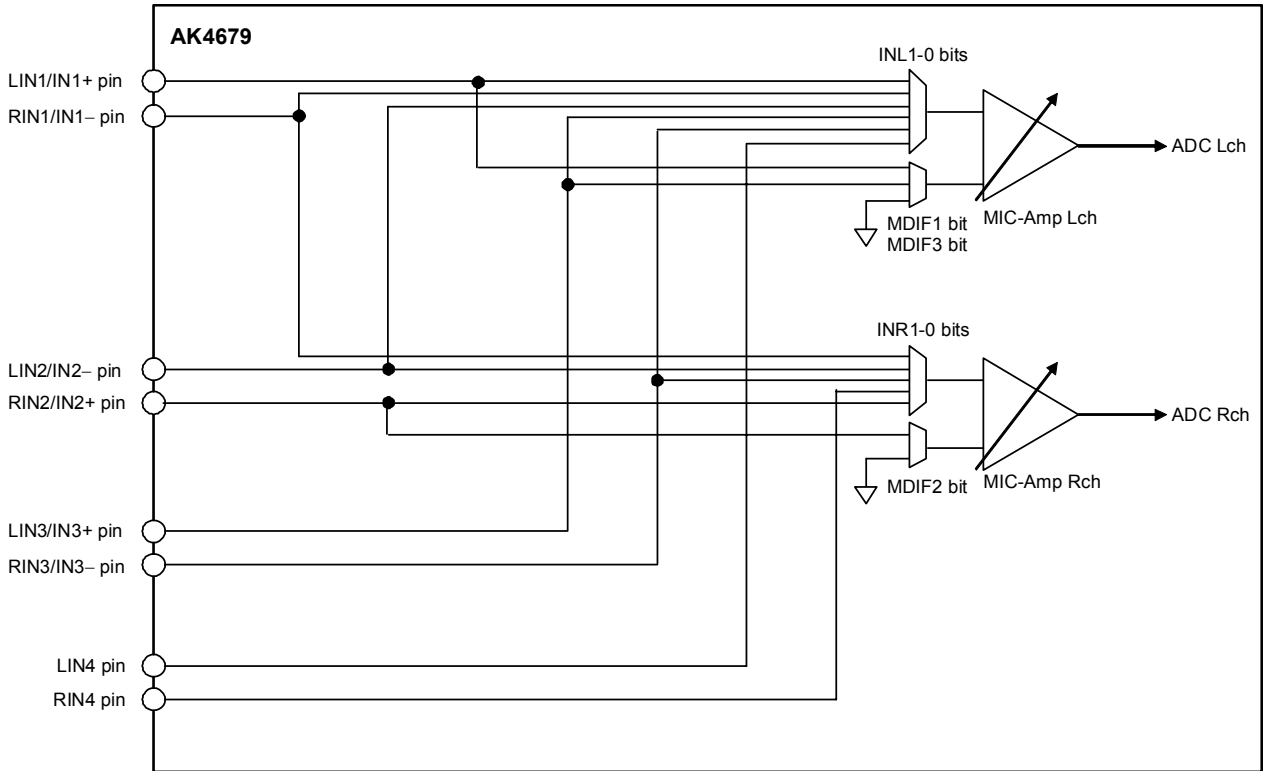


Figure 53. Mic/Line Input Selector (DMIC bit = "0")

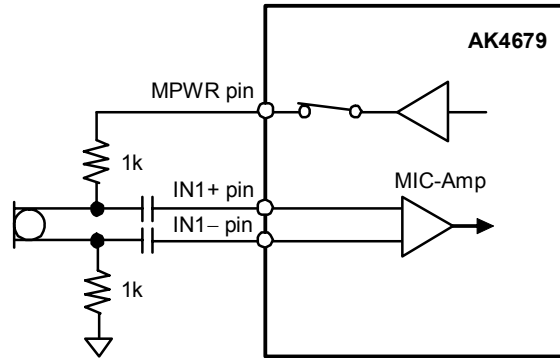


Figure 54. Connection Example for Full-differential Mic Input (MDIF1/2/3 bits = "1")

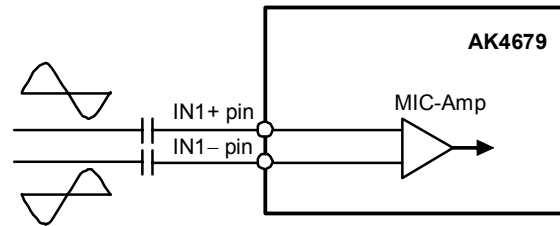


Figure 55. Connection Example for Full-differential Mic Input (MDIF1/2/3 bits = "1")

■ MIC Gain Amplifier

The AK4679 has a gain amplifier for microphone input. The gain of MIC-Amp Lch and Rch is independently selected by the MGNL3-0 and MGNR3-0 bits (Table 20).

| Mode | MGNL3 /MGNR3 bits | MGNL2 /MGNR2 bits | MGNL1 /MGNR1 bits | MGNL0 /MGNR0 bits | Input Gain |
|------|-------------------------|-------------------------|-------------------------|-------------------------|---------------|
| 0 | 0 | 0 | 0 | 0 | N/A |
| 1 | 0 | 0 | 0 | 1 | N/A |
| 2 | 0 | 0 | 1 | 0 | N/A |
| 3 | 0 | 0 | 1 | 1 | -6dB |
| 4 | 0 | 1 | 0 | 0 | -3dB |
| 5 | 0 | 1 | 0 | 1 | 0dB (default) |
| 6 | 0 | 1 | 1 | 0 | +3dB |
| 7 | 0 | 1 | 1 | 1 | +6dB |
| 8 | 1 | 0 | 0 | 0 | +9dB |
| 9 | 1 | 0 | 0 | 1 | +12dB |
| 10 | 1 | 0 | 1 | 0 | +15dB |
| 11 | 1 | 0 | 1 | 1 | +18dB |
| 12 | 1 | 1 | 0 | 0 | +21dB |
| 13 | 1 | 1 | 0 | 1 | +24dB |
| 14 | 1 | 1 | 1 | 0 | N/A |
| 15 | 1 | 1 | 1 | 1 | N/A |

Table 20. Mic Input Gain (N/A: Not available)

■ MIC Power

When PMMP1 bit (PMMP2 bit) = “1”, the MPWR1 pin (MPWR2 pin) supplies power for the microphone. This output voltage is typically 2.5V @MICL1 bit (MICL2 bit) = “0” (SVDD=3.0 ~ 5.5V), and typically 2.8V@MICL1 bit (MICL2 bit) = “1” (SVDD=3.3 ~ 5.5V) (Table 21). The load resistance is minimum 1kΩ for each MPWR1 pin and MPWR2 pin. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR1 pin (MPWR2 pin) (Figure 56).

| MICL1 bit MICL2 bit | SVDD Voltage Range | Output Level (typ) | Output Level (typ) AVDD=1.8V |
|------------------------|--------------------|--------------------|---------------------------------|
| 0 | 3.0 ~ 5.5V | 1.39 x AVDD | 2.5V |
| 1 | 3.3 ~ 5.5V | 1.56 x AVDD | 2.8V |

(default)

Table 21. MIC Power 1, MC Power 2 Output Level

| PMMP1 bit | MPWR1 pin |
|-----------|-----------|
| 0 | Hi-Z |
| 1 | Output |

(default)

Table 22. MIC Power 1 Status

| PMMP2 bit | MPWR2 pin |
|-----------|-----------|
| 0 | Hi-Z |
| 1 | Output |

(default)

Table 23. MIC Power 2 Status

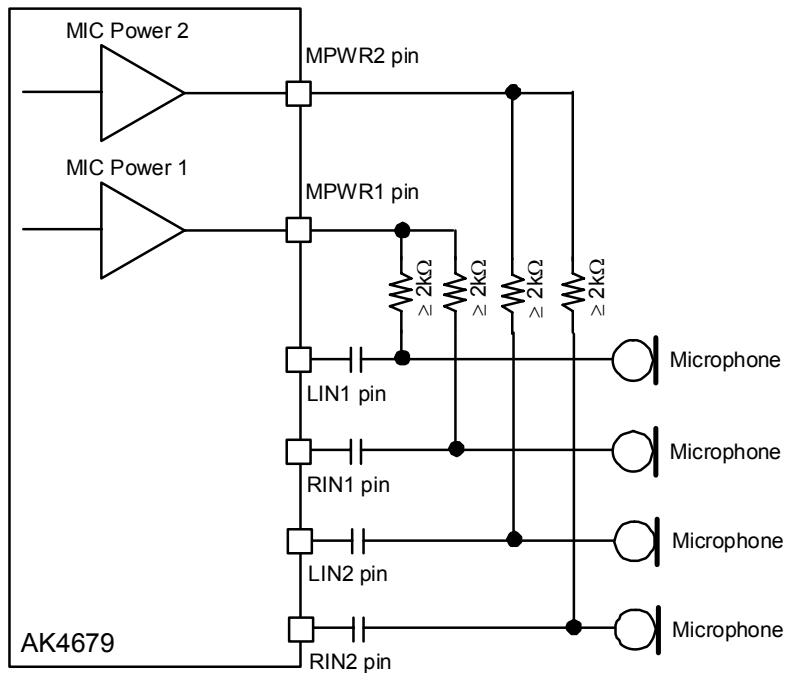


Figure 56. MIC Block Circuit

■ Digital MIC

1. Connection to Digital MIC

The AK4679 can be connected to digital microphone by setting DMIC bit = “1”. When DMIC bit is set to “1”, the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins respectively. The same power supply as AVDD must be provided to the digital microphone. The Figure 57 and Figure 58 show mono/stereo connection examples. The DMCLK signal is output from the AK4679, and the digital microphone outputs 1bit data, which generated by $\Delta\Sigma$ Modulator, from DMDAT. PMDML/R bits control power up/down of the digital block (Decimation Filter and HPF1). PMADL/PMADR bits settings do not affect the digital microphone power management. The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4679 is powered down (PDNA pin= “L”), the DMCLK and DMDAT pins are pulled-down by internal 2.7k Ω (typ.) resistor. However, when the AK4679 is powered-up (PDNA pin = “H”), path of the internal pulled-down resistor is OFF. Therefore, external pull-down resistor(R) should be connected to the DMDAT pin to avoid floating state.

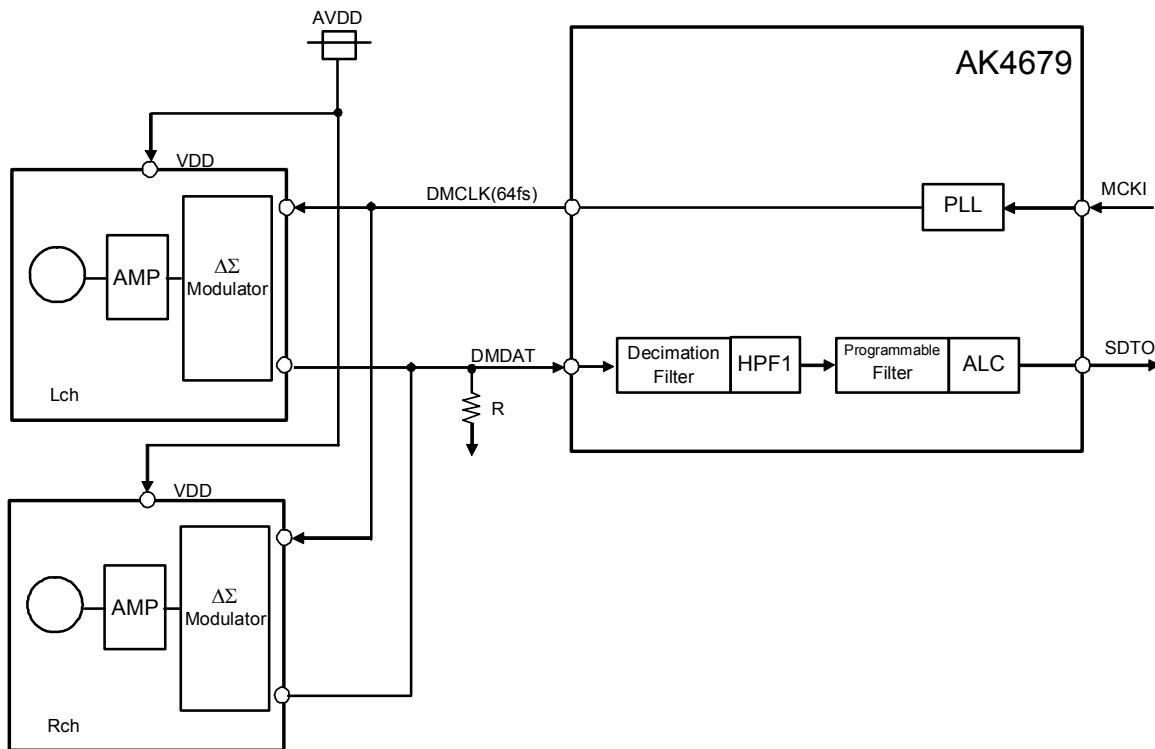


Figure 57. Connection Example of Stereo Digital MIC

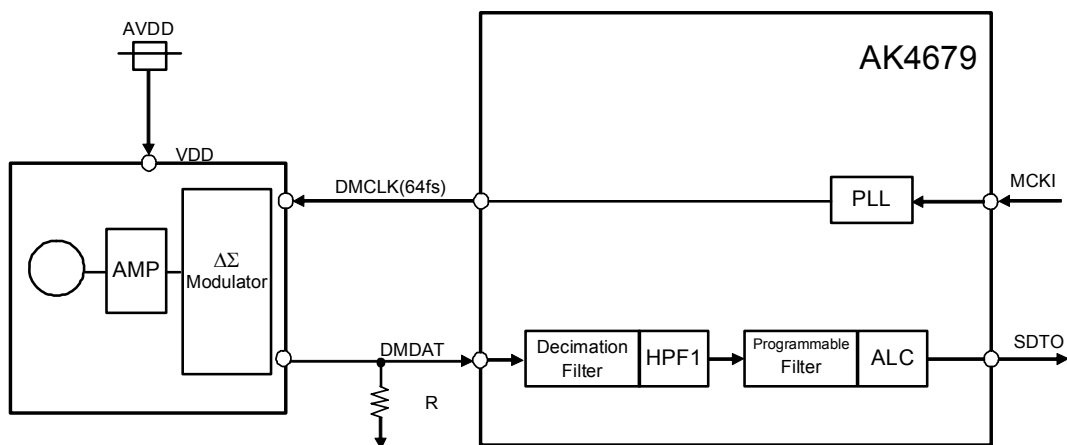


Figure 58. Connection Example of Mono Digital MIC

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = “1”, Lch data is input to the Decimation Filter if DMCLK = “H”, Rch data is input if DMCLK = “L”. When DCLKP bit = “0”, Rch data is input to the Decimation Filter if DMCLK = “H”, Lch data is input if DMCLK = “L”. The DMCLK pin outputs “L” when DCLKE bit = “0”, and only supports 64fs. In this case, necessary clocks must be supplied to the AK4679 for ADC operation. The output data through “the Decimation and Digital Filters” is the negative full-scale with 0% 1’s density of 1bit output data and positive full-scale with the 100% 1’s density of 1bit output data.

| DCLKP bit | DMCLK pin = “H” | DMCLK pin = “L” |
|-----------|-----------------|-----------------|
| 0 | Rch | Lch |
| 1 | Lch | Rch |

(default)

Table 24. Data In/Output Timing with Digital MIC

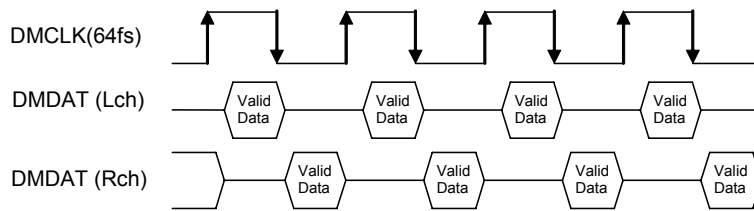


Figure 59. Data In/Output Timing with Digital MIC (DCLKP bit = “1”)

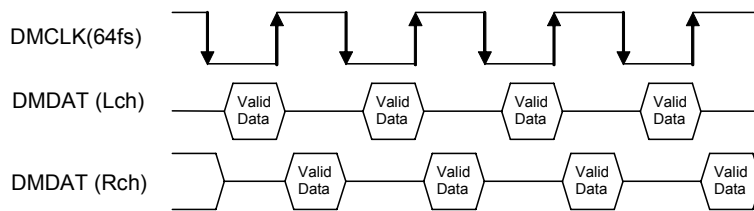


Figure 60. Data In/Output Timing with Digital MIC (DCLKP bit = “0”)

■ Digital Block

Digital block is composed as Figure 61. Each block can be powered-down by power management bits (PMADL, PMADR, PMDAL, PMDAR, PMPFIL, PMEQ, PMDRC, PMSRAI, PMSRAO, PMSRBI and PMSRBO bits).

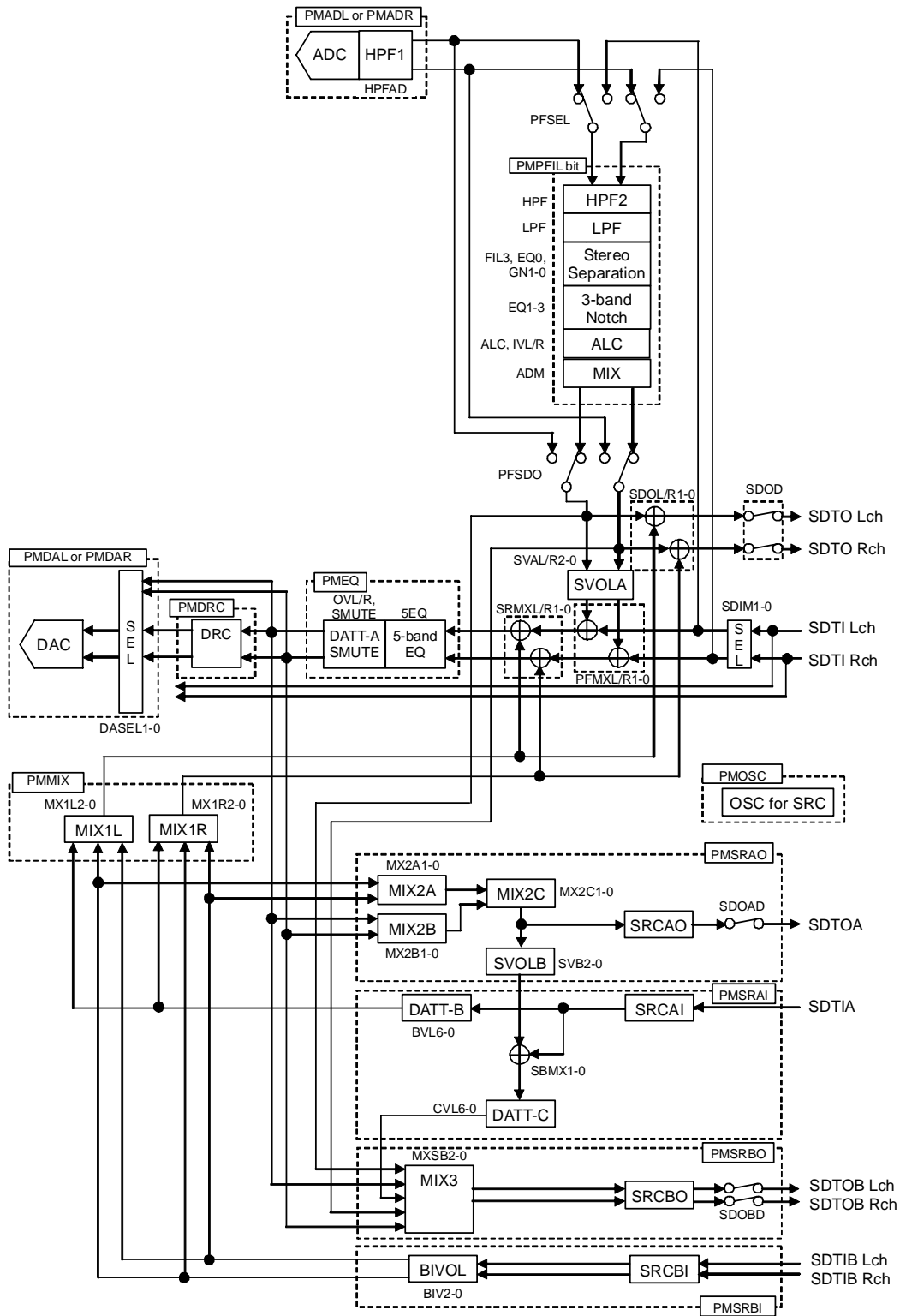


Figure 61. Path Select of Digital Block

1. ADC: Include the Digital Filter (LPF) for ADC as shown in “FILTER CHARACTERISTICS”.
2. HPF1: Include the Digital Filter (HPF) for ADC as shown in “FILTER CHARACTERISTICS”.
3. DAC: Include the Digital Filter (LPF) for DAC as shown in “FILTER CHARACTERISTICS”.
4. HPF2: High Pass Filter. Applicable to use as Wind-Noise Reduction Filter. (See “Digital Programmable Filter”.)
5. LPF: Low Pass Filter (See “Digital Programmable Filter”.)
6. Stereo Separation: Stereo Separation Emphasis Filter & Gain Compensation. (See “Digital Programmable Filter”.)
Gain Compensation is composed with EQ0 and Gain blocks. This block adjusts the frequency response after Stereo Separation Emphasis.
7. 3-Band Notch: Applicable to use as Equalizer or Notch Filter. (See “Digital Programmable Filter”.)
8. ALC: Input Digital Volume with ALC function. (See “Input Digital Volume” and “ALC Operation”.)
9. SVOLA: Side Tone Volume at Internal MIC/SPK or External Headset Phone Call. (See “Side Tone Volume”.)
10. 5-Band EQ: Equalizer for playback path. (See “5-band Equalizer”.)
11. DATT-A: Digital Volume for playback path. (See “Digital Output Volume”.)
12. SMUTE: Soft mute. (See “Soft Mute”.)
13. DRC: Dynamic Range Control for playback path. (See “Dynamic Range Control”.)
14. DATT-B: Digital Volume for Recording of Received Voice. (See “Digital Volume for Recording of Received Voice”)
15. DATT-C: Digital Volume of Received Voice. (See “Digital Volume for Received Voice”)
16. SVOLB: Side Tone Volume at B/T Headset Phone Call. (See “Side Tone Volume for B/T Phone Call”.)

| Mode | PMADL bit (PMDML bit) | PMADR bit (PMDMR bit) | PMPFIL bit | PFSEL bit | PFSDO bit | PMDAL/R bits | PMEQ bit | PMDRC bit | DASEL1-0 bits | Figure |
|-----------------------------|--------------------------|--------------------------|---------------|--------------|--------------|-----------------|-------------|--------------|------------------|-----------|
| Recording 1 | 1 | 1 | 1 | 0 | 1 | 00 | 0 | 0 | x | Figure 62 |
| | 1 | 0 | 1 | 0 | 1 | 00 | 0 | 0 | x | |
| | 0 | 1 | 1 | 0 | 1 | 00 | 0 | 0 | x | |
| Recording 1 & Playback 2 | 1 | 1 | 1 | 0 | 1 | 11 | 1 | 1 | 01 | Figure 63 |
| | 1 | 0 | 1 | 0 | 1 | 11 | 1 | 1 | 01 | |
| | 0 | 1 | 1 | 0 | 1 | 11 | 1 | 1 | 01 | |
| Playback 1 | 0 | 0 | 1 | 1 | 1 | 11 | 1 | 1 | 01 | Figure 64 |
| Playback 2 | 0 | 0 | 0 | 0 | 1 | 11 | 1 | 1 | 01 | Figure 65 |

Table 25. Recode/Playback Mode (x: Don't care)

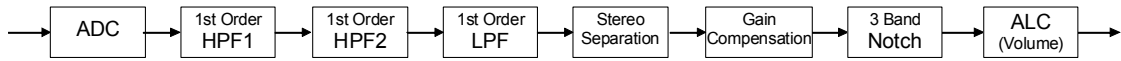


Figure 62. Path at Recording Mode 1

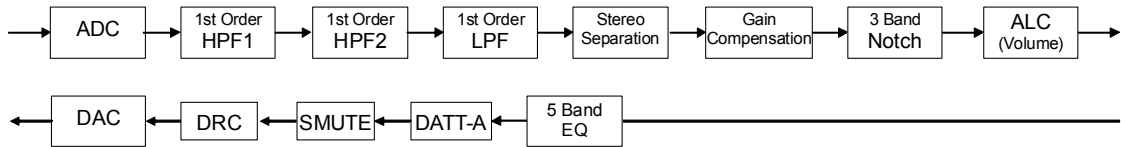


Figure 63. Path at Recording Mode 1 & Playback Mode 2

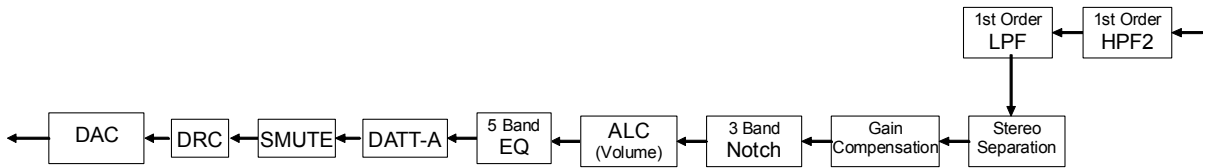


Figure 64. Path at Playback Mode 1

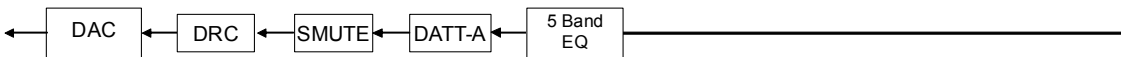


Figure 65. Path at Playback Mode 2

■ Digital Programmable Filter

(1) High Pass Filter (HPF2)

Normally, this HPF is used for Wind-Noise Reduction. This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPF bit = "0" or PMPFIL bit = "0". The HPF2 starts operation 4/fs(max) after when HPF bit = "1" and PMPFIL bit = "1" are set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 74)

HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPF bit = "0" or PMPFIL bit = "0". The LPF starts operation 4/fs(max) after when LPF bit = "1" and PMPFIL bit = "1" are set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 74)

LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo mic recording data or playback data. F3A13-0 and F3B13-0 bits set the filter coefficient of FIL3. FIL3 becomes High Pass Filter (HPF) at F3AS bit = "0", and Low Pass Filter (LPF) at F3AS bit = "1". FIL3 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit = "0" or PMPFIL bit = "0". The FIL3 starts operation $4/f_s(\max)$ after when FIL3 bit = "1" and PMPFIL bit = "1" are set.

1) When FIL3 is set to "HPF"

f_s : Sampling frequency

f_c : Cut-off frequency

K: Filter gain [dB] ($0\text{dB} \geq K \geq -10\text{dB}$)

Register setting (Note 74)

FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

f_s : Sampling frequency

f_c : Cut-off frequency

K: Filter gain [dB] ($0\text{dB} \geq K \geq -10\text{dB}$)

Register setting (Note 74)

FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed with Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0, E0B13-0 and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 26). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". EQ0 starts operation 4/fs(max) after when EQ0 bit = "1" and PMPFIL bit = "1" are set.

- fs: Sampling frequency
- fc₁: Pole frequency
- fc₂: Zero-point frequency
- K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 74)

E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
 (MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

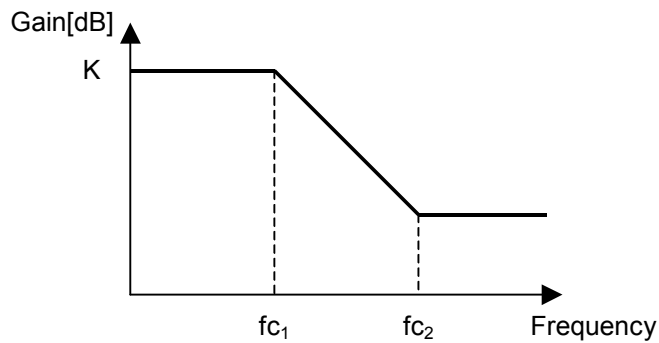


Figure 66. EQ0 Frequency Response

| GN1 bit | GN0 bit | Gain |
|---------|---------|-------|
| 0 | 0 | 0dB |
| 0 | 1 | +12dB |
| 1 | x | +24dB |

(default)

Table 26. Gain select of gain block (x: Don't care)

(5) 3-band Equalizer

This block can be used as Equalizer or Notch Filter. 3-band Equalizer (EQ1, EQ2 and EQ3) is selected ON/OFF independently by EQ1, EQ2 and EQ3 bits. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. The EQ_x (x=1~3) coefficient must be set when EQ_x bit = "0" or PMPFIL bit = "0". EQ1-3 start operation 4/fs(max) after when (EQ_x (x=1~3) = "1") and PMPFIL bit = "1" is set

fs: Sampling frequency

fo₁ ~ fo₃: Center frequency

fb₁ ~ fb₃: Band width where the gain is 3dB different from center frequency

K₁ ~ K₃: Gain (-1 ≤ K_n ≤ 3)

Register setting (Note 74)

EQ1: E1A[15:0] bits =A₁, E1B[15:0] bits =B₁, E1C[15:0] bits =C₁

EQ2: E2A[15:0] bits =A₂, E2B[15:0] bits =B₂, E2C[15:0] bits =C₂

EQ3: E3A[15:0] bits =A₃, E3B[15:0] bits =B₃, E3C[15:0] bits =C₃

(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0)

$$A_n = K_n \times \frac{\tan(\pi f b_n / f_s)}{1 + \tan(\pi f b_n / f_s)}, \quad B_n = \cos(2\pi f o_n / f_s) \times \frac{2}{1 + \tan(\pi f b_n / f_s)}, \quad C_n = -\frac{1 - \tan(\pi f b_n / f_s)}{1 + \tan(\pi f b_n / f_s)}$$

(n = 1, 2, 3)

Transfer function

$$H(z) = 1 + h_1(z) + h_2(z) + h_3(z)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3)

The center frequency should be set as below.

$$0.003 < f o_n / f_s < 0.497$$

Note 74. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

$$X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$$

X should be rounded to integer, and then should be translated to binary code (2's complement).

MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is executed by ALC block when ALC bit is “1”. ALC circuit operates at playback path for Playback mode (Figure 64 and Figure 65) and operates at recording path for Recording mode (Figure 62 and Figure 63).

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 27), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 28).

When ZELMN bit = “0” (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 29). When ALC output level exceeds full-scale at LFST bit = “1”, IVL and IVR values are immediately (period: 1/fs) changed in 1 step(L/R common). When ALC output level is less than full-scale, the IVL and IVR values are changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = “1” (zero cross detection is disabled.), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting LMAT1-0 bits.

The attenuation operation is exceeded continuously until the input signal level becomes ALC limiter detection level (Table 27) or less. After completing the attenuate operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds LMTH1-0 bits.

| LMTH1 bit | LMTH0 bit | ALC Limier Detection Level | ALC Recovery Waiting Counter Reset Level | (default) |
|-----------|-----------|-----------------------------------|--|-----------|
| 0 | 0 | ALC Output $\geq -2.5\text{dBFS}$ | $-2.5\text{dBFS} > \text{ALC Output} \geq -4.1\text{dBFS}$ | |
| 0 | 1 | ALC Output $\geq -4.1\text{dBFS}$ | $-4.1\text{dBFS} > \text{ALC Output} \geq -6.0\text{dBFS}$ | |
| 1 | 0 | ALC Output $\geq -6.0\text{dBFS}$ | $-6.0\text{dBFS} > \text{ALC Output} \geq -8.5\text{dBFS}$ | |
| 1 | 1 | ALC Output $\geq -8.5\text{dBFS}$ | $-8.5\text{dBFS} > \text{ALC Output} \geq -12\text{dBFS}$ | |

Table 27. ALC Limiter Detection Level / Recovery Counter Reset Level

| LMAT1 bit | LMAT0 bit | ALC Limiter ATT Step | | | | (default) |
|-----------|-----------|-------------------------------|-----------------------------|--|---|-----------|
| | | ALC Output $\geq \text{LMTH}$ | ALC Output $\geq \text{FS}$ | ALC Output $\geq \text{FS} + 6\text{dB}$ | ALC Output $\geq \text{FS} + 12\text{dB}$ | |
| 0 | 0 | 1 | 1 | 1 | 1 | |
| 0 | 1 | 2 | 2 | 2 | 2 | |
| 1 | 0 | 2 | 4 | 4 | 8 | |
| 1 | 1 | 1 | 2 | 4 | 8 | |

Table 28. ALC Limiter ATT Step

| ZTM1 bit | ZTM0 bit | Zero Crossing Timeout Period | | | | (default) |
|----------|----------|------------------------------|-------|-------|---------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 29. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 30) to be set after completing the ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 27) during the wait time, the ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 31) up to the set reference level (Table 32) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 29). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed in a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed. If ZTM1-0 bits is longer than WTM2-0 bits and no zero crossing occurs, the ALC recovery operation is executed in a period set by ZTM1-0 bits.

For example, when the current IVL and IVR values are 30H and RGAIN1-0 bits are set to “01”, IVL and IVR values are changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVL and IVR values exceed the reference level (REF7-0 bits), the IVL and IVR values are not increased.

When

“ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

“ALC recovery waiting counter reset level (LMTH1-0) > Output Signal”, the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 33).

| WTM2 bit | WTM1 bit | WTM0 bit | ALC Recovery Operation Waiting Period | | | (default) |
|----------|----------|----------|---------------------------------------|--------|---------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms |
| 0 | 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms |
| 0 | 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms |
| 0 | 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms |
| 1 | 0 | 0 | 2048/fs | 256ms | 128ms | 46.4ms |
| 1 | 0 | 1 | 4096/fs | 512ms | 256ms | 92.9ms |
| 1 | 1 | 0 | 8192/fs | 1024ms | 512ms | 185.8ms |
| 1 | 1 | 1 | 16384/fs | 2048ms | 1024ms | 371.5ms |

Table 30. ALC Recovery Operation Waiting Period

| RGAIN1 bit | RGAIN0 bit | GAIN STEP | | (default) |
|------------|------------|-----------|---------|-----------|
| 0 | 0 | 1 step | 0.375dB | |
| 0 | 1 | 2 step | 0.750dB | |
| 1 | 0 | 3 step | 1.125dB | |
| 1 | 1 | 4 step | 1.500dB | |

Table 31. ALC Recovery GAIN Step

| REF7-0 bits | GAIN (dB) | Step |
|-------------|-----------|-------------------|
| F1H | +36.0 | 0.375dB (default) |
| F0H | +35.625 | |
| EFH | +35.25 | |
| : | : | |
| E1H | +30.0 | |
| : | : | |
| 92H | +0.375 | |
| 91H | 0.0 | |
| 90H | -0.375 | |
| : | : | |
| 02H | -53.625 | |
| 01H | -54.0 | |
| 00H | MUTE | |

Table 32. Reference Level at ALC Recovery Operation

| RFST1 bit | RFST0 bit | Recovery Speed |
|-----------|-----------|-------------------|
| 0 | 0 | 4 times (default) |
| 0 | 1 | 8 times |
| 1 | 0 | 16times |
| 1 | 1 | N/A |

Table 33. Fast Recovery Speed Setting (N/A: Not available)

3. Example of ALC Operation

Table 34 and Table 35 show the examples of the ALC setting for mic recording and playback, respectively.

| Register Name | Comment | fs=8kHz | | fs=44.1kHz | |
|-------------------|---|---------|-----------|------------|-----------|
| | | Data | Operation | Data | Operation |
| LMTH1-0 | Limiter detection Level | 01 | -4.1dBFS | 01 | -4.1dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period * ZTM1-0 bits should be equal to or shorter than WTM2-0 bits. | 01 | 32ms | 11 | 23.2ms |
| WTM2-0 | Recovery waiting period | 001 | 32ms | 100 | 46.4ms |
| REF7-0 | Maximum gain at recovery operation | E1H | +30dB | E1H | +30dB |
| IVL7-0, IVR7-0 | Gain of IVOL | E1H | +30dB | E1H | +30dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| RFST1-0 | Fast Recovery Speed | 00 | 4 times | 00 | 4 times |
| ALC | ALC enable | 1 | Enable | 1 | Enable |

Table 34. Example of the ALC setting (Recording Path)

| Register Name | Comment | fs=8kHz | | fs=44.1kHz | |
|-------------------|--|---------|-----------|------------|-----------|
| | | Data | Operation | Data | Operation |
| LMTH1-0 | Limiter detection Level | 01 | -4.1dBFS | 01 | -4.1dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 01 | 32ms | 11 | 23.2ms |
| WTM2-0 | Recovery waiting period *WTM2-0 bits should be the same or longer data as ZTM1-0 bits | 001 | 32ms | 100 | 46.4ms |
| REF7-0 | Maximum gain at recovery operation | A1H | +6dB | A1H | +6dB |
| IVL7-0, IVR7-0 | Gain of IVOL | 91H | 0dB | 91H | 0dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| RFST1-0 | Fast Recovery Speed | 00 | 4 times | 00 | 4 times |
| ALC | ALC enable | 1 | Enable | 1 | Enable |

Table 35. Example of the ALC setting (Playback Path)

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0".

- LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0, LFST and FR bits

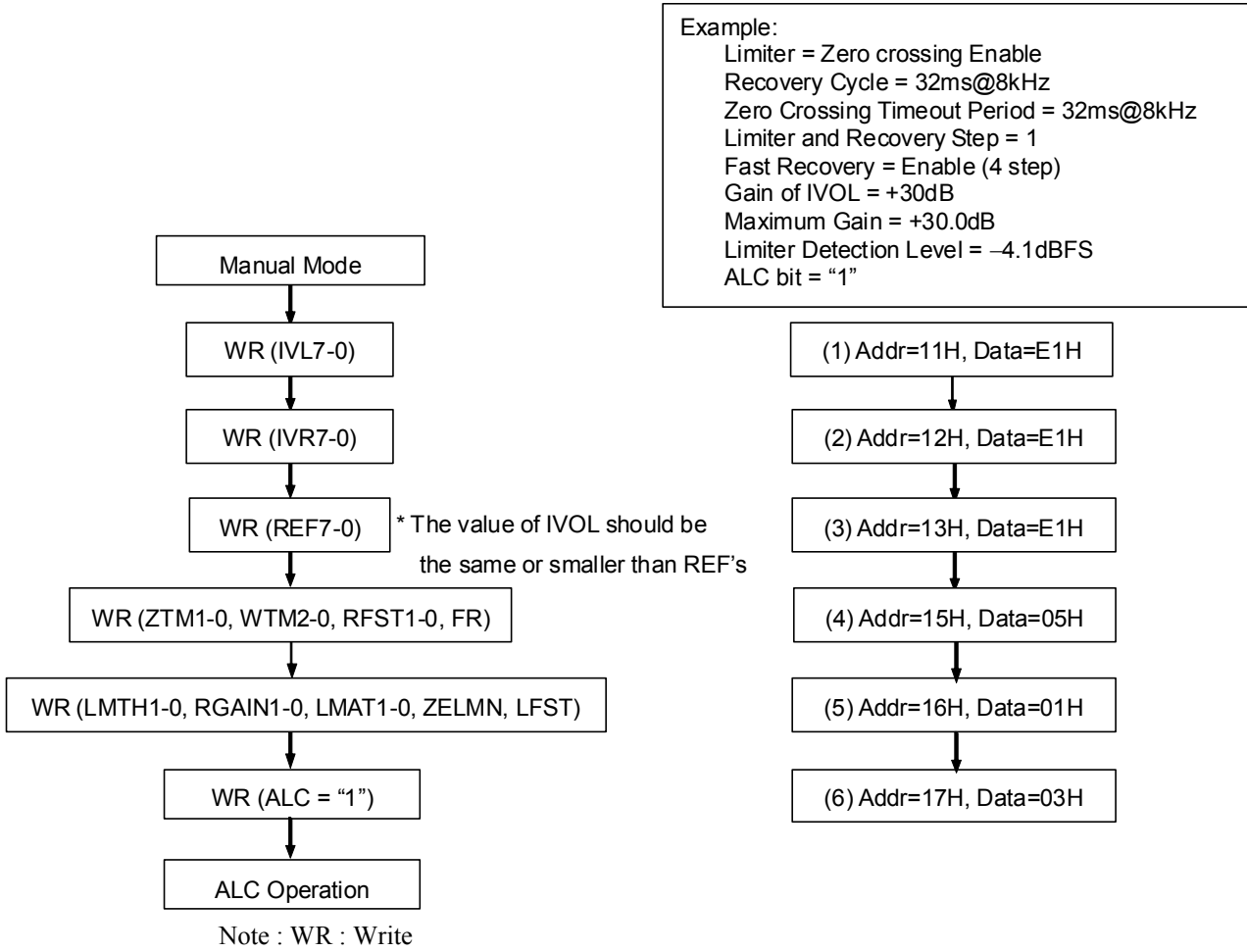


Figure 67. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is “0”. This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH1-0 bits and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed.
For example, in case of changing the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 36). When IVOLC bit is “0”, IVL7-0 and IVR7-0 bits control Lch and Rch volume values independently. When IVOLC bit is “1”, IVL7-0 bits controls both channels. The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR=PMDML=PMDMR bits = “0”, IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL, PMADR, PMDML or PMMDR bit is changed to “1”.

| IVL7-0 bits IVR7-0 bits | GAIN (dB) | Step |
|----------------------------|-----------|-------------------|
| F1H | +36.0 | 0.375dB (default) |
| F0H | +35.625 | |
| EFH | +35.25 | |
| : | : | |
| 92H | +0.375 | |
| 91H | 0.0 | |
| 90H | -0.375 | |
| : | : | |
| 03H | -53.25 | |
| 02H | -53.625 | |
| 01H | -54 | |
| 00H | MUTE | |

Table 36. Input Digital Volume Setting

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 37). It is proportional to the sampling frequency (f_s) and default is 3.4Hz (@ $f_s = 44.1\text{kHz}$). HPFAD bit controls the ON/OFF of the HPF1 (Recommend HPF enable).

| HPFC1 bit | HPFC0 bit | f_c | | |
|-----------|-----------|----------------------|-----------------------|-------------------|
| | | $f_s=44.1\text{kHz}$ | $f_s=22.05\text{kHz}$ | $f_s=8\text{kHz}$ |
| 0 | 0 | 3.4Hz | 1.7Hz | 0.62Hz |
| 0 | 1 | 13.6Hz | 6.8Hz | 2.47Hz |
| 1 | 0 | 108.8Hz | 54.4Hz | 19.7Hz |
| 1 | 1 | 217.6Hz | 108.8Hz | 39.5Hz |

(default)

Table 37. HPF1 Cut-off Frequency

■ Side Tone Volume (SVOLA)

The AK4679 has the channel independent side tone volume (5 levels, 6dB step). The volume can be set by the SVAL/R2-0 bits. The volume is included at mixing path from ALC to 5-band EQ. The output data of ALC is changed from 0 to -24dB.

| SVAL/R2-0 bits | Gain |
|----------------|-------|
| 0H | 0dB |
| 1H | -6dB |
| 2H | -12dB |
| 3H | -18dB |
| 4H | -24dB |
| Others | N/A |

(default)

Table 38. Side Tone Volume A Code Table (N/A: Not available)

■ 5-Band Equalizer

The AK4679 has 5-Band Equalizer before DAC of Stereo CODEC. The 5-band Equalizer is selected ON/OFF by 5EQ bit. When 5-band Equalizer is OFF, the audio data passes this block by 0dB gain. Each coefficient and transfer function of 5-band Equalizer is as follows. The coefficient must be set when 5EQ bit = "0" or PMEQ bit = "0".

Gain range of 5-band equalizer is set from +12dB to -12dB (0.5dB step) independently by 5EQ1G5-0, 5EQ2G5-0, 5EQ3G5-0, 5EQ4G5-0 or 5EQ5G5-0 bits.

The 5-band Equalizer starts operation $4/f_s(\text{max})$ after when 5EQ bit = "1" and PMEQ bit = "1" is set.

1. EQ1: 1st order Low Pass Filter

<Low Pass Filter>

f_s : Sampling frequency

f_c : Cut-off frequency

k : Filter gain

Register setting (Note 75)

5E1A[13:0] bits =A, 5E1B[13:0] bits =B

(MSB=5E1A13, 5E1B13; LSB=5E1A0, 5E1B0)

$$A = k \times \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function

$$h_{1L}(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$f_c / f_s \geq 0.05 \quad (f_c \text{ min} = 2205\text{Hz at } 44.1\text{kHz})$$

2. EQ2, EQ3, EQ4: Equalizer

5E2A15-0, 5E2B15-0 and 5E2C15-0 bits set the coefficient of EQ2. 5E3A15-0, 5E3B15-0 and 5E3C15-0 bits set the coefficient of EQ3. 5E4A15-0, 5E4B15-0 and 5E4C15-0 bits set the coefficient of EQ4.

fs: Sampling frequency

fo₂ ~ fo₄: Center frequency

fb₂ ~ fb₄: Band width where the gain is 3dB different from center frequency

k₂ ~ k₄: Filter gain

Register setting (Note 75)

EQ2: 5E2A[15:0] bits =A₁, 5E2B[15:0] bits =B₁, 5E2C[15:0] bits =C₂

EQ3: 5E3A[15:0] bits =A₂, 5E3B[15:0] bits =B₂, 5E3C[15:0] bits =C₃

EQ4: 5E4A[15:0] bits =A₃, 5E4B[15:0] bits =B₃, 5E4C[15:0] bits =C₄

(MSB=5E2A15, 5E2B15, 5E2C15, 5E3A15, 5E3B15, 5E3C15, 5E4A15, 5E4B15, 5E4C15; LSB= 5E2A0, 5E2B0, 5E2C0, 5E3A0, 5E3B0, 5E3C0, 5E4A0, 5E4B0, 5E4C0)

$$A_n = k_n \times \frac{\tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1 + \tan(\pi fb_n/fs)}, \quad C_n = \frac{1 - \tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}$$

(n = 2, 3, 4)

Transfer function

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 2, 3, 4)

The center frequency should be set as below.

$$fo_n / fs < 0.497$$

3. EQ5: 1st order High Pass Filter

<High Pass Filter>

fs: Sampling frequency

fc: Cut-off frequency

k: Filter gain

Register setting (Note 75)

5E5A[13:0] bits =A, 5E5B[13:0] bits =B

(MSB=5E5A13, 5E5B13; LSB=5E5A0, 5E5B0)

$$A = k \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$h_{5H}(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc/fs \geq 0.0001 \quad (fc \text{ min} = 4.41\text{Hz at } 44.1\text{kHz})$$

Note 75. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

$$X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$$

X should be rounded to integer, and then should be translated to binary code (2's complement).

MSB of each filter coefficient setting register is sine bit.

Total Transfer Function:

$$H(z) = K_1 \times h_{1L}(z) + K_2 \times h_2(z) + K_3 \times h_3(z) + K_4 \times h_4(z) + K_5 \times h_{5H}(z)$$

$K_1 \sim 5$: EQ Gain (+12 ~ -12dB, 0.5dB step). This value is changed by control register.

K_1 : 5EQ1G5-0 bits (Addr=6AH)

K_2 : 5EQ2G5-0 bits (Addr=6BH)

K_3 : 5EQ3G5-0 bits (Addr=6CH)

K_4 : 5EQ4G5-0 bits (Addr=6DH)

K_5 : 5EQ5G5-0 bits (Addr=6EH)

Default Center Frequency (Sampling Frequency = 44.1kHz):

EQ1: fc=100Hz

EQ2: fo₂=250Hz (fb₂=50Hz)

EQ3: fo₃=1kHz (fb₃=200Hz)

EQ4: fo₄=3.5kHz (fb₄=700Hz)

EQ5: fc=10kHz

| EQ1G5-0 bits EQ2G5-0 bits EQ3G5-0 bits EQ4G5-0 bits EQ5G5-0 bits | GAIN (dB) | EQ1G5-0 bits EQ2G5-0 bits EQ3G5-0 bits EQ4G5-0 bits EQ5G5-0 bits | GAIN (dB) |
|--|-----------|--|-----------|
| 30H | -12 | 17H | +0.5 |
| 2FH | -11.5 | 16H | +1 |
| 2EH | -11 | 15H | +1.5 |
| 2DH | -10.5 | 14H | +2 |
| 2CH | -10 | 13H | +2.5 |
| 2BH | -9.5 | 12H | +3 |
| 2AH | -9 | 11H | +3.5 |
| 29H | -8.5 | 10H | +4 |
| 28H | -8 | 0FH | +4.5 |
| 27H | -7.5 | 0EH | +5 |
| 26H | -7 | 0DH | +5.5 |
| 25H | -6.5 | 0CH | +6 |
| 24H | -6 | 0BH | +6.5 |
| 23H | -5.5 | 0AH | +7 |
| 22H | -5 | 09H | +7.5 |
| 21H | -4.5 | 08H | +8 |
| 20H | -4 | 07H | +8.5 |
| 1FH | -3.5 | 06H | +9 |
| 1EH | -3 | 05H | +9.5 |
| 1DH | -2.5 | 04H | +10 |
| 1CH | -2 | 03H | +10.5 |
| 1BH | -1.5 | 02H | +11 |
| 1AH | -1 | 01H | +11.5 |
| 19H | -0.5 | 00H | +12 |
| 18H | 0 | | |

Table 39. 5-band Equalizer Gain Setting (Default: 0dB)

■ Dynamic Range Control

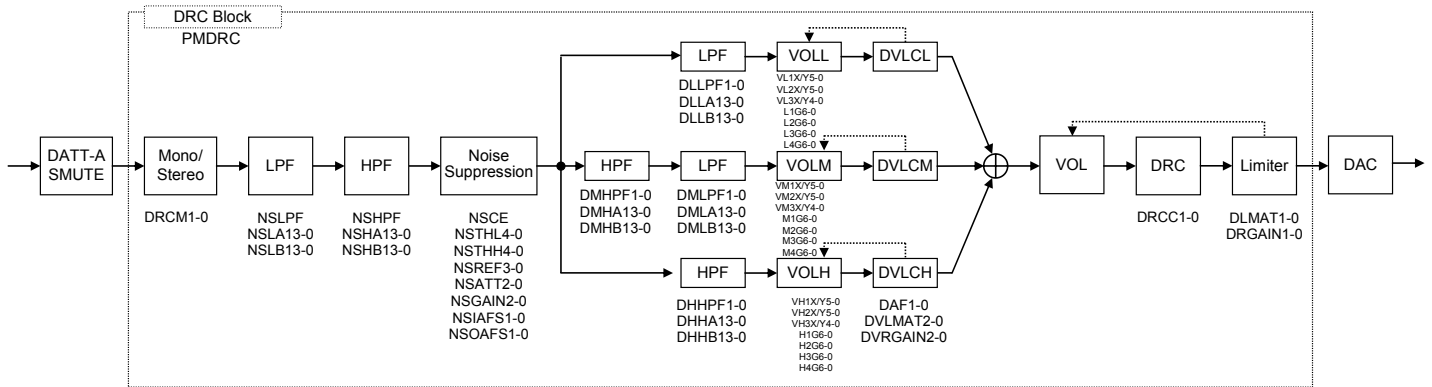


Figure 68. DRC Functions and Signal Path

DRCM1-0 bits select stereo or mono of DRC input data. In case of mono mode, the same data is input to both channels.

| DRCM1 bit | DRCM0 bit | Lch | Rch |
|-----------|-----------|-----|-----|
| 0 | 0 | L | R |
| 0 | 1 | L | L |
| 1 | 0 | R | R |
| 1 | 1 | N/A | |

(default)

Table 40. DRC Stereo/Mono Select (N/A: Not available)

1. Noise Suppression Block

(1) Low Pass Filter (LPF)

This is composed with 1st order LPF. NSLA13-0 bits and NSLB13-0 bits set the coefficient of LPF. NSLPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when NSLPF bit = “0” or PMDRC bit = “0”. The LPF starts operation 4/fs(max) after when NSLPF bit = “1” and PMDRC bit = “1” are set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting

LPF: NSLA[13:0] bits =A, NSLB[13:0] bits =B
(MSB=NSLA13, NSLB13; LSB=NSLA0, NSLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(2) High Pass Filter (HPF)

This is composed 1st order HPF. The coefficient of HPF is set by NSHA13-0 bits and NSHB13-0 bits. NSHPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when NSHPF bit = "0" or PMDRC bit = "0". The HPF starts operation $4/f_s(\max)$ after when NSHPF bit = "1" and PMDRC bit = "1" are set.

f_s : Sampling frequency
 f_c : Cut-off frequency

Register setting

HPF: NSHA[13:0] bits =A, NSHB[13:0] bits =B
 (MSB=NSHA13, NSHB13; LSB=NSHA0, NSHB0)

$$A = \frac{1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
 $f_c / f_s \geq 0.0001$ ($f_c \min = 4.41\text{Hz}$ at 44.1kHz)

(3) Noise Suppression

The Noise Suppression is enabled when NSCE bit (Noise suppression enable bit) = "1" during DRC operation (PMDRC bit = "1"). This function attenuates output signal level automatically when minute amount of the signal is input.

NSCE bit: Noise Suppression Enable
 0: Disable (default)
 1: Enable

(3-1) Noise Level Suppressing Operation

The output signal is suppressed when the input moving average level set by NSIAF1-0 bits (Table 41) is lower than "Noise Suppression Threshold Low Level" set by NSTHL4-0 bits (Table 42) during the normal operation.

This operation attenuates the volume automatically to the reference level set by NSREF3-0 bits (Table 43) with the soft transition of the attenuation speed set by NSATT2-0 bits (Table 44).

| NSIAF1-0 bits | Moving Average Parameter | | | |
|---------------|--------------------------|-------------------|--------------------|----------------------|
| | | $f_s=8\text{kHz}$ | $f_s=16\text{kHz}$ | $f_s=44.1\text{kHz}$ |
| 00 | 256/ f_s | 32ms | 16ms | 5.8ms |
| 01 | 512/ f_s | 64ms | 32ms | 11.6ms |
| 10 | 1024/ f_s | 128ms | 64ms | 23.2ms |
| 11 | 2048/ f_s | 256ms | 128ms | 46.4ms |

(default)

Table 41. Moving Average Parameter Setting at Noise Suppression Off

| NSTHL4-0 bits | Noise Suppression Threshold Low Level [dB] | Step |
|---------------|--|-------|
| 00H | -36.0 | 1.5dB |
| 01H | -37.5 | |
| 02H | -39.0 | |
| : | : | |
| 10H | -60.0 | |
| : | : | |
| 1EH | -81.0 | |
| 1FH | -82.5 | |

(default)

Table 42. Noise Suppression Threshold Low Level

| NSREF3-0 bits | GAIN [dB] | Step |
|---------------|-----------|------|
| 0H | -9 | 3dB |
| 1H | -12 | |
| 2H | -15 | |
| : | : | |
| AH | -39 | |
| BH | -42 | |
| CH | -45 | |
| DH | -48 | |
| EH | -51 | |
| FH | -54 | |

(default)

Table 43. Reference Value Setting when Noise Suppression is ON

| NSATT2 bit | NSATT1 bit | NSATT0 bit | ATT Speed | | |
|------------|------------|------------|-----------|----------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 0 | 1.1dB/s | 2.1dB/s | 5.8dB/s |
| 0 | 0 | 1 | 2.1dB/s | 4.2dB/s | 11.7dB/s |
| 0 | 1 | 0 | 4.2dB/s | 8.5dB/s | 23.4dB/s |
| 0 | 1 | 1 | 8.5dB/s | 17.0dB/s | 46.8dB/s |
| 1 | 0 | 0 | 17.0dB/s | 33.9dB/s | 93.5dB/s |
| 1 | 0 | 1 | 33.9dB/s | 67.9dB/s | 187.1dB/s |
| 1 | 1 | 0 | N/A | | |
| 1 | 1 | 1 | | | |

(default)

Table 44. Noise Suppression ATT Speed Setting (N/A: Not available)

(3-2) Noise Suppression → Normal Operation

During noise suppressing operation, if the input moving average level set by NSOAF1-0 bits (Table 45) exceeds Noise Suppression Threshold High Level set by NSTHH4-0 bits (Table 46), the operation switches to normal operation from noise suppressing operation.

This recovery operation sets the volume automatically to 0dB with the soft transition of the recovery speed set by NSGAIN2-0 bits (Table 47).

| NSOAF1-0 bits | Moving Average Parameter | | | |
|---------------|--------------------------|---------|----------|------------|
| | | fs=8kHz | fs=16kHz | fs=44.1kHz |
| 00 | 4/fs | 0.5ms | 0.3ms | 0.1ms |
| 01 | 8/fs | 1.0ms | 0.5ms | 0.2ms |
| 10 | 16/fs | 2.0ms | 1.0ms | 0.4ms |
| 11 | 32/fs | 4.0ms | 2.0ms | 0.7ms |

Table 45. Moving Average Parameter Setting at Noise Suppression On

| NSTHH4-0 bits | Noise Suppression Threshold High Level [dBFS] | Step |
|---------------|---|-------|
| 00H | -36.0 | 1.5dB |
| 01H | -37.5 | |
| 02H | -39.0 | |
| : | : | |
| 10H | -60.0 | |
| : | : | |
| 1EH | -81.0 | |
| 1FH | -82.5 | |

Table 46. Noise Suppression Threshold High Level

| NSGAIN2 bit | NSGAIN1 bit | NSGAIN0 bit | Recovery Speed | | |
|-------------|-------------|-------------|----------------|----------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 0 | 0.3dB/ms | 0.5dB/ms | 1.5dB/ms |
| 0 | 0 | 1 | 0.5dB/ms | 1.1dB/ms | 3.0dB/ms |
| 0 | 1 | 0 | 1.1dB/ms | 2.2dB/ms | 6.0dB/ms |
| 0 | 1 | 1 | 2.2dB/ms | 4.4dB/ms | 12.2dB/ms |
| 1 | 0 | 0 | 4.5dB/ms | 9.0dB/ms | 24.7dB/ms |
| 1 | 0 | 1 | N/A | | |
| 1 | 1 | 0 | | | |
| 1 | 1 | 1 | | | |

Table 47. Recovery Speed Setting from Noise Suppression to Normal Operation (N/A: Not available)

2. Dynamic Volume Control Block

The AK4679 has the dynamic volume control (DVLC) circuits before DRC. DVLC divides frequency range into three band (Low, Middle, High) and controls independently.

(1) Low Frequency Range

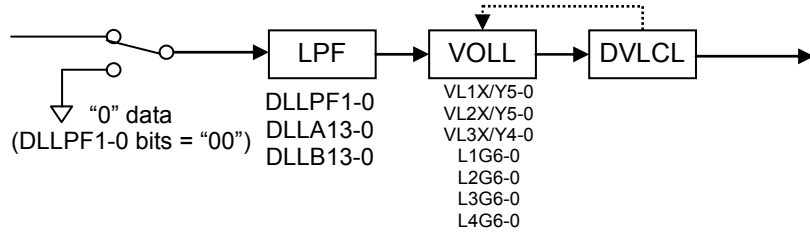


Figure 69. DVLC Functions and Signal Path for Low Frequency Range

(1-1) Low Pass Filter (LPF)

This is composed with 1st or 2nd order LPF. DLLA13-0 bits and DLLB13-0 bits set the coefficient of LPF. DLLPF1-0 bits controls ON/OFF of the LPF. When the LPF is OFF, the audio data does not pass this block. The coefficient must be set when DLLPF1-0 bits = "00" or PMDRC bit = "0". The LPF starts operation $4/f_s(\max)$ after when DLLPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

| DLLPF1 bit | DLLPF0 bit | Mode |
|------------|------------|----------------|
| 0 | 0 | OFF ("0" data) |
| 0 | 1 | 1st order LPF |
| 1 | 0 | 2nd order LPF |
| 1 | 1 | N/A |

(default)

Table 48. DLLPF Mode Setting (N/A: Not available)

f_s : Sampling frequency
 f_c : Cut-off frequency

Register setting

LPF: DLLA[13:0] bits =A, DLLB[13:0] bits =B
 (MSB=DLLA13, DLLB13; LSB=DLLA0, DLLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}} \times A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$f_c / f_s \geq 0.002 \quad (f_c \min = 88\text{Hz at } 44.1\text{kHz})$$

(1-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VL1X5-0, VL1Y5-0, VL2X5-0, VL2Y5-0, VL3X4-0 and VL3Y4-0 bits). The setting of three inflection points are calculated the values of (X_{1L}, Y_{1L}) , (X_{2L}, Y_{2L}) , (X_{3L}, Y_{3L}) in dB. The inflection points should be set in such a way that $VL1X \leq VL2X \leq VL3X$, $VL1Y \leq VL2Y \leq VL3Y$. And the each slope is set by L1G6-0, L2G6-0, L3G6-0 and L4G6-0 bits. X_{4L} is fixed full-scale, Y_{4L} is calculated by the L4G value. The initial value of the DVLC gain is set by the L1G.

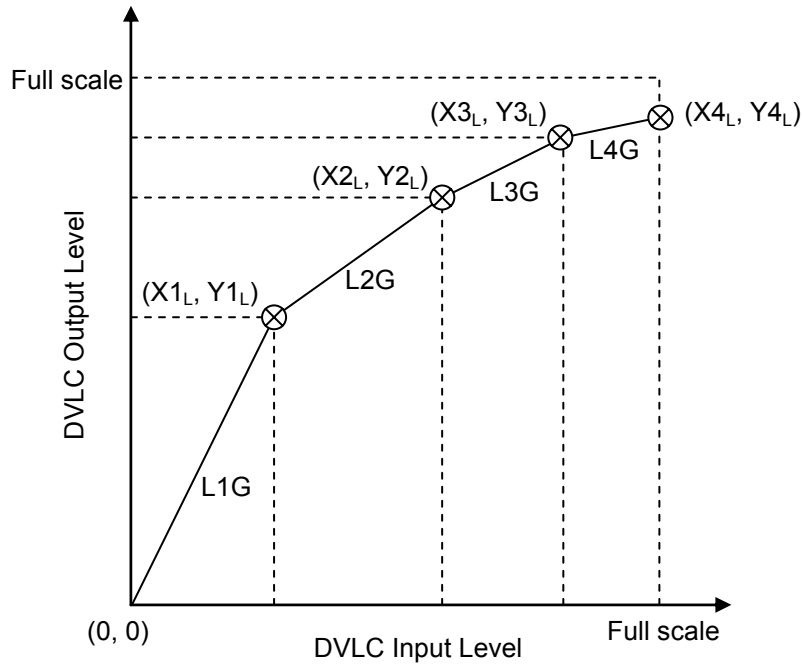


Figure 70. DVLC Curve for Low Frequency Range

| VL1X/Y5-0 bits VL2X/Y5-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------------------------|-------------------------------------|-------|
| 00H | 0 | 1.5dB |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 2EH | -69.0 | |
| 2FH | -70.5 | N/A |
| 30H | N/A | |
| 3FH | N/A | |

Table 49. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

| VL3X/Y4-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------|-------------------------------------|-------|
| 00H | 0 | 1.5dB |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 1EH | -45.0 | |
| 1FH | -46.5 | |

Table 50. DVLC Point Setting for X/Y3

Slope Setting

$$L1G = \frac{Y1_L}{X1_L} \times 16, \quad L2G = \frac{(Y2_L - Y1_L)}{(X2_L - X1_L)} \times 16,$$

$$L3G = \frac{(Y3_L - Y2_L)}{(X3_L - X2_L)} \times 16, \quad L4G = \frac{(Y4_L - Y3_L)}{(X4_L - X3_L)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data.

| L1G6-0 bits, L2G6-0 bits, L3G6-0 bits, L4G6-0 bits | Slope Data |
|---|------------|
| 00H | 0 |
| 01H | 1 |
| 02H | 2 |
| : | : |
| 7EH | 126 |
| 7FH | 127 |

(default)

Table 51. DVLC Slope Setting for Low Frequency Range

(2) Middle Frequency Range

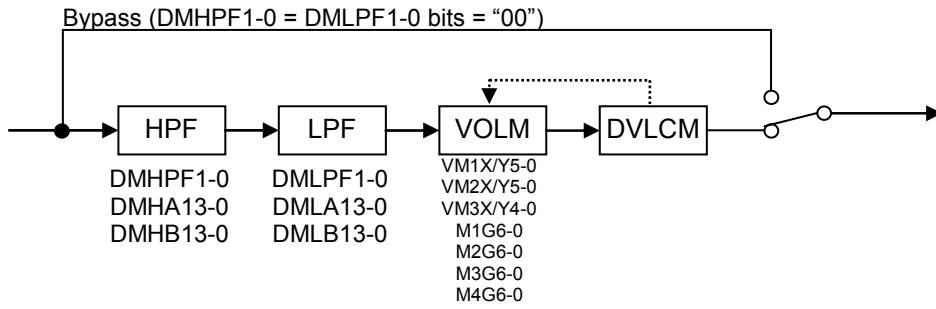


Figure 71. DVLC Functions and Signal Path for Middle Frequency Range

(2-1) High Pass Filter (HPF)

This is composed with 1st or 2nd order HPF. The coefficient of HPF is set by DMHA13-0 bits and DMHB13-0 bits. HPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMHPF1-0 bits = "00" or PMDRC bit = "0". The HPF starts operation 4/fs(max) after when DMHPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

| DMHPF1 bit | DMHPF0 bit | Mode |
|------------|------------|---------------|
| 0 | 0 | Bypass |
| 0 | 1 | 1st order HPF |
| 1 | 0 | 2nd order HPF |
| 1 | 1 | N/A |

(default)

Table 52. DMHPF Mode Setting (N/A: Not available)

fs: Sampling frequency

fc: Cut-off frequency

Register setting

HPF: DMHA[13:0] bits =A, DMHB[13:0] bits =B
 (MSB=DMHA13, DMHB13; LSB=DMHA0, DMHB0)

$$A = \frac{1 / \tan(\pi fc / fs)}{1 + 1 / \tan(\pi fc / fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc / fs)}{1 + 1 / \tan(\pi fc / fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}} \times A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc / fs \geq 0.0001 \quad (fc \text{ min} = 4.41\text{Hz at } 44.1\text{kHz})$$

(2-2) Low Pass Filter (LPF)

This is composed with 1st or 2nd order LPF. DLLA13-0 bits and DMLB13-0 bits set the coefficient of LPF. DMLPF1-0 bits controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMLPF1-0 bits = "00" or PMDRC bit = "0". The LPF starts operation $4/f_s(\max)$ after when DMLPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

| DMLPF1 bit | DMLPF0 bit | Mode |
|------------|------------|---------------|
| 0 | 0 | Bypass |
| 0 | 1 | 1st order LPF |
| 1 | 0 | 2nd order LPF |
| 1 | 1 | N/A |

(default)

Table 53. DMLPF Mode Setting (N/A: Not available)

fs: Sampling frequency

fc: Cut-off frequency

Register setting

LPF: DMLA[13:0] bits =A, DMLB[13:0] bits =B
(MSB=DMLA13, DMLB13; LSB=DMLA0, DMLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}} \times A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc/fs \geq 0.05 \quad (fc \text{ min} = 2205\text{Hz at } 44.1\text{kHz})$$

(2-3) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VM1X5-0, VM1Y5-0, VM2X5-0, VM2Y5-0, VM3X4-0 and VM3Y4-0 bits). The setting of three inflection points are calculated the values of (X_{1M}, Y_{1M}) , (X_{2M}, Y_{2M}) , (X_{3M}, Y_{3M}) in dB. The inflection points should be set in such a way that $VM1X \leq VM2X \leq VM3X$, $VM1Y \leq VM2Y \leq VM3Y$. And the each slope is set by M1G6-0, M2G6-0, M3G6-0 and M4G6-0 bits. X_{4M} is fixed full-scale, Y_{4M} is calculated by the M4G value. The initial value of the DVLC gain is set by the M1G. When the HPF and LPF is bypass (DMHPF1-0 = DMLPF1-0 bits = "00"), the audio data passes this block by 0dB gain.

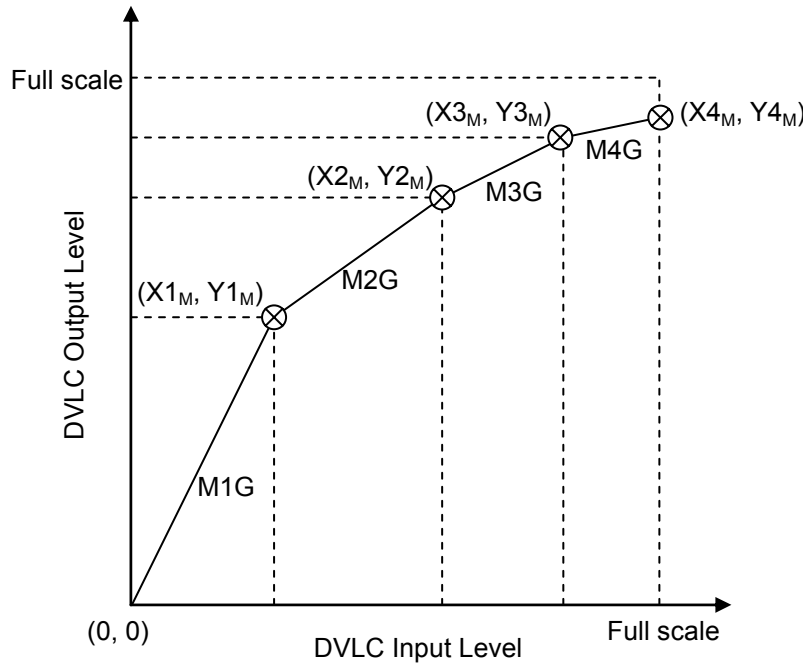


Figure 72. DVLC Curve for Middle Frequency Range

| VM1X/Y5-0 bits VM2X/Y5-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------------------------|-------------------------------------|-----------------|
| 00H | 0 | 1.5dB (default) |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 2EH | -69.0 | |
| 2FH | -70.5 | |
| 30H | N/A | N/A |
| : | : | |
| 3FH | N/A | |

Table 54. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

| VM3X/Y4-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------|-------------------------------------|-----------------|
| 00H | 0 | 1.5dB (default) |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 1EH | -45.0 | |
| 1FH | -46.5 | |

Table 55. DVLC Point Setting for X/Y3

Slope Setting

$$M1G = \frac{Y1_M}{X1_M} \times 16, \quad M2G = \frac{(Y2_M - Y1_M)}{(X2_M - X1_M)} \times 16,$$

$$M3G = \frac{(Y3_M - Y2_M)}{(X3_M - X2_M)} \times 16, \quad M4G = \frac{(Y4_M - Y3_M)}{(X4_M - X3_M)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data.

| M1G6-0 bits, M2G6-0 bits, M3G6-0 bits, M4G6-0 bits | Slope Data |
|---|------------|
| 00H | 0 |
| 01H | 1 |
| 02H | 2 |
| : | : |
| 7EH | 126 |
| 7FH | 127 |

(default)

Table 56. DVLC Slope Setting for Middle Frequency Range

(3) High Frequency Range

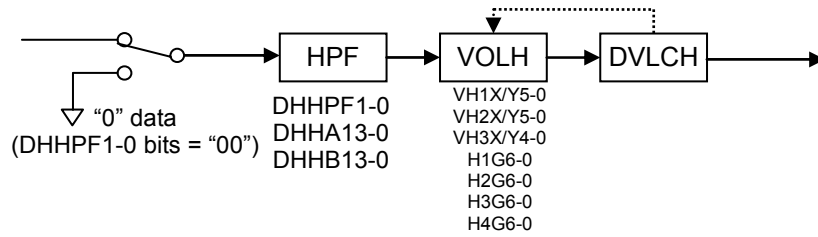


Figure 73. DVLC Functions and Signal Path for High Frequency Range

(3-1) High Pass Filter (HPF)

This is composed with 1st or 2nd order HPF. The coefficient of HPF is set by DHHA13-0 bits and DHHB13-0 bits. HPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data does not pass this block. The coefficient must be set when DHHHPF1-0 bits = "00" or PMDRC bit = "0". The HPF starts operation 4/fs(max) after when DHHHPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

| DHHHPF1 bit | DHHHPF0 bit | Mode |
|-------------|-------------|----------------|
| 0 | 0 | OFF ("0" data) |
| 0 | 1 | 1st order HPF |
| 1 | 0 | 2nd order HPF |
| 1 | 1 | N/A |

(default)

Table 57. DHHHPF Mode Setting (N/A: Not available)

fs: Sampling frequency

fc: Cut-off frequency

Register setting

HPF: DHHA[13:0] bits =A, DHHB[13:0] bits =B
 (MSB=DHHA13, DMHB13; LSB=DHHA0, DHHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}} \times A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc/fs \geq 0.0001 \quad (fc \text{ min} = 4.41\text{Hz at } 44.1\text{kHz})$$

(3-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VH1X5-0, VH1Y5-0, VH2X5-0, VH2Y5-0, VH3X4-0 and VH3Y4-0 bits). The setting of three inflection points are calculated the values of (X_{1H}, Y_{1H}), (X_{2H}, Y_{2H}), (X_{3H}, Y_{3H}) in dB. The inflection points should be set in such a way that VH1X ≤ VH2X ≤ VH3X, VH1Y ≤ VH2Y ≤ VH3Y. And the each slope is set by H1G6-0, H2G6-0, H3G6-0 and H4G6-0 bits. X_{4H} is fixed full-scale, Y_{4H} is calculated by the H4G value. The initial value of the DVLC gain is set by the H1G.

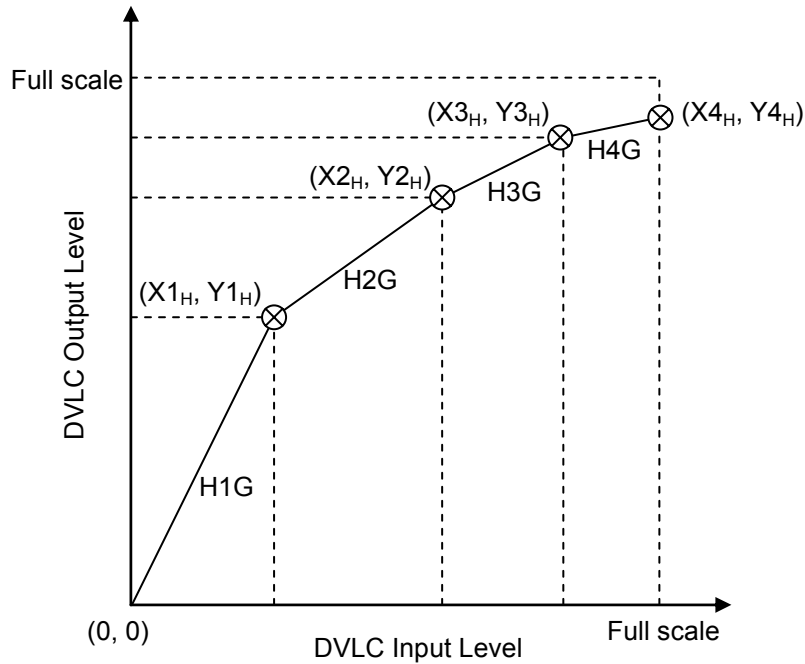


Figure 74. DVLC Curve for High Frequency Range

| VH1X/Y5-0 bits VH2X/Y5-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------------------------|-------------------------------------|-------|
| 00H | 0 | 1.5dB |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 2EH | -69.0 | |
| 2FH | -70.5 | |
| 30H | N/A | N/A |
| : | : | |
| 3FH | N/A | |

Table 58. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

| VH3X/Y4-0 bits | Dynamic Volume Control Point [dBFS] | Step |
|----------------|-------------------------------------|-------|
| 00H | 0 | 1.5dB |
| 01H | -1.5 | |
| 02H | -3.0 | |
| : | : | |
| 1EH | -45.0 | |
| 1FH | -46.5 | |

Table 59. DVLC Point Setting for X/Y3

Slope Setting

$$H1G = \frac{Y1_H}{X1_H} \times 16, \quad H2G = \frac{(Y2_H - Y1_H)}{(X2_H - X1_H)} \times 16,$$

$$H3G = \frac{(Y3_H - Y2_H)}{(X3_H - X2_H)} \times 16, \quad H4G = \frac{(Y4_H - Y3_H)}{(X4_H - X3_H)} \times 16$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data.

| H1G6-0 bits, H2G6-0 bits, H3G6-0 bits, H4G6-0 bits | Slope Data |
|---|------------|
| 00H | 0 |
| 01H | 1 |
| 02H | 2 |
| : | : |
| 7EH | 126 |
| 7FH | 127 |

(default)

Table 60. DVLC Slope Setting for High Frequency Range

(4) Dynamic Volume Control

The DVLC automatically controls the volume at the attenuation speed set by DVLMAT2-0 bits (Table 62) or the recovery speed set by DVRGAIN2-0 bits (Table 63) in such a way that the input moving average level set by DAF1-0 bits (Table 61) is reached the output level of the DVLC curve set by each frequency range.

| DAF1-0 bits | Moving Average Parameter | | | |
|-------------|--------------------------|---------|----------|------------|
| | | fs=8kHz | fs=16kHz | fs=44.1kHz |
| 00 | 256/fs | 32ms | 16ms | 5.8ms |
| 01 | 512/fs | 64ms | 32ms | 11.6ms |
| 10 | 1024/fs | 128ms | 64ms | 23.2ms |
| 11 | 2048/fs | 256ms | 128ms | 46.4ms |

(default)

Table 61. DVLC Moving Average Parameter Setting

| DVLMAT2 bit | DVLMAT1 bit | DVLMAT0 bit | ATT Speed | | |
|-------------|-------------|-------------|-----------|-----------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 0 | 1.1dB/s | 2.1dB/s | 5.8dB/s |
| 0 | 0 | 1 | 2.1dB/s | 4.2dB/s | 11.7dB/s |
| 0 | 1 | 0 | 4.2dB/s | 8.5dB/s | 23.4dB/s |
| 0 | 1 | 1 | 8.5dB/s | 17.0dB/s | 46.8dB/s |
| 1 | 0 | 0 | 17.0dB/s | 33.9dB/s | 93.5dB/s |
| 1 | 0 | 1 | 33.9dB/s | 67.9dB/s | 187.1dB/s |
| 1 | 1 | 0 | 67.9dB/s | 135.8dB/s | 374.3dB/s |
| 1 | 1 | 1 | N/A | | |

(default)

Table 62. DVLC ATT Speed Setting (N/A: Not available)

| DVRGAIN2 bit | DVRGAIN1 bit | DVRGAIN0 bit | Recovery Speed | | |
|--------------|--------------|--------------|----------------|----------|----------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 0 | 0.07dB/s | 0.13dB/s | 0.37dB/s |
| 0 | 0 | 1 | 0.13dB/s | 0.27dB/s | 0.73dB/s |
| 0 | 1 | 0 | 0.27dB/s | 0.53dB/s | 1.46dB/s |
| 0 | 1 | 1 | 0.53dB/s | 1.06dB/s | 2.92dB/s |
| 1 | 0 | 0 | 1.06dB/s | 2.12dB/s | 5.84dB/s |
| 1 | 0 | 1 | 2.12dB/s | 4.24dB/s | 11.7dB/s |
| 1 | 1 | 0 | 4.24dB/s | 8.48dB/s | 23.4dB/s |
| 1 | 1 | 1 | N/A | | |

(default)

Table 63. DVLC Recovery Speed Setting (N/A: Not available)

3. Dynamic Range Control Block

The AK4679 has the dynamic range control (DRC) circuits. The compression level is selected in three levels and set by DRCC1-0 bits (Table 64).

When the DRC is OFF (DRCC1-0 bits = "00"), the audio data passes this block by 0dB gain. However limiter and recovery operation is always ON. The compression level must be set when PMDRC bit = "0".

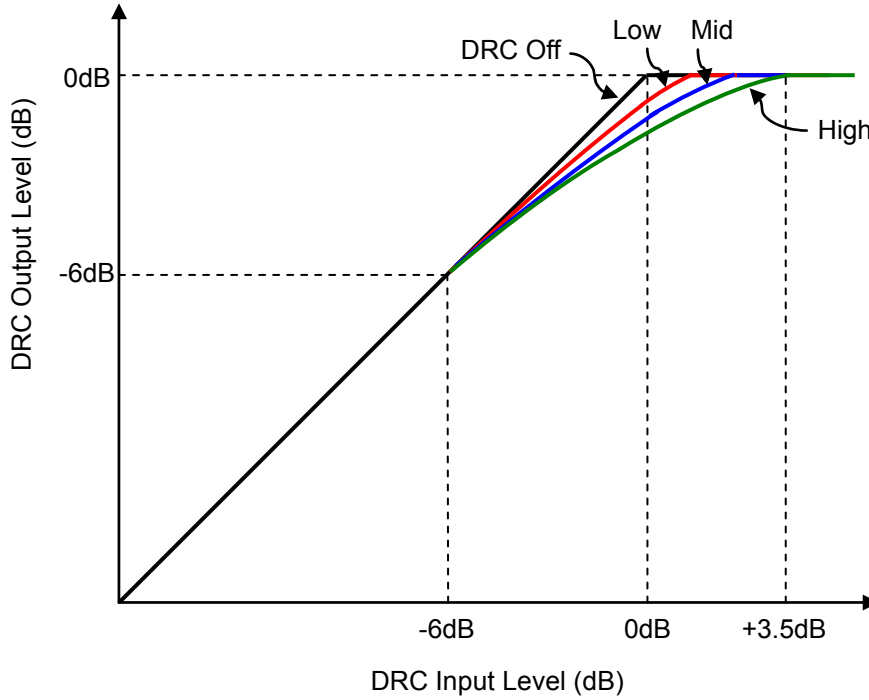


Figure 75. DRC Gain Curve

| DRCC1 bit | DRCC0 bit | Compression Level |
|-----------|-----------|-------------------|
| 0 | 0 | OFF |
| 0 | 1 | Low |
| 1 | 0 | Middle |
| 1 | 1 | High |

(default)

Table 64. DRC Compression Level Setting

1. DRC Limiter Operation

During the DRC limiter operation, when the output level of DRC exceeds full-scale, the DRC volume are attenuated automatically with the soft transition in the attenuation speed set by DLMAT2-0 bits (Table 65).

| DLMAT2 bit | DLMAT1 bit | DLMAT0 bit | ATT Speed | | |
|------------|------------|------------|-----------|----------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 0 | 0.1dB/ms | 0.3dB/ms | 0.7dB/ms |
| 0 | 0 | 1 | 0.3dB/ms | 0.5dB/ms | 1.5dB/ms |
| 0 | 1 | 0 | 0.5dB/ms | 1.1dB/ms | 3.0dB/ms |
| 0 | 1 | 1 | 1.1dB/ms | 2.2dB/ms | 6.0dB/ms |
| 1 | 0 | 0 | 2.2dB/ms | 4.4dB/ms | 12.2dB/ms |
| 1 | 0 | 1 | 4.5dB/ms | 9.0dB/ms | 24.7dB/ms |
| 1 | 1 | 0 | N/A | | |
| 1 | 1 | 1 | | | |

(default)

Table 65. DRC ATT Speed Setting (N/A: Not available)

2. DRC Recovery Operation

During the DRC recovery operation, when the DRC volume reaches 0dB or the output level of DRC exceeds limiter detection level, the DRC volume are set automatically with the soft transition in the recovery speed set by DRGAIN1-0 bits (Table 66).

| DRGAIN1 bit | DRGAIN0 bit | Recovery Speed | | |
|----------------|----------------|----------------|----------|----------|
| | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 1.1dB/s | 2.1dB/s | 5.9dB/s |
| 0 | 1 | 2.1dB/s | 4.2dB/s | 11.7dB/s |
| 1 | 0 | 4.2dB/s | 8.5dB/s | 23.4dB/s |
| 1 | 1 | 8.5dB/s | 17.0dB/s | 46.7dB/s |

(default)

Table 66. DRC Recovery Speed Setting

■ Digital Output Volume (DATT-A)

The AK4679 has a digital output volume (DATT-A: 128 levels, 0.5dB step, Mute). The volume can be set by the OVL6-0 and OVR6-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +6 to -57dB or MUTE. When the OVOLC bit = "1", the OVL6-0 bits control both Lch and Rch attenuation levels. When the OVOLC bit = "0", the OVL6-0 bits control Lch level and OVR6-0 bits control Rch level. This volume has a soft transition function. The OVTM bit sets the transition time between set values of OVL/R6-0 bits as either 128/fs or 256/fs (Table 68). When OVTM bit = "1", a soft transition between the set values occurs (256 levels). It takes 256/fs (=5.8ms@fs=44.1kHz) from 00H (+6dB) to 7FH (MUTE).

| OVL/R6-0 bits | Gain | Step |
|---------------|-----------|--------------------|
| 00H | +6.0dB | 0.5dB (default) |
| 01H | +5.5dB | |
| 02H | +5.0dB | |
| ⋮ | ⋮ | |
| 0CH | 0dB | |
| ⋮ | ⋮ | |
| 7DH | -56.5dB | |
| 7EH | -57.0dB | |
| 7FH | MUTE (-∞) | |

Table 67. Digital Volume A Code Table

| OVTM bit | Transition time between OVL/R6-0 bits = 00H and 7FH | | |
|----------|---|---------|------------|
| | Setting | fs=8kHz | fs=44.1kHz |
| 0 | 128/fs | 16ms | 2.9ms |
| 1 | 256/fs | 32ms | 5.8ms |

Table 68. Transition Time Setting of Digital Output Volume A

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is changed to “1”, the output signal is attenuated to $-\infty$ (“0”) during the cycle set by the OVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by the OVL/R6-0 bits during the cycle set of the OVTM bit. If the soft mute is cancelled within the cycle set by the OVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the OVL/R6-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 76).

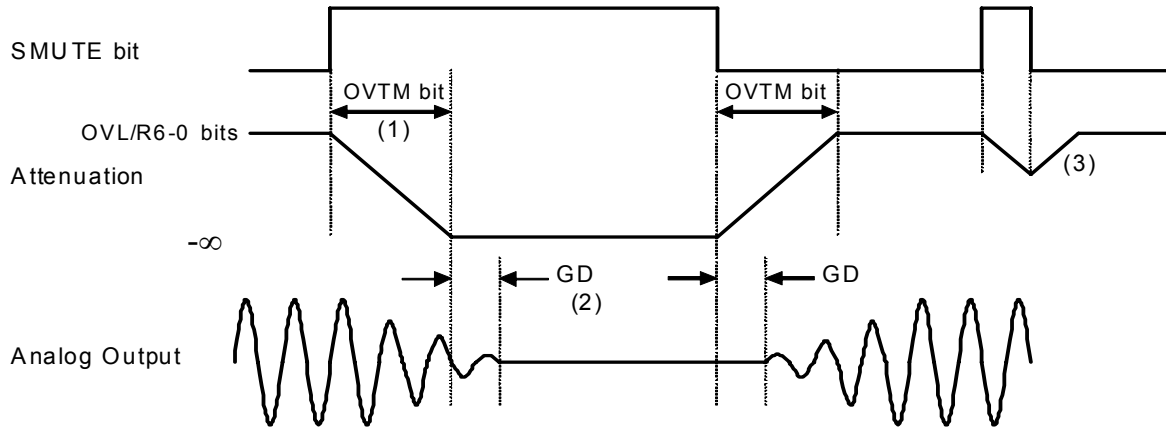


Figure 76. Soft Mute Function

- (1) The output signal is attenuated until $-\infty$ (“0”) in the cycle set by the OVTM bit.
- (2) Analog output corresponding to digital input has the group delay (GD).
- (3) If the soft mute is cancelled within the cycle set by the OVTM bit, the attenuation is discontinued and returned to the value set by the OVL/R6-0 bits.

■ Digital Volume for Recording of Received Voice (DATT-B)

The AK4679 has a digital output volume control (DATT-B: 128 levels, 0.5dB step, Mute) for recording of received voice. The volume can be set by the BVL6-0 bits. This volume is included in SRCAL blocks. The output data of SRCAL is changed from +6 to -57dB or MUTE. This volume control is in common for left and right channels. This volume has a soft transit function. The OVTMB bit sets the transition time between set values of BVL6-0 bits as either 128/fs or 256/fs (Table 70). When OVTMB bit = "1", a soft transition between the set values occurs (256 levels). It takes 256/fs (=5.8ms @ fs=44.1kHz, PMMIX bit = "1") from 00H (+6dB) to 7FH (MUTE).

| BVL6-0 bits | Gain | Step |
|-------------|-----------|--------------------|
| 00H | +6.0dB | 0.5dB (default) |
| 01H | +5.5dB | |
| 02H | +5.0dB | |
| ⋮ | ⋮ | |
| 0CH | 0dB | |
| ⋮ | ⋮ | |
| 7DH | -56.5dB | |
| 7EH | -57.0dB | |
| 7FH | MUTE (-∞) | |

Table 69. Digital Volume B Table

| OVTMB bit | Transition time between BVL6-0 bits = 00H and 7FH | | |
|-----------|---|---------|------------|
| | Setting | fs=8kHz | fs=44.1kHz |
| 0 | 128/fs | 16ms | 2.9ms |
| 1 | 256/fs | 32ms | 5.8ms |

(PMMIX bit = "0": fs = SYNCB Frequency, PMMIX bit = "1": fs = LRCK Frequency)

Table 70. Transition Time Setting of Digital Output Volume B

■ Digital Volume for Received Voice (DATT-C)

The AK4679 has a digital output volume control (DATT-C: 128 levels, 0.5dB step, Mute) for recording of received voice. The volume can be set by the CVL6-0 bits. The volume range is from +6 to -57dB or MUTE. This volume control is in common for left and right channels. This volume has a soft transit function. The OVTMB bit sets the transition time between set values of CVL6-0 bits as either 128/fs or 256/fs (Table 72). When OVTMB bit = "1", a soft transition between the set values occurs (256 levels). It takes 256/fs (=5.8ms @ fs =44.1kHz, PMMIX bit = "1") from 00H (+6dB) to 7FH (MUTE).

| CVL6-0 bits | Gain | Step |
|-------------|-----------|--------------------|
| 00H | +6.0dB | 0.5dB (default) |
| 01H | +5.5dB | |
| 02H | +5.0dB | |
| ⋮ | ⋮ | |
| 0CH | 0dB | |
| ⋮ | ⋮ | |
| 7DH | -56.5dB | |
| 7EH | -57.0dB | |
| 7FH | MUTE (-∞) | |

Table 71. Digital Volume C Table

| OVTMB bit | Transition time between CVL6-0 bits = 00H and 7FH | | |
|-----------|---|---------|------------|
| | Setting | fs=8kHz | fs=44.1kHz |
| 0 | 128/fs | 16ms | 2.9ms |
| 1 | 256/fs | 32ms | 5.8ms |

(PMMIX bit = "0": fs = SYNCB Frequency, PMMIX bit = "1": fs = LRCK Frequency)

Table 72. Transition Time Setting of Digital Output Volume C

■ Side Tone Volume for B/T Phone Call (SVOLB)

The AK4679 has the side tone volume control (5 levels, 6dB step) for B/T phone call. The volume can be set by the SVB2-0 bits. The volume range is from 0dB to -24dB.

| SVB2-0 bits | Gain |
|-------------|-------|
| 0H | 0dB |
| 1H | -6dB |
| 2H | -12dB |
| 3H | -18dB |
| 4H | -24dB |
| Others | N/A |

(default)

Table 73. Side Tone Volume B Table (N/A: Not available)

■ Digital Volume for B/T MIC Input (BIVOL)

The AK4679 has the digital volume control (5 levels, 6dB step) for B/T mic input. The volume can be set by the BIV2-0 bits. The volume range is from 0 to -24dB.

| BIV2-0 bits | Gain |
|-------------|-------|
| 0H | 0dB |
| 1H | -6dB |
| 2H | -12dB |
| 3H | -18dB |
| 4H | -24dB |
| Others | N/A |

(default)

Table 74. SDTIB Volume Table (N/A: Not available)

■ Path & Mixing Setting of Digital Block (Figure 61)

PMADL, PMADR, PMDML and PMDMR bits set both ADC power management and output data selection. In case of mono operation, the same data is output to both channel slots.

| PMADL bit | PMADR bit | ADC Lch data | ADC Rch data | |
|-----------|-----------|------------------|------------------|-----------|
| 0 | 0 | All "0" | All "0" | (default) |
| 0 | 1 | Rch Input Signal | Rch Input Signal | |
| 1 | 0 | Lch Input Signal | Lch Input Signal | |
| 1 | 1 | Lch Input Signal | Rch Input Signal | |

Table 75. ADC Mono/Stereo Select (Analog MIC: DMIC bit = "0")

| PMDML bit | PMDMR bit | ADC Lch data | ADC Rch data | |
|-----------|-----------|------------------|------------------|-----------|
| 0 | 0 | All "0" | All "0" | (default) |
| 0 | 1 | Rch Input Signal | Rch Input Signal | |
| 1 | 0 | Lch Input Signal | Lch Input Signal | |
| 1 | 1 | Lch Input Signal | Rch Input Signal | |

Table 76. ADC Mono/Stereo Select (Digital MIC: DMIC bit = "1")

PFSEL bit select the input data of programmable filter.

| PFSEL | Programmable Filter Input | |
|-------|--|-----------|
| 0 | ADC Output (selected by Table 75) | (default) |
| 1 | SDTI Input (selected by Table 83) | |

Table 77. Programmable Filter Input Signal Select

When ADM bit is "1", ALC output data is output to both channels of SDTO and SVOLA as (L+R)/2, respectively.

| ADM bit | Lch | Rch | |
|---------|---------|---------|-----------|
| 0 | L | R | (default) |
| 1 | (L+R)/2 | (L+R)/2 | |

Table 78. ALC Output Mono Mixing

PFSDO bit select the input data both SDTO and SVOLA.

| PFSDO bit | SDTO and SVOLA Input | |
|-----------|--|-----------|
| 0 | ADC Output (selected by Table 75) | |
| 1 | Programmable Filter Output (selected by Table 78) | (default) |

Table 79. SDTO, SVOLA Input Signal Select

SDOL1-0 and SDOR1-0 bits set the data mixing for each channel of SDTO from the data selected by Table 79 and MIX1L/R output data.

| SDOL1 bit | SDOL0 bit | SDTO Lch | (default) |
|-----------|-----------|---|-----------|
| 0 | 0 | Lch Signal selected by Table 79 | |
| 0 | 1 | MIX1L | |
| 1 | 0 | (Lch Signal selected by Table 79) + (MIX1L) | |
| 1 | 1 | (Lch Signal selected by Table 79)/2 + (MIX1L)/2 | |

Table 80. SDTO Lch Output Mixing

| SDOR1 bit | SDOR0 bit | SDTO Rch | (default) |
|-----------|-----------|---|-----------|
| 0 | 0 | Rch Signal selected by Table 79 | |
| 0 | 1 | MIX1R | |
| 1 | 0 | (Rch Signal selected by Table 79) + (MIX1R) | |
| 1 | 1 | (Rch Signal selected by Table 79)/2 + (MIX1R)/2 | |

Table 81. SDTO Rch Output Mixing

When SDOD bit is “1”, SDTO output data can be disabled (fixed to “L”). Input data of SVOLA is not disabled.

| SDOD bit | SDTO | (default) |
|----------|----------------------|-----------|
| 0 | Enable (Output) | |
| 1 | Disable (“L” Output) | |

Table 82. SDTO Disable

SDIM1-0 bits select stereo or mono of SDTI input data. In case of mono mode, the same data is input to both channels.

| SDIM1 bit | SDIM0 bit | Lch | Rch | (default) |
|-----------|-----------|-----|-----|-----------|
| 0 | 0 | L | R | |
| 0 | 1 | L | L | |
| 1 | 0 | R | R | |
| 1 | 1 | N/A | | |

Table 83. SDTI Stereo/Mono Select (N/A: Not available)

PFMXL1-0 and PFMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by Table 83 and SVOLA output data.

| PFMXL1 bit | PFMXL0 bit | 5-band EQ Lch Input | (default) |
|------------|------------|---|-----------|
| 0 | 0 | Lch Signal selected by Table 83 | |
| 0 | 1 | SVOLA Lch | |
| 1 | 0 | (Lch Signal selected by Table 83) + (SVOLA Lch) | |
| 1 | 1 | N/A | |

Table 84. 5-band EQ Lch Input Mixing 1 (N/A: Not available)

| PFM XR1 bit | PFM XR0 bit | 5-band EQ Rch Input | (default) |
|-------------|-------------|---|-----------|
| 0 | 0 | Rch Signal selected by Table 83 | |
| 0 | 1 | SVOLA Rch | |
| 1 | 0 | (Rch Signal selected by Table 83) + (SVOLA Rch) | |
| 1 | 1 | N/A | |

Table 85. 5-band EQ Rch Input Mixing 1 (N/A: Not available)

SRMXL1-0 and SRMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by [Table 84/](#)[Table 85](#) and MIX1L/R output data.

| SRMXL1 bit | SRMXL0 bit | 5-band EQ Lch Input | |
|------------|------------|--|-----------|
| 0 | 0 | Signal selected by Table 84 | (default) |
| 0 | 1 | MIX1L | |
| 1 | 0 | (Signal selected by Table 84) + (MIX1L) | |
| 1 | 1 | N/A | |

Table 86. 5-band EQ Lch Input Mixing 2 (N/A: Not available)

| SRMXR1 bit | SRMXR0 bit | 5-band EQ Rch Input | |
|------------|------------|--|-----------|
| 0 | 0 | Signal selected by Table 85 | (default) |
| 0 | 1 | MIX1R | |
| 1 | 0 | (Signal selected by Table 85) + (MIX1R) | |
| 1 | 1 | N/A | |

Table 87. 5-band EQ Rch Input Mixing 2 (N/A: Not available)

DASEL1-0 bits select the input data of DAC.

| DASEL1 bit | DASEL0 bit | DAC Lch | DAC Rch | |
|------------|------------|------------|------------|-----------|
| 0 | 0 | DATT-A Lch | DATT-A Rch | (default) |
| 0 | 1 | DRC Lch | DRC Rch | |
| 1 | 0 | SDTI Lch | SDTI Rch | |
| 1 | 1 | N/A | | |

Table 88. DAC Input Signal Select (N/A: Not available)

MX1L2-0 bits set the data mixing for Audio I/F Lch input.

| MX1L2 bit | MX1L1 bit | MX1L0 bit | Audio I/F Lch Input | |
|-----------|-----------|-----------|--|-----------|
| 0 | 0 | 0 | DATT-B | (default) |
| 0 | 0 | 1 | BIVOL Lch | |
| 0 | 1 | 0 | BIVOL Rch | |
| 0 | 1 | 1 | $((\text{BIVOL Lch}) + (\text{BIVOL Rch}))/2$ | |
| 1 | 0 | 0 | $(\text{DATT-B}) + (\text{BIVOL Lch})$ | |
| 1 | 0 | 1 | $(\text{DATT-B}) + (\text{BIVOL Rch})$ | |
| 1 | 1 | 0 | $((\text{BIVOL Lch}) + (\text{BIVOL Rch}))/2 + (\text{DATT-B}))/2$ | |
| 1 | 1 | 1 | N/A | |

Table 89. Audio I/F Lch Input Mixing (N/A: Not available)

MX1R2-0 bits set the data mixing for Audio I/F Rch input.

| MX1R2 bit | MX1R1 bit | MX1R0 bit | Audio I/F Rch Input | |
|-----------|-----------|-----------|--|-----------|
| 0 | 0 | 0 | DATT-B | (default) |
| 0 | 0 | 1 | BIVOL Lch | |
| 0 | 1 | 0 | BIVOL Rch | |
| 0 | 1 | 1 | $((\text{BIVOL Lch}) + (\text{BIVOL Rch}))/2$ | |
| 1 | 0 | 0 | $(\text{DATT-B}) + (\text{BIVOL Lch})$ | |
| 1 | 0 | 1 | $(\text{DATT-B}) + (\text{BIVOL Rch})$ | |
| 1 | 1 | 0 | $((\text{BIVOL Lch}) + (\text{BIVOL Rch}))/2 + (\text{DATT-B}))/2$ | |
| 1 | 1 | 1 | N/A | |

Table 90. Audio I/F Rch Input Mixing (N/A: Not available)

MX2A1-0 bits set the data mixing for MIX2C input.

| MX2A1 bit | MX2A0 bit | MIX2C Input | (default) |
|-----------|-----------|---|-----------|
| 0 | 0 | BIVOL Lch | |
| 0 | 1 | BIVOL Rch | |
| 1 | 0 | $(\text{BIVOL Lch}) + (\text{BIVOL Rch})$ | |
| 1 | 1 | $((\text{BIVOL Lch}) + (\text{BIVOL Rch}))/2$ | |

Table 91. MIX2C Input Mixing 1

MX2B1-0 bits set the data mixing for MIX2C input.

| MX2B1 bit | MX2B0 bit | MIX2C Input | (default) |
|-----------|-----------|---|-----------|
| 0 | 0 | DATT-A Lch | |
| 0 | 1 | DATT-A Rch | |
| 1 | 0 | $(\text{DATT-A Lch}) + (\text{DATT-A Rch})$ | |
| 1 | 1 | $((\text{DATT-A Lch}) + (\text{DATT-A Rch}))/2$ | |

Table 92. MIX2C Input Mixing 2

MX2C1-0 bits set the data mixing for SRCAO and SVOLB input.

| MX2C1 bit | MX2C0 bit | SRCAO/SVOLB Input | (default) |
|-----------|-----------|---------------------------------------|-----------|
| 0 | 0 | MIX2A | |
| 0 | 1 | MIX2B | |
| 1 | 0 | $(\text{MIX2A}) + (\text{MIX2B})$ | |
| 1 | 1 | $((\text{MIX2A}) + (\text{MIX2B}))/2$ | |

Table 93. SRCAO/SVOLB Input Mixing

MXSB2-0 bits set the data mixing for SRCBO input.

| MXSB2 bit | MXSB1 bit | MXSB0 bit | SRCBO Lch | SRCBO Rch | (default) |
|-----------|-----------|-----------|---|---|-----------|
| 0 | 0 | 0 | DATT-A Lch | DATT-A Rch | |
| 0 | 0 | 1 | DATT-A Lch | ← | |
| 0 | 1 | 0 | DATT-A Rch | ← | |
| 0 | 1 | 1 | $(\text{DATT-A Lch}) + (\text{DATT-A Rch})$ | ← | |
| 1 | 0 | 0 | $((\text{DATT-A Lch}) + (\text{DATT-A Rch}))/2$ | ← | |
| 1 | 0 | 1 | $((\text{DATT-A Lch}) + (\text{DATT-A Rch}))/2 + (\text{DATT-C})$ | ← | |
| 1 | 1 | 0 | Lch Signal selected by Table 79 | Rch Signal selected by Table 79 | |
| 1 | 1 | 1 | DATT-C | ← | |

Table 94. SRCBO Input Mixing

When SDOAD bit is “1”, SDTOA output data can be disabled (fixed to “L”). Input data of SVOLB is not disabled.

| SDOAD bit | SDTOA | (default) |
|-----------|----------------------|-----------|
| 0 | Enable (Output) | |
| 1 | Disable (“L” Output) | |

Table 95. SDTOA Disable

SBMX1-0 bits set the data mixing from SDTIA input and SVOLB output. The mixed data is input to DATT-C.

| SBMX1 bit | SBMX0 bit | DATT-C Input |
|-----------|-----------|-------------------|
| 0 | 0 | SRCAI |
| 0 | 1 | SVOLB |
| 1 | 0 | (SRCAI) + (SVOLB) |
| 1 | 1 | N/A |

(default)

Table 96. SDTOB Mixing (N/A: Not available)

When SDOBD bit is “1”, SDTOB output data can be disabled (fixed to “L”).

| SDOBD bit | SDTOB |
|-----------|----------------------|
| 0 | Enable (Output) |
| 1 | Disable (“L” Output) |

(default)

Table 97. SDTOB Disable

■ Stereo Line Output (LOUT/ROUT pins)

When DACL and DACR bits are “1”, Lch/Rch signal of DAC is output from the LOUT/ROUT pins in single-ended. When DACL and DACR bits are “0” in normal operation (PMDAC=PML/RO bits = “1”, LOPS bit = “0”), output signal is muted and LOUT/ROUT pins output common voltage (typ. 0.8 x AVDD). The load impedance is 10kΩ (min.). When the PMLO=PMRO=LOPS bits = “0”, LOUT/ROUT enters power-down mode and the output is pulled-down to VSS1 by 100kΩ (typ). When the LOPS bit is “1”, LOUT/ROUT enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO and PMRO bits at LOPS bit = “1”. In this case, output signal line should be pulled-down to VSS1 by 20kΩ after AC coupled as Figure 78. Rise/Fall time is 300ms (max) at C=1μF and AVDD=1.8V. When PMLO=PMRO bits = “1” and LOPS bit = “0”, LOUT/ROUT is in normal operation. LVL2-0 bits control the volume of LOUT/ROUT. When LOM bit = “1”, DAC output signal is output to LOUT and ROUT pins as (L+R) mono signal.

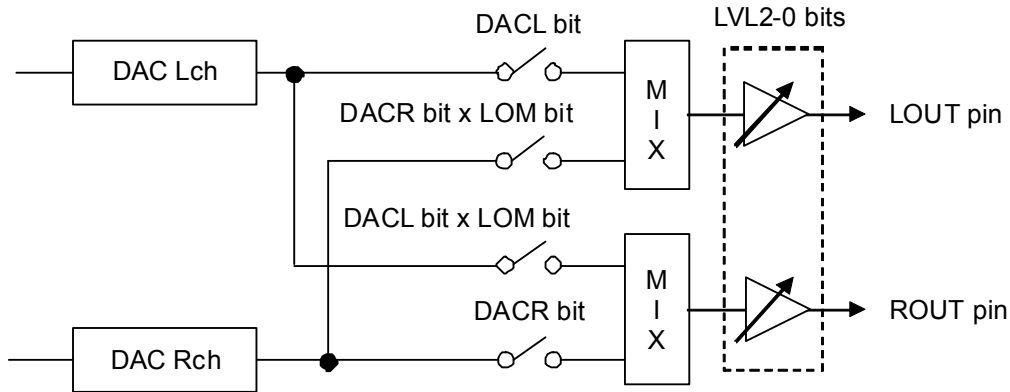


Figure 77. Stereo Line Output

| LOPS bit | PMLO bit | Mode | LOUT pin |
|----------|----------|------------------|---------------------------|
| 0 | 0 | Power-down | Pull-down to VSS1 |
| | 1 | Normal Operation | Normal Operation |
| 1 | 0 | Power-save | Fall down to VSS1 |
| | 1 | Power-save | Rise up to common voltage |

Table 98. Stereo Line Output Mode Select (LOUT)

| LOPS bit | PMRO bit | Mode | ROUT pin |
|----------|----------|------------------|---------------------------|
| 0 | 0 | Power-down | Pull-down to VSS1 |
| | 1 | Normal Operation | Normal Operation |
| 1 | 0 | Power-save | Fall down to VSS1 |
| | 1 | Power-save | Rise up to common voltage |

Table 99. Stereo Line Output Mode Select (ROUT)

| LVL2-0 bits | Attenuation |
|-------------|-------------|
| 7H | N/A |
| 6H | N/A |
| 5H | +6dB |
| 4H | +3dB |
| 3H | 0dB |
| 2H | -3dB |
| 1H | -6dB |
| 0H | -9dB |

Table 100. Stereo Line Output Volume Setting (N/A: Not available)

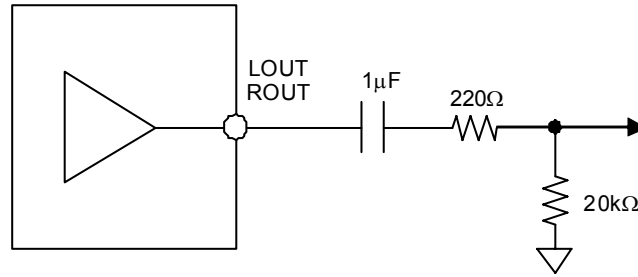


Figure 78. External Circuit for Stereo Line Output (in case of using Pop Noise Reduction Circuit)

<Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

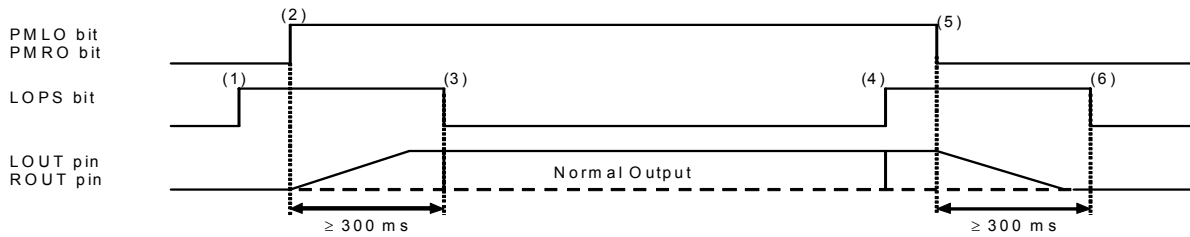


Figure 79. Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)

- (1) Set LOPS bit = "1". Stereo line output enters power-save mode.
- (2) Set PMLO=PMRO bits = "1". Stereo line output enters power-down mode.
LOUT and ROUT pins rise up to common voltage (typ. $0.8 \times AVDD$). Rise time is 200ms (max 300ms) at $C=1\mu F$ and $AVDD=1.8V$.
- (3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits power-save mode.
Stereo line output is enabled.
- (4) Set LOPS bit = "1". Stereo line output enters power-save mode.
- (5) Set PMLO=PMRO bits = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to VSS1. Fall time is 200ms (max 300ms) at $C=1\mu F$ and $AVDD=1.8V$.
- (6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits power-save mode.

■ Full-differential Mono Line Output (LOP/LON pins)

When LODIF bit = “1”, LOUT/ROUT pins become LOP/LON pins, respectively. Lch/Rch signal of DAC or LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the LOP/LON pins in full-differential as (L+R) signal. The load impedance is 10kΩ (min) for each LOP pin and LON pin. When the PMLO = PMRO bits = “0”, the mono line output enters power-down mode and the output is pulled-down to VSS1. When the PMLO = PMRO bits = “1” and LOPS bit = “1”, mono line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO and PMRO bits when LOPS bit = “1”. When PMLO = PMRO bits = “1” and LOPS bit = “0”, mono line output enters in normal operation. LVL2-0 bits set the volume of mono line output.

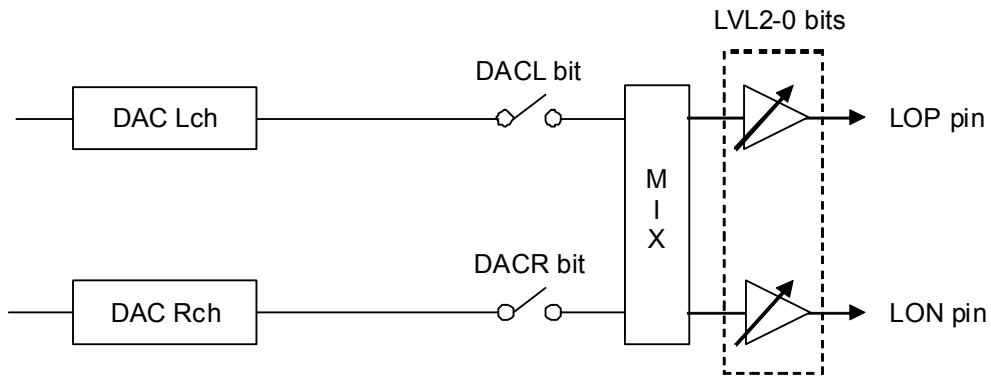


Figure 80. Full-differential Mono Line Output

| LVL2-0 bits | Attenuation |
|-------------|-------------|
| 7H | N/A |
| 6H | N/A |
| 5H | +12dB |
| 4H | +9dB |
| 3H | +6dB |
| 2H | +3dB |
| 1H | 0dB |
| 0H | -3dB |

(default)

Table 101. Mono Line Output Gain Setting (N/A: Not available)

| LOPS bit | PMLO/RO bits | Mode | LON/LOP pins |
|----------|--------------|------------------|---------------------------|
| 0 | 0 | Power-down | Pull-down to VSS1 |
| | 1 | Normal Operation | Normal Operation |
| 1 | 0 | Power-save | Fall down to VSS1 |
| | 1 | Power-save | Rise up to common voltage |

(default)

Table 102. Mono Line Output Mode Setting

<Full-differential Mono Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

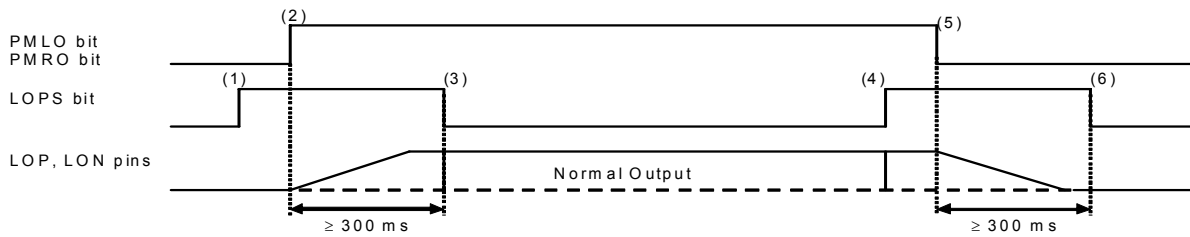


Figure 81. Mono Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)

- (1) Set LOPS bit = "1". Mono line output enters power-save mode.
- (2) Set PMLO = PMRO bits = "1". Mono line output exits power-down mode.
LOP and LON pins rise up to common voltage (typ. $0.8 \times AVDD$). Rise time is 200ms (max 300ms) at $C=1\mu F$ and $AVDD=1.8V$.
- (3) Set LOPS3 bit = "0" after LOP and LON pins rise up. Mono line output exits power-save mode.
Mono line output is enabled.
- (4) Set LOPS bit = "1". Mono line output enters power-save mode.
- (5) Set PMLO = PMRO bits = "0". Mono line output enters power-down mode.
LOP and LON pins fall down to VSS1. Fall time is 200ms (max 300ms) at $C=1\mu F$ and $AVDD=1.8V$.
- (6) Set LOPS bit = "0" after LOP and LON pins fall down. Mono line output exits power-save mode.

■ Receiver-Amp (RCP/RCN pins)

Lch/Rch signal of DAC is output from the RCP/RCN pins which is BTL as (L+R) signal. The load impedance is 32Ω (min). When the PMRCV bit = “0”, the mono receiver output enters power-down mode and the output is Hi-Z. When the PMRCV bit = “1” and RCVPS bit = “1”, mono receiver output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMRCV bit when RCVPS bit = “1”. When PMRCV bit = “1” and RCVPS bit = “0”, mono receiver output enters in normal operation. RCVG3-0 bits control the volume of mono receiver output.

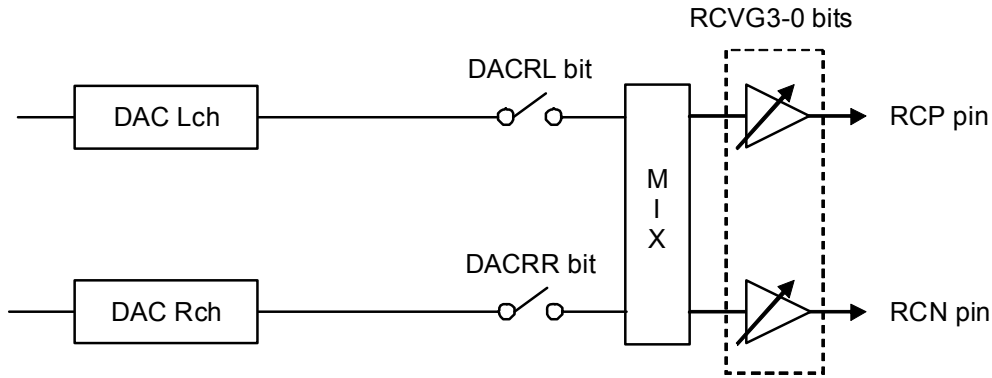


Figure 82. Mono Receiver Output

| RCVG3-0 bits | Attenuation |
|--------------|-------------|
| FH | +12dB |
| EH | +9dB |
| DH | +6dB |
| CH | +3dB |
| BH | 0dB |
| AH | -3dB |
| 9H | -6dB |
| 8H | -9dB |
| 7H | -12dB |
| 6H | -15dB |
| 5H | -18dB |
| 4H | -21dB |
| 3H | -24dB |
| 2H | -27dB |
| 1H | -30dB |
| 0H | MUTE |

(default)

Table 103. Mono Receiver Output Volume Setting

| PMRCV bit | RCVPS bit | Mode | RCP pin | RCN pin |
|-----------|-----------|------------------|------------------|----------------------------------|
| 0 | x | Power-down | Hi-Z | Hi-Z |
| 1 | 1 | Power-save | Hi-Z | Common Voltage (typ. 0.8 x AVDD) |
| | 0 | Normal Operation | Normal Operation | Normal Operation |

(default)

Table 104. Receiver-Amp Mode Setting (x: Don't care)

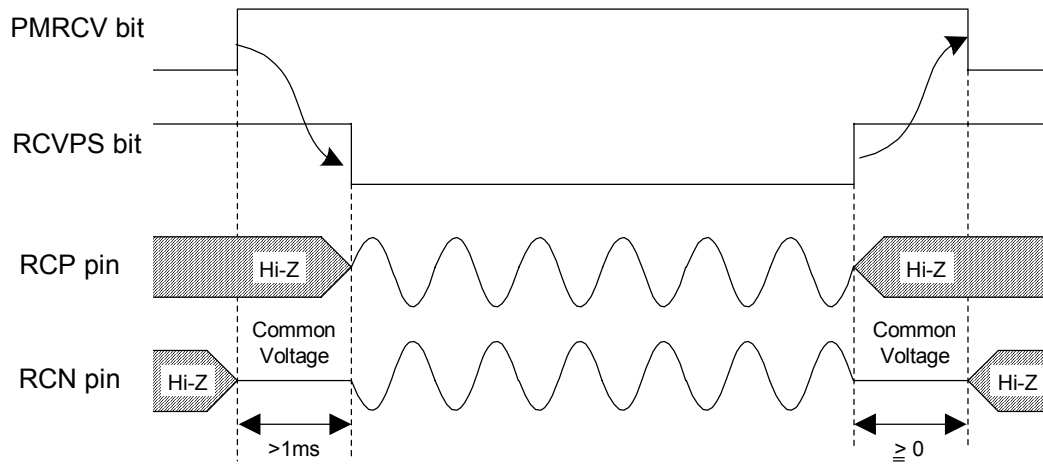


Figure 83. Power-up/Power-down Timing for Receiver-Amp

■ Headphone Output (HPL/HPR pins)

The headphone amplifiers are operated by positive and negative power supplied from charge pump circuit. The VEE pin outputs the negative voltage generated by the internal charge pump circuit from PVDD. This charge pump circuit is switched between VDD mode and 1/2VDD mode by the output level of the headphone amplifiers.

The headphone amplifier output is single-ended and centered on 0V (VSS1). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. The output power is 20mW (@ 0dBFS, $R_L = 16\Omega$, AVDD=1.8V, HPG = -4dB) and 25mW (@ 0dBFS, $R_L = 32\Omega$, AVDD=1.8V, HPG=0dB).

The output level of headphone-amp can be controlled by HPG5-0 bits. This volume setting is in common for L/R channels and can attenuate/gain the mixer output from +6dB to -62dB in 2dB steps (Table 105). The HPG value is changed independently on L/R channels by zero crossing or timeout. Zero crossing timeout period is set by HPTM1-0 bits. When LOHM bit = “1”, the headphone-amp output to HPL and HPR pins as (L+R) mono signal.

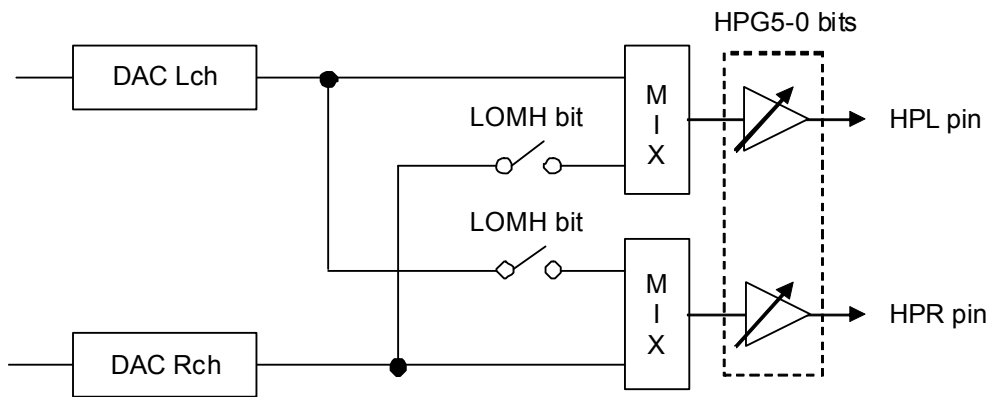


Figure 84. Stereo Headphone Output

| HPG5-0 bits | GAIN (dB) | HPG5-0 bits | GAIN (dB) |
|-------------|-----------|-------------|-----------|
| 29H | N/A | 14H | -30 |
| 28H | N/A | 13H | -32 |
| 27H | N/A | 12H | -34 |
| 26H | +6 | 11H | -36 |
| 25H | +4 | 10H | -38 |
| 24H | +2 | 0FH | -40 |
| 23H | 0 | 0EH | -42 |
| 22H | -2 | 0DH | -44 |
| 21H | -4 | 0CH | -46 |
| 20H | -6 | 0BH | -48 |
| 1FH | -8 | 0AH | -50 |
| 1EH | -10 | 09H | -52 |
| 1DH | -12 | 08H | -54 |
| 1CH | -14 | 07H | -56 |
| 1BH | -16 | 06H | -58 |
| 1AH | -18 | 05H | -60 |
| 19H | -20 | 04H | -62 |
| 18H | -22 | 03H | MUTE |
| 17H | -24 | 02H | MUTE |
| 16H | -26 | 01H | MUTE |
| 15H | -28 | 00H | MUTE |

Table 105. Headphone-Amp Volume Setting (Default: 0dB, N/A: Not available)

| HPTM1 bit | HPTM0 bit | Zero Crossing Timeout Period | | | | (default) |
|--------------|--------------|------------------------------|-------|-------|---------|-----------|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 106. Headphone-Amp Volume Zero Crossing Timeout Period

| CPMODE1 bit | CPMODE0 bit | Mode | Operation Voltage | (default) |
|-------------|-------------|------------------------------|---------------------|-----------|
| 0 | 0 | Class-G Operation Mode | Automatic Switching | |
| 0 | 1 | \pm VDD Operation Mode | \pm VDD | |
| 1 | 0 | $\pm 1/2$ VDD Operation Mode | $\pm 1/2$ VDD | |
| 1 | 1 | N/A | | |

Table 107. Charge Pump Mode Setting (N/A: Not available)

| VDDTM2 bit | VDDTM1 bit | VDDTM0 bit | VDD Mode Holding Period | | | | (default) |
|---------------|---------------|---------------|-------------------------|--------|--------|---------|-----------|
| | | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 0 | 1024/fs | 128ms | 64ms | 23.2ms | |
| 0 | 0 | 1 | 2048/fs | 256ms | 128ms | 46.4ms | |
| 0 | 1 | 0 | 4096/fs | 512ms | 256ms | 92.9ms | |
| 0 | 1 | 1 | 8192/fs | 1024ms | 512ms | 186ms | |
| 1 | 0 | 0 | 16384/fs | 2048ms | 1024ms | 372ms | |
| 1 | 0 | 1 | 32768/fs | 4096ms | 2048ms | 743ms | |
| 1 | 1 | 0 | 65536/fs | 8192ms | 4096ms | 1486ms | |
| 1 | 1 | 1 | N/A | | | | |

Table 108. VDD Mode Waiting Period (N/A: Not available)

<HP-Amp External Circuit>

It is necessary to put an oscillation prevention circuit (0.22μF±20% capacitor and 15Ω±20% resistor) because it has the possibility that Headphone-Amp oscillates.

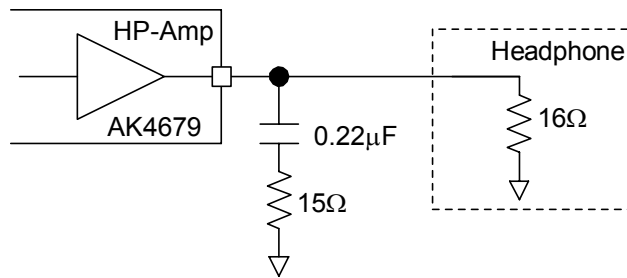


Figure 85. HP-Amp oscillation prevention circuit example

When PMHPL or PMHPR bit = “1”, headphone outputs are in normal operation after the charge pump circuit is powered up. When PMHPL and PMHPR bits = “0”, the headphone-amps and the charge pump circuit are powered-down completely. At that time, the HPL and HPR pins go to VSS1 voltage via the internal pulled-down resistor. The pulled-down resistor is 120Ω (typ).

The power-up time of HP-Amp block is 28ms and then HPL and HPR pins output 0V (VSS1). The power-down is executed immediately.

| PMVCM bit | PMHPL/R bits | Mode | HPL/R pins |
|-----------|--------------|-------------------|-------------------------|
| x | 0 | Power-down & Mute | Pull-down by 120Ω (typ) |
| 1 | 1 | Normal Operation | Normal Operation |

(default)

Table 109. Headphone-Amp Mode Setting (x: Don't care)

■ Speaker Output (SPP/SPN pins)

Lch/Rch signal of DAC is converted by PWM and is output from SPP/SPN pins by BTL. When Lch/Rch signal of DAC is 0dBFS, the speaker amplifier outputs 0.89W (@ 8Ω, AVDD=1.8V, SVDD=4.2V, SPKG=-6dB). The load impedance is 8Ω (min). A 2.2nF capacitor should be connected between SPFIL pin and VSS1 pin to reduce out-of-band noise from DAC. SPKG3-0 bits control the volume of SPP/SPN.

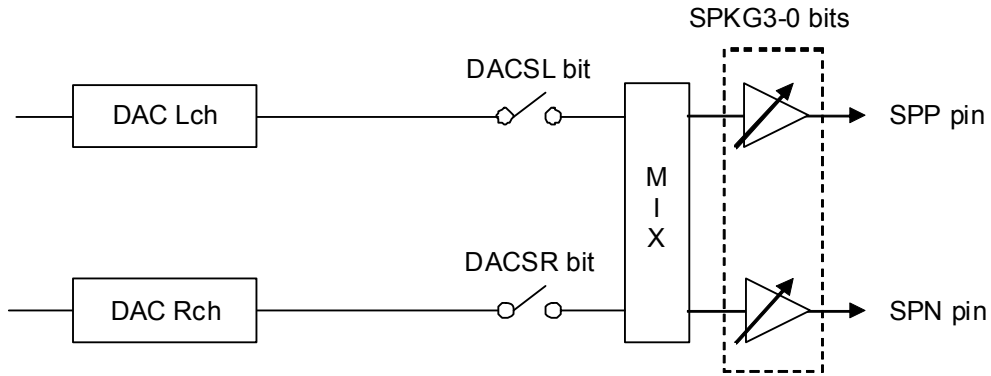


Figure 86. Mono Speaker Output

| SPKG3-0 bits | Attenuation |
|--------------|---------------|
| FH | +12dB |
| EH | +9dB |
| DH | +6dB |
| CH | +3dB |
| BH | 0dB (default) |
| AH | -3dB |
| 9H | -6dB |
| 8H | -9dB |
| 7H | -12dB |
| 6H | -15dB |
| 5H | -18dB |
| 4H | -21dB |
| 3H | -24dB |
| 2H | -27dB |
| 1H | -30dB |
| 0H | MUTE |

Table 110. Speaker Output Volume Setting

| PMSPK bit | Speaker-Amp |
|-----------|-----------------------------|
| 0 | Power-down & Hi-Z (default) |
| 1 | Power-up & Output |

Table 111. Speaker-Amp output state

When PMSPK bit is “1”, the speaker-amp is powered-up. The power-up time of SPK-Amp block is 32ms and then SPP and SPN pins output 0V (VSS3). When PMSPK bit is “0”, the SPK-Amp block can be powered-down. The clock supplied to SPK-Amp block must not be stopped for more than 0.5ms. Once SPK-Amp block is powered-down, the SPK-Amp block should be powered-up again with an interval of 0.5ms or more.

■ Thermal Shutdown Function

When PMVCM bit is “1” and the internal device temperature rises up irregularly (E.g. Output pins of speaker amplifier are shortened.), all amplifier blocks are automatically powered-down (PMLO, PMRO, PMRCV, PMHPL, PMHPR and PMSPK bits = “0”) and then THDET bit becomes “1”. The other control registers are not initialized. When the internal device temperature falls down, THDET bit becomes “0”, but the amplifier blocks do not return to normal operation unless the amplifier blocks are powered-up (PMLO, PMRO, PMRCV, PMHPL, PMHPR or PMSPK bits = “1”). The device status can be monitored by THDET bit.

■ System Clock (PCM I/F)

The AK4679 has two PCM I/F ports. PCM I/F A is for baseband module and PCM I/F B is for Bluetooth mode. PCM I/F A, PCM I/F B and Audio I/F can be operated by asynchronous clock because the AK4679 has four SRCs. PCM I/F A and PCM I/F B support slave mode only. The required clock PCM I/F is BICKA (BICKB) and SYNCA (SYNCB). When PMPCMA bit is “1”, PCM I/F A port is powered-up. When PMPCMB bit is “1”, PCM I/F B port is powered-up.

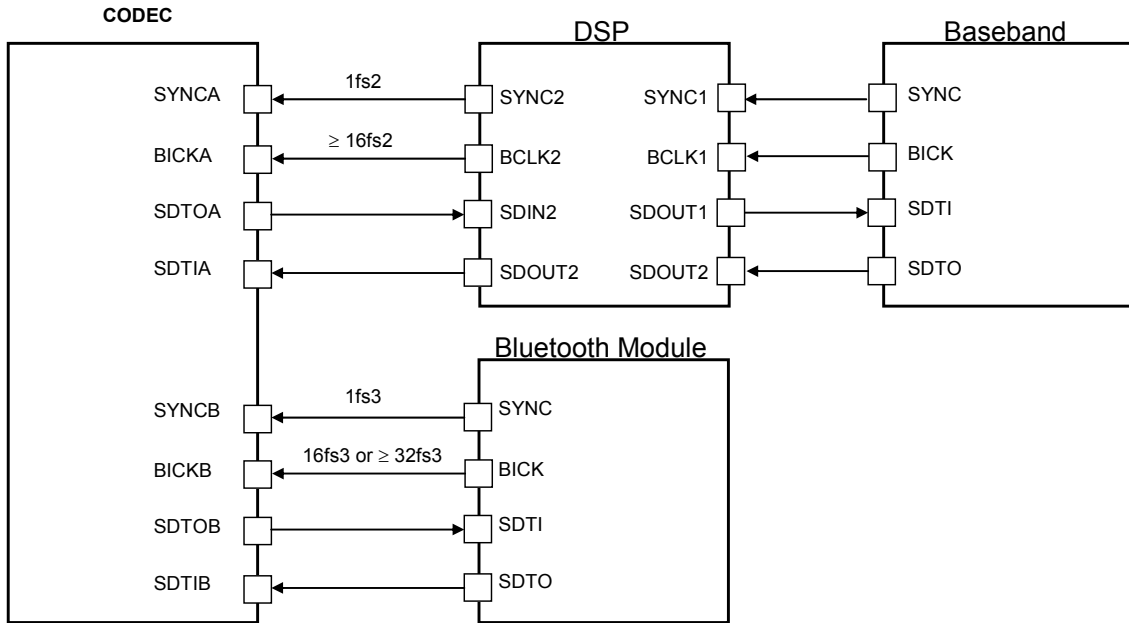


Figure 87. PCM I/F A and B

■ SRC (Sample Rate Converter)

The AK4679 has four asynchronous SRCs. The SRCs are operated by internal oscillator. When PMSRAI, PMSRAO, PMSRBI or PMSRBO bit is “1” and PMOSC bit is “1”, SRC starts operation. Initial time of SRC is 164/fs2(164/fs3) for SDTOA(SDTOB) output enable after power-down state is released by a clock input(SYNC clock). Until then, SDTOA and SDTOB output data as shown in Table 112. Ratio of Input / Output is decided by PMMIX bit.

| Mode | PMSRx bit = “0” | After PMSRx bit = “0” → “1” & Before SYNCA/SYNCB Input | PMSRx bit = “1” During initial time |
|--------------|-----------------|--|-------------------------------------|
| 16bit Linear | L | L | 0000H |
| 8bit A-Law | L | H | 11010101b |
| 8bit μ-Law | L | H | 11111111b |

Table 112. SDTOA and SDTOB pins Output Data (PMSRx: PMSRAI, PMSRAO, PMSRBI, PMSRBO)

| PMMIX bit | SRC | Input Sampling Rate (FSI) | Output Sampling Rate (FSO) |
|-----------|-------|---------------------------|----------------------------|
| 0 | SRCAI | SYNCA | SYNCB |
| | SRCAO | SYNCB | SYNCA |
| 1 | SRCAI | SYNCA | LRCK |
| | SRCAO | LRCK | SYNCA |
| | SRCBI | SYNCB | LRCK |
| | SRCBO | LRCK | SYNCB |

Table 113. PCM I/F Input Output rate

■ PCM I/F A & B Format

AK4679 supports dual PCM I/F (PCM I/F A & PCM I/F B) that supports 3 kind of I/F (16bit Linear, 8bit A-Law and 8bit μ -Law) independently (Table 114 and Table 115).

| Mode | LAWA1 bit | LAWA0 bit | Format |
|------|-----------|-----------|-----------------|
| 0 | 0 | 0 | 16bit Linear |
| 1 | 0 | 1 | N/A |
| 2 | 1 | 0 | 8bit A-Law |
| 3 | 1 | 1 | 8bit μ -Law |

(default)

Table 114. PCM I/F A Mode (N/A: Not available)

| Mode | LAWB1 bit | LAWB0 bit | Format |
|------|-----------|-----------|-----------------|
| 0 | 0 | 0 | 16bit Linear |
| 1 | 0 | 1 | N/A |
| 2 | 1 | 0 | 8bit A-Law |
| 3 | 1 | 1 | 8bit μ -Law |

(default)

Table 115. PCM I/F B Mode (N/A: Not available)

Four types of data formats are available and are selected by setting the FMTA1-0 and FMTB1-0 bits independently (Table 116 and Table 117). In 16bit Linear mode, the serial data is MSB first, 2's complement format. In 8bit A-Law and μ -Law Mode, the serial data is MSB first. PCM I/F formats support slave mode only. SYNCA/B and BICKA/B are input to the AK4679.

| Mode | FMTA1 bit | FMTA0 bit | Format | BICKA | Figure |
|------|-----------|-----------|------------------|--------------|------------|
| 0 | 0 | 0 | Short Frame Sync | $\geq 16fs2$ | Table 118 |
| 1 | 0 | 1 | Long Frame Sync | $\geq 16fs2$ | Table 120 |
| 2 | 1 | 0 | MSB justified | $\geq 32fs2$ | Figure 104 |
| 3 | 1 | 1 | I ² S | $\geq 32fs2$ | Figure 106 |

(default)

Table 116. PCM I/F A Format

| Mode | FMTB1 bit | FMTB0 bit | Format | BICKB | Figure |
|------|-----------|-----------|------------------|-----------------------|------------|
| 0 | 0 | 0 | Short Frame Sync | 16fs3 or $\geq 32fs3$ | Table 119 |
| 1 | 0 | 1 | Long Frame Sync | 16fs3 or $\geq 32fs3$ | Table 121 |
| 2 | 1 | 0 | MSB justified | $\geq 32fs3$ | Figure 105 |
| 3 | 1 | 1 | I ² S | $\geq 32fs3$ | Figure 107 |

(default)

Table 117. PCM I/F B Format

In modes 2 and 3, the SDTOA/B is clocked out on the falling edge (“ \downarrow ”) of BICKA/B and the SDTIA/B is latched on the rising edge (“ \uparrow ”).

In Modes 0 and 1, PCM I/F A timing is changed by BCKPA and MSBSA bits, and PCM I/F B timing is changed by BCKPB and MSBSB bits.

When BCKPA bit = “0”, the SDTOA is clocked out on the rising edge (“ \uparrow ”) of BICKA and the SDTIA is latched on the falling edge (“ \downarrow ”). When BCKPA bit = “1”, the SDTOA is clocked out on the falling edge (“ \downarrow ”) of BICKA and the SDTIA is latched on the rising edge (“ \uparrow ”).

MSBSA bit can shift the MSB position of SDTOA and SDTIA by half period of BICKA.

When BCKPB bit = “0”, the SDTOB is clocked out on the rising edge (“ \uparrow ”) of BICKB and the SDTIB is latched on the falling edge (“ \downarrow ”). When BCKPB bit = “1”, the SDTOB is clocked out on the falling edge (“ \downarrow ”) of BICKB and the SDTIB is latched on the rising edge (“ \uparrow ”).

MSBSB bit can shift the MSB position of SDTOB and SDTIB by half period of BICKB.

| MSBSA bit | BCKPA bit | Data Interface Format | Figure |
|-----------|-----------|---|-----------|
| 0 | 0 | MSB of SDTOA is output by next rising edge (“↑”) of the falling edge (“↓”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 88 |
| 0 | 1 | MSB of SDTOA is output by next falling edge (“↓”) of the rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 89 |
| 1 | 0 | MSB of SDTOA is output by the 2nd rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 90 |
| 1 | 1 | MSB of SDTOA is output by the 2nd falling edge (“↓”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 91 |

Table 118. PCM I/F A Format in Mode 0

| MSBSB bit | BCKPB bit | Data Interface Format | Figure |
|-----------|-----------|---|-----------|
| 0 | 0 | MSB of SDTOB is output by next rising edge (“↑”) of the falling edge (“↓”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 96 |
| 0 | 1 | MSB of SDTOB is output by next falling edge (“↓”) of the rising edge (“↑”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 97 |
| 1 | 0 | MSB of SDTOB is output by the 2nd rising edge (“↑”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 98 |
| 1 | 1 | MSB of SDTOB is output by the 2nd falling edge (“↓”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 99 |

Table 119. PCM I/F B Format in Mode 0

| MSBSA bit | BCKPA bit | Data Interface Format | Figure |
|-----------|-----------|--|-----------|
| 0 | 0 | MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 92 |
| 0 | 1 | MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 93 |
| 1 | 0 | MSB of SDTOA is output by the rising edge (“↑”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 94 |
| 1 | 1 | MSB of SDTOA is output by the falling edge (“↓”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB. | Figure 95 |

Table 120. PCM I/F A Format in Mode 1

| MSBSB bit | BCKPB bit | Data Interface Format | Figure |
|-----------|-----------|--|------------|
| 0 | 0 | MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 100 |
| 0 | 1 | MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 101 |
| 1 | 0 | MSB of SDTOB is output by the rising edge (“↑”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 102 |
| 1 | 1 | MSB of SDTOB is output by the falling edge (“↓”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB. | Figure 103 |

Table 121. PCM I/F B Format in Mode 1

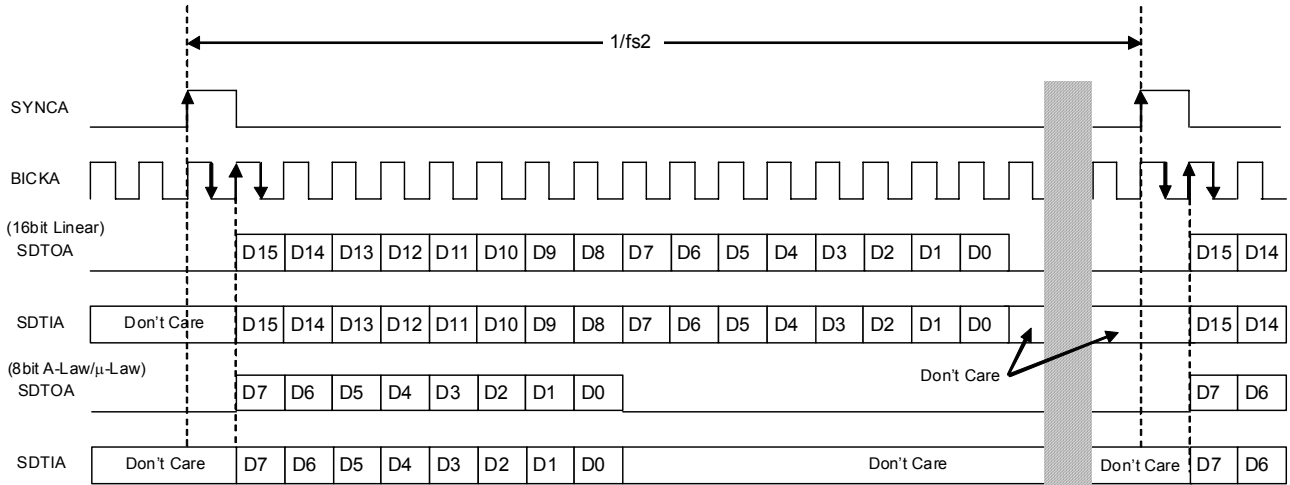


Figure 88. Timing of Short Frame Sync (PCM I/F A: MSBSA bit = "0", BCKPA bit = "0")

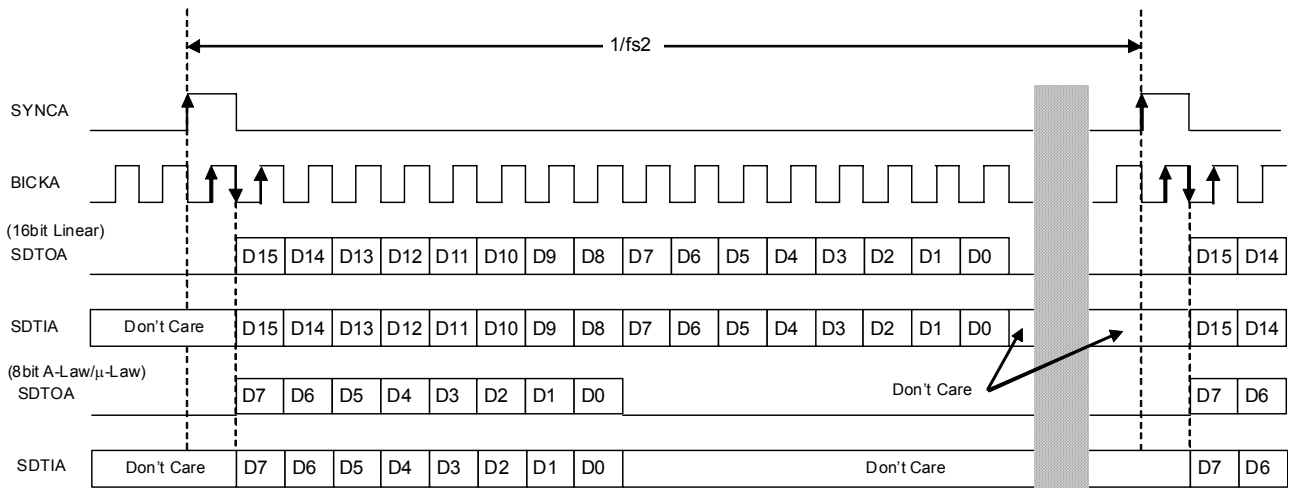


Figure 89. Timing of Short Frame Sync (PCM I/F A: MSBSA bit = "0", BCKPA bit = "1")

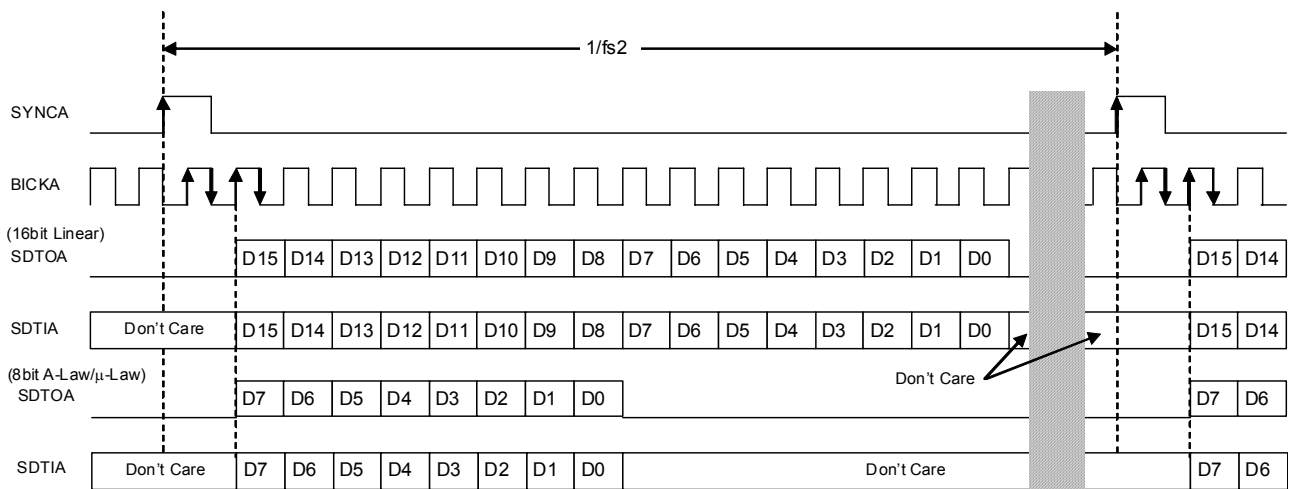


Figure 90. Timing of Short Frame Sync (PCM I/F A: MSBSA bit = "1", BCKPA bit = "0")

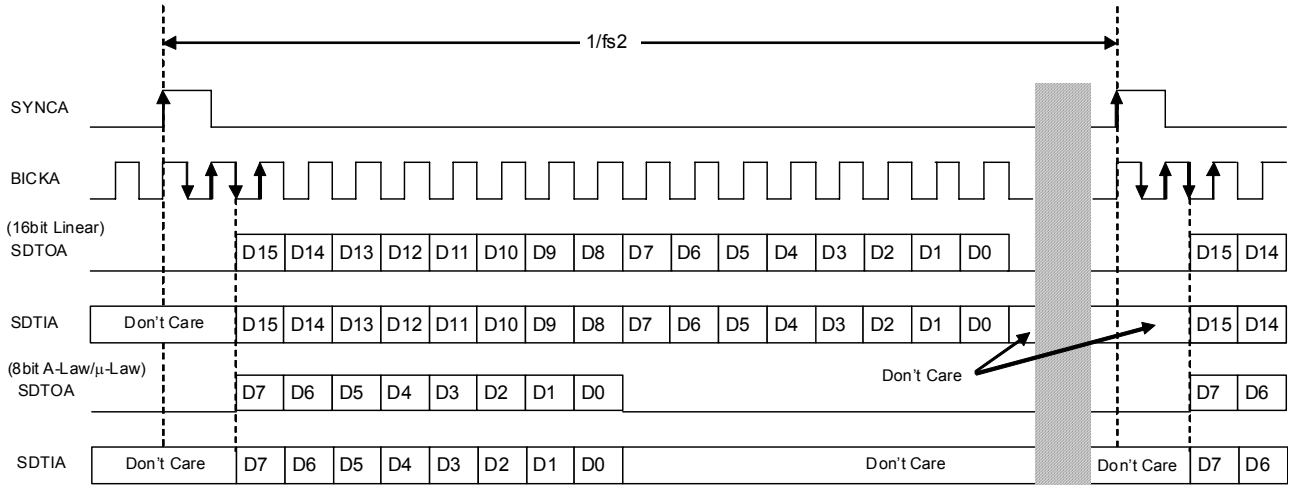


Figure 91. Timing of Short Frame Sync (PCM I/F A: MSBSA bit = "1", BCKPA bit = "1")

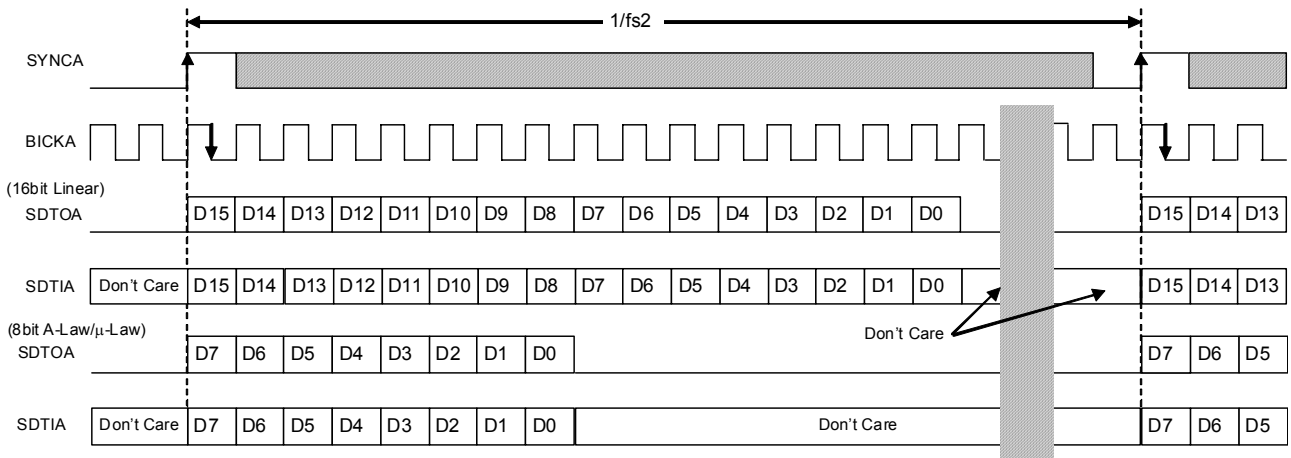


Figure 92. Timing of Long Frame Sync (PCM I/F A: MSBSA bit = "0", BCKPA bit = "0")

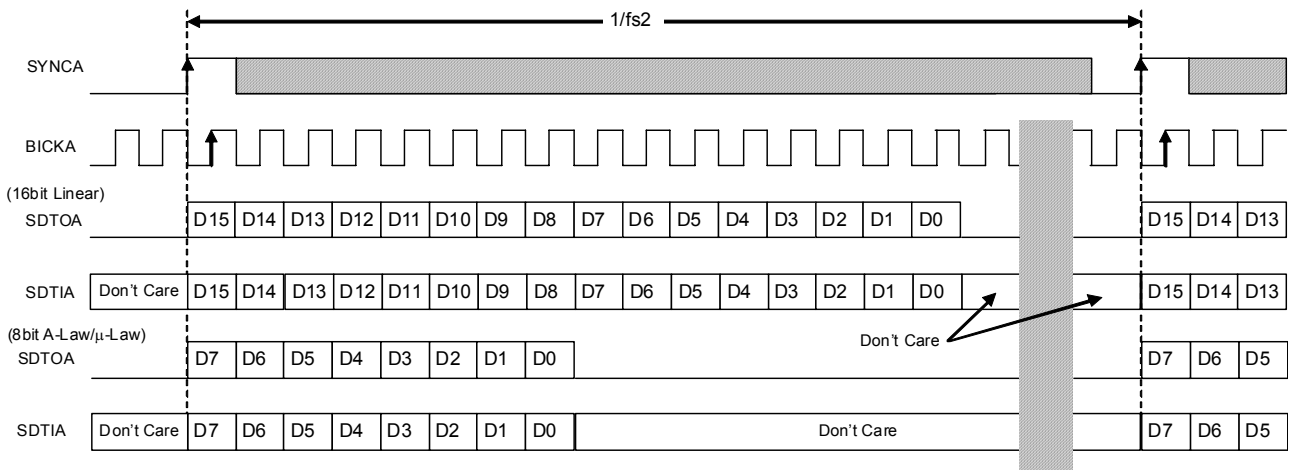


Figure 93. Timing of Long Frame Sync (PCM I/F A: MSBSA bit = "0", BCKPA bit = "1")

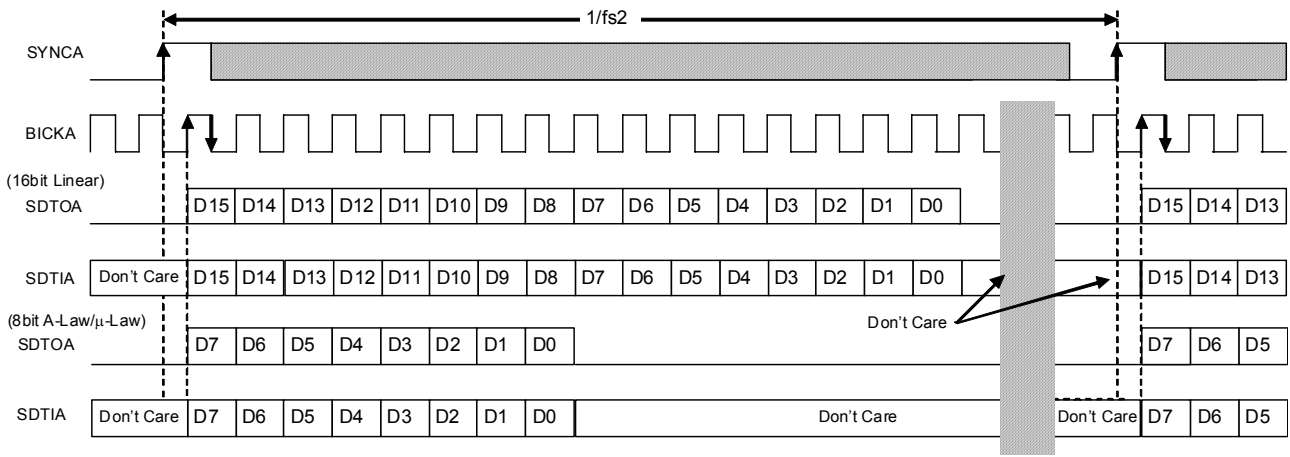


Figure 94. Timing of Long Frame Sync (PCM I/F A: MSBSA bit = "1", BCKPA bit = "0")

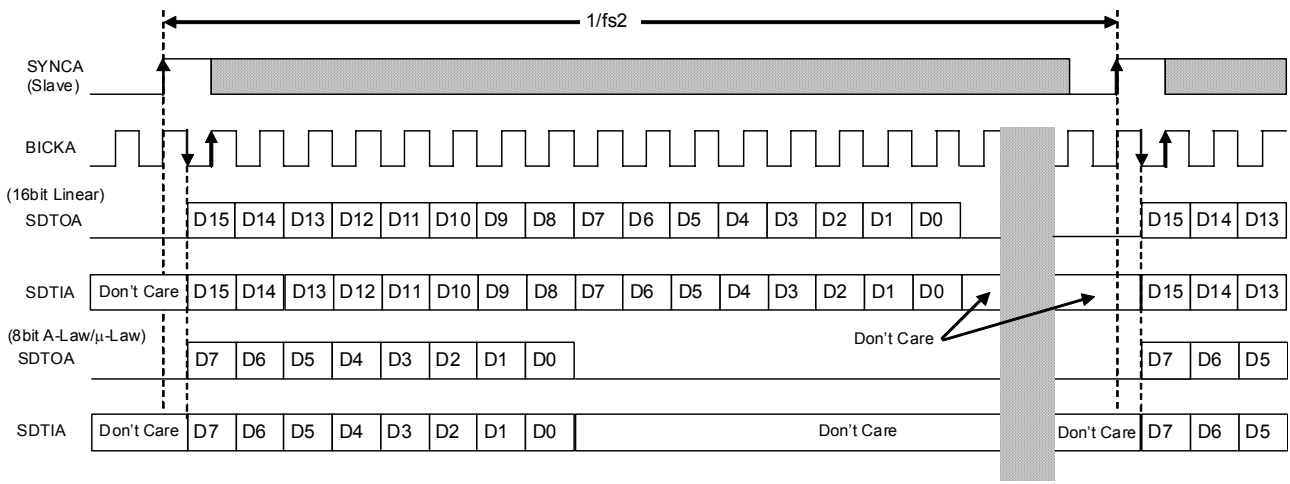


Figure 95. Timing of Long Frame Sync (PCM I/F A: MSBSA bit = "1", BCKPA bit = "1")

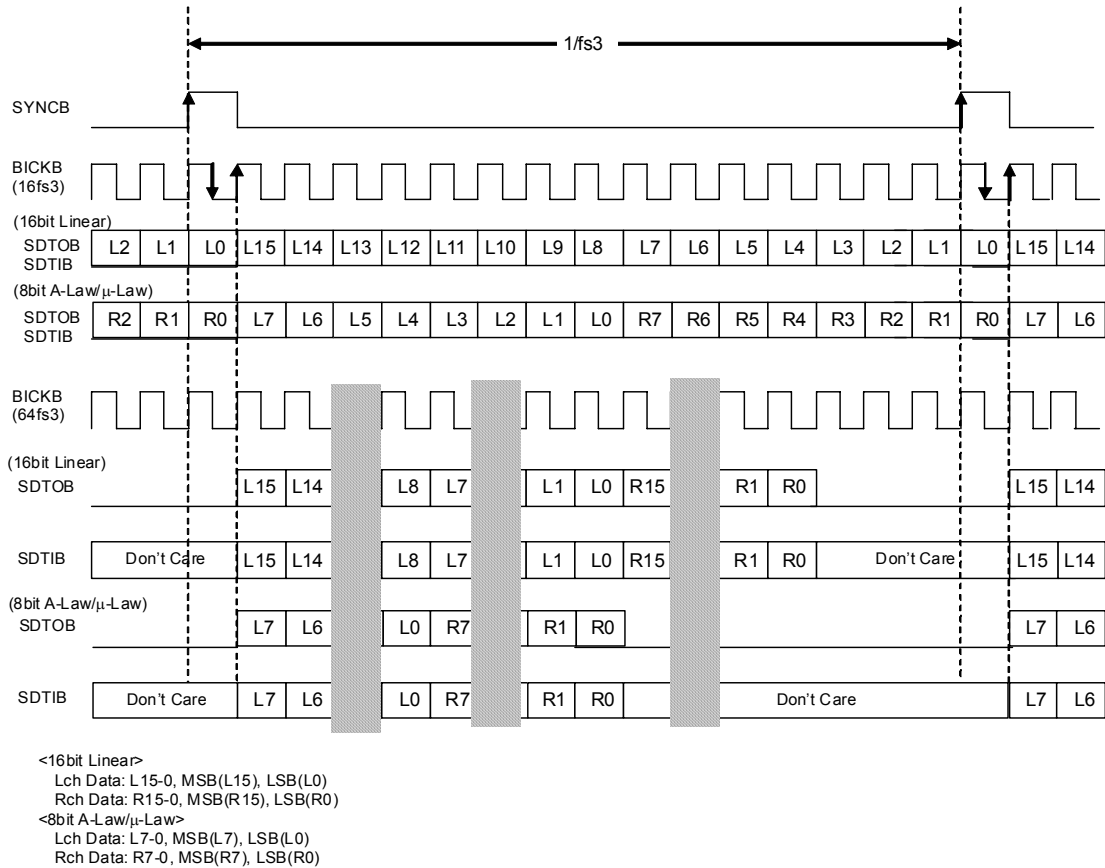


Figure 96. Timing of Short Frame Sync (PCM I/F B: MSBSB bit = “0”, BCKPB bit = “0”)

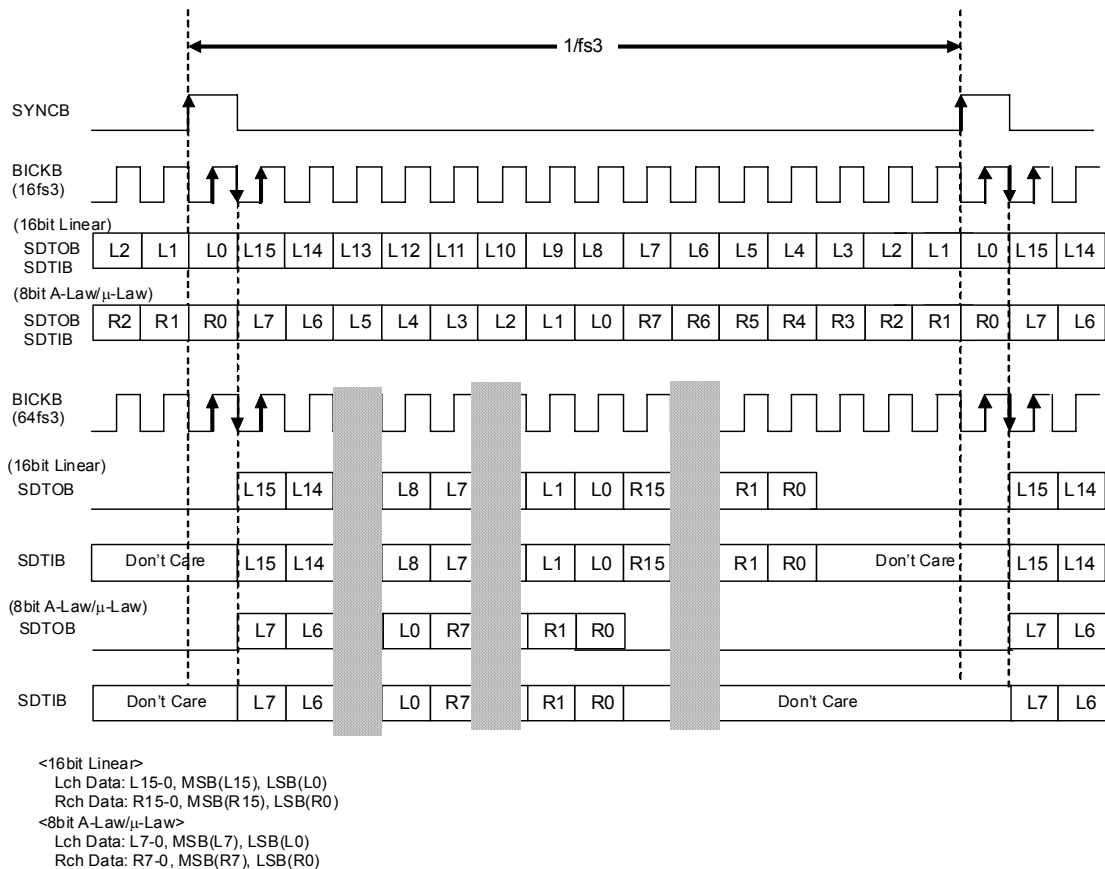


Figure 97. Timing of Short Frame Sync (PCM I/F B: MSBSB bit = “0”, BCKPB bit = “1”)

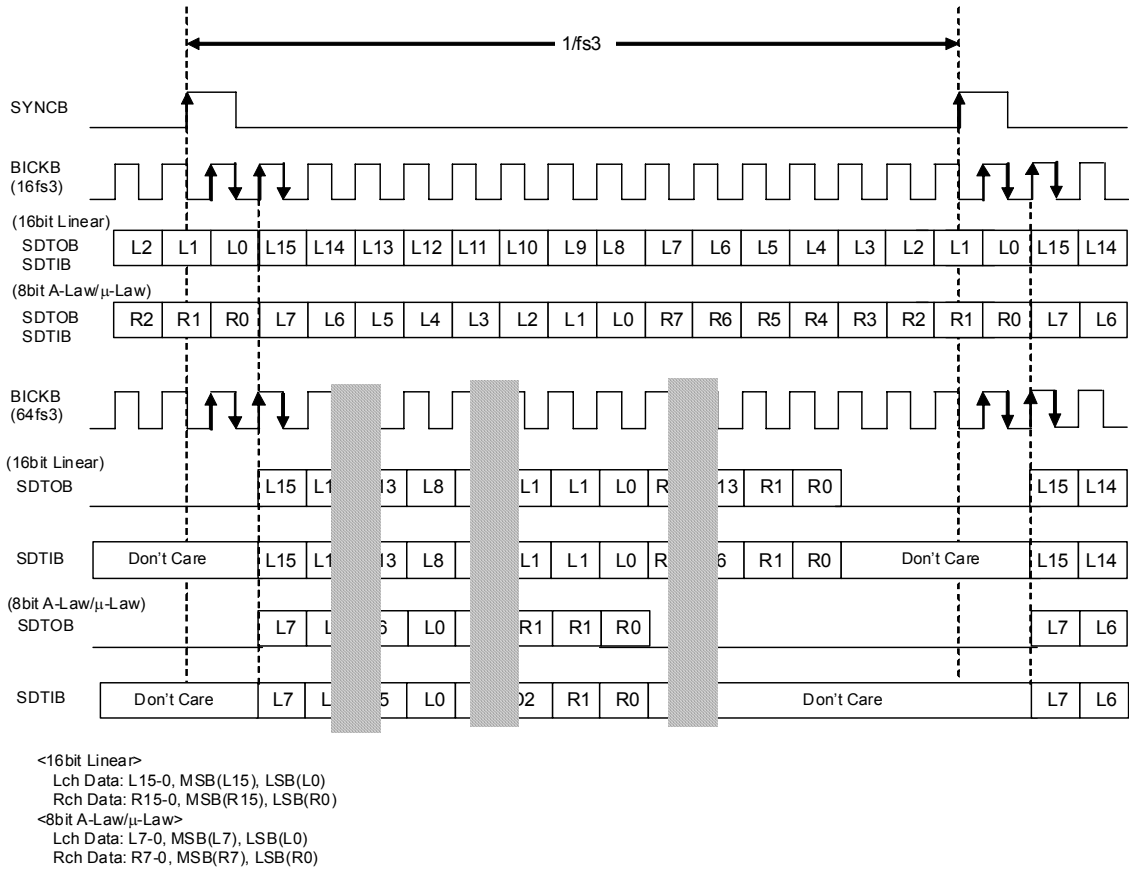


Figure 98. Timing of Short Frame Sync (PCM I/F B: MSBSB bit = "1", BCKPB bit = "0")

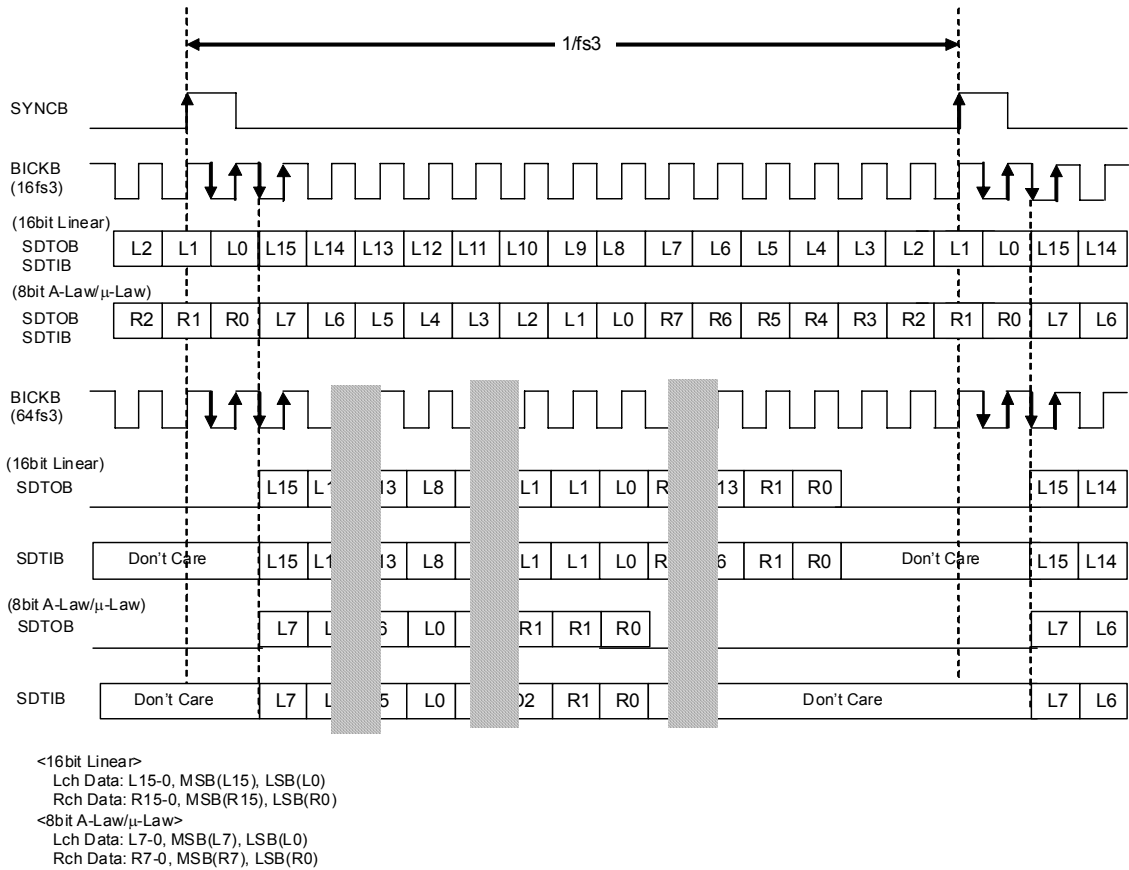


Figure 99. Timing of Short Frame Sync (PCM I/F B: MSBSB bit = "1", BCKPB bit = "1")

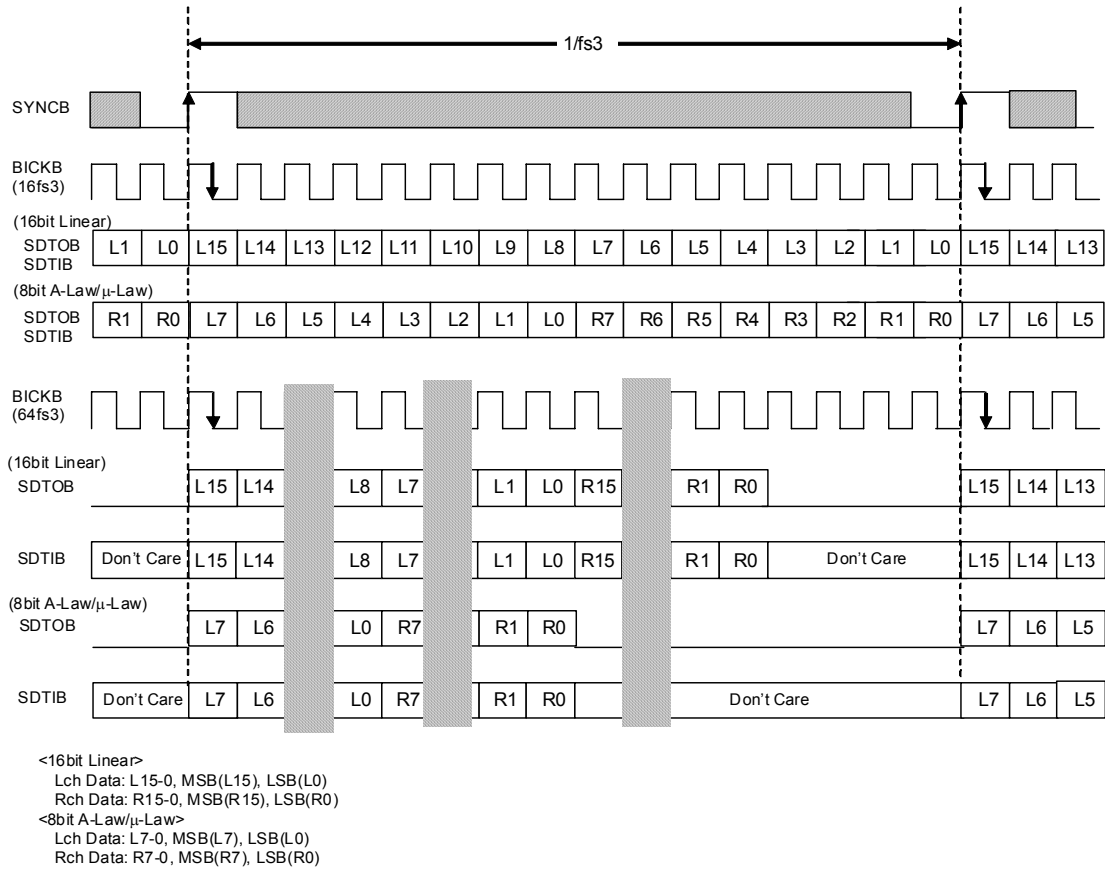


Figure 100. Timing of Long Frame Sync (PCM I/F B: MSBSB bit = “0”, BCKPB bit = “0”)

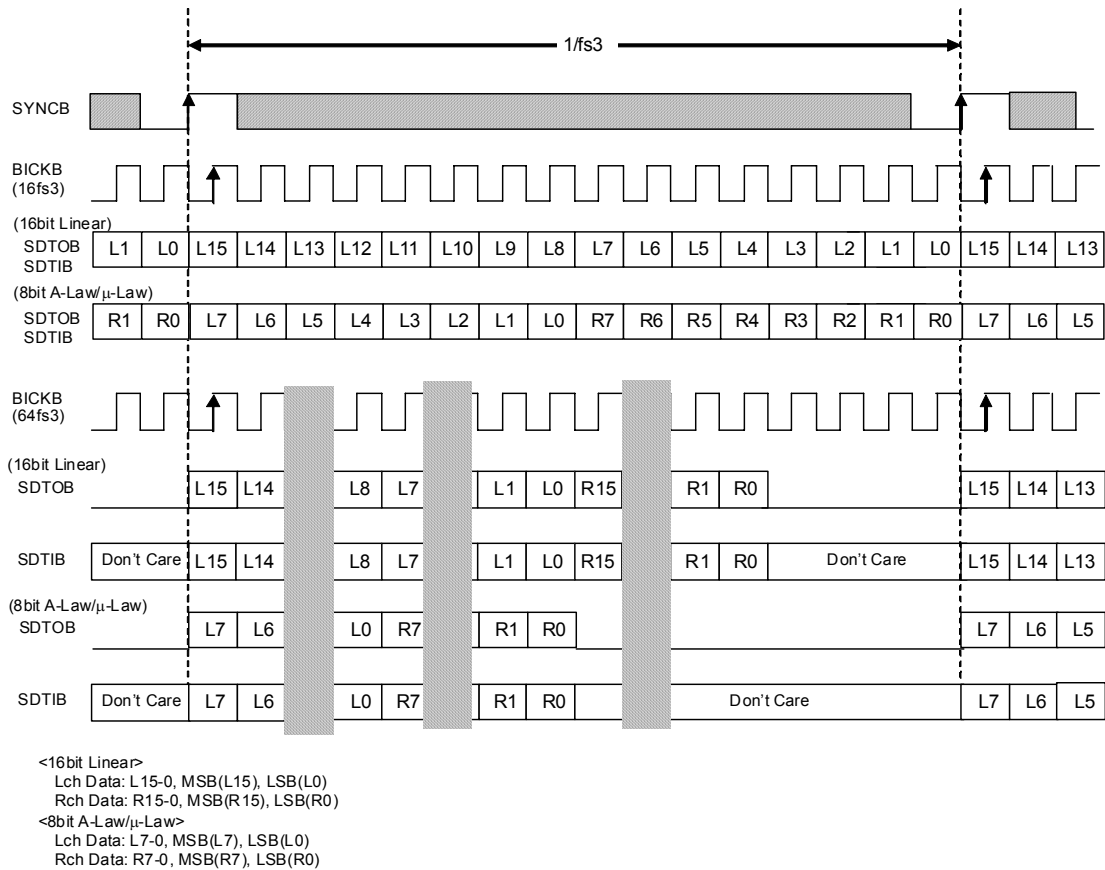


Figure 101. Timing of Long Frame Sync (PCM I/F B: MSBSB bit = “0”, BCKPB bit = “1”)

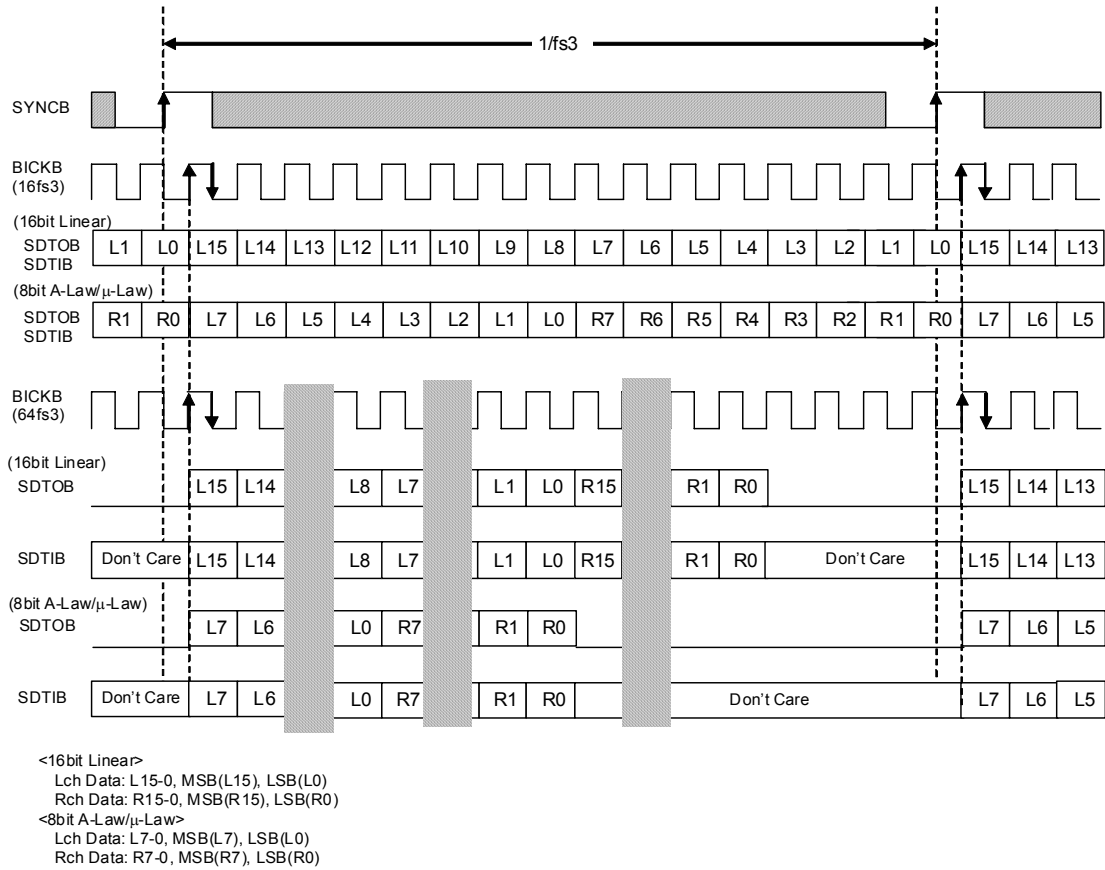


Figure 102. Timing of Long Frame Sync (PCM I/F B MSBSB bit = "1", BCKPB bit = "0")

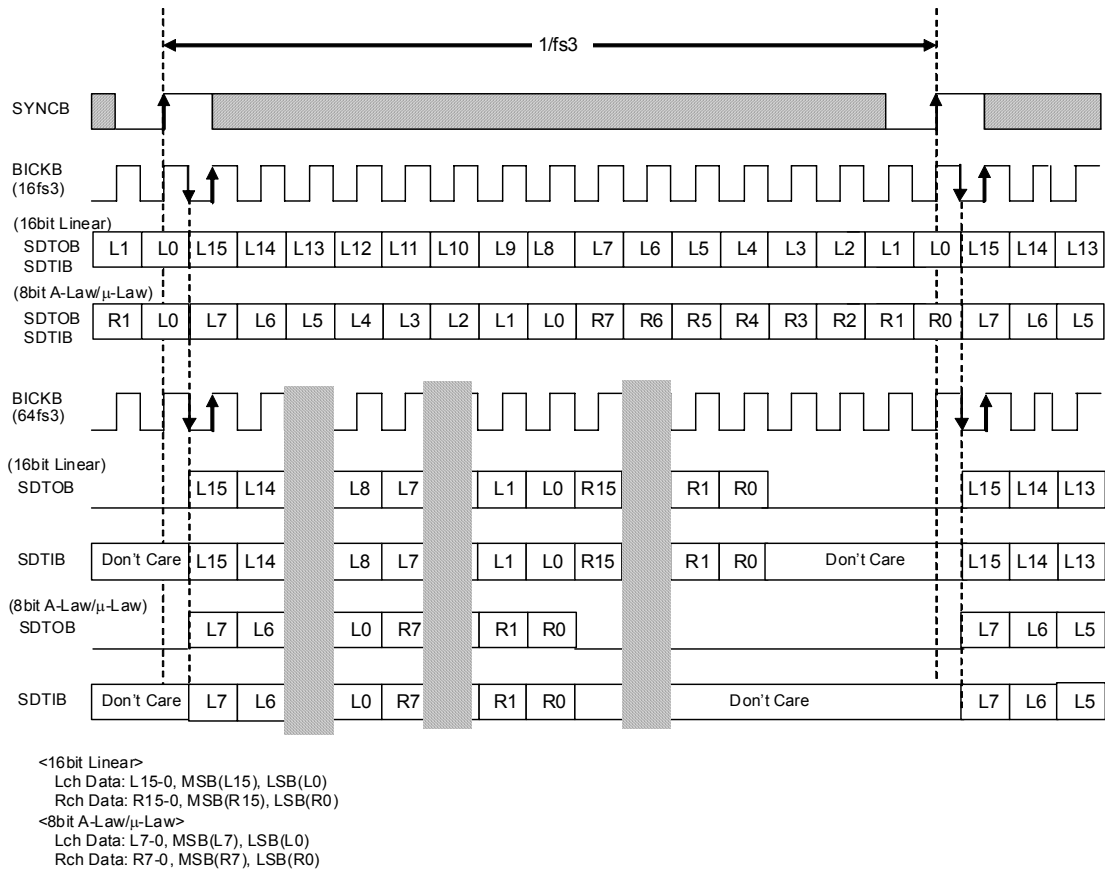


Figure 103. Timing of Long Frame Sync (PCM I/F B: MSBSB bit = "1", BCKPB bit = "1")

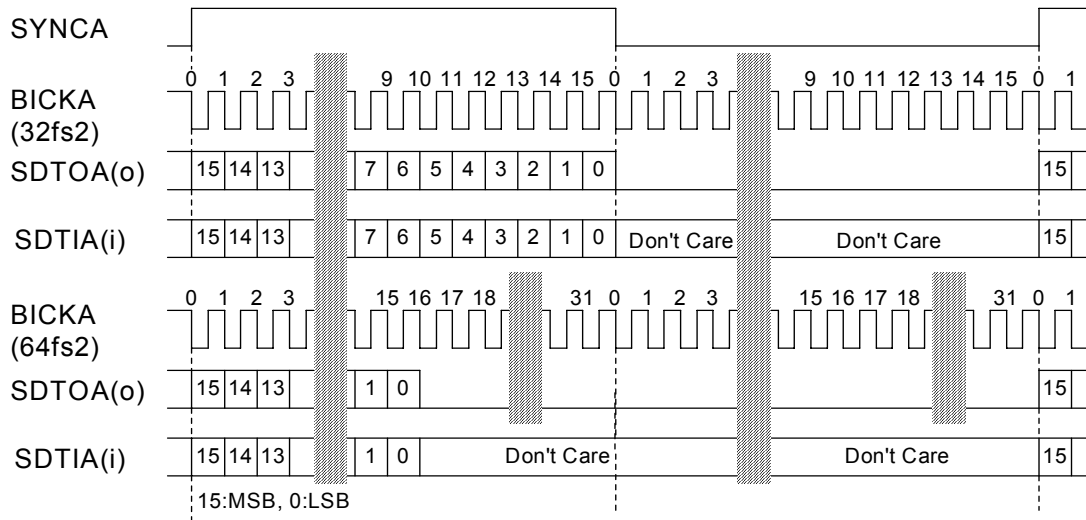


Figure 104. Timing of MSB justified (PCM I/F A)

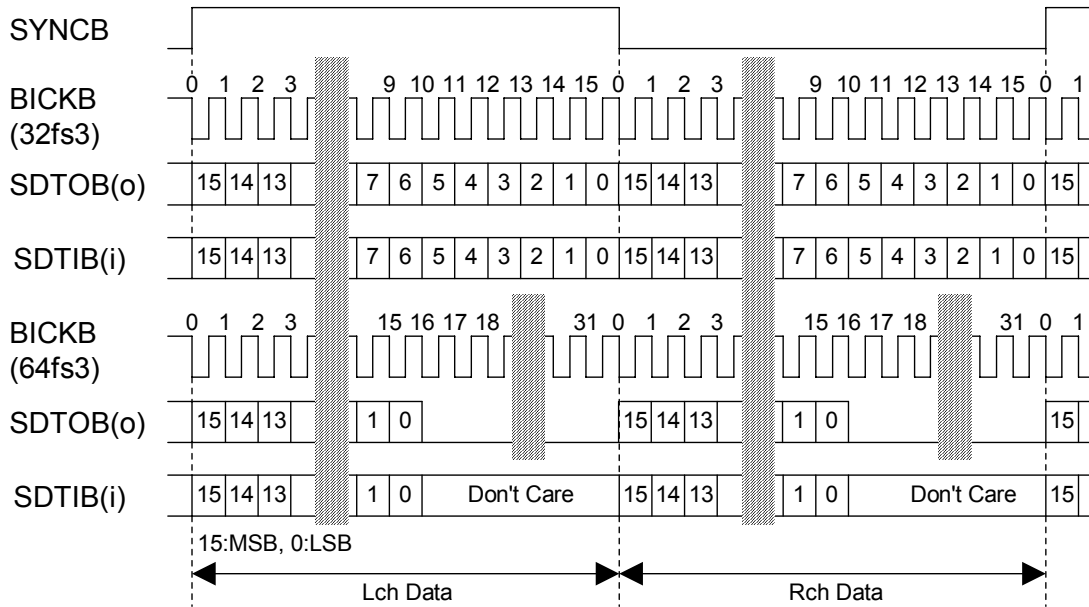


Figure 105. Timing of MSB justified (PCM I/F B)

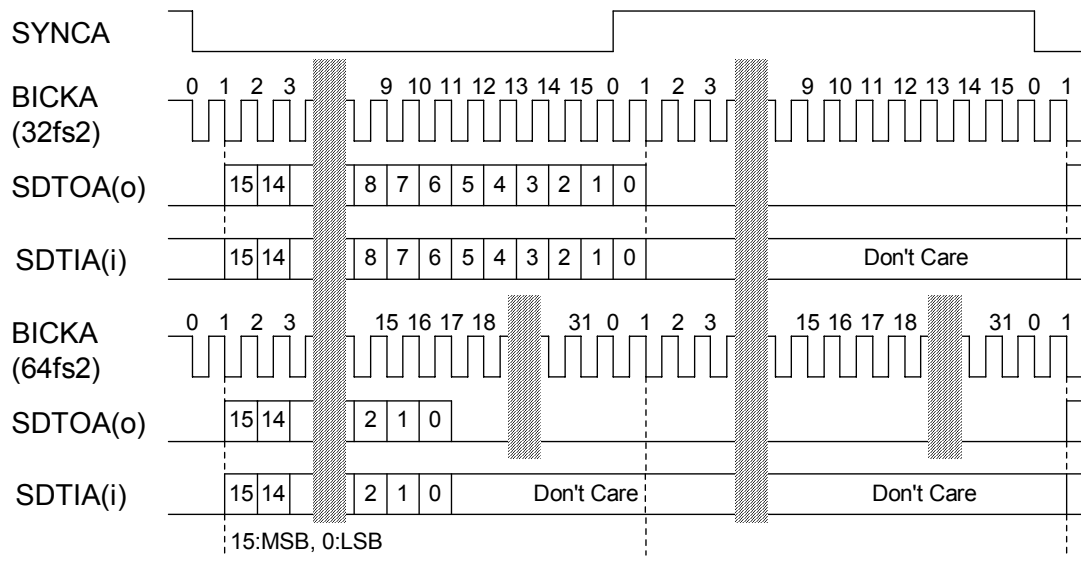


Figure 106. Timing of I²S (PCM I/F A)

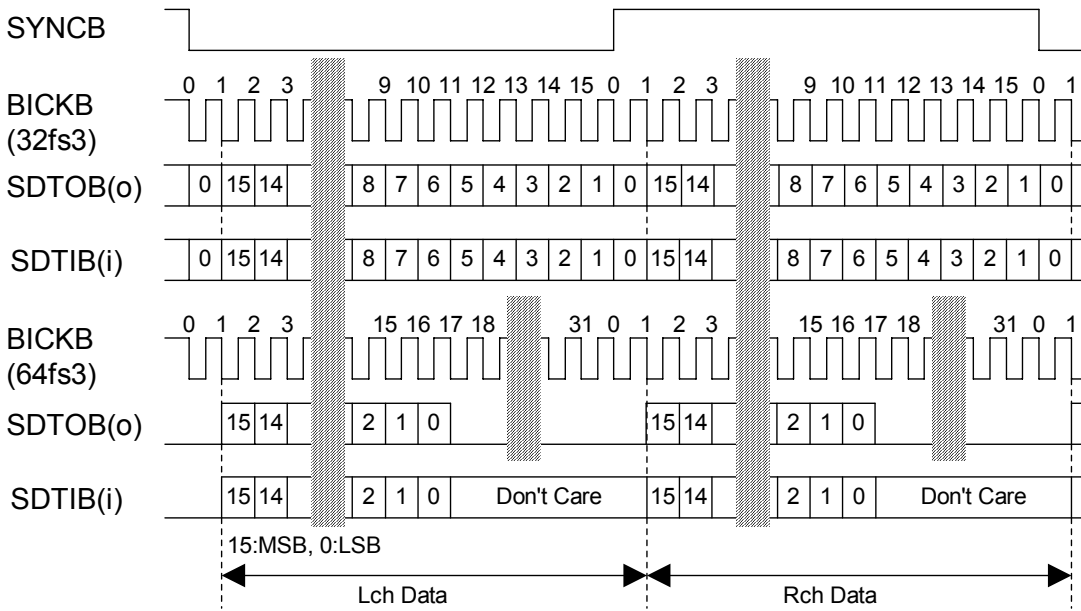


Figure 107. Timing of I²S (PCM I/F B)

■ DSP Block Sampling Frequency Setting

Select sampling frequency (FSD[3:0] bits) on the sleep mode. In FSD mode 6, the Up-Down sampling converter is powered-up and the AK4679 enters double sampling mode (fs1 =8kHz, fs2 =16kHz). In the other modes (using unity sampling rate), fs2 is output at the same timing of fs1 input.

| FSD Mode | FSD3 bit | FSD2 bit | FSD1 bit | FSD0 bit | Sampling Frequency | | | |
|----------|----------|----------|----------|----------|--------------------|-----------|-----------|----------------|
| | | | | | fs1 Port1 | fs2 Port2 | fs3 Port3 | |
| 0 | 0 | 0 | 0 | 0 | 8kHz | 8kHz | 8kHz | (default) |
| 6 | 0 | 1 | 1 | 0 | 8kHz | 16kHz | 8kHz | Double FS mode |
| 1 | 0 | 0 | 0 | 1 | 12kHz | 12kHz | 12kHz | |
| 2 | 0 | 0 | 1 | 0 | 16kHz | 16kHz | 16kHz | |
| 3 | 0 | 0 | 1 | 1 | 24kHz | 24kHz | 24kHz | |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz | 11.025kHz | 11.025kHz | |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz | 22.05kHz | 22.05kHz | |
| 10 | 1 | 0 | 1 | 0 | 32kHz | 32kHz | 32kHz | |
| 11 | 1 | 0 | 1 | 1 | 48kHz | 48kHz | 48kHz | |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz | 44.1kHz | 44.1kHz | |
| Others | N/A | | | | N/A | | | |

Table 122. Setting of Sampling Frequency (N/A: Not available)

■ Selection of Input Port

The selection of the signal path of the input clock for Port#1 and #3 is set by the SELPT bit. SYNC2 clock is selected by FSD bits and processed on the clock generator (CGU) block. The frequency of SYNC2 is double as that of SYNC1 on the FSD mode 6 while the BCLK2 bit clock rate is same as BCLK1. When PT2N bit = “1”, BCLK2 and SYNC2 pin outputs are low level. When BCLK1 and SYNC1 pins are selected as input pins, BCLK3/JX0 and SYNC3/JX1 pins could act as JX0 and JX1 pins function respectively.

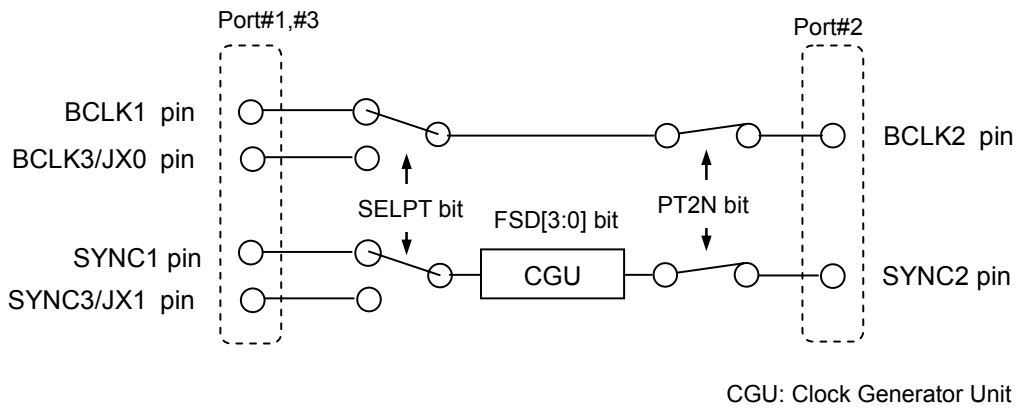


Figure 108. Port#1/2/3 Signal Setting (PT2N bit = “0”)

■ Output Selector of Port#1, Port#2 and Port#3

The AK4679 has output selectors. After releasing hardware suspend, LPDO1/2 bits control signal path of SDOUT1/2 respectively. On both hardware reset and suspend states, Port#1 input/output are bypassed to Port#2 output/input respectively. The output pin selection of the Port#3 is done by LPDO3 and 4 bits. Each output pin has an output enable switch. (OUTxN bit x = 1, 2, 3, 4)

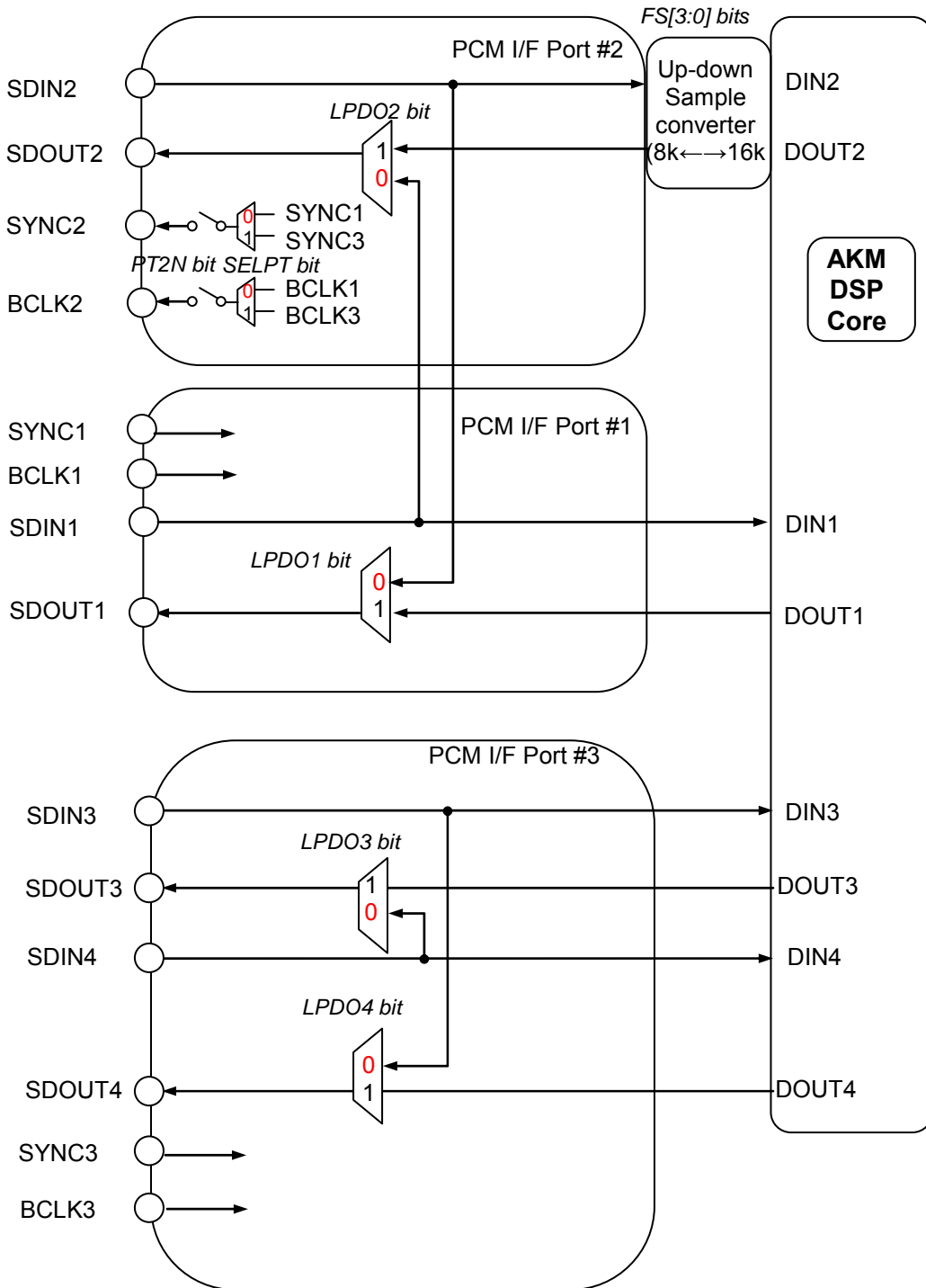


Figure 109. Output Selector of Port#1, Port#2 and Port#3 (Red: hardware reset)

■ PCM Audio Interface Format

LAW [1:0] and DIFD [1:0] bits select interface format of Port#1, Port#2 and Port#3. The interface format is in common for all ports. BCLK1/2 frequency ranges from 16fs1 to 256fs1. In all modes, the data format is MSB first, 2's complement and supporting 2channel data only. The data length supports 16/24bit Linear, 8bit μ -Law, and 8bit A-Law (Table 124)., On the PCM short/long frame, the AK4679 only accepts 1channel data when BICK1/2 is 16fs and in/output data length is 16bit Linear. The AK4679 can support 16bit PCM (short frame, long frame), Left justified and I²S mode (Table 125).

When the data format of Port#1 and Port#2 is 8bit A-Law or 8bit μ -Law, the data format of Port#3 will be 16bit Linear.

BCLK1 and BCLK3 input frequency to the Port#1, 3 are dependent on DIFD mode as shown below.

| fBCLK1, fBCLK3 frequency range | Remark |
|--|-------------------------------|
| 4 x DataLength(8,16,24) x fs ~ 256 x fs | FSD mode 6 |
| 2 x DataLength (8,16,24) x fs ~ 256 x fs | Others (Except FSD mode 6) |

Table 123. BCLK Setting

| Mode | LAW [1:0]bits | Digital I/F Format | | (default) |
|------|---------------|--------------------|---------------|-----------|
| | | Port#1, Port#2 | Port#3 | |
| 0 | 00 | 16-bit Linear | 16-bit Linear | |
| 1 | 01 | 24-bit Linear | 24-bit Linear | |
| 2 | 10 | 8-bit A-Law | 16-bit Linear | |
| 3 | 11 | 8-bit μ -Law | 16-bit Linear | |

Table 124. PCM Data Format Setting

| DIFD Mode | DIFD[1:0]bits | Digital I/F Format | BCLK1 | (default) |
|-----------|---------------|--------------------|--------------|-----------|
| 0 | 00 | PCM Short Frame | $\geq 16fs1$ | |
| 1 | 01 | PCM Long Frame | $\geq 16fs1$ | |
| 2 | 10 | Left justified | $\geq 32fs1$ | |
| 3 | 11 | I ² S | $\geq 32fs1$ | |

Table 125. PCM Interface Format Setting

In format mode 1/2, PCM data format is selected by BCKPD bit (Table 126). SDOOUT output data and SDIN input data are latched and output on the falling or rising edge of BCLK. Refer to: Figure 110-Figure 113 for selectable format of BCLK against SYNC1/2 edge.

| BCKPD bit | BCLK edge referenced to SYNC edge | (default) |
|-----------|-----------------------------------|--------------------------|
| 0 | falling (FE) | Figure 110 Figure 112 |
| 1 | rising (RE) | Figure 111 Figure 113 |

Table 126. PCM Interface format in (DIFD[1:0] = "00", "01")

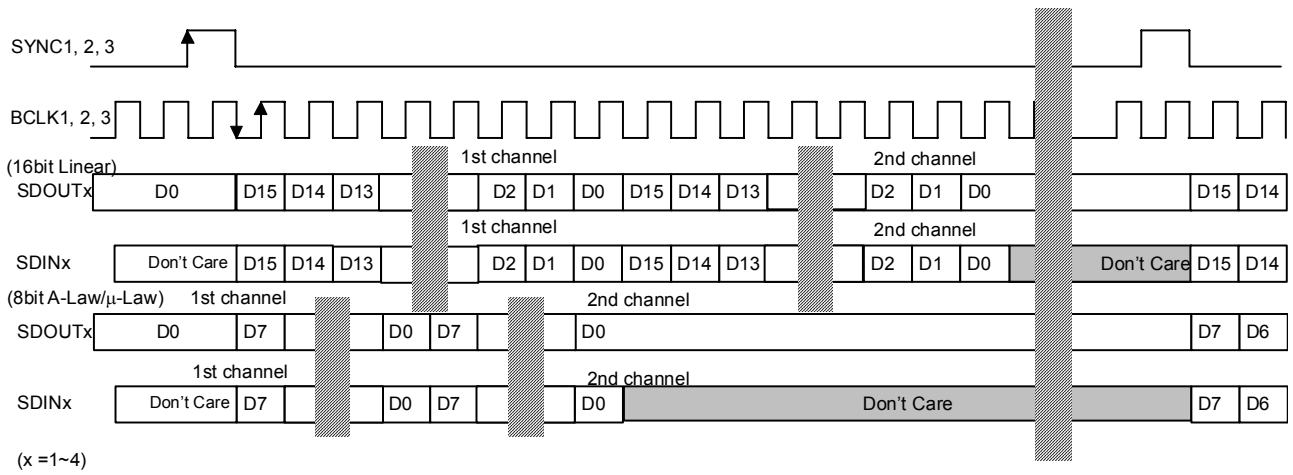


Figure 110. PCM Short Frame Falling-edge (LAW bits = “00”, DIFD bits = “00”, BCKPD bit = “0”)

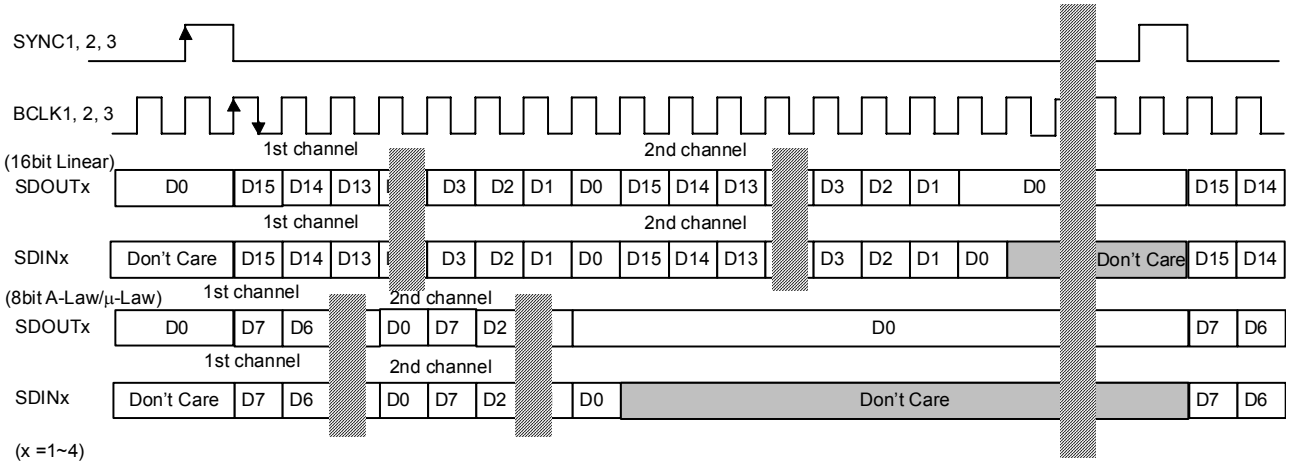


Figure 111. PCM Short Frame Rising-edge (LAW bit = “00”, DIFD bits = “00”, BCKPD bit = “1”)

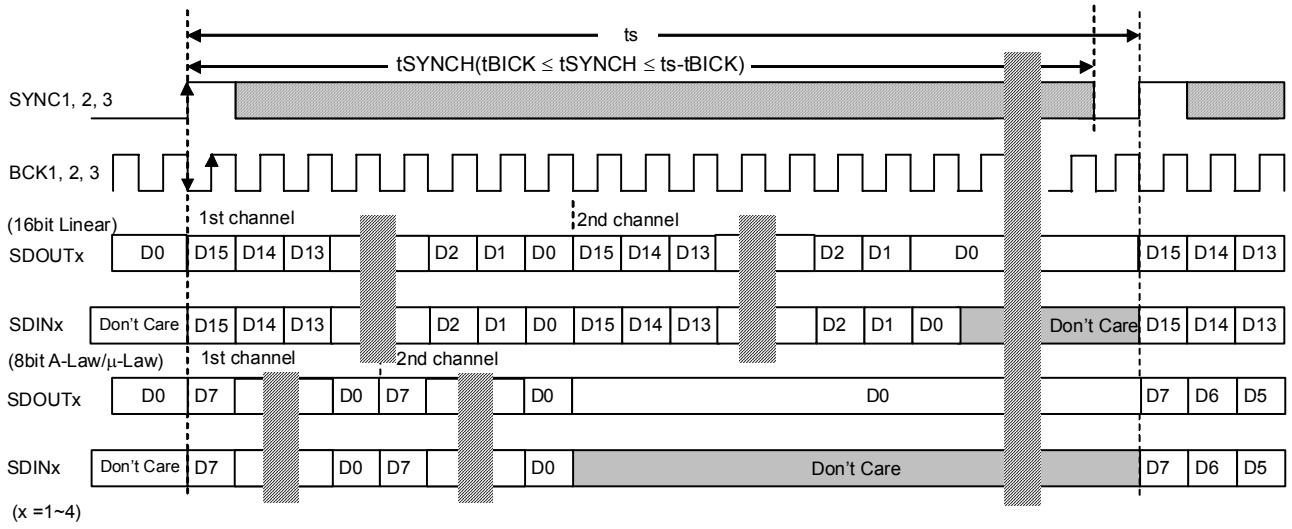


Figure 112. PCM Long Frame Falling-edge (LAW bit = "00", DIFD bits = "01", BCKPD bit = "0")

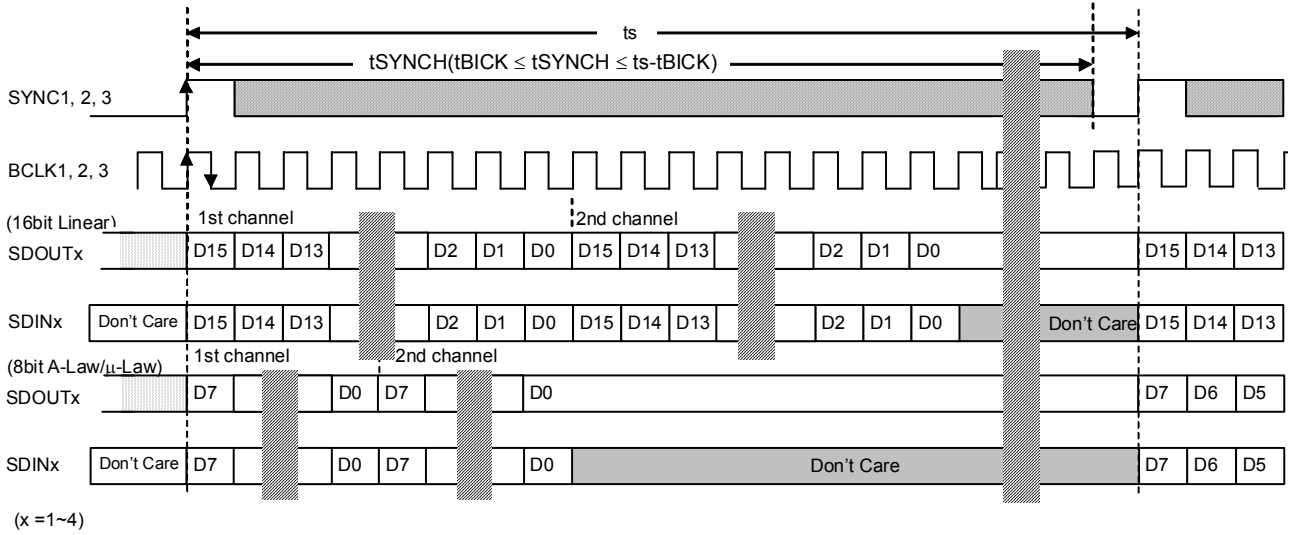


Figure 113. PCM Long Frame Rising-edge (LAW bit = "00", DIFD bits = "01", BCKPD bit = "1")

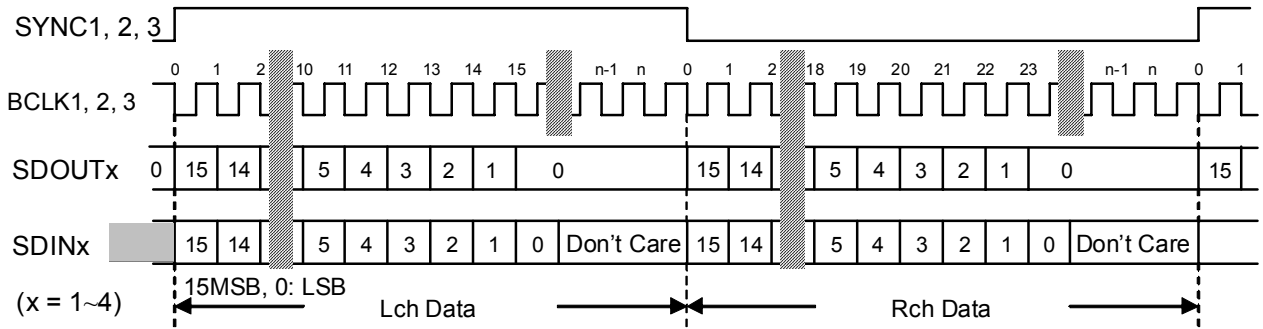


Figure 114. Left Justified format (LAW bits = "00", DIFD bits = "10")

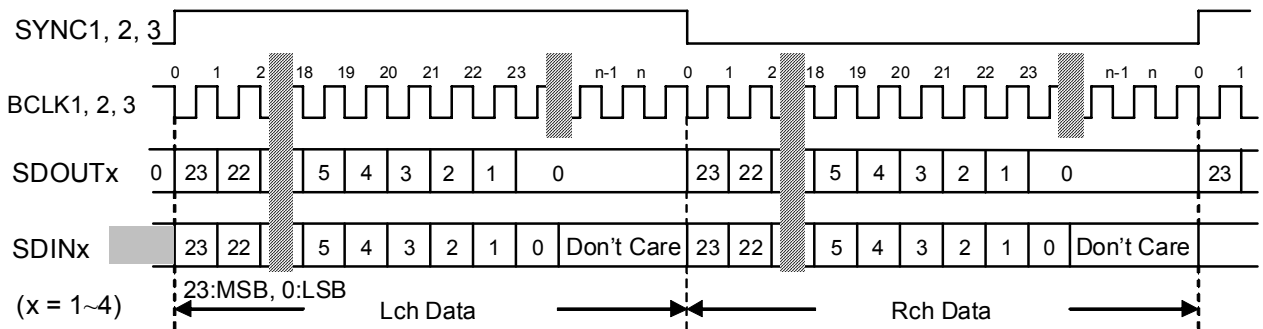


Figure 115. Left Justified format (LAW bits = "01", DIFD bits = "10")

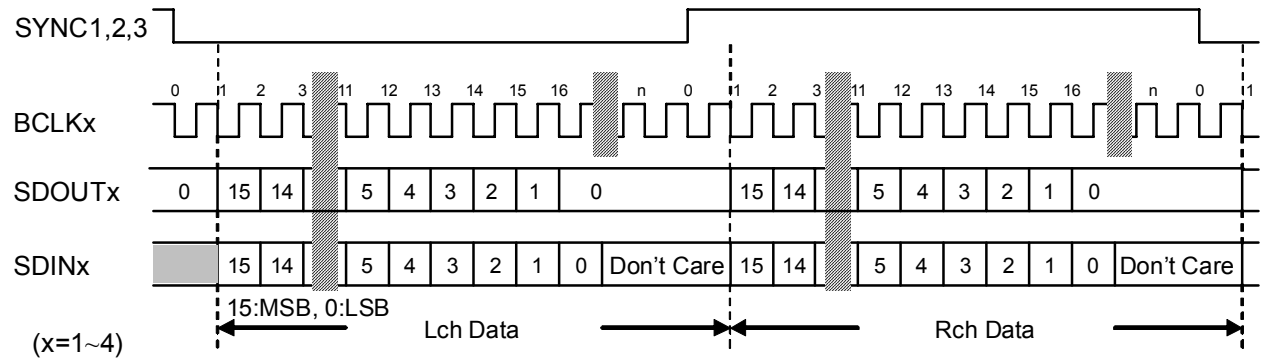


Figure 116. I²S Format (LAW bits = "00", DIFD bits = "11")

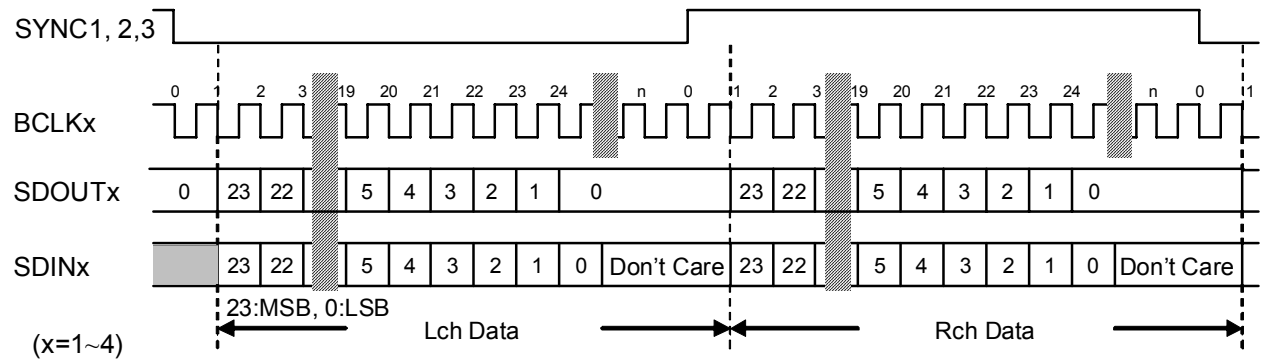


Figure 117. I²S Format (LAW bits = "01", DIFD bits = "11")

■ DSP STATE TRANSITION

The DSP block has following operating modes which are controlled by power supply, registers setting, program setting and external clocks.

◆ Power Down (PDNE pin= “L”)

When the PDNE pin = “L” the DSP block is in powered-down state. Power supplies must be applied when the PDNE pin = “L”. Set the PDNE pin to “H” to release the power-down after all power supplies are fed. More than tPDNE cycle of “L” period is needed before releasing the power-down. The state moves the Hardware Reset state by bringing the PDNE pin = “H”.

◆ Hardware Reset

The DSP is also in reset state in this mode. The clocks and digital signals are bypassed to the output pins as shown in [Figure 109](#). The frame sync SYNC1 goes through SYNC2, and BCLK1 through BCLK2. The digital signal path is shown in [Figure 109](#). Do not apply a clock over 3.072MHz to the BCLK pin. In hardware reset state, control registers (CONT0~8) cannot be accessed. The DSP block enters hardware suspended state when the internal digital block is powered-up by setting the system power supply register (PCONT0: PWSW bit) to “1”.

◆ Hardware Suspended

The power supply control block is initialized when the system power supply register (PCONT1: MRSTN bit) is set to “1”. Control registers are reset and the DSP block goes into sleep state.

◆ Sleep (Standby)

In this state, all internal registers are in their default values. Register settings and DSP program downloading to the RAM are available. TESTA, B, C bit, Digital I/F format and DSP related register settings should be made in DSP reset state (DSPRSTN bit = “0”). After these settings, set DLRDY bit for the access permission of internal memories to download DSP programs. The DLRDY bit must be cleared after downloading DSP programs. Then, release the DSP reset (DSPRSTN bit = “1”).

◆ Wait Sync

After releasing DSP reset, DRAM and DLRAM data are cleared by “0” and the DSP block enters wait sync state. In this state, the clock generator (CGU) is powered-up if an external clock is input to Port#1 or Port#3. Then the DSP block enters normal operation mode after the output clock of CGU is stabilized.

◆ DSP Operational (Run state)

The CGU block is powered-up when BCLK and SYNC clocks are detected in Wait Sync mode. The DSP block becomes RUN state and CGU block starts to control clocks and DSP core.

The CGU block is unlocked when no input clocks are present during an operation and the DSP block enters either Wait Sync state or Hardware Reset.

1. Wait Sync State

When the input clock at Port#1 or Port#3 is stopped for a certain period ([Figure 120](#)), the DSP block enters wait sync state. Registers, PRAM, CRAM and OFREG data are maintained. The CGU block is in powered-down state until the clock is input again.

2. Hardware Reset State

When MRSTN bit = “0” and PWSW bit = “0”, the CGU block is powered-down and the internal registers are initialized. The system power supply switch is turned off and PRAM, CRAM and DLRAM are cleared. Register values are also cleared to the default values. This mode is suitable for standby in low power consumption. To resume the device operation, register settings and program downloadings are necessary.

| Mode | Setting | | | | | | State | |
|---------------------------|-------------|-------------|--------------|--------------|----------------|-----------------|-------|------------|
| | PDNE pin | PWSW bit | MRSTN bit | DLRDY bit | DSPRSTN bit | BCLKx, SYNCx | CGU | DSP RAM |
| Power Down | L | 0 | 0 | 0 | 0 | None | PD | PD |
| Hardware Reset | H | 0 | 0 | 0 | 0 | Don't Care | PD | PD |
| Hardware Suspended | H | 1 | 0 | 0 | 0 | Don't Care | PD | PD |
| Sleep/Standby | H | 1 | 1 | 0 | 0 | Don't Care | PD | PD |
| Wait Sync | H | 1 | 1 | 0 | 1 | Don't Care | PD | PU |
| CG Ctrl | H | 1 | 1 | 0 | 1 | Input | PU | PU |
| Device Operating State | H | 1 | 1 | 0 | 1 | Input | PU | PU |

(PD: Power Down, PU: Power Up)

Table 127. Modes Definitions

DSP Operational Transition Diagram

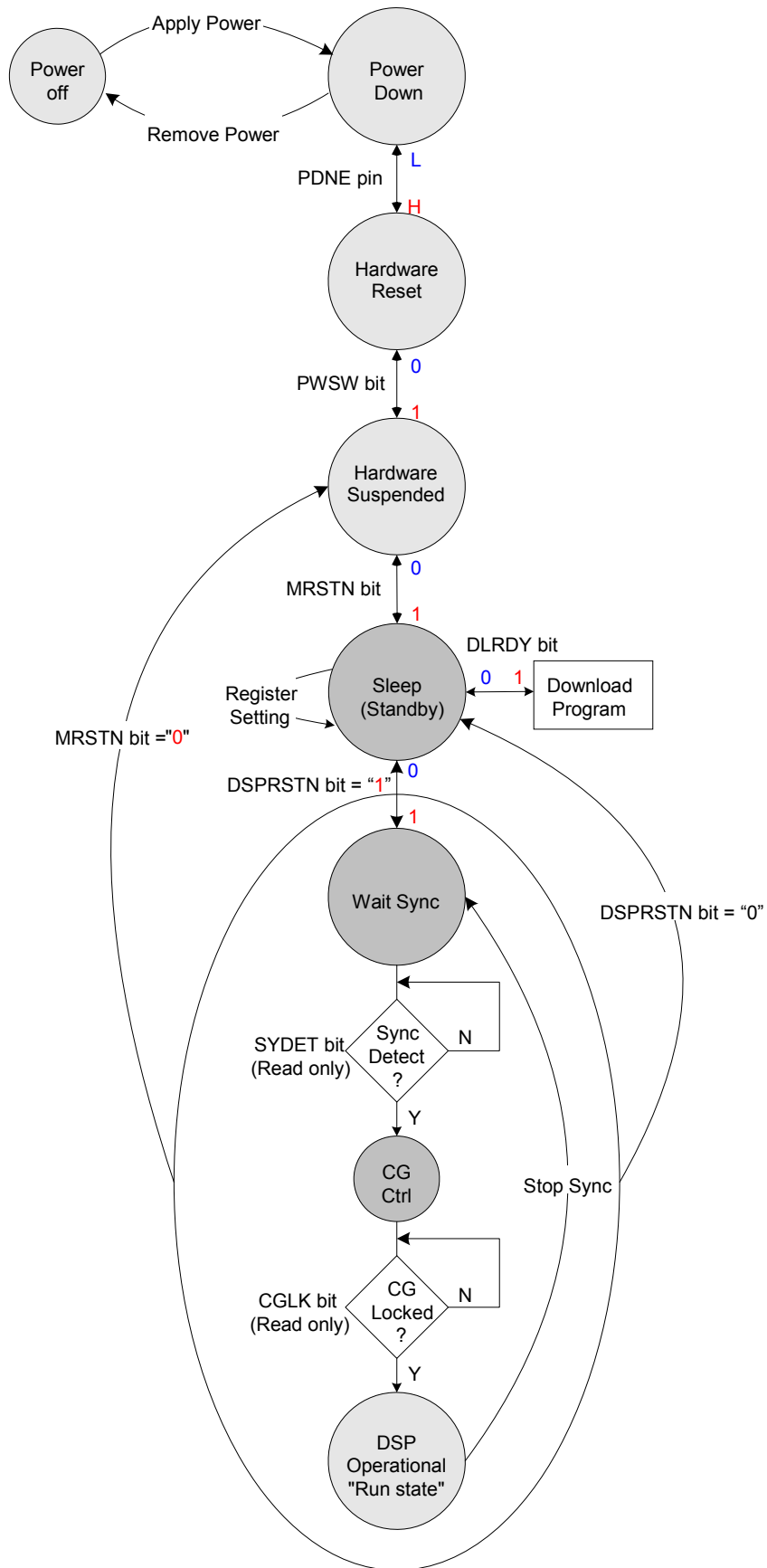


Figure 118. DSP Block State Diagram

■ Power-up Sequence and Device Setting

- Power-up, register setting, program download and RUN state sequence

The DSP must be in sleep state when downloading the program. Set DLRDY bit to “1” to power-up the internal oscillation circuit, and after 100μs downloading becomes available. DLRDY bit must always be cleared when complete a download. Then DSPTRSTN bit is cleared, the DSP block enters wait sync mode. In this state, CGU block is locked when serial data clock input is detected and the DSP block becomes operating state.

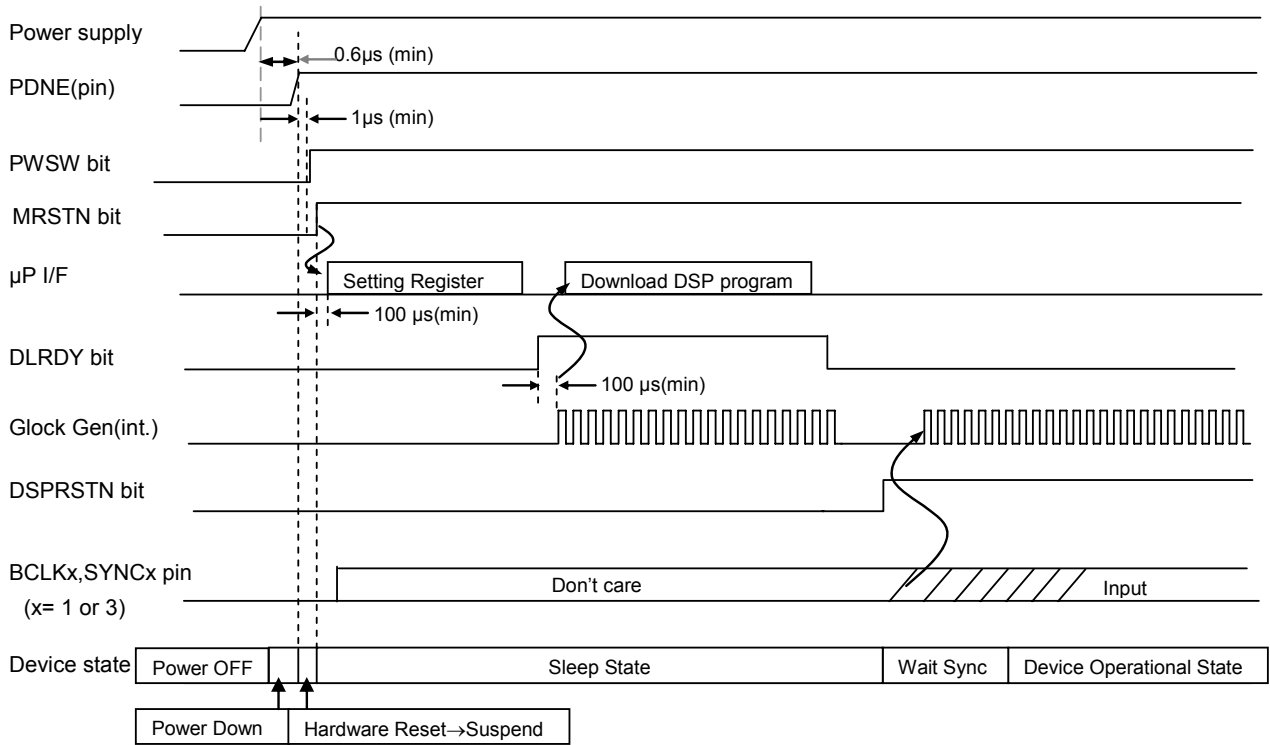


Figure 119. DSP Block Status

■ DSP State Transition (operational state ↔ wait sync)

Standby Sequence by SYNC1 and SYNC3

When SYNC input is stopped, fixed to “L” or “H” for more than 0.8ms during RUN state, CGU block is powered-down and the DSP block enters the wait sync mode.

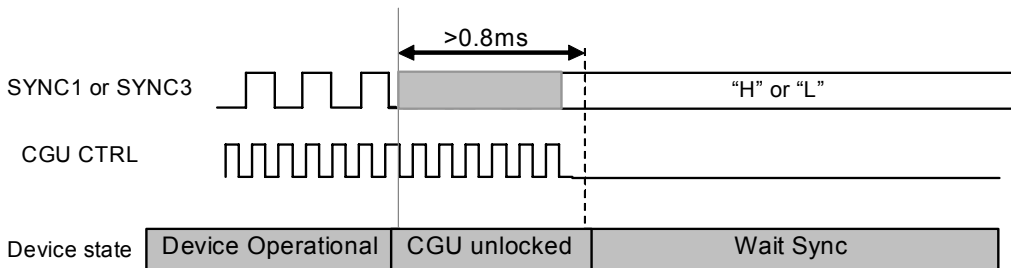


Figure 120. Standby Sequence Example by SYNC1/3

Resume Sequence by SYNC1 and SYNC3

In wait sync mode, CGU block will be powered up in 5ms after SYNC1/3 input. The DSP block resumes operation when DSP reset is released internally and the RAM data is cleared.

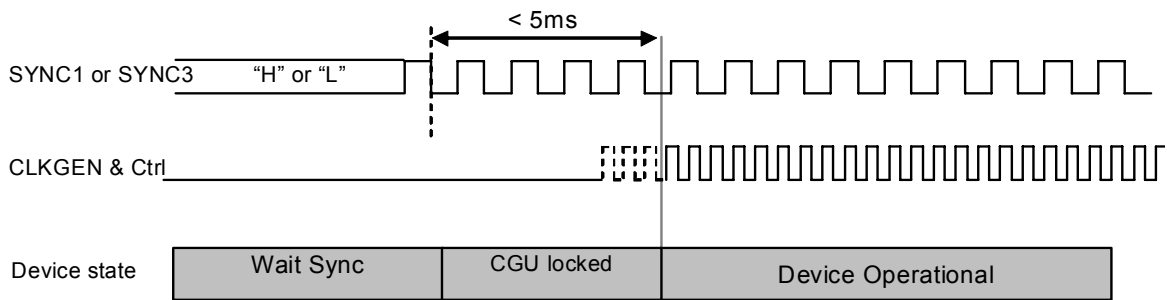


Figure 121. Resume Sequence by SYNC1/3

Refer to [Figure 118](#) for the sequence when resuming the operation from hardware default state.

■ RAM Clear

The DSP block has a RAM clear function. After the DSP reset release (during RUN), data RAM, delay RAM, coefficient RAM and accelerator are cleared by “0” (RAM clear). The required time to clear RAM is about 400µs. In the RAM clear sequence, it is possible to order command to DSP. (DSP is stopped during RAM clear sequence. The ordered command is accepted automatically after this sequence is completed.)

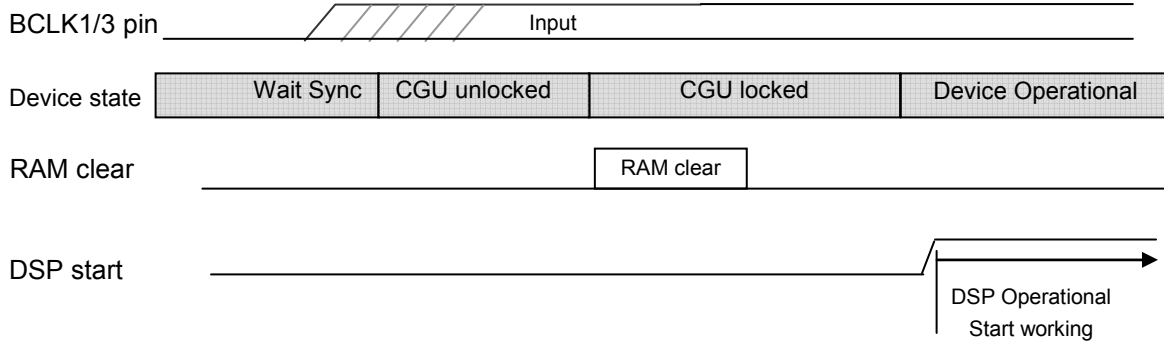


Figure 122. RAM Clear Sequence

■ Status Output Pin

STRDY bit selects the output of the STO/RDY pin. When STRDY bit = “0”, the STO/RDY pin outputs STO. The STO/RDY pin outputs “L” after the DSP block is powered-up during the PDN pin = “L”. When the DSP block exits power-down mode, WDT (watch dog timer) error, CRC error and lock error of CGU block can be output by control register settings. Each error OR’ed status is output by active-low output when these errors occur. WDT error detection result output is enabled by DSP instruction setting.

| PWSW bit | MRSTN bit | CRCE bit | WDTN bit | LOCKE bit | STO pin | Note | |
|----------|-----------|----------|----------|-----------|-------------------------------|-------------------------------|-------------------------------|
| 0 | - | -- | -- | -- | L | | |
| 1 | 1 | 0 | 0 | 0 | L | | |
| | | | | | WDTERRN | Needs DSP Instruction Setting | |
| | | 0 | 1 | 0 | 0 | H | |
| | | | | | | CRCERRN | |
| | | 1 | 0 | 0 | 0 | WDTERRN | Needs DSP Instruction Setting |
| | | | | | | CRCERRN | |
| | | 0 | 0 | 0 | 1 | WDTERRN | Needs DSP Instruction Setting |
| | | | | | | LOCKERRN | |
| | | 0 | 1 | 1 | 1 | LOCKERRN | |
| | | | | | | CRCERRN | |
| 1 | 0 | 0 | 1 | CRCERRN | | | |
| | | | | WDTERRN | Needs DSP Instruction Setting | | |
| 1 | 1 | 1 | 1 | LOCKERRN | | | |
| | | | | CRCERRN | | | |

Table 128. STO pin Configuration

■ DSP Programmable Output

The DSP block has two General Purpose Output (GP0 and GP1) pins for external device controlling. The outputs can be controlled by DSP programs. SELDO3 and SELDO4 bits control SDOUT3/GP0 and SDOUT4/GP1 pins respectively. OUT3N and OUT4N bits switch output enable/disable of these. When controlling the GPC by the GP0 and GP1 pins, the initial state of the GP0 and GP1 pins are “L”.

| OUT3N bit | SELDO3 bit | Output Data Select | |
|-----------|------------|--------------------|-----------|
| 0 | 0 | DSP DOUT3 | (default) |
| | 1 | DSP GP output 0 | |
| 1 | 0 | Low | |
| | 1 | | |

Table 129. SDOUT3/GP0 pin Select

| OUT4N bit | SELDO4 bit | Output Data Select | |
|-----------|------------|--------------------|-----------|
| 0 | 0 | DSP DOUT4 | (default) |
| | 1 | DSP GP output 1 | |
| 1 | 0 | Low | |
| | 1 | | |

Table 130. SDOUT4/GP1 pin Select

Serial Control Interface (SPI, I²C-bus)

■ General

Audio Block is controlled by I²C bus only while DSP Block is controlled by the SPI or I²C bus which is set by I2CE pin state.

■ Serial Control Interface (I²C-bus)

The AK4679 supports the fast-mode I²C-bus (max: 400 kHz). Pull-up resistors at SDAA and SCLA pins must be connected to (TVDDA+0.3)V or less voltage. Pull-up resistors at SDAE and SCLE pins must be connected to (TVDDA+0.3)V or less voltage.

SCLA and SCLE are denoted by SCL. SDAA and SDAE are denoted by SDA in this document.

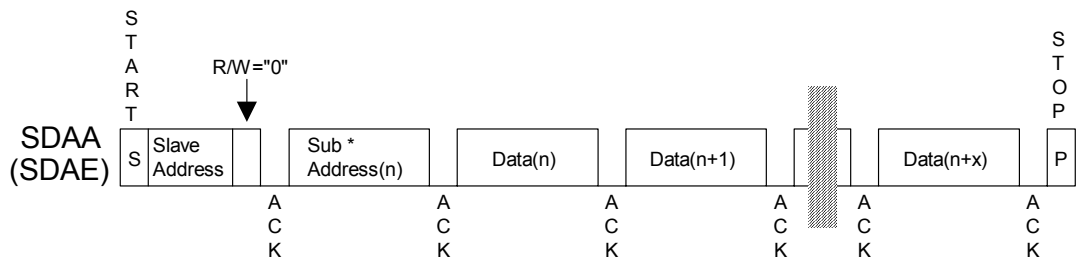
(2)-1. WRITE Operations

[Figure 123](#) shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition ([Figure 131](#)). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are shown in [Figure 124](#) and [Figure 125](#). If the slave address matches that of the AK4679, the AK4679 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse ([Figure 133](#)). A R/W bit value of “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4679. When accessing the PRAM, CRAM and OFFREG the second byte consists command code at this time. This address is 8bits and the format is MSB first ([Figure 126](#)). The data after the second byte contains control data. The format is MSB first, 8bits ([Figure 127](#)). The AK4679 generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition ([Figure 131](#)).

The AK4679 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4679 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 8-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address for CODEC registers exceeds AFH prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW ([Figure 134](#)) except for the START and STOP conditions.



(*: Command code)

Figure 123. Data Transfer Sequence at the I²C-Bus Mode

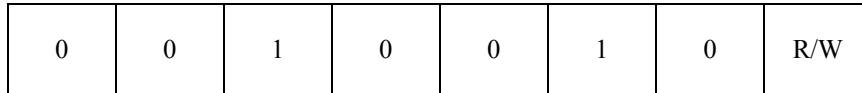


Figure 124. The First Byte for Audio Block

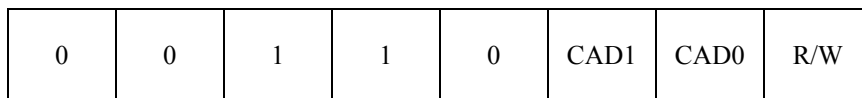


Figure 125. The First Byte for DSP Block
CAD1, CAD0 bits defined by the related pins.

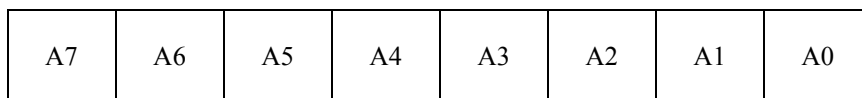


Figure 126. The Second Byte

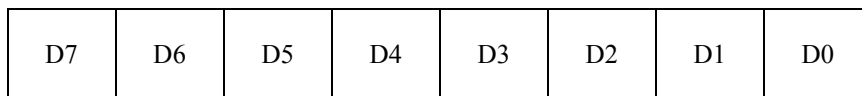


Figure 127. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4679. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 8-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds AFH prior to generating a stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out. The AK4679 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4679 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit set to "1", the AK4679 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4679 ceases transmission.

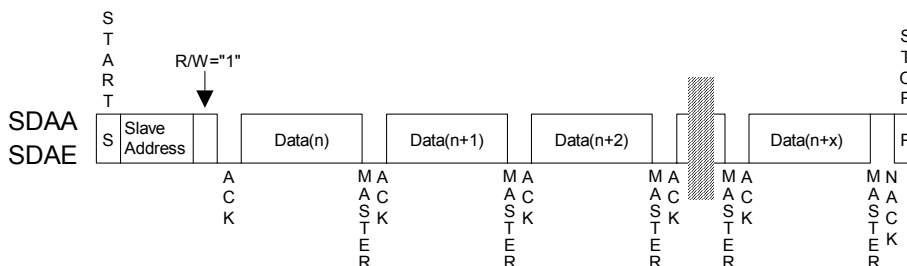
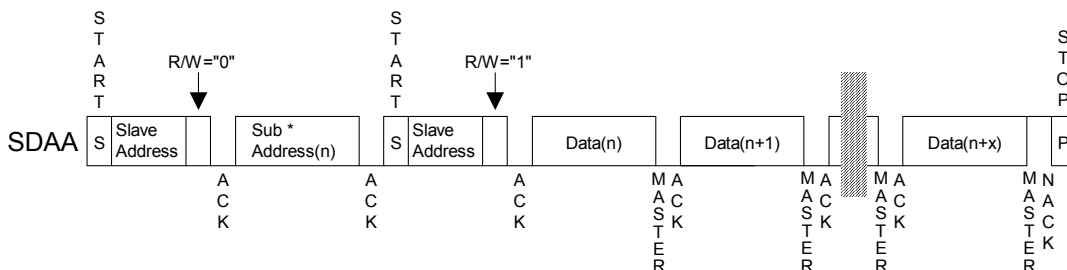


Figure 128. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4679 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4679 ceases transmission.



(*: Command code)

Figure 129. RANDOM ADDRESS READ (Audio Block)

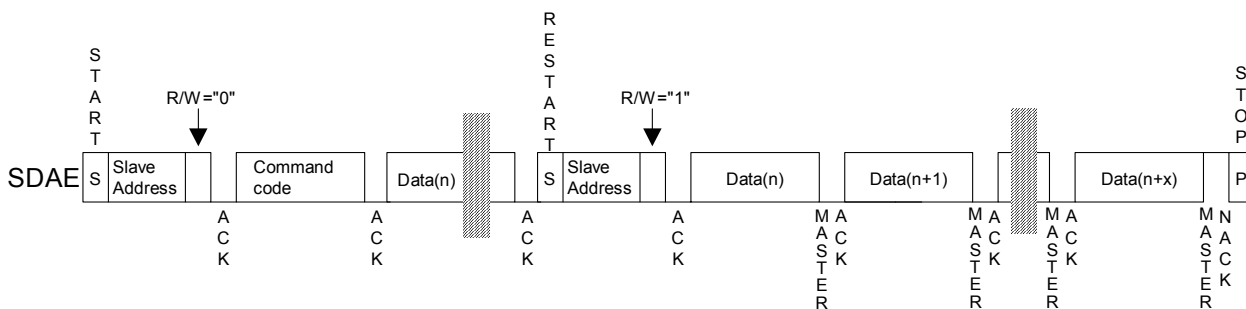


Figure 130. RANDOM ADDRESS READ (DSP Block)

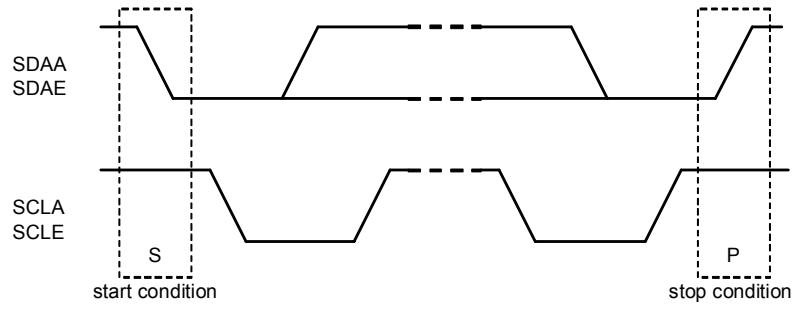


Figure 131. START and STOP Conditions

When Start condition is received again instead of Stop condition, the bus changes to Repeated Start condition. Repeated Start condition is functionally the same as Start condition.

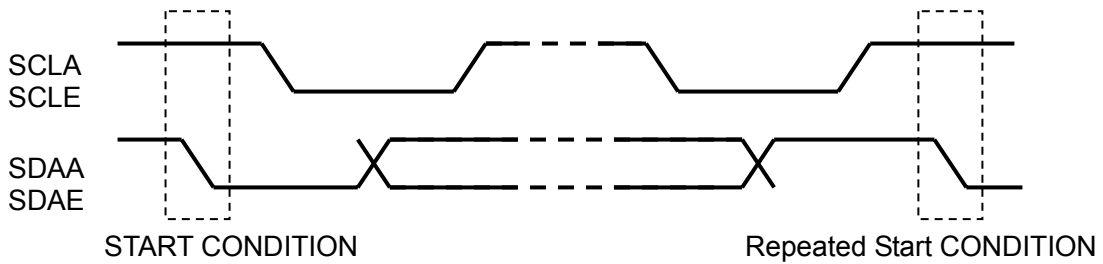


Figure 132. Repeated Start Conditions

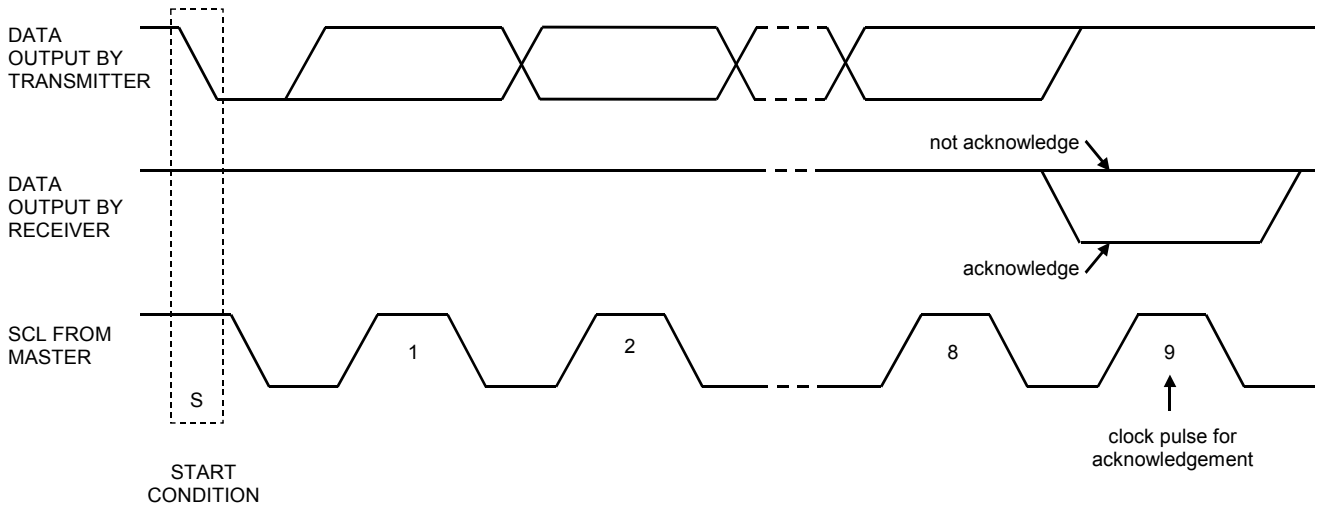


Figure 133. Acknowledge on the I²C-Bus

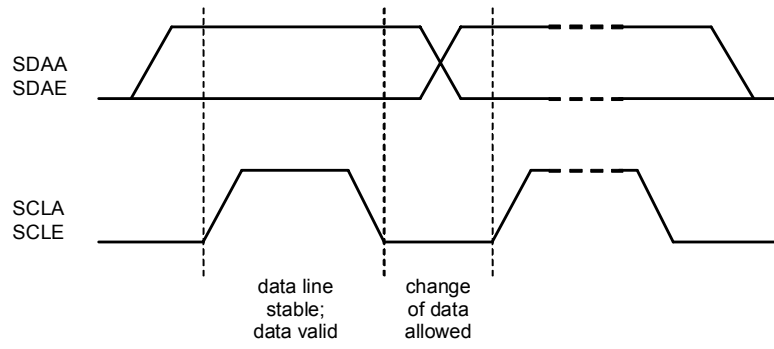


Figure 134. Bit Transfer on the I²C-Bus

■ SPI Serial Control Interface (DSP block)

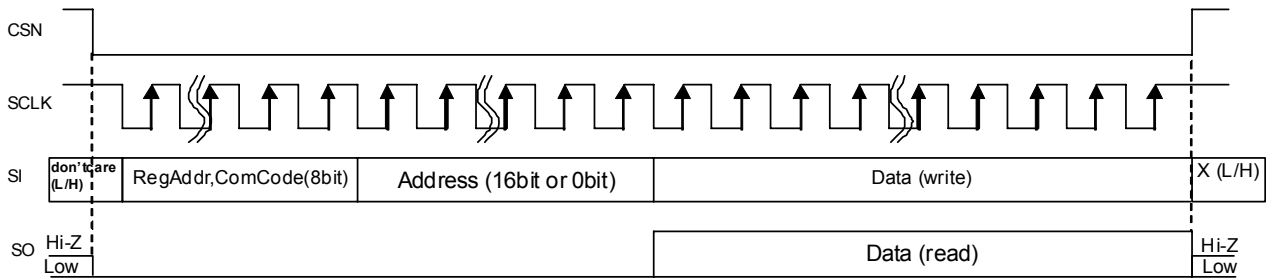
DSP block can be controlled by SPI.

1. Configuration

The access format is: Command code (8bit) + Address + Data (MSB First)

| | Bit Length | |
|--|---------------|--|
| Register address or Command code | 8 | MSB bit is R/W flag. The following 7bits indicate access area such as PRAM/ CRAM/Registers. |
| Address to be accessed | 16 or 0 | Valid only for those cases where accessed areas have addresses such as PRAM /CRAM/OFREG. When no address is assigned, there is no data. |
| Data | later section | Write or Read data |

Note 76. The address field is fixed to 0000h when writing to PRAM.



The output level of SO pin is set by SOCFG bit on CSN pin = "H".

□ Echo back

The input data of the SI pin is echoed back to the SO pin by shifting 8bit to the right.

1-1. Write Sequence 1

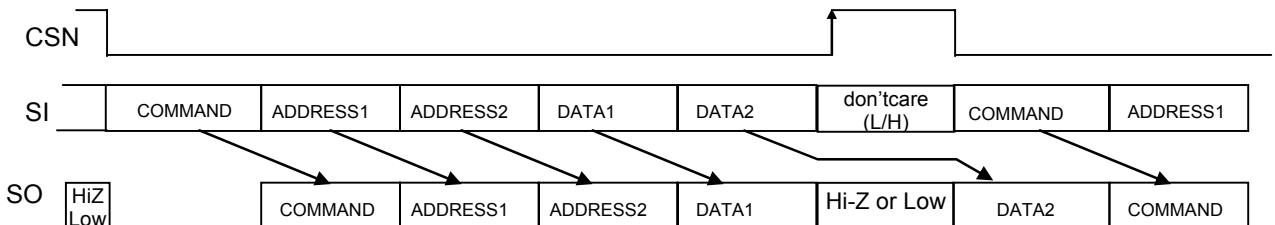
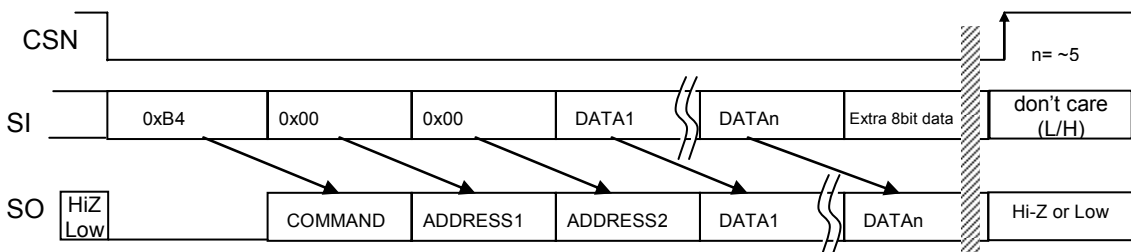


Figure 135. Echo-Back Writing 1

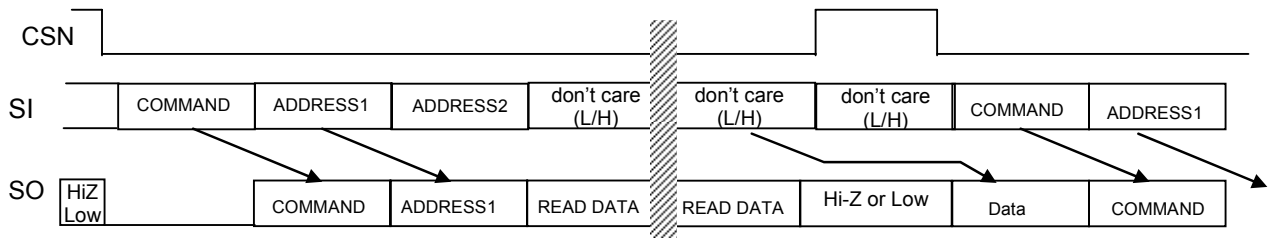
1-2 Write Sequence 2



It is possible to verify the written data by inputting extra 8bit clock. If the dummy data is more than the data length, this dummy data is written on the next address. (24bit for CRAM writing and 16bit for OFREG writing)

Figure 136. Echo-Back Writing 2

2. Read Sequence



Data of the address2 field is not echoed back in read operation. The read data on the SO pin is output after writing to the address2 field.

Figure 137. Echo-Back Mode Reading

■ Register Map (Audio block)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------------|--------|--------|--------|--------|--------|--------|---------|---------|
| 00H | Power Management 0 | 0 | 0 | PMADR | PMADL | 0 | 0 | PMPFIL | PMVCM |
| 01H | Power Management 1 | 0 | 0 | 0 | 0 | PMDAR | PMDAL | PMDRC | PMEQ |
| 02H | Power Management 2 | ADRST | 0 | 0 | 0 | MICL2 | PMMP2 | MICL1 | PMMP1 |
| 03H | PLL Mode Select 0 | FS3 | FS2 | FS1 | FS0 | PLL3 | PLL2 | PLL1 | PLL0 |
| 04H | PLL Mode Select 1 | CM1 | CM0 | BCKO | 0 | 0 | 0 | M/S | PMPLL |
| 05H | Audio I/F Format Select | 0 | 0 | 0 | SDOD | MSBS | BCKP | DIF1 | DIF0 |
| 06H | MIC Signal Select | 0 | MDIF3 | MDIF2 | MDIF1 | INR1 | INR0 | INL1 | INL0 |
| 07H | MIC Amp Gain | MGNR3 | MGNR2 | MGNR1 | MGNR0 | MGNL3 | MGNL2 | MGNL1 | MGNL0 |
| 08H | Digital MIC | 0 | 0 | PMDMR | PMDML | DCLKE | 0 | DCLKP | DMIC |
| 09H | DAC Signal Pass Select | DACSR | DACSL | DACRR | DACRL | 0 | 0 | DACR | DACL |
| 0AH | LINEOUT Power Management | 0 | 0 | 0 | LODIF | LOM | LOPS | PMRO | PMLO |
| 0BH | HP Power Management | HPTM1 | HPTM0 | 0 | 0 | LOMH | 0 | PMHPR | PMHPL |
| 0CH | Charge Pump Control | 0 | VDDTM2 | VDDTM1 | VDDTM0 | 0 | 0 | CPMODE1 | CPMODE0 |
| 0DH | SPK&RCV Power Management | THDET | 0 | TEST | PMSPK | 0 | 0 | RCVPS | PMRCV |
| 0EH | LINEOUT Volume Control | 0 | 0 | 0 | 0 | 0 | LVL2 | LVL1 | LVL0 |
| 0FH | HP Volume Control | 0 | 0 | HPG5 | HPG4 | HPG3 | HPG2 | HPG1 | HPG0 |
| 10H | SPK & RCV Volume Control | RCVG3 | RCVG2 | RCVG1 | RCVG0 | SPKG3 | SPKG2 | SPKG1 | SPKG0 |
| 11H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 12H | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| 13H | ALC Reference Select | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 14H | Digital Mixing Control | SRMXR1 | SRMXR0 | SRMXL1 | SRMXL0 | PFMXR1 | PFMXR0 | PFMXL1 | PFMXL0 |
| 15H | ALC Timer Select | FR | RFST1 | RFST0 | WTM2 | WTM1 | WTM0 | ZTM1 | ZTM0 |
| 16H | ALC Mode Control | LFST | ZELMN | LMAT1 | LMAT0 | RGAIN1 | RGAIN0 | LMTH1 | LMTH0 |
| 17H | Mode Control 0 | 0 | 0 | SDIM1 | SDIM0 | 5EQ | ADM | IVOLC | ALC |
| 18H | Mode Control 1 | 0 | OVTMB | BIV2 | BIV1 | BIV0 | SMUTE | OVTM | OVOLC |
| 19H | Digital Filter Select 0 | 0 | HPFC1 | HPFC0 | HPFAD | DASEL1 | DASEL0 | PFSDO | PFSEL |
| 1AH | Digital Filter Select 1 | GN1 | GN0 | LPF | HPF | EQ0 | FIL3 | 0 | 0 |
| 1BH | Digital Filter Select 2 | 0 | 0 | 0 | EQ5 | EQ4 | EQ3 | EQ2 | EQ1 |
| 1CH | Side Tone Volume A Control | 0 | SVAR2 | SVAR1 | SVAR0 | 0 | SVAL2 | SVAL1 | SVAL0 |
| 1DH | Lch Output Volume Control | 0 | OVL6 | OVL5 | OVL4 | OVL3 | OVL2 | OVL1 | OVL0 |
| 1EH | Rch Output Volume Control | 0 | OVR6 | OVR5 | OVR4 | OVR3 | OVR2 | OVR1 | OVR0 |
| 1FH | PCM I/F Power Management | PMMIX | PMSRBO | PMSRBI | PMPCMB | PMOSC | PMSRAO | PMSRAI | PMPCMA |
| 20H | PCM I/F Control 0 | SDOAD | 0 | MSBSA | BCKPA | LAWA1 | LAWA0 | FMTA1 | FMTA0 |
| 21H | PCM I/F Control 1 | SDOBD | 0 | MSBSB | BCKPB | LAWB1 | LAWB0 | FMTB1 | FMTB0 |
| 22H | Side Tone Volume B Control | 0 | 0 | 0 | 0 | 0 | SVB2 | SVB1 | SVB0 |
| 23H | Digital Volume B Control | 0 | BVL6 | BVL5 | BVL4 | BVL3 | BVL2 | BVL1 | BVL0 |
| 24H | Digital Volume C Control | 0 | CVL6 | CVL5 | CVL4 | CVL3 | CVL2 | CVL1 | CVL0 |
| 25H | Digital Mixing Control 0 | 0 | 0 | MX1R2 | MX1R1 | MX1R0 | MX1L2 | MX1L1 | MX1L0 |
| 26H | Digital Mixing Control 1 | 0 | 0 | MX2C1 | MX2C0 | MX2B1 | MX2B0 | MX2A1 | MX2A0 |
| 27H | Digital Mixing Control 2 | 0 | 0 | 0 | 0 | 0 | MXSB2 | MXSB1 | MXSB0 |
| 28H | Digital Mixing Control 3 | SDOR1 | SDOR0 | SDOL1 | SDOL0 | 0 | 0 | SBMX1 | SBMX0 |
| 29H | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 2AH | FIL1 Co-efficient 1 | 0 | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 2BH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 2CH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| 2DH | FIL2 Co-efficient 0 | F2A7 | F2A6 | F2A5 | F2A4 | F2A3 | F2A2 | F2A1 | F2A0 |
| 2EH | FIL2 Co-efficient 1 | 0 | 0 | F2A13 | F2A12 | F2A11 | F2A10 | F2A9 | F2A8 |
| 2FH | FIL2 Co-efficient 2 | F2B7 | F2B6 | F2B5 | F2B4 | F2B3 | F2B2 | F2B1 | F2B0 |
| 30H | FIL2 Co-efficient 3 | 0 | 0 | F2B13 | F2B12 | F2B11 | F2B10 | F2B9 | F2B8 |
| 31H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 32H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 33H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 34H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 35H | EQ Co-efficient 0 | E0A7 | E0A6 | E0A5 | E0A4 | E0A3 | E0A2 | E0A1 | E0A0 |
| 36H | EQ Co-efficient 1 | E0A15 | E0A14 | E0A13 | E0A12 | E0A11 | E0A10 | E0A9 | E0A8 |
| 37H | EQ Co-efficient 2 | E0B7 | E0B6 | E0B5 | E0B4 | E0B3 | E0B2 | E0B1 | E0B0 |
| 38H | EQ Co-efficient 3 | 0 | 0 | E0B13 | E0B12 | E0B11 | E0B10 | E0B9 | E0B8 |
| 39H | EQ Co-efficient 4 | E0C7 | E0C6 | E0C5 | E0C4 | E0C3 | E0C2 | E0C1 | E0C0 |
| 3AH | EQ Co-efficient 5 | E0C15 | E0C14 | E0C13 | E0C12 | E0C11 | E0C10 | E0C9 | E0C8 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| 3BH | E1 Co-efficient 0 | E1A7 | E1A6 | E1A5 | E1A4 | E1A3 | E1A2 | E1A1 | E1A0 |
| 3CH | E1 Co-efficient 1 | E1A15 | E1A14 | E1A13 | E1A12 | E1A11 | E1A10 | E1A9 | E1A8 |
| 3DH | E1 Co-efficient 2 | E1B7 | E1B6 | E1B5 | E1B4 | E1B3 | E1B2 | E1B1 | E1B0 |
| 3EH | E1 Co-efficient 3 | E1B15 | E1B14 | E1B13 | E1B12 | E1B11 | E1B10 | E1B9 | E1B8 |
| 3FH | E1 Co-efficient 4 | E1C7 | E1C6 | E1C5 | E1C4 | E1C3 | E1C2 | E1C1 | E1C0 |
| 40H | E1 Co-efficient 5 | E1C15 | E1C14 | E1C13 | E1C12 | E1C11 | E1C10 | E1C9 | E1C8 |
| 41H | E2 Co-efficient 0 | E2A7 | E2A6 | E2A5 | E2A4 | E2A3 | E2A2 | E2A1 | E2A0 |
| 42H | E2 Co-efficient 1 | E2A15 | E2A14 | E2A13 | E2A12 | E2A11 | E2A10 | E2A9 | E2A8 |
| 43H | E2 Co-efficient 2 | E2B7 | E2B6 | E2B5 | E2B4 | E2B3 | E2B2 | E2B1 | E2B0 |
| 44H | E2 Co-efficient 3 | E2B15 | E2B14 | E2B13 | E2B12 | E2B11 | E2B10 | E2B9 | E2B8 |
| 45H | E2 Co-efficient 4 | E2C7 | E2C6 | E2C5 | E2C4 | E2C3 | E2C2 | E2C1 | E2C0 |
| 46H | E2 Co-efficient 5 | E2C15 | E2C14 | E2C13 | E2C12 | E2C11 | E2C10 | E2C9 | E2C8 |
| 47H | E3 Co-efficient 0 | E3A7 | E3A6 | E3A5 | E3A4 | E3A3 | E3A2 | E3A1 | E3A0 |
| 48H | E3 Co-efficient 1 | E3A15 | E3A14 | E3A13 | E3A12 | E3A11 | E3A10 | E3A9 | E3A8 |
| 49H | E3 Co-efficient 2 | E3B7 | E3B6 | E3B5 | E3B4 | E3B3 | E3B2 | E3B1 | E3B0 |
| 4AH | E3 Co-efficient 3 | E3B15 | E3B14 | E3B13 | E3B12 | E3B11 | E3B10 | E3B9 | E3B8 |
| 4BH | E3 Co-efficient 4 | E3C7 | E3C6 | E3C5 | E3C4 | E3C3 | E3C2 | E3C1 | E3C0 |
| 4CH | E3 Co-efficient 5 | E3C15 | E3C14 | E3C13 | E3C12 | E3C11 | E3C10 | E3C9 | E3C8 |
| 4DH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4EH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 50H | 5band E1 Co-efficient 0 | 5E1A7 | 5E1A6 | 5E1A5 | 5E1A4 | 5E1A3 | 5E1A2 | 5E1A1 | 5E1A0 |
| 51H | 5band E1 Co-efficient 1 | 0 | 0 | 5E1A13 | 5E1A12 | 5E1A11 | 5E1A10 | 5E1A9 | 5E1A8 |
| 52H | 5band E1 Co-efficient 2 | 5E1B7 | 5E1B6 | 5E1B5 | 5E1B4 | 5E1B3 | 5E1B2 | 5E1B1 | 5E1B0 |
| 53H | 5band E1 Co-efficient 3 | 0 | 0 | 5E1B13 | 5E1B12 | 5E1B11 | 5E1B10 | 5E1B9 | 5E1B8 |
| 54H | 5band E2 Co-efficient 0 | 5E2A7 | 5E2A6 | 5E2A5 | 5E2A4 | 5E2A3 | 5E2A2 | 5E2A1 | 5E2A0 |
| 55H | 5band E2 Co-efficient 1 | 5E2A15 | 5E2A14 | 5E2A13 | 5E2A12 | 5E2A11 | 5E2A10 | 5E2A9 | 5E2A8 |
| 56H | 5band E2 Co-efficient 2 | 5E2B7 | 5E2B6 | 5E2B5 | 5E2B4 | 5E2B3 | 5E2B2 | 5E2B1 | 5E2B0 |
| 57H | 5band E2 Co-efficient 3 | 5E2B15 | 5E2B14 | 5E2B13 | 5E2B12 | 5E2B11 | 5E2B10 | 5E2B9 | 5E2B8 |
| 58H | 5band E2 Co-efficient 4 | 5E2C7 | 5E2C6 | 5E2C5 | 5E2C4 | 5E2C3 | 5E2C2 | 5E2C1 | 5E2C0 |
| 59H | 5band E2 Co-efficient 5 | 5E2C15 | 5E2C14 | 5E2C13 | 5E2C12 | 5E2C11 | 5E2C10 | 5E2C9 | 5E2C8 |
| 5AH | 5band E3 Co-efficient 0 | 5E3A7 | 5E3A6 | 5E3A5 | 5E3A4 | 5E3A3 | 5E3A2 | 5E3A1 | 5E3A0 |
| 5BH | 5band E3 Co-efficient 1 | 5E3A15 | 5E3A14 | 5E3A13 | 5E3A12 | 5E3A11 | 5E3A10 | 5E3A9 | 5E3A8 |
| 5CH | 5band E3 Co-efficient 2 | 5E3B7 | 5E3B6 | 5E3B5 | 5E3B4 | 5E3B3 | 5E3B2 | 5E3B1 | 5E3B0 |
| 5DH | 5band E3 Co-efficient 3 | 5E3B15 | 5E3B14 | 5E3B13 | 5E3B12 | 5E3B11 | 5E3B10 | 5E3B9 | 5E3B8 |
| 5EH | 5band E3 Co-efficient 4 | 5E3C7 | 5E3C6 | 5E3C5 | 5E3C4 | 5E3C3 | 5E3C2 | 5E3C1 | 5E3C0 |
| 5FH | 5band E3 Co-efficient 5 | 5E3C15 | 5E3C14 | 5E3C13 | 5E3C12 | 5E3C11 | 5E3C10 | 5E3C9 | 5E3C8 |
| 60H | 5band E4 Co-efficient 0 | 5E4A7 | 5E4A6 | 5E4A5 | 5E4A4 | 5E4A3 | 5E4A2 | 5E4A1 | 5E4A0 |
| 61H | 5band E4 Co-efficient 1 | 5E4A15 | 5E4A14 | 5E4A13 | 5E4A12 | 5E4A11 | 5E4A10 | 5E4A9 | 5E4A8 |
| 62H | 5band E4 Co-efficient 2 | 5E4B7 | 5E4B6 | 5E4B5 | 5E4B4 | 5E4B3 | 5E4B2 | 5E4B1 | 5E4B0 |
| 63H | 5band E4 Co-efficient 3 | 5E4B15 | 5E4B14 | 5E4B13 | 5E4B12 | 5E4B11 | 5E4B10 | 5E4B9 | 5E4B8 |
| 64H | 5band E4 Co-efficient 4 | 5E4C7 | 5E4C6 | 5E4C5 | 5E4C4 | 5E4C3 | 5E4C2 | 5E4C1 | 5E4C0 |
| 65H | 5band E4 Co-efficient 5 | 5E4C15 | 5E4C14 | 5E4C13 | 5E4C12 | 5E4C11 | 5E4C10 | 5E4C9 | 5E4C8 |
| 66H | 5band E5 Co-efficient 0 | 5E5A7 | 5E5A6 | 5E5A5 | 5E5A4 | 5E5A3 | 5E5A2 | 5E5A1 | 5E5A0 |
| 67H | 5band E5 Co-efficient 1 | 0 | 0 | 5E5A13 | 5E5A12 | 5E5A11 | 5E5A10 | 5E5A9 | 5E5A8 |
| 68H | 5band E5 Co-efficient 2 | 5E5B7 | 5E5B6 | 5E5B5 | 5E5B4 | 5E5B3 | 5E5B2 | 5E5B1 | 5E5B0 |
| 69H | 5band E5 Co-efficient 3 | 0 | 0 | 5E5B13 | 5E5B12 | 5E5B11 | 5E5B10 | 5E5B9 | 5E5B8 |
| 6AH | 5band EQ1 Gain | 0 | 0 | EQ1G5 | EQ1G4 | EQ1G3 | EQ1G2 | EQ1G1 | EQ1G0 |
| 6BH | 5band EQ2 Gain | 0 | 0 | EQ2G5 | EQ2G4 | EQ2G3 | EQ2G2 | EQ2G1 | EQ2G0 |
| 6CH | 5band EQ3 Gain | 0 | 0 | EQ3G5 | EQ3G4 | EQ3G3 | EQ3G2 | EQ3G1 | EQ3G0 |
| 6DH | 5band EQ4 Gain | 0 | 0 | EQ4G5 | EQ4G4 | EQ4G3 | EQ4G2 | EQ4G1 | EQ4G0 |
| 6EH | 5band EQ5 Gain | 0 | 0 | EQ5G5 | EQ5G4 | EQ5G3 | EQ5G2 | EQ5G1 | EQ5G0 |
| 6FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|----------|----------|----------|------------|---------|------------|------------|------------|
| 70H | DRC Mode Control | 0 | DLMAT2 | DLMAT1 | DLMAT0 | DRGAIN1 | DRGAIN0 | DRCC1 | DRCC0 |
| 71H | NS Control | 0 | 0 | DRCM1 | DRCM0 | 0 | NSLPF | NSHPPF | NSCE |
| 72H | NS Gain & ATT Control | 0 | NSGAIN2 | NSGAIN1 | NSGAIN0 | 0 | NSATT2 | NSATT1 | NSATTO |
| 73H | NS On Level | NSIAF1 | NSIAF0 | 0 | NSTHL4 | NSTHL3 | NSTHL2 | NSTHL1 | NSTHL0 |
| 74H | NS Off Level | NSOAF1 | NSOAF0 | 0 | NSTHH 4 | NSTHH3 | NSTHH 2 | NSTHH 1 | NSTHH 0 |
| 75H | NS Reference Select | 0 | 0 | 0 | 0 | NSREF3 | NSREF2 | NSREF1 | NSREF0 |
| 76H | NS LPF Co-efficient 0 | NSLA7 | NSLA6 | NSLA5 | NSLA4 | NSLA3 | NSLA2 | NSLA1 | NSLA0 |
| 77H | NS LPF Co-efficient 1 | 0 | 0 | NSLA13 | NSLA12 | NSLA11 | NSLA10 | NSLA9 | NSLA8 |
| 78H | NS LPF Co-efficient 2 | NSLB7 | NSLB6 | NSLB5 | NSLB4 | NSLB3 | NSLB2 | NSLB1 | NSLB0 |
| 79H | NS LPF Co-efficient 3 | 0 | 0 | NSLB13 | NSLB12 | NSLB11 | NSLB10 | NSLB9 | NSLB8 |
| 7AH | NS HPF Co-efficient 0 | NSHA7 | NSHA6 | NSHA5 | NSHA4 | NSHA3 | NSHA2 | NSHA1 | NSHA0 |
| 7BH | NS HPF Co-efficient 1 | 0 | 0 | NSHA13 | NSHA12 | NSHA11 | NSHA10 | NSHA9 | NSHA8 |
| 7CH | NS HPF Co-efficient 2 | NSHB7 | NSHB6 | NSHB5 | NSHB4 | NSHB3 | NSHB2 | NSHB1 | NSHB0 |
| 7DH | NS HPF Co-efficient 3 | 0 | 0 | NSHB13 | NSHB12 | NSHB11 | NSHB10 | NSHB9 | NSHB8 |
| 7EH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 80H | DVLC Filter Select | DLLPF1 | DLLPF0 | DMHPF1 | DMHPF0 | DMLPF1 | DMLPF0 | DHHPF1 | DHHPF0 |
| 81H | DVLC Mode Control | DVRGAIN2 | DVRGAIN1 | DVRGAIN0 | DVLMAT2 | DVLMAT1 | DVLMAT0 | DAF1 | DAF0 |
| 82H | DVLCL Curve X1 | 0 | 0 | VL1X5 | VL1X4 | VL1X3 | VL1X2 | VL1X1 | VL1X0 |
| 83H | DVLCL Curve Y1 | 0 | 0 | VL1Y5 | VL1Y4 | VL1Y3 | VL1Y2 | VL1Y1 | VL1Y0 |
| 84H | DVLCL Curve X2 | 0 | 0 | VL2X5 | VL2X4 | VL2X3 | VL2X2 | VL2X1 | VL2X0 |
| 85H | DVLCL Curve Y2 | 0 | 0 | VL2Y5 | VL2Y4 | VL2Y3 | VL2Y2 | VL2Y1 | VL2Y0 |
| 86H | DVLCL Curve X3 | 0 | 0 | 0 | VL3X4 | VL3X3 | VL3X2 | VL3X1 | VL3X0 |
| 87H | DVLCL Curve Y3 | 0 | 0 | 0 | VL3Y4 | VL3Y3 | VL3Y2 | VL3Y1 | VL3Y0 |
| 88H | DVLCL Slope 1 | 0 | L1G6 | L1G5 | L1G4 | L1G3 | L1G2 | L1G1 | L1G0 |
| 89H | DVLCL Slope 2 | 0 | L2G6 | L2G5 | L2G4 | L2G3 | L2G2 | L2G1 | L2G0 |
| 8AH | DVLCL Slope 3 | 0 | L3G6 | L3G5 | L3G4 | L3G3 | L3G2 | L3G1 | L3G0 |
| 8BH | DVLCL Slope 4 | 0 | L4G6 | L4G5 | L4G4 | L4G3 | L4G2 | L4G1 | L4G0 |
| 8CH | DVLCM Curve X1 | 0 | 0 | VM1X5 | VM1X4 | VM1X3 | VM1X2 | VM1X1 | VM1X0 |
| 8DH | DVLCM Curve Y1 | 0 | 0 | VM1Y5 | VM1Y4 | VM1Y3 | VM1Y2 | VM1Y1 | VM1Y0 |
| 8EH | DVLCM Curve X2 | 0 | 0 | VM2X5 | VM2X4 | VM2X3 | VM2X2 | VM2X1 | VM2X0 |
| 8FH | DVLCM Curve Y2 | 0 | 0 | VM2Y5 | VM2Y4 | VM2Y3 | VM2Y2 | VM2Y1 | VM2Y0 |
| 90H | DVLCM Curve X3 | 0 | 0 | 0 | VM3X4 | VM3X3 | VM3X2 | VM3X1 | VM3X0 |
| 91H | DVLCM Curve Y3 | 0 | 0 | 0 | VM3Y4 | VM3Y3 | VM3Y2 | VM3Y1 | VM3Y0 |
| 92H | DVLCM Slope 1 | 0 | M1G6 | M1G5 | M1G4 | M1G3 | M1G2 | M1G1 | M1G0 |
| 93H | DVLCM Slope 2 | 0 | M2G6 | M2G5 | M2G4 | M2G3 | M2G2 | M2G1 | M2G0 |
| 94H | DVLCM Slope 3 | 0 | M3G6 | M3G5 | M3G4 | M3G3 | M3G2 | M3G1 | M3G0 |
| 95H | DVLCM Slope 4 | 0 | M4G6 | M4G5 | M4G4 | M4G3 | M4G2 | M4G1 | M4G0 |
| 96H | DVLCH Curve X1 | 0 | 0 | VH1X5 | VH1X4 | VH1X3 | VH1X2 | VH1X1 | VH1X0 |
| 97H | DVLCH Curve Y1 | 0 | 0 | VH1Y5 | VH1Y4 | VH1Y3 | VH1Y2 | VH1Y1 | VH1Y0 |
| 98H | DVLCH Curve X2 | 0 | 0 | VH2X5 | VH2X4 | VH2X3 | VH2X2 | VH2X1 | VH2X0 |
| 99H | DVLCH Curve Y2 | 0 | 0 | VH2Y5 | VH2Y4 | VH2Y3 | VH2Y2 | VH2Y1 | VH2Y0 |
| 9AH | DVLCH Curve X3 | 0 | 0 | 0 | VH3X4 | VH3X3 | VH3X2 | VH3X1 | VH3X0 |
| 9BH | DVLCH Curve Y3 | 0 | 0 | 0 | VH3Y4 | VH3Y3 | VH3Y2 | VH3Y1 | VH3Y0 |
| 9CH | DVLCH Slope 1 | 0 | H1G6 | H1G5 | H1G4 | H1G3 | H1G2 | H1G1 | H1G0 |
| 9DH | DVLCH Slope 2 | 0 | H2G6 | H2G5 | H2G4 | H2G3 | H2G2 | H2G1 | H2G0 |
| 9EH | DVLCH Slope 3 | 0 | H3G6 | H3G5 | H3G4 | H3G3 | H3G2 | H3G1 | H3G0 |
| 9FH | DVLCH Slope 4 | 0 | H4G6 | H4G5 | H4G4 | H4G3 | H4G2 | H4G1 | H4G0 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|-------|-------|--------|--------|--------|--------|-------|-------|
| A0H | DVLCL LPF Co-efficient 0 | DLLA7 | DLLA6 | DLLA5 | DLLA4 | DLLA3 | DLLA2 | DLLA1 | DLLA0 |
| A1H | DVLCL LPF Co-efficient 1 | 0 | 0 | DLLA13 | DLLA12 | DLLA11 | DLLA10 | DLLA9 | DLLA8 |
| A2H | DVLCL LPF Co-efficient 2 | DLLB7 | DLLB6 | DLLB5 | DLLB4 | DLLB3 | DLLB2 | DLLB1 | DLLB0 |
| A3H | DVLCL LPF Co-efficient 3 | 0 | 0 | DLLB13 | DLLB12 | DLLB11 | DLLB10 | DLLB9 | DLLB8 |
| A4H | DVLCM HPF Co-efficient 0 | DMHA7 | DMHA6 | DMHA5 | DMHA4 | DMHA3 | DMHA2 | DMHA1 | DMHA0 |
| A5H | DVLCM HPF Co-efficient 1 | 0 | 0 | DMHA13 | DMHA12 | DMHA11 | DMHA10 | DMHA9 | DMHA8 |
| A6H | DVLCM HPF Co-efficient 2 | DMHB7 | DMHB6 | DMHB5 | DMHB4 | DMHB3 | DMHB2 | DMHB1 | DMHB0 |
| A7H | DVLCM HPF Co-efficient 3 | 0 | 0 | DMHB13 | DMHB12 | DMHB11 | DMHB10 | DMHB9 | DMHB8 |
| A8H | DVLCM LPF Co-efficient 0 | DMLA7 | DMLA6 | DMLA5 | DMLA4 | DMLA3 | DMLA2 | DMLA1 | DMLA0 |
| A9H | DVLCM LPF Co-efficient 1 | 0 | 0 | DMLA13 | DMLA12 | DMLA11 | DMLA10 | DMLA9 | DMLA8 |
| AAH | DVLCM LPF Co-efficient 2 | DMLB7 | DMLB6 | DMLB5 | DMLB4 | DMLB3 | DMLB2 | DMLB1 | DMLB0 |
| ABH | DVLCM LPF Co-efficient 3 | 0 | 0 | DMLB13 | DMLB12 | DMLB11 | DMLB10 | DMLB9 | DMLB8 |
| ACH | DVLCH HPF Co-efficient 0 | DHHA7 | DHHA6 | DHHA5 | DHHA4 | DHHA3 | DHHA2 | DHHA1 | DHHA0 |
| ADH | DVLCH HPF Co-efficient 1 | 0 | 0 | DHHA13 | DHHA12 | DHHA11 | DHHA10 | DHHA9 | DHHA8 |
| AEH | DVLCH HPF Co-efficient 2 | DHHB7 | DHHB6 | DHHB5 | DHHB4 | DHHB3 | DHHB2 | DHHB1 | DHHB0 |
| AFH | DVLCH HPF Co-efficient 3 | 0 | 0 | DHHB13 | DHHB12 | DHHB11 | DHHB10 | DHHB9 | DHHB8 |

Note 77. PDNA pin = "L" resets the registers to their default values.

Note 78. The bits defined as 0 must contain a "0" value.

Note 79. For Addresses B0H to FFH, data must not be written.

■ Register Definition

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|-------|-------|----|----|--------|-------|
| 00H | Power Management 0 | 0 | 0 | PMADR | PMADL | 0 | 0 | PMPFIL | PMVCM |
| | R/W | R | R | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMVCM: VCOM Power Management

0: Power down (default)

1: Power up

When any blocks are powered-up, the PMVCM bit must be set to “1”. PMVCM bit can be set to “0” only when all power management bits are “0”.

PMPFIL: Programmable Filter Block Power Management

0: Power down (default)

1: Power up

PMADL: MIC-Amp Lch & ADC Lch Power Management

0: Power down (default)

1: Power up

When the PMADL(PMDML) or PMADR(PMDMR) bit is changed from “0” to “1”, the digital initialization cycle ($1059/f_s=24\text{ms}$ @ 44.1kHz, ADRST bit = “0”) starts. After initializing, digital data of the ADC is output.

PMADR: MIC-Amp Rch & ADC Rch Power Management

0: Power down (default)

1: Power up

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDNA pin is “L”, Audio blocks are powered-down regardless of setting of this address. In this case, CODEC register is initialized to the default value.

When all power management bits are “0”, Audio blocks are powered-down. The register values remain unchanged. Power supply current is 50 μA (typ) in this case. For fully shut down (typ. 1 μA), PDNA pin should be “L”.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|----|----|-------|-------|-------|------|
| 01H | Power Management 1 | 0 | 0 | 0 | 0 | PMDAR | PMDAL | PMDRC | PMEQ |
| | R/W | R | R | R | R | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMEQ: 5-band Parametric Equalizer Block Power Management

- 0: Power down (default)
- 1: Power up

PMDRC: Dynamic Range Control Block Power Management

- 0: Power down (default)
- 1: Power up

PMDAL: DAC Lch Power Management

- 0: Power down (default)
- 1: Power up

PMDAR: DAC Rch Power Management

- 0: Power down (default)
- 1: Power up

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDNA pin is “L”, all blocks are powered-down regardless of setting of this address. In this case, register is initialized to the default value.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|-------|----|----|----|-------|-------|-------|-------|
| 02H | Power Management 1 | ADRST | 0 | 0 | 0 | MICL2 | PMMP2 | MICL1 | PMMP1 |
| | R/W | R/W | R | R | R | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMMP1: MPWR1 pin Power Management

- 0: Power down: Hi-Z (default)
- 1: Power up

MICL1: MIC Power (MPWR1 pin) Output Level select

Default “0”, typ. 2.5V ([Table 21](#))

PMMP2: MPWR2 pin Power Management

- 0: Power down: Hi-Z (default)
- 1: Power up

MICL2: MIC Power (MPWR2 pin) Output Level Select

Default “0”, typ. 2.5V ([Table 21](#))

ADRST: ADC Initialization Cycle Setting

- 0: 1059/fs (default)
- 1: 267/fs

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|-----|-----|-----|-----|------|------|------|------|
| 03H | PLL Mode Select 0 | FS3 | FS2 | FS1 | FS0 | PLL3 | PLL2 | PLL1 | PLL0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

PLL3-0: PLL Reference Clock Select ([Table 5](#))

Default: "0110" (MCKI pin, 12MHz)

FS3-0: Sampling Frequency Select ([Table 6](#), [Table 10](#) and [Table 13](#))

Default: "1111" (fs=44.1kHz)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|-----|-----|------|----|----|----|-----|-------|
| 04H | PLL Mode Select 1 | CM1 | CM0 | BCKO | 0 | 0 | 0 | M/S | PMPLL |
| | R/W | R/W | R/W | R/W | R | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPLL: PLL Power Management

0: EXT Mode and Power Down (default)

1: PLL Mode and Power up

M/S: Master / Slave Mode Select

0: Slave Mode (default)

1: Master Mode

BCKO: BICK Output Frequency Select at Master Mode ([Table 8](#))

CM1-0: MCKI Frequency Select at EXT Mode ([Table 9](#) and [Table 12](#))

Default: "00" (256fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|----|----|----|------|------|------|------|------|
| 05H | Audio I/F Format Select | 0 | 0 | 0 | SDOD | MSBS | BCKP | DIF1 | DIF0 |
| | R/W | R | R | R | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DIF1-0: Audio Interface Format ([Table 17](#))

Default: "10" (24bit Left justified)

BCKP: BICK Polarity at DSP Mode ([Table 18](#))

"0": SDTO is output by the rising edge ("↑") of BICK and SDTI is latched by the falling edge ("↓"). (default)

"1": SDTO is output by the falling edge ("↓") of BICK and SDTI is latched by the rising edge ("↑").

MSBS: LRCK Phase at DSP Mode ([Table 18](#))

"0": The rising edge ("↑") of LRCK is half clock of BICK before the channel change. (default)

"1": The rising edge ("↑") of LRCK is one clock of BICK before the channel change.

SDOD: SDTO Disable ([Table 82](#))

"0": Enable (default)

"1": Disable ("L")

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|-------|-------|-------|------|------|------|------|
| 06H | MIC Signal Select | 0 | MDIF3 | MDIF2 | MDIF1 | INR1 | INR0 | INL1 | INL0 |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INL1-0: MIC-Amp Lch Input Source Select (Table 19)
Default: "00" (LIN1)

INR1-0: MIC-Amp Rch Input Source Select (Table 19)
Default: "00" (RIN1)

MDIF1: Line1 Input Type Select
0: Single-ended input (LIN1/RIN1 pins: default)
1: Full-differential input (IN1+/IN1- pins)

MDIF2: Line2 Input Type Select
0: Single-ended input (LIN2/RIN2 pins: default)
1: Full-differential input (IN2-/IN2+ pins)

MDIF3: Line3 Input Type Select
0: Single-ended input (LIN3/RIN3 pins: default)
1: Full-differential input (IN3+/IN3- pins)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 07H | MIC Amp Gain | MGNR3 | MGNR2 | MGNR1 | MGNR0 | MGNL3 | MGNL2 | MGNL1 | MGNL0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

MGNL3-0: MIC-Amp Lch Gain Control (Table 20)
Default: "0101" (0dB)

MGNR3-0: MIC-Amp Rch Gain Control (Table 20)
Default: "0101" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|-------|-------|-------|----|-------|------|
| 08H | Digital MIC | 0 | 0 | PMDMR | PMDML | DCLKE | 0 | DCLKP | DMIC |
| | R/W | R | R | R/W | R/W | R/W | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge ("↑"). (default)
1: Lch data is latched on the DMCLK falling edge ("↓").

DCLKE: DMCLK pin Output Clock Control
0: "L" Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 76)
Default: "0"

When DMIC bit is "1", these registers are enabled. ADC digital block is powered-down by PMDML = PMDMR bits = "0" when selecting a digital microphone input (DMIC bit = "1").

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|-------|-------|-------|-------|----|----|------|------|
| 09H | DAC Signal Pass Select | DACSR | DACSL | DACRR | DACRL | 0 | 0 | DACR | DACL |
| | R/W | R/W | R/W | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DACL: Switch Control from DAC Lch to LOUT

0: OFF (default)

1: ON

DACR: Switch Control from DAC Rch to ROUT

0: OFF (default)

1: ON

DACRL: Switch Control from DAC Lch to RCV-Amp

0: OFF (default)

1: ON

DACRR: Switch Control from DAC Rch to RCV-Amp

0: OFF (default)

1: ON

DACSL: Switch Control from DAC Lch to SPK-Amp

0: OFF (default)

1: ON

DACSR: Switch Control from DAC Rch to SPK-Amp

0: OFF (default)

1: ON

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|----|----|-------|-----|------|------|------|
| 0AH | LINEOUT Power Management | 0 | 0 | 0 | LODIF | LOM | LOPS | PMRO | PMLO |
| | R/W | R | R | R | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMLO: LOUT Power Management

- 0: Power down (default)
- 1: Power up

PMRO: ROUT Power Management

- 0: Power down (default)
- 1: Power up

LOPS: LOUT/ROUT Power Management

- 0: Normal Operation (default)
- 1: Power Save Mode

LOM: Mono Mixing from DAC to LOUT/ROUT

- 0: Stereo Mixing (default)
- 1: Mono Mixing

LODIF: Lineout Mode Select

- 0: Stereo Single-ended Line Output (LOUT/ROUT pins) (default)
- 1: Mono Full-differential Output (LOP/LON pins)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|-------|-------|----|----|------|----|-------|-------|
| 0BH | HP Power Management | HPTM1 | HPTM0 | 0 | 0 | LOMH | 0 | PMHPR | PMHPL |
| | R/W | R/W | R/W | R | R | R/W | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMHPL: HPL Power Management

- 0: Power down (default)
- 1: Power up

PMHPR: HPR Power Management

- 0: Power down (default)
- 1: Power up

LOMH: Mono Mixing from DAC to HPL/HPR

- 0: Stereo Mixing (default)
- 1: Mono Mixing

HPTM1-0: Headphone-Amp Volume Zero Crossing Timeout Period ([Table 106](#))

- Default: "00" (128/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|----|--------|--------|--------|----|----|---------|---------|
| 0CH | Charge Pump Control | 0 | VDDTM2 | VDDTM1 | VDDTM0 | 0 | 0 | CPMODE1 | CPMODE0 |
| | R/W | R | R/W | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

CPMODE1-0: Charge-pump Mode Setting (Table 107)

Default: "00" (Automatic Switching)

VDDTM2-0: VDD Mode Waiting Period (Table 108)

Default: "101" (32768/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------------|-------|----|------|-------|----|----|-------|-------|
| 0DH | SPK & RCV Power Management | THDET | 0 | TEST | PMSPK | 0 | 0 | RCVPS | PMRCV |
| | R/W | R | R | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMRCV: Receiver-Amp Power Management

0: Power down (default)

1: Power up

RCVPS: Receiver-Amp Power Save Mode

0: Normal Operation (default)

1: Power Save Mode

PMSPK: Speaker-Amp Power Management

0: Power down (default)

1: Power up

TEST: Device TEST mode Enable.

0: Normal operation (default)

1: TEST mode

TEST bit must be always "0".

THDET: Thermal Shutdown Detection

0: Normal Operation (default)

1: Thermal Shutdown status

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|----|----|----|----|----|------|------|------|
| 0EH | LINEOUT Volume Control | 0 | 0 | 0 | 0 | 0 | LVL2 | LVL1 | LVL0 |
| | R/W | R | R | R | R | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

LVL2-0: LINEOUT Volume Control (Table 100)

Default: "3H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|------|------|------|------|------|------|
| 0FH | HP Volume Control | 0 | 0 | HPG5 | HPG4 | HPG3 | HPG2 | HPG1 | HPG0 |
| | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

HPG5-0: Headphone Volume Control ([Table 105](#))

Default: "23H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 10H | SPK & RCV Volume Control | RCVG3 | RCVG2 | RCVG1 | RCVG0 | SPKG3 | SPKG2 | SPKG1 | SPKG0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |

SPKG3-0: Speaker Volume Control ([Table 110](#))

Default: "BH" (0dB)

RCVG3-0: Receiver Volume Control ([Table 103](#))

Default: "BH" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|------|------|------|------|------|------|------|------|
| 11H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 12H | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level ([Table 36](#))

Default: "91H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|------|------|------|------|------|------|------|------|
| 13H | ALC Reference Select | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

REF7-0: Reference Value at ALC Recovery Operation (Recording); 0.375dB step, 242 Level ([Table 32](#))

Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 14H | Digital Mixing Control | SRMXR1 | SRMXR0 | SRMXL1 | SRMXL0 | PFMXR1 | PFMXR0 | PFMXL1 | PFMXL0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PFMXL1-0: 5-band EQ Lch Input Mixing 1 ([Table 84](#))

Default: "00" (SDTI)

PFMXR1-0: 5-band EQ Rch Input Mixing 1 ([Table 85](#))

Default: "00" (SDTI)

SRMXL1-0: 5-band EQ Lch Input Mixing 2 ([Table 86](#))

Default: "00" (SDTI)

SRMXR1-0: 5-band EQ Rch Input Mixing 2 ([Table 87](#))

Default: "00" (SDTI)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|-----|-------|-------|------|------|------|------|------|
| 15H | ALC Timer Select | FR | RFST1 | RFST0 | WTM2 | WTM1 | WTM0 | ZTM1 | ZTM0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period ([Table 29](#))

Default: "00" (128/fs)

WTM2-0: ALC Recovery Waiting Period ([Table 30](#))

Default: "000" (128/fs)

RFST1-0: ALC Fast recovery Speed ([Table 33](#))

Default: "00" (4times)

FR: Fast recovery Enable

0: Enable (default)

1: Disable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|------|-------|-------|-------|--------|--------|-------|-------|
| 16H | ALC Mode Control | LFST | ZELMN | LMAT1 | LMAT0 | RGAIN1 | RGAIN0 | LMTH1 | LMTH0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level ([Table 27](#))

Default: "00"

RGAIN1-0: ALC Recovery GAIN Step ([Table 31](#))

Default: "00"

LMAT1-0: ALC Limiter ATT Step ([Table 28](#))

Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation

0: Enable (default)

1: Disable

LFST: ALC Limiter operation when the output level exceeds FS(full-scale) level.

0: The volume is changed at zero crossing or zero crossing time out (default)

1: When output of ALC is larger than FS, IVL/IVR values are changed immediately (1/fs).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|-------|-------|-----|-----|-------|-----|
| 17H | Mode Control 0 | 0 | 0 | SDIM1 | SDIM0 | 5EQ | ADM | IVOLC | ALC |
| | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

ALC: ALC Enable

0: ALC Disable (default)

1: ALC Enable

IVOLC: Input Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

ADM: Mono Recording (Table 78)

0: Stereo (default)

1: Mono: (L+R)/2

5EQ: Select 5-Band Equalizer

0: OFF (default)

1: ON

SDIM1-0: SDTI Input Signal Select (Table 83)

Default: "00" (L=Lch, R=Rch)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|-------|------|------|------|-------|------|-------|
| 18H | Mode Control 0 | 0 | OVTMB | BIV2 | BIV1 | BIV0 | SMUTE | OVTM | OVOLC |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

OVOLC: Output Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When OVOLC bit = "1", OVL6-0 bits control both Lch and Rch volume level, while register values of OVL6-0 bits are not written to OVR6-0 bits. When OVOLC bit = "0", OVL6-0 bits control Lch level and OVR6-0 bits control Rch level, respectively.

OVTM: Digital Volume Transition Time Setting

0: 128/fs

1: 256/fs (default)

This is the transition time between OVL/R6-0 bits = 00H and 7FH.

SMUTE: Soft Mute Control

0: Normal Operation (default)

1: DAC outputs soft-muted

BIV2-0: SDTIB Input Volume Control (Table 74)

Default: "0H" (0dB)

OVTMB: Digital Volume Control (DATT-B and DATT-C) Transition Time Setting

0: 128/fs

1: 256/fs (default)

This is the transition time between BVL6-0 bits or CVL6-0 bits = 00H and 7FH.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|----|-------|-------|-------|--------|--------|-------|-------|
| 19H | Digital Filter Select 0 | 0 | HPFC1 | HPFC0 | HPFAD | DASEL1 | DASEL0 | PFSDO | PFSEL |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

PFSEL: Signal Select of Programmable Filter Block ([Table 77](#))

- 0: ADC Output Data (default)
- 1: SDTI Input Data

PFSDO: SDTO Output and SVOLA Input Signal Select ([Table 79](#))

- 0: ADC (+1st HPF) Output
- 1: Programmable Filter Output (default)

DASEL1-0: DAC Input Signal Select ([Table 88](#))

Default: "00" (L= DATT-A Lch, R= DATT-A Rch)

HPFAD: HPF1 Control of ADC

0: OFF

1: ON (default)

When HPFAD bit is "1", the settings of HPFC1-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).

When PMADL bit = "1" or PMADR bit = "1", set HPFAD bit to "1".

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) ([Table 37](#))

Default: "00" (3.4Hz @ fs = 44.1kHz)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|-----|-----|-----|-----|-----|------|----|----|
| 1AH | Digital Filter Select 1 | GN1 | GN0 | LPF | HPF | EQ0 | FIL3 | 0 | 0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R | R |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When FIL3 bit is “1”, the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is “0”, FIL3 block is OFF (MUTE).

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ0 bit is “1”, the settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit is “0”, EQ0 block is through (0dB).

HPF: HPF Coefficient Setting Enable

0: Disable (default)

1: Enable

When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable

0: Disable (default)

1: Enable

When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, LPF block is through (0dB).

GN1-0: Gain Select at GAIN block ([Table 26](#))

Default: “00” (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|----|----|----|----|----|-----|-----|-----|
| 1BH | Digital Filter Select 2 | 0 | 0 | 0 | 0 | 0 | EQ3 | EQ2 | EQ1 |
| | R/W | R | R | R | R | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EQ1: Equalizer 1 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ1 bit is “1”, the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is “0”, EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ2 bit is “1”, the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is “0”, EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ3 bit is “1”, the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is “0”, EQ3 block is through (0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|---------------------|----|-------|-------|-------|----|-------|-------|-------|
| 1CH | Side Tone A Control | 0 | SVAR2 | SVAR1 | SVAR0 | 0 | SVAL2 | SVAL1 | SVAL0 |
| R/W | | R | R/W | R/W | R/W | R | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SVAL2-0, SVAR2-0: Side Tone Volume A (SVOLA) (Table 38)

Default: "000" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|---------------------------|----|------|------|------|------|------|------|------|
| 1DH | Lch Output Volume Control | 0 | OVL6 | OVL5 | OVL4 | OVL3 | OVL2 | OVL1 | OVL0 |
| 1EH | Rch Output Volume Control | 0 | OVR6 | OVR5 | OVR4 | OVR3 | OVR2 | OVR1 | OVR0 |
| R/W | | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

OVL6-0, OVR6-0: Output Digital Volume (Table 67)

Default: "0CH" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------------|-------|--------|--------|--------|-------|--------|--------|--------|
| 1FH | PCM I/F Power Management | PMMIX | PMSRBO | PMSRBI | PMPCMB | PMOSC | PMSRAO | PMSRAI | PMPCMA |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPCMA: PCM I/F A Power Management

0: Power down (default)

1: Power up

PMSRAI: SRC AI Power Management

0: Power down (default)

1: Power up

PMSRAO: SRC AO Power Management

0: Power down (default)

1: Power up

PMOSC: Internal Oscillator Power Management

0: Power down (default)

1: Power up

PMPCMB: PCM I/F B Power Management

0: Power down (default)

1: Power up

PMSRBI: SRC BI Power Management

0: Power down (default)

1: Power up

PMSRBO: SRC BO Power Management

0: Power down (default)

1: Power up

PMMIX: MIX1 Block Power Management

0: Power down (default)

1: Power up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|-------|----|-------|-------|-------|-------|-------|-------|
| 20H | PCM I/F Control 0 | SDOAD | 0 | MSBSA | BCKPA | LAWA1 | LAWA0 | FMTA1 | FMTA0 |
| | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FMTA1-0: PCM I/F A Format (Table 116)

Default: "00" (Mode 0)

LAWA1-0: PCM I/F A Mode (Table 114)

Default: "00" (Mode 0)

BCKPA: P BICKA Polarity of PCM I/F A (Table 118)

"0": SDTOA is output by the rising edge ("↑") of BICKA and SDTIA is latched by the falling edge ("↓"). (default)

"1": SDTOA is output by the falling edge ("↓") of BICKA and SDTIA is latched by the rising edge ("↑").

MSBSA: SYNCA Phase of PCM I/F A (Table 118)

"0": The rising edge ("↑") of SYNCA is half clock of BICKA before the channel change. (default)

"1": The rising edge ("↑") of SYNCA is one clock of BICKA before the channel change.

SDOAD: SDTOA Disable (Table 95)

"0": Enable (default)

"1": Disable ("L")

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|-------|----|-------|-------|-------|-------|-------|-------|
| 21H | PCM I/F Control 1 | SDOBD | 0 | MSBSB | BCKPB | LAWB1 | LAWB0 | FMTB1 | FMTB0 |
| | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FMTB1-0: PCM I/F B Format (Table 117)

Default: "00" (Mode 0)

LAWB1-0: PCM I/F B Mode (Table 115)

Default: "00" (Mode 0)

BCKPB: BICKB Polarity of PCM I/F B (Table 119)

"0": SDTOB is output by the rising edge ("↑") of BICKB and SDTIB is latched by the falling edge ("↓"). (default)

"1": SDTOB is output by the falling edge ("↓") of BICKB and SDTIB is latched by the rising edge ("↑").

MSBSB: SYNCB Phase of PCM I/F B (Table 119)

"0": The rising edge ("↑") of SYNCB is half clock of BICKB before the channel change. (default)

"1": The rising edge ("↑") of SYNCB is one clock of BICKB before the channel change.

SDOBD: SDTOB Disable (Table 97)

"0": Enable (default)

"1": Disable ("L")

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------------|----|----|----|----|----|------|------|------|
| 22H | Side Tone Volume B Control | 0 | 0 | 0 | 0 | 0 | SVB2 | SVB1 | SVB0 |
| | R/W | R | R | R | R | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SVB2-0: Side Tone Volume B (Table 73)

Default: "0H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|------|------|------|------|------|------|------|
| 23H | Digital Volume B Control | 0 | BVL6 | BVL5 | BVL4 | BVL3 | BVL2 | BVL1 | BVL0 |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

BVL6-0: Digital Volume B (Table 69)
Default: "0CH" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|------|------|------|------|------|------|------|
| 24H | Digital Volume C Control | 0 | CVL6 | CVL5 | CVL4 | CVL3 | CVL2 | CVL1 | CVL0 |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

CVL6-0: Digital Volume C (Table 71)
Default: "0CH" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|----|-------|-------|-------|-------|-------|-------|
| 25H | Digital Mixing Control 0 | 0 | 0 | MX1R2 | MX1R1 | MX1R0 | MX1L2 | MX1L1 | MX1L0 |
| | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MX1L2-0: MIX1 Lch Output Signal Select (Table 89)
Default: "000" (DATT-B)

MX1R2-0: MIX1 Rch Output Signal Select (Table 90)
Default: "000" (DATT-B)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|----|-------|-------|-------|-------|-------|-------|
| 26H | Digital Mixing Control 1 | 0 | 0 | MX2C1 | MX2C0 | MX2B1 | MX2B0 | MX2A1 | MX2A0 |
| | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MX2A1-0: MIX2A Output Signal Select (Table 91)
Default: "00" (BIVOL Lch)

MX2B1-0: MIX2B Output Signal Select (Table 92)
Default: "00" (DATT-A Lch)

MX2C1-0: MIX2C Output Signal Select (Table 93)
Default: "00" (MIX2A)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|----|----|----|----|----|-------|-------|-------|
| 27H | Digital Mixing Control 2 | 0 | 0 | 0 | 0 | 0 | MXSB2 | MXSB1 | MXSB0 |
| | R/W | R | R | R | R | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MXSB2-0: MIX3 Output Signal Select (Table 94)
Default: "000" (DATT-A Lch, DATT-A Rch)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|-------|-------|-------|-------|----|----|-------|-------|
| 28H | Digital Mixing Control 3 | SDOR1 | SDOR0 | SDOL1 | SDOL0 | 0 | 0 | SBMX1 | SBMX0 |
| | R/W | R/W | R/W | R/W | R/W | R | R | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SBXM1-0: DATT-C Input Signal Selec ([Table 96](#))

Default: "00" (SRCAI)

SDOL1-0: SDTO Lch Output Mixing ([Table 80](#))

Default: "00" (Lch Signal Selected by [Table 79](#))

SDOR1-0: SDTO Rch Output Mixing ([Table 81](#))

Default: "00" (Rch Signal Selected by [Table 79](#))

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|--|------|-------|-------|-------|-------|------|------|
| 29H | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 2AH | FIL1 Co-efficient 1 | 0 | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 2BH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 2CH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH" | | | | | | | |

F1A13-0, F1B13-B0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)

Default: F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH" (fc=150Hz@fs=44.1kHz)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|------|------|-------|-------|-------|-------|------|------|
| 2DH | FIL2 Co-efficient 0 | F2A7 | F2A6 | F2A5 | F2A4 | F2A3 | F2A2 | F2A1 | F2A0 |
| 2EH | FIL2 Co-efficient 1 | 0 | 0 | F2A13 | F2A12 | F2A11 | F2A10 | F2A9 | F2A8 |
| 2FH | FIL2 Co-efficient 2 | F2B7 | F2B6 | F2B5 | F2B4 | F2B3 | F2B2 | F2B1 | F2B0 |
| 30H | FIL2 Co-efficient 3 | 0 | 0 | F2B13 | F2B12 | F2B11 | F2B10 | F2B9 | F2B8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

F2A13-0, F2B13-B0: FIL2 (LPF) Coefficient (14bit x 2)

Default: "0000H"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|-------|-------|-------|-------|-------|-------|------|------|
| 31H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 32H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 33H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 34H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 35H | EQ Co-efficient 0 | E0A7 | E0A6 | E0A5 | E0A4 | E0A3 | E0A2 | E0A1 | E0A0 |
| 36H | EQ Co-efficient 1 | E0A15 | E0A14 | E0A13 | E0A12 | E0A11 | E0A10 | E0A9 | E0A8 |
| 37H | EQ Co-efficient 2 | E0B7 | E0B6 | E0B5 | E0B4 | E0B3 | E0B2 | E0B1 | E0B0 |
| 38H | EQ Co-efficient 3 | 0 | 0 | E0B13 | E0B12 | E0B11 | E0B10 | E0B9 | E0B8 |
| 39H | EQ Co-efficient 4 | E0C7 | E0C6 | E0C5 | E0C4 | E0C3 | E0C2 | E0C1 | E0C0 |
| 3AH | EQ Co-efficient 5 | E0C15 | E0C14 | E0C13 | E0C12 | E0C11 | E0C10 | E0C9 | E0C8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)

Default: "0000H"

F3AS: FIL3(Stereo Separation Emphasis Filter) Select

0: HPF (default)

1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ0 (Gain Compensation Filter) Coefficient (14bit x 1 + 16bit x 2)

Default: "0000H"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-------------------|-------|-------|-------|-------|-------|-------|------|------|
| 3BH | E1 Co-efficient 0 | E1A7 | E1A6 | E1A5 | E1A4 | E1A3 | E1A2 | E1A1 | E1A0 |
| 3CH | E1 Co-efficient 1 | E1A15 | E1A14 | E1A13 | E1A12 | E1A11 | E1A10 | E1A9 | E1A8 |
| 3DH | E1 Co-efficient 2 | E1B7 | E1B6 | E1B5 | E1B4 | E1B3 | E1B2 | E1B1 | E1B0 |
| 3EH | E1 Co-efficient 3 | E1B15 | E1B14 | E1B13 | E1B12 | E1B11 | E1B10 | E1B9 | E1B8 |
| 3FH | E1 Co-efficient 4 | E1C7 | E1C6 | E1C5 | E1C4 | E1C3 | E1C2 | E1C1 | E1C0 |
| 40H | E1 Co-efficient 5 | E1C15 | E1C14 | E1C13 | E1C12 | E1C11 | E1C10 | E1C9 | E1C8 |
| 41H | E2 Co-efficient 0 | E2A7 | E2A6 | E2A5 | E2A4 | E2A3 | E2A2 | E2A1 | E2A0 |
| 42H | E2 Co-efficient 1 | E2A15 | E2A14 | E2A13 | E2A12 | E2A11 | E2A10 | E2A9 | E2A8 |
| 43H | E2 Co-efficient 2 | E2B7 | E2B6 | E2B5 | E2B4 | E2B3 | E2B2 | E2B1 | E2B0 |
| 44H | E2 Co-efficient 3 | E2B15 | E2B14 | E2B13 | E2B12 | E2B11 | E2B10 | E2B9 | E2B8 |
| 45H | E2 Co-efficient 4 | E2C7 | E2C6 | E2C5 | E2C4 | E2C3 | E2C2 | E2C1 | E2C0 |
| 46H | E2 Co-efficient 5 | E2C15 | E2C14 | E2C13 | E2C12 | E2C11 | E2C10 | E2C9 | E2C8 |
| 47H | E3 Co-efficient 0 | E3A7 | E3A6 | E3A5 | E3A4 | E3A3 | E3A2 | E3A1 | E3A0 |
| 48H | E3 Co-efficient 1 | E3A15 | E3A14 | E3A13 | E3A12 | E3A11 | E3A10 | E3A9 | E3A8 |
| 49H | E3 Co-efficient 2 | E3B7 | E3B6 | E3B5 | E3B4 | E3B3 | E3B2 | E3B1 | E3B0 |
| 4AH | E3 Co-efficient 3 | E3B15 | E3B14 | E3B13 | E3B12 | E3B11 | E3B10 | E3B9 | E3B8 |
| 4BH | E3 Co-efficient 4 | E3C7 | E3C6 | E3C5 | E3C4 | E3C3 | E3C2 | E3C1 | E3C0 |
| 4CH | E3 Co-efficient 5 | E3C15 | E3C14 | E3C13 | E3C12 | E3C11 | E3C10 | E3C9 | E3C8 |
| R/W | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: "0000H"

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: "0000H"

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: "0000H"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| 50H | 5band E1 Co-efficient 0 | 5E1A7 | 5E1A6 | 5E1A5 | 5E1A4 | 5E1A3 | 5E1A2 | 5E1A1 | 5E1A0 |
| 51H | 5band E1 Co-efficient 1 | 0 | 0 | 5E1A13 | 5E1A12 | 5E1A11 | 5E1A10 | 5E1A9 | 5E1A8 |
| 52H | 5band E1 Co-efficient 2 | 5E1B7 | 5E1B6 | 5E1B5 | 5E1B4 | 5E1B3 | 5E1B2 | 5E1B1 | 5E1B0 |
| 53H | 5band E1 Co-efficient 3 | 0 | 0 | 5E1B13 | 5E1B12 | 5E1B11 | 5E1B10 | 5E1B9 | 5E1B8 |
| 54H | 5band E2 Co-efficient 0 | 5E2A7 | 5E2A6 | 5E2A5 | 5E2A4 | 5E2A3 | 5E2A2 | 5E2A1 | 5E2A0 |
| 55H | 5band E2 Co-efficient 1 | 5E2A15 | 5E2A14 | 5E2A13 | 5E2A12 | 5E2A11 | 5E2A10 | 5E2A9 | 5E2A8 |
| 56H | 5band E2 Co-efficient 2 | 5E2B7 | 5E2B6 | 5E2B5 | 5E2B4 | 5E2B3 | 5E2B2 | 5E2B1 | 5E2B0 |
| 57H | 5band E2 Co-efficient 3 | 5E2B15 | 5E2B14 | 5E2B13 | 5E2B12 | 5E2B11 | 5E2B10 | 5E2B9 | 5E2B8 |
| 58H | 5band E2 Co-efficient 4 | 5E2C7 | 5E2C6 | 5E2C5 | 5E2C4 | 5E2C3 | 5E2C2 | 5E2C1 | 5E2C0 |
| 59H | 5band E2 Co-efficient 5 | 5E2C15 | 5E2C14 | 5E2C13 | 5E2C12 | 5E2C11 | 5E2C10 | 5E2C9 | 5E2C8 |
| 5AH | 5band E3 Co-efficient 0 | 5E3A7 | 5E3A6 | 5E3A5 | 5E3A4 | 5E3A3 | 5E3A2 | 5E3A1 | 5E3A0 |
| 5BH | 5band E3 Co-efficient 1 | 5E3A15 | 5E3A14 | 5E3A13 | 5E3A12 | 5E3A11 | 5E3A10 | 5E3A9 | 5E3A8 |
| 5CH | 5band E3 Co-efficient 2 | 5E3B7 | 5E3B6 | 5E3B5 | 5E3B4 | 5E3B3 | 5E3B2 | 5E3B1 | 5E3B0 |
| 5DH | 5band E3 Co-efficient 3 | 5E3B15 | 5E3B14 | 5E3B13 | 5E3B12 | 5E3B11 | 5E3B10 | 5E3B9 | 5E3B8 |
| 5EH | 5band E3 Co-efficient 4 | 5E3C7 | 5E3C6 | 5E3C5 | 5E3C4 | 5E3C3 | 5E3C2 | 5E3C1 | 5E3C0 |
| 5FH | 5band E3 Co-efficient 5 | 5E3C15 | 5E3C14 | 5E3C13 | 5E3C12 | 5E3C11 | 5E3C10 | 5E3C9 | 5E3C8 |
| 60H | 5band E4 Co-efficient 0 | 5E4A7 | 5E4A6 | 5E4A5 | 5E4A4 | 5E4A3 | 5E4A2 | 5E4A1 | 5E4A0 |
| 61H | 5band E4 Co-efficient 1 | 5E4A15 | 5E4A14 | 5E4A13 | 5E4A12 | 5E4A11 | 5E4A10 | 5E4A9 | 5E4A8 |
| 62H | 5band E4 Co-efficient 2 | 5E4B7 | 5E4B6 | 5E4B5 | 5E4B4 | 5E4B3 | 5E4B2 | 5E4B1 | 5E4B0 |
| 63H | 5band E4 Co-efficient 3 | 5E4B15 | 5E4B14 | 5E4B13 | 5E4B12 | 5E4B11 | 5E4B10 | 5E4B9 | 5E4B8 |
| 64H | 5band E4 Co-efficient 4 | 5E4C7 | 5E4C6 | 5E4C5 | 5E4C4 | 5E4C3 | 5E4C2 | 5E4C1 | 5E4C0 |
| 65H | 5band E4 Co-efficient 5 | 5E4C15 | 5E4C14 | 5E4C13 | 5E4C12 | 5E4C11 | 5E4C10 | 5E4C9 | 5E4C8 |
| 66H | 5band E5 Co-efficient 0 | 5E5A7 | 5E5A6 | 5E5A5 | 5E5A4 | 5E5A3 | 5E5A2 | 5E5A1 | 5E5A0 |
| 67H | 5band E5 Co-efficient 1 | 0 | 0 | 5E5A13 | 5E5A12 | 5E5A11 | 5E5A10 | 5E5A9 | 5E5A8 |
| 68H | 5band E5 Co-efficient 2 | 5E5B7 | 5E5B6 | 5E5B5 | 5E5B4 | 5E5B3 | 5E5B2 | 5E5B1 | 5E5B0 |
| 69H | 5band E5 Co-efficient 3 | 0 | 0 | 5E5B13 | 5E5B12 | 5E5B11 | 5E5B10 | 5E5B9 | 5E5B8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

5E1A13-0, 5E1B13-B0: 5-band Equalizer 1 Coefficient (14bit x 2)

Default: 5E1A13-0 bits = "003AH", 5E1B13-0 bits = "2074H" (fc=100Hz@fs=44.1kHz)

5E2A15-0, 5E2B15-0, 5E2C15-0: 5-band Equalizer 2 Coefficient (16bit x3)

Default: 5E2A15-0 bits = "001DH", 5E2B15-0 bits = "3FBB H", 5E2C15-0 bits = "E03AH"
(fo₂=250Hz, fb₂=50Hz@fs=44.1kHz)

5E3A15-0, 5E3B15-0, 5E3C15-0: 5-band Equalizer 3 Coefficient (16bit x3)

Default: 5E3A15-0 bits = "0073H", 5E3B15-0 bits = "3E76H", 5E3C15-0 bits = "E0E6H"
(fo₃=1kHz, fb₃=200Hz@fs=44.1kHz)

5E4A15-0, 5E4B15-0, 5E4C15-0: 5-band Equalizer 4 Coefficient (16bit x3)

Default: 5E4A15-0 bits = "0185H", 5E4B15-0 bits = "3589H", 5E4C15-0 bits = "E30BH"
(fo₄=3.5kHz, fb₄=700Hz@fs=44.1kHz)

5E5A13-0, 5E5B13-B0: 5-band Equalizer 5 Coefficient (14bit x 2)

Default: 5E5A13-0 bits = "112CH", 5E5B13-0 bits = "3DA9H" (fc=10kHz@fs=44.1kHz)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|--------|--------|--------|--------|--------|--------|
| 6AH | 5band EQ1 Gain | 0 | 0 | 5EQ1G5 | 5EQ1G4 | 5EQ1G3 | 5EQ1G2 | 5EQ1G1 | 5EQ1G0 |
| 6BH | 5band EQ2 Gain | 0 | 0 | 5EQ2G5 | 5EQ2G4 | 5EQ2G3 | 5EQ2G2 | 5EQ2G1 | 5EQ2G0 |
| 6CH | 5band EQ3 Gain | 0 | 0 | 5EQ3G5 | 5EQ3G4 | 5EQ3G3 | 5EQ3G2 | 5EQ3G1 | 5EQ3G0 |
| 6DH | 5band EQ4 Gain | 0 | 0 | 5EQ4G5 | 5EQ4G4 | 5EQ4G3 | 5EQ4G2 | 5EQ4G1 | 5EQ4G0 |
| 6EH | 5band EQ5 Gain | 0 | 0 | 5EQ5G5 | 5EQ5G4 | 5EQ5G3 | 5EQ5G2 | 5EQ5G1 | 5EQ5G0 |
| | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

5EQ1G5-0: 5-band Equalizer 1 Gain Setting
Default: 18H (0dB)

5EQ2G5-0: 5-band Equalizer 2 Gain Setting
Default: 18H (0dB)

5EQ3G5-0: 5-band Equalizer 3 Gain Setting
Default: 18H (0dB)

5EQ4G5-0: 5-band Equalizer 4 Gain Setting
Default: 18H (0dB)

5EQ5G5-0: 5-band Equalizer 5 Gain Setting
Default: 18H (0dB)

EQ gain: +12dB(00H) ~ -12dB(30H), 0.5dB step

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|----|--------|--------|--------|---------|---------|-------|-------|
| 70H | DRC Mode Control | 0 | DLMAT2 | DLMAT1 | DLMAT0 | DRGAIN1 | DRGAIN0 | DRCC1 | DRCC0 |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DRCC1-0: DRC Enable (Table 64)

00: Disable (default)

01: Low

10: Middle

11: High

When DRCC1-0 bits are “00”, DRC is through (0dB).

DRGAIN1-0: DRC Recovery Speed Setting (Table 66)

Default: “00”

DLMAT2-0: DRC ATT Speed Setting (Table 65)

Default: “000”

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|-------|-------|----|-------|-------|------|
| 71H | NS Control | 0 | 0 | DRCM1 | DRCM0 | 0 | NSLPF | NSHPF | NSCE |
| | R/W | R | R | R/W | R/W | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NSCE: Noise Suppression Enable

0: Disable (default)

1: Enable

When NSCE bit is “0”, Noise Suppression is through (0dB).

NSHPF: HPF for Noise Suppression Coefficient Setting Enable

0: Disable (default)

1: Enable

When NSHPF bit is “1”, the settings of NSHA13-0 and NSHB13-0 bits are enabled. When NSHPF bit is “0”, HPF block is through (0dB).

NSLPF: LPF for Noise Suppression Coefficient Setting Enable

0: Disable (default)

1: Enable

When NSLPF bit is “1”, the settings of NSLA13-0 and NSLB13-0 bits are enabled. When NSLPF bit is “0”, LPF block is through (0dB).

DRCM1-0: DRC Input Signal Setting (Table 40)

Default: “00” (L = Lch, R = Rch)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|----|---------|---------|---------|----|--------|--------|--------|
| 72H | NS Gain & ATT Control | 0 | NSGAIN2 | NSGAIN1 | NSGAIN0 | 0 | NSATT2 | NSATT1 | NSATT0 |
| | R/W | R | R/W | R/W | R/W | R | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

NSATT2-0: Noise Suppression ATT Speed Setting (Table 44)

Default: “001”

NSGAIN2-0: Noise Suppression Recovery Speed Setting (Table 47)

Default: “001”

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|--------|--------|----|--------|--------|--------|--------|--------|
| 73H | NS On Level | NSIAF1 | NSIAF0 | 0 | NSTHL4 | NSTHL3 | NSTHL2 | NSTHL1 | NSTHL0 |
| | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NSTHL4-0: Noise Suppression Threshold Low Level Setting (Table 42)

Default: "00H" (-36dB)

NSIAF1-0: Moving Average Parameter Setting at Noise Suppression Off (Table 41)

Default: "10" (1024/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|--------|--------|----|--------|--------|--------|--------|--------|
| 74H | NS Off Level | NSOAF1 | NSOAF0 | 0 | NSTHH4 | NSTHH3 | NSTHH2 | NSTHH1 | NSTHH0 |
| | R/W | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |
| | Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NSTHH4-0: Noise Suppression Threshold High Level Setting (Table 46)

Default: "00H" (-36dB)

NSOAF1-0: Moving Average Parameter Setting at Noise Suppression On (Table 45)

Default: "10" (16/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|----|----|----|----|--------|--------|--------|--------|
| 75H | NS Reference Select | 0 | 0 | 0 | 0 | NSREF3 | NSREF2 | NSREF1 | NSREF0 |
| | R/W | R | R | R | R | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

NSREF3-0: Reference Value at Noise Suppression (Table 43)

Default: "0H" (-9dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|-------|-------|--------|--------|--------|--------|-------|-------|
| 76H | NS LPF Co-efficient 0 | NSLA7 | NSLA6 | NSLA5 | NSLA4 | NSLA3 | NSLA2 | NSLA1 | NSLA0 |
| 77H | NS LPF Co-efficient 1 | 0 | 0 | NSLA13 | NSLA12 | NSLA11 | NSLA10 | NSLA9 | NSLA8 |
| 78H | NS LPF Co-efficient 2 | NSLB7 | NSLB6 | NSLB5 | NSLB4 | NSLB3 | NSLB2 | NSLB1 | NSLB0 |
| 79H | NS LPF Co-efficient 3 | 0 | 0 | NSLB13 | NSLB12 | NSLB11 | NSLB10 | NSLB9 | NSLB8 |
| 7AH | NS HPF Co-efficient 0 | NSHA7 | NSHA6 | NSHA5 | NSHA4 | NSHA3 | NSHA2 | NSHA1 | NSHA0 |
| 7BH | NS HPF Co-efficient 1 | 0 | 0 | NSHA13 | NSHA12 | NSHA11 | NSHA10 | NSHA9 | NSHA8 |
| 7CH | NS HPF Co-efficient 2 | NSHB7 | NSHB6 | NSHB5 | NSHB4 | NSHB3 | NSHB2 | NSHB1 | NSHB0 |
| 7DH | NS HPF Co-efficient 3 | 0 | 0 | NSHB13 | NSHB12 | NSHB11 | NSHB10 | NSHB9 | NSHB8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

NSLA13-0, NSLB13-0: Noise Suppression LPF Coefficient (14bit x 2)

Default: "0000H"

NSHA13-0, NSHB13-0: Noise Suppression HPF Coefficient (14bit x 2)

Default: "0000H"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 80H | DVLC Filter Select | DLLPF1 | DLLPF0 | DMHPF1 | DMHPF0 | DMLPF1 | DMLPF0 | DHHPF1 | DHHPF0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DHHPF1-0: DVLC High Frequency Range HPF Coefficient Setting Enable ([Table 57](#))

- 00: Disable (default)
- 01: 1st order HPF
- 10: 2nd order HPF
- 11: N/A

When DHHPF1-0 bits are “01” or “10”, the settings of DHHA13-0 and DHHB13-0 bits are enabled. When DHHPF1-0 bits are “00”, HPF block outputs “0” data.

DMLPF1-0: DVLC Middle Frequency Range LPF Coefficient Setting Enable ([Table 53](#))

- 00: Disable (default)
- 01: 1st order LPF
- 10: 2nd order LPF
- 11: N/A

When DMLPF1-0 bits are “01” or “10”, the settings of DMLA13-0 and DMLB13-0 bits are enabled. When DMLPF1-0 bits are “00”, LPF block of DVLC middle frequency range is through (0dB).

DMHPF1-0: DVLC Middle Frequency Range HPF Coefficient Setting Enable ([Table 52](#))

- 00: Disable (default)
- 01: 1st order HPF
- 10: 2nd order HPF
- 11: N/A

When DMHPF1-0 bits are “01” or “10”, the settings of DMHA13-0 and DMHB13-0 bits are enabled. When DMHPF1-0 bits are “00”, HPF block of DVLC middle frequency range is through (0dB).

DLLPF1-0: DVLC Low Frequency Range LPF Coefficient Setting Enable ([Table 48](#))

- 00: Disable (default)
- 01: 1st order LPF
- 10: 2nd order LPF
- 11: N/A

When DLLPF1-0 bits are “01” or “10”, the settings of DLLA13-0 and DLLB13-0 bits are enabled. When DLLPF1-0 bits are “00”, LPF block outputs “0” data.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----------|----------|----------|---------|---------|---------|------|------|
| 81H | DVLC Mode Control | DVRGAIN2 | DVRGAIN1 | DVRGAIN0 | DVLMAT2 | DVLMAT1 | DVLMAT0 | DAF1 | DAF0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

DAF1-0: Moving Average Parameter Setting for DVLC ([Table 61](#))

Default: “11” (Default: 2048/fs)

DVLMAT2-0: DVLC ATT Speed Setting ([Table 62](#))

Default: “011”

DVRGAIN2-0: DVLC Recovery Speed Setting ([Table 63](#))

Default: “011”

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|----------------|----|------|-------|-------|-------|-------|-------|-------|
| 82H | DVLCL Curve X1 | 0 | 0 | VL1X5 | VL1X4 | VL1X3 | VL1X2 | VL1X1 | VL1X0 |
| 83H | DVLCL Curve Y1 | 0 | 0 | VL1Y5 | VL1Y4 | VL1Y3 | VL1Y2 | VL1Y1 | VL1Y0 |
| 84H | DVLCL Curve X2 | 0 | 0 | VL2X5 | VL2X4 | VL2X3 | VL2X2 | VL2X1 | VL2X0 |
| 85H | DVLCL Curve Y2 | 0 | 0 | VL2Y5 | VL2Y4 | VL2Y3 | VL2Y2 | VL2Y1 | VL2Y0 |
| 86H | DVLCL Curve X3 | 0 | 0 | 0 | VL3X4 | VL3X3 | VL3X2 | VL3X1 | VL3X0 |
| 87H | DVLCL Curve Y3 | 0 | 0 | 0 | VL3Y4 | VL3Y3 | VL3Y2 | VL3Y1 | VL3Y0 |
| 88H | DVLCL Slope 1 | 0 | L1G6 | L1G5 | L1G4 | L1G3 | L1G2 | L1G1 | L1G0 |
| 89H | DVLCL Slope 2 | 0 | L2G6 | L2G5 | L2G4 | L2G3 | L2G2 | L2G1 | L2G0 |
| 8AH | DVLCL Slope 3 | 0 | L3G6 | L3G5 | L3G4 | L3G3 | L3G2 | L3G1 | L3G0 |
| 8BH | DVLCL Slope 4 | 0 | L4G6 | L4G5 | L4G4 | L4G3 | L4G2 | L4G1 | L4G0 |
| 8CH | DVLCM Curve X1 | 0 | 0 | VM1X5 | VM1X4 | VM1X3 | VM1X2 | VM1X1 | VM1X0 |
| 8DH | DVLCM Curve Y1 | 0 | 0 | VM1Y5 | VM1Y4 | VM1Y3 | VM1Y2 | VM1Y1 | VM1Y0 |
| 8EH | DVLCM Curve X2 | 0 | 0 | VM2X5 | VM2X4 | VM2X3 | VM2X2 | VM2X1 | VM2X0 |
| 8FH | DVLCM Curve Y2 | 0 | 0 | VM2Y5 | VM2Y4 | VM2Y3 | VM2Y2 | VM2Y1 | VM2Y0 |
| 90H | DVLCM Curve X3 | 0 | 0 | 0 | VM3X4 | VM3X3 | VM3X2 | VM3X1 | VM3X0 |
| 91H | DVLCM Curve Y3 | 0 | 0 | 0 | VM3Y4 | VM3Y3 | VM3Y2 | VM3Y1 | VM3Y0 |
| 92H | DVLCM Slope 1 | 0 | M1G6 | M1G5 | M1G4 | M1G3 | M1G2 | M1G1 | M1G0 |
| 93H | DVLCM Slope 2 | 0 | M2G6 | M2G5 | M2G4 | M2G3 | M2G2 | M2G1 | M2G0 |
| 94H | DVLCM Slope 3 | 0 | M3G6 | M3G5 | M3G4 | M3G3 | M3G2 | M3G1 | M3G0 |
| 95H | DVLCM Slope 4 | 0 | M4G6 | M4G5 | M4G4 | M4G3 | M4G2 | M4G1 | M4G0 |
| 96H | DVLCH Curve X1 | 0 | 0 | VH1X5 | VH1X4 | VH1X3 | VH1X2 | VH1X1 | VH1X0 |
| 97H | DVLCH Curve Y1 | 0 | 0 | VH1Y5 | VH1Y4 | VH1Y3 | VH1Y2 | VH1Y1 | VH1Y0 |
| 98H | DVLCH Curve X2 | 0 | 0 | VH2X5 | VH2X4 | VH2X3 | VH2X2 | VH2X1 | VH2X0 |
| 99H | DVLCH Curve Y2 | 0 | 0 | VH2Y5 | VH2Y4 | VH2Y3 | VH2Y2 | VH2Y1 | VH2Y0 |
| 9AH | DVLCH Curve X3 | 0 | 0 | 0 | VH3X4 | VH3X3 | VH3X2 | VH3X1 | VH3X0 |
| 9BH | DVLCH Curve Y3 | 0 | 0 | 0 | VH3Y4 | VH3Y3 | VH3Y2 | VH3Y1 | VH3Y0 |
| 9CH | DVLCH Slope 1 | 0 | H1G6 | H1G5 | H1G4 | H1G3 | H1G2 | H1G1 | H1G0 |
| 9DH | DVLCH Slope 2 | 0 | H2G6 | H2G5 | H2G4 | H2G3 | H2G2 | H2G1 | H2G0 |
| 9EH | DVLCH Slope 3 | 0 | H3G6 | H3G5 | H3G4 | H3G3 | H3G2 | H3G1 | H3G0 |
| 9FH | DVLCH Slope 4 | 0 | H4G6 | H4G5 | H4G4 | H4G3 | H4G2 | H4G1 | H4G0 |
| R/W | | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VL1X5-0, VL2X5-0, VL3X4-0: Input Gain Setting for Low Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

VL1Y5-0, VL2Y5-0, VL3Y4-0: Output Gain Setting for Low Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

L1G6-0, L2G6-0, L3G6-0, L4G6-0: DVLC Slope Setting for Low Range (Table 51)
Default: "00H"

VM1X5-0, VM2X5-0, VM3X4-0: Input Gain Setting for Middle Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

VM1Y5-0, VM2Y5-0, VM3Y4-0: Output Gain Setting for Middle Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

M1G6-0, M2G6-0, M3G6-0, M4G6-0: DVLC Slope Setting for Middle Range (Table 51)
Default: "00H"

VH1X5-0, VH2X5-0, VH3X4-0: Input Gain Setting for High Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

VH1Y5-0, VH2Y5-0, VH3Y4-0: Output Gain Setting for High Range DVLC Point (Table 49, Table 50)
Default: "00H" (0dB)

H1G6-0, H2G6-0, H3G6-0, H4G6-0: DVLC Slope Setting for High Range (Table 51)
Default: "00H"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------------|-------|-------|--------|--------|--------|--------|-------|-------|
| A0H | DVLCL LPF Co-efficient 0 | DLLA7 | DLLA6 | DLLA5 | DLLA4 | DLLA3 | DLLA2 | DLLA1 | DLLA0 |
| A1H | DVLCL LPF Co-efficient 1 | 0 | 0 | DLLA13 | DLLA12 | DLLA11 | DLLA10 | DLLA9 | DLLA8 |
| A2H | DVLCL LPF Co-efficient 2 | DLLB7 | DLLB6 | DLLB5 | DLLB4 | DLLB3 | DLLB2 | DLLB1 | DLLB0 |
| A3H | DVLCL LPF Co-efficient 3 | 0 | 0 | DLLB13 | DLLB12 | DLLB11 | DLLB10 | DLLB9 | DLLB8 |
| A4H | DVLCM HPF Co-efficient 0 | DMHA7 | DMHA6 | DMHA5 | DMHA4 | DMHA3 | DMHA2 | DMHA1 | DMHA0 |
| A5H | DVLCM HPF Co-efficient 1 | 0 | 0 | DMHA13 | DMHA12 | DMHA11 | DMHA10 | DMHA9 | DMHA8 |
| A6H | DVLCM HPF Co-efficient 2 | DMHB7 | DMHB6 | DMHB5 | DMHB4 | DMHB3 | DMHB2 | DMHB1 | DMHB0 |
| A7H | DVLCM HPF Co-efficient 3 | 0 | 0 | DMHB13 | DMHB12 | DMHB11 | DMHB10 | DMHB9 | DMHB8 |
| A8H | DVLCM LPF Co-efficient 0 | DMLA7 | DMLA6 | DMLA5 | DMLA4 | DMLA3 | DMLA2 | DMLA1 | DMLA0 |
| A9H | DVLCM LPF Co-efficient 1 | 0 | 0 | DMLA13 | DMLA12 | DMLA11 | DMLA10 | DMLA9 | DMLA8 |
| AAH | DVLCM LPF Co-efficient 2 | DMLB7 | DMLB6 | DMLB5 | DMLB4 | DMLB3 | DMLB2 | DMLB1 | DMLB0 |
| ABH | DVLCM LPF Co-efficient 3 | 0 | 0 | DMLB13 | DMLB12 | DMLB11 | DMLB10 | DMLB9 | DMLB8 |
| ACH | DVLCH HPF Co-efficient 0 | DHHA7 | DHHA6 | DHHA5 | DHHA4 | DHHA3 | DHHA2 | DHHA1 | DHHA0 |
| ADH | DVLCH HPF Co-efficient 1 | 0 | 0 | DHHA13 | DHHA12 | DHHA11 | DHHA10 | DHHA9 | DHHA8 |
| AEH | DVLCH HPF Co-efficient 2 | DHHB7 | DHHB6 | DHHB5 | DHHB4 | DHHB3 | DHHB2 | DHHB1 | DHHB0 |
| AFH | DVLCH HPF Co-efficient 3 | 0 | 0 | DHHB13 | DHHB12 | DHHB11 | DHHB10 | DHHB9 | DHHB8 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

DLLA13-0, DLLB13-0: DVLC Low Frequency Range LPF Coefficient (14bit x 2)
Default: "0000H"

DMHA13-0, DMHB13-0: DVLC Middle Frequency Range HPF Coefficient (14bit x 2)
Default: "0000H"

DMLA13-0, DMLB13-0: DVLC Middle Frequency Range LPF Coefficient (14bit x 2)
Default: "0000H"

DHHA13-0, DHHB13-0: DVLC High Frequency Range HPF Coefficient (14bit x 2)
Default: "0000H"

■ Register Map (DSP block)

The DSP block control register settings are executed through a microcontroller interface. All registers below are initialized by the power down (PDNE pin = “L”). To ensure control register settings, this power-down (PDNE pin= “L”) must always be made when power up the AK4679.

Control register settings should be made during DSP reset (DSRSTN bit = “0”).

| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------|----|----|----|-------|----|----|----|-------|
| PCONT0 | 0 | 0 | 0 | SOCFG | 0 | 0 | 0 | PWSW |
| PCONT1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MRSTN |

| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------|---------|---------|---------|---------|---------|--------|----------|----------|
| CONT0 | FSD[3] | FSD[2] | FSD[1] | FSD[0] | 0 | 0 | 0 | 0 |
| CONT1 | LAW[1] | LAW[0] | DIFD[1] | DIFD[0] | BCKPD | 0 | TESTB | TESTA |
| CONT2 | BANK[3] | BANK[2] | BANK[1] | BANK[0] | LOCKE | CRCE | WDTN | EFEN |
| CONT3 | POMODE | DRMS[1] | DRMS[0] | DRAD[1] | DRAD[0] | 0 | WAVP1[1] | WAVP1[0] |
| CONT4 | LPDO4 | LPDO3 | LPDO2 | LPDO1 | SELDO4 | SELDO3 | PT2N | SELPT |
| CONT5 | OUT4N | OUT3N | OUT2N | OUT1N | 0 | 0 | 0 | STRDY |
| CONT6 | 0 | 0 | DLRDY | 0 | 0 | DSRSTN | 0 | 0 |
| CONT7 | SYDET | CGLK | 0 | 0 | 0 | 0 | 0 | 0 |
| CONT8 | TESTC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note 80. The bits defined as 0 must set a “0” value.

Note 81. Default value is the value after power-down release.

Power Control: Internal Power Supply Control**PCONT0: Internal power supply control**

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|----|----|----|-------|----|----|----|------|
| | | PCONT0 | 0 | 0 | 0 | SOCFG | 0 | 0 | 0 | PWSW |
| W | R | R/W | R | R | R | R/W | R | R | R | R/W |
| D0h | 50h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PWSW bit: Internal power supply switch control

0: power control SW off (default)

1: power control SW on

SOCFG: SO pin configuration (this bit is valid for I2C pin = "L")

0: CMOSL (default)

1: Wired 'OR' (Hi-impedance)

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|----|----|----|----|----|----|----|-------|
| | | PCONT1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MRSTN |
| W | R | R/W | R | R | R | R | R | R | R | R/W |
| D1h | 51h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MRSTN: Internal power supply reset control

0: Reset state (Default)

1: Reset Released

Device Control Register**CONT0: Initial Setting1**

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|----------|-----|-----|-----|----|----|----|----|
| | | CONT0 | FSD[3:0] | | | | 0 | 0 | 0 | 0 |
| W | R | R/W | R/W | R/W | R/W | R/W | R | R | R | R |
| C0h | 40h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FSD3-0: Sampling Frequency Select ([Table 6](#))

00: fs1=fs2=8kHz (default)

Write “0” into the “0” registers.

CONT1: Initial Setting 2

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|----------|-----|-----------|-----|-------|----|-------|-------|
| | | CONT1 | LAW[1:0] | | DIFD[1:0] | | BCKPD | 0 | TESTB | TESTA |
| W | R | R/W | R/W | R/W | R/W | R/W | R/W | R | R | R |
| C1h | 41h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LAW[1:0]: PCM I/F Port#1 Data Format ([Table 124](#))

00: 16 bit Linear (default)

DIFD[1:0]: PCM I/F Port#1 SYNC Format Setting ([Table 125](#))

00: PCM Short Frame (default)

BCKPD: PCM Format BCLK Edge Select ([Table 123](#))

0: Falling Edge (default)

1: Rising Edge

TESTB, TESTA: Must write “0” into these bits.

CONT2: Initial Setting 3

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|------------------|-----|---------------|-----------|-----|-----|-----|-------|------|------|------|--|
| | | CONT2 | BANK[3:0] | | | | LOCKE | CRCE | WDTN | EFEN | |
| W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| C2h | 42h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

BANK[3:0]: DSP DLRAM Mode Setting

| DLRAM Partition Mode | BANK [3:0] Bit | DSP Delay RAM | | |
|----------------------|----------------|---------------------|-----------------------|--|
| | | Bank0 Ring 20.4f | Bank1 Linear 20.4f | Bank2 Linear 8bit μ -law codec |
| 0 | 0000b | 16384 words | 0 | 0 |
| 1 | 0001b | 14336 words | 2048 words | 0 |
| 2 | 0010b | 12288 words | 4096 words | 0 |
| 3 | 0011b | 10240 words | 6144 words | 0 |
| 4 | 0100b | 8192 words | 8192 words | 0 |
| 5 | 0101b | 6144 words | 10240 words | 0 |
| 6 | 0110b | 4096 words | 12288 words | 0 |
| 7 | 0111b | 2048 words | 14336 words | 0 |
| 8 | 1000b | 0 | 16384 words | 0 |
| 9 | 1001b | 10240 words | 0 | 18432words |
| 10 | 1010b | 8192 words | 2048 words | 18432words |
| 11 | 1011b | 6144 words | 4096 words | 18432words |
| 12 | 1100b | 4096 words | 6144 words | 18432words |
| 13 | 1101b | 2048 words | 8192 words | 18432words |
| 14 | 1110b | 0 | 10240 words | 18432words |
| 15 | 1111b | N/A | | |

(default)

(N/A: Not available)

LOCKE: Clock Generator Unit Lock Error status selects ([Table 128](#))

0: lock status monitor invalid (default)

1: lock status monitor Enable

CRCE: DSP CRC status selects ([Table 128](#))

0: CRC status monitor invalid (default)

1: CRC status monitor enable

WDTN: WDT Disable Switch of DSP ([Table 128](#))

0: WDT Enable (default)

1: WDT Disable

EFEN: Extended Instruction Enable of DSP

0: Valid (default)

1: Invalid

CONT3: DSP Setting 1

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|--------|-----------|-----|-----------|-----|----|-----------|-----|
| C3h | | CONT3 | POMODE | DRMS[1:0] | | DRAD[1:0] | | 0 | WAVP[1:0] | |
| W | R | R/W | R/W | R/W | R/W | R/W | R/W | R | R/W | R/W |
| C3h | 43h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

POMODE1: DLYRAM Pointer 0 Select
 0: OFREG (default)
 1: DBUS Immediate Data

DRAM: DATA RAM Size Setting

| DRAM Mode | DRMS[1:0] Bit | DSP Data RAM | |
|-----------|---------------|---------------------------|---------------------------|
| | | Bank1 Memory size [words] | Bank0 Memory size [words] |
| 0 | 00 | 512 | 1536 |
| 1 | 01 | 1024 | 1024 |
| 2 | 10 | 1536 | 512 |
| others | others | N/A | |

(default)

(N/A: Not available)

Addressing Mode Setting bit [1:0]

| Addressing mode | DRAD Pointer | DSP Data RAM | |
|-----------------|--------------|--------------|-----------|
| | | Bank1 DP1 | Bank0 DP0 |
| 0 | 00 | Ring | Ring |
| 1 | 01 | Ring | Linear |
| 2 | 10 | Linear | Ring |
| 3 | 11 | Linear | Linear |

(default)

WAVP[1:0]: CRAM Memory Assignment of DSP

| WAVP Mode | WAVP[1] | WAVP[0] | | FFT point |
|-----------|---------|---------|---------|-----------|
| 0 | 0 | 0 | 33word | 128 |
| 1 | 0 | 1 | 65word | 256 |
| 2 | 1 | 0 | 129word | 512 |
| 3 | 1 | 1 | 257word | 1024 |

(default)

CONT4: DSP Setting 2

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|-------|-------|-------|-------|--------|--------|------|-------|
| | | CONT4 | LPDO4 | LPDO3 | LPDO2 | LPDO1 | SELDO4 | SELDO3 | PT2N | SELPT |
| W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| C4h | 44h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LPDO4: SDOUT4 Signal Select ([Figure 109](#)) Valid when OUT4N bit = “0”
 0: SDIN3 to SDOUT4 (default)
 1: DSP DOUT4 to SDOUT4 pin

LPDO3: SDOUT3 Signal Select ([Figure 109](#)) Valid when OUT3N bit = “0”
 0: SDIN4 to SDOUT3 (default)
 1: DSP DOUT3 to SDOUT3 pin

LPDO2: SDOUT2 Signal Select ([Figure 109](#)) Valid when OUT2N bit = “0”
 0: SDIN1 to SDOUT2 (default)
 1: DSP DOUT2 to SDOUT2 pin

LPDO1: SDOUT1 Signal Select ([Figure 109](#)) Valid when OUT1N bit = “0”
 0: SDIN2 pin to SDOUT1 pin (default)
 1: DSP DOUT1 to SDOUT1 pin

SELDO4: SDOUT4/GP1 pin Signal Select ([Table 130](#))
 0: DSP DOUT4 Output (default)
 1: DSP GP Output 1

SELDO3: SDOUT3/GP0 Signal Select ([Table 129](#))
 0: DSP DOUT3 Output (default)
 1: DSP GP Output 1

PT2N: Port#2 Output Enable ([Figure 108](#))
 0: Enable (default)
 1: Disable (BCLK2 and SYNC2 pin output Low level)

SELPT: Port Select of Port #2 Output ([Figure 108](#))
 0: Port#1 (SYNC1, BCLK1) (default)
 SYNC3/JX1 and BCLK3/JX0 pins can be used as JX1 and JX0 pins respectively.
 1: Port#3 (SYNC3, BCLK3)

CONT5: Signal Setting 1

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|-------|-------|-------|-------|----|----|----|-------|
| | | CONT5 | OUT4N | OUT3N | OUT2N | OUT1N | 0 | 0 | 0 | STRDY |
| W | R | R/W | R/W | R/W | R/W | R/W | R | R | R | R/W |
| C5h | 45h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

OUT4N: SDOUT4 pin output enable (active low)
 0: SDOUT4 Output Enable (default)
 1: SDOUT4 pin = "L"

OUT3N: SDOUT3 pin output enable (active low)
 0: SDOUT3 Output Enable (default)
 1: SDOUT3 pin = "L"

OUT2N: SDOUT2 pin output enable (active low)
 0: SDOUT2 Output Enable (default)
 1: SDOUT2 pin = "L"

OUT1N: SDOUT1 pin output enable (active low)
 0: SDOUT1 Output Enable (default)
 1: SDOUT1 pin = "L"

STRDY: STO/RDY pin select
 0: STO Output (default)
 1: RDY Output

CONT6: Signal Setting 2

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|----|----|-------|----|----|---------|----|----|
| | | CONT6 | 0 | 0 | DLRDY | 0 | 0 | DSPRSTN | 0 | 0 |
| W | R | R/W | R | R | R/W | R | R | R/W | R | R |
| C6h | 46h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DLRDY: DSP Download Preparation

0: download inhibit (default)

1: download ready

This bit is used when start to download the DSP programs. The bit must be cleared after downloading programs are completed.

DSPRSTN: DSP Reset

0: DSP Reset (default)

1: DSP Reset Release

CONT7: State Signal (Read only)

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|-------|------|----|----|----|----|----|----|
| | | CONT7 | SYDET | CGLK | 0 | 0 | 0 | 0 | 0 | 0 |
| W | R | R/W | R | R | R | R | R | R | R | R |
| C7h | 47h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DSP status output from the wait sync state to operational state (Run State)

SYDET: SYNC Signal Detection flag

0: No SYNC1 pin Signal (Low or High fixed) (default)

1: SYNC1 pin Signal Detect

This bit outputs DSP status in Wait Sync State until DSP Operational state (RUN).

CGLK: Clock Generator Unit Lock Status

0: Clock Generator Unlocked State (default)

1: Clock Generator Locked State

CONT8: Initial Setting 4

| Register Address | | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|---------------|-------|----|----|----|----|----|----|----|
| | | CONT8 | TESTC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | R | R/W | R/W | R | R | R | R | R | R | R |
| C8h | 48h | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TESTC bit must be set "1". (i.e. set the 80h value in this register)

The TESTC bit is set after writing the power control register with the power supply on.

■ Command Code map for the DSP

1. Command Code

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|----------|---------------------|------|------|--------------------------------------|------|------|------|
| R/W flag | Area to be accessed | | | Accompanying data to the access area | | | |

R/W Flag

Write at “1”, Read at “0”.

Access data and accompanying data

| BIT6 | BIT5 | BIT4 | BIT3~0 | |
|------|------|------|--|---|
| 0 | 0 | 0 | Number of Write | Write preparation to CRAM during RUN |
| 0 | 0 | 1 | Number of Write | Write preparation to OFREG during RUN |
| 0 | 1 | 0 | 0100 0010 | Write operation to CRAM during RUN Write operation to OFREG during RUN |
| 0 | 1 | 1 | 1000 0100 0010 | Write operation to PRAM during DSP reset Write operation to CRAM during DSP reset Write operation to OFREG during DSP reset |
| 1 | 0 | 0 | Register Address | Internal control registers 00h~08h |
| 1 | 0 | 1 | Register Address | System power registers 00h~01h |
| 1 | 1 | 0 | 0000 | Device Identification (Read only) |
| 1 | 1 | 1 | 0000 0010 0100 0110 1000 1010 1100 | Error Status Read CRC Write/Read Write operation of JX code Read operation from MIR1 Read operation from MIR2 Read operation from MIR3 Read operation from MIR4 |

2. Address

Address description is always LSB justified. Accessing command code BIT[6:4]= “000” to “011” requires 16bit address. Accessing command code BIT[6:4]= “100” to “111” requires no address.

3. Data

Length of write data is depending on the writing area size. When accessing RAM, data may be written to sequential address locations by writing data continuously.

■ Write

| Command Code | Address | Data Length | Description |
|--------------|----------------------|-------------|--|
| 0x80~0x8F | 16bit | 24bit×n | Write preparation to CRAM during RUN. Command code BIT3~BIT0 bits determines the amount of write operation. (0x80 # of write: 1, 0x81 # of write: 2, ---, 0x8F # of write: 16) If the actual amount of write operations exceeds the defined amount, that data will be ignored. |
| 0x90~0x9F | 16bit | 24bit×n | Write preparation to OFREG during RUN Command code BIT3~BIT0 bits determines the amount of write operation. (0x90 # of write: 1, 0x91 # of write: 2, ---, 0x9F # of write: 16) If the actual amount of write operations exceeds the defined amount, that data will be ignored. |
| 0xA2 | 16bit | None | Write operation to OFREG during RUN. 0 address should be written. |
| 0xA4 | 16bit | None | Write operation to CRAM during RUN. 0 address should be written. |
| 0xB2 | 16bit | 24bit×n | Write operation to OFREG during DSP reset |
| 0xB4 | 16bit | 24bit×n | Write operation to CRAM during DSP reset |
| 0xB8 | 16bit (0000h fix) | 40bit×n | Write operation to PRAM during DSP reset |
| 0xC0~0xC8 | None | 8bit | Write operation to Register 0h~8h (except 7h) |
| 0xD0~0xD1 | None | 8bit | System Power Supply Registers 0h~1h Write |
| 0xF2 | None | 16bit | CRC Write |
| 0xF4 | None | 8bit | Write operation of DSP JX code |

Data length is defined by the command code which specifies the area to be accessed. When accessing RAM, data may be read from sequential address locations by reading data continuously. Writing other than the above-mentioned command code is prohibited.

Table 131. List of Usable Command Codes in Write Sequence

■ Read

| Command Code | Address | Data Length | Description |
|--------------|----------------------|-------------|---|
| 0x24 | 16bit | 24bit×n | CRAM/OFREG Write preparation data Read during RUN |
| 0x32 | 16bit | 24bit×n | Read operation from OFREG during DSP reset |
| 0x34 | 16bit | 24bit×n | Read operation from CRAM during DSP reset |
| 0x38 | 16bit (0000h fix) | 40bit×n | Read operation from PRAM during DSP reset |
| 0x40~0x48 | None | 8bit | Read operation from Register 0h~8h |
| 0x50~0x51 | None | 8bit | Read operation from System Power Supply Register 0h~1h |
| 0x60 | None | 8bit | Device Identification |
| 0x70 | None | 8bit | DSP Error Status Read |
| 0x72 | None | 16bit | CRC result Read |
| 0x76 | None | 32bit | Read operation from MIR1 28-bit is upper-bit justified. Lower 4-bits are for validity flags. |
| 0x78 | None | 32bit | Read operation from MIR2 28-bit is upper-bit justified. Lower 4-bits are for validity flags. |
| 0x7A | None | 32bit | Read operation from MIR3 28-bit is upper-bit justified. Lower 4-bits are for validity flags. |
| 0x7C | None | 32bit | Read operation from MIR4 28-bit is upper-bit justified. Lower 4-bits are for validity flags. |

Reading other than the above-mentioned command code is prohibited.

Table 132. List of Usable Command Codes in Read Sequence

■ Command Format

DLRDY bit must be set “1” when the PRAM, CRAM, OFFREG will access on the sleep state.

1. Write Operation during DSP Reset

1-1. Program RAM (PRAM) Write (during DSP Reset)

| Field | Write data |
|------------------|--|
| (1) COMMAND Code | 0xB8 |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 |
| (3) ADDRESS2 | 0 0 0 0 0 0 0 0 |
| (4) DATA1 | 0 0 0 0 D35 D34 D33 D32 |
| (5) DATA2 | D31~D24 |
| (6) DATA3 | D23~D16 |
| (7) DATA4 | D15~D8 |
| (8) DATA5 | D7~D0 |
| | Five bytes of data may be written continuously for each address. |

Note 76. The address field is fixed to 0000h when writing to PRAM.

1-2. Coefficient RAM (CRAM) Write (during DSP Reset)

| Field | Write data |
|------------------|---|
| (1) COMMAND Code | 0xB4 |
| (2) ADDRESS1 | 0 0 0 0 0 A10 A9 A8 |
| (3) ADDRESS2 | A7 A6 A5 A4 A3 A2 A1 A0 |
| (4) DATA1 | D19~D12 |
| (5) DATA2 | D11~D4 |
| (6) DATA3 | D3~D0 0 0 0 0 |
| | Two bytes of data may be written continuously for each address. |

1-3. Offset REG (OFREG) Write (during DSP Rest)

| Field | Write data |
|------------------|---|
| (1) COMMAND Code | 0xB2 |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 |
| (3) ADDRESS2 | 0 0 0 A4 A3 A2 A1 A0 |
| (4) DATA1 | 0 0 0 0 0 0 0 0 |
| (5) DATA2 | 0 D14 D13 D12 D11 D10 D9 D8 |
| (6) DATA3 | D7~D0 |
| | Three bytes of data may be written continuously for each address. |

2. Write Operation during DSP Reset (DLRDY bit = “1”) and RUN

2-1. Control Register Write (during DSP reset and RUN)

| Field | Write data |
|------------------|------------|
| (1) COMMAND Code | 0xC0~0xC8 |
| (2) DATA | D7~D0 |

Note 82. Write operation may be limited depending on register settings. (C7: read only register)

2-2. System Power Supply Register Write (during DSP Reset and RUN)

| Field | Write data |
|------------------|------------|
| (1) COMMAND Code | 0xD0~0xD1 |
| (2) DATA | D7~D0 |

Note 83. Write operation may be limited depending on register settings.

2-3. External Conditional Jump Code Write (during DSP Reset and RUN)

| Field | Write data |
|------------------|------------|
| (1) COMMAND Code | 0xF4 |
| (2) DATA | D7~D0 |

2-4. CRC Code Write (during DSP Reset and RUN)

| Field | Write data |
|------------------|------------|
| (1) COMMAND Code | 0xF2 |
| (2) DATA | D15~D8 |
| (3) DATA | D7~D0 |

3. Write Operation during RUN

3-1. Coefficient RAM (CRAM) Write Preparation (during Run)

| Preparation | Write data |
|------------------|---|
| (1) COMMAND Code | 0x80~0x8F (one data at 80h, sixteen data at 8Fh) |
| (2) ADDRESS1 | 0 0 0 0 0 A10 A9 A8 |
| (3) ADDRESS2 | A7 ~ A0 |
| (4) DATA1 | D19~D12 |
| (5) DATA2 | D11~D4 |
| (6) DATA3 | D3~D0 0 0 0 0 |
| | Three bytes of data may be written continuously for each address. |

3-2. Coefficient RAM (CRAM) Write Operation (during RUN)

| Execute | Write data |
|------------------|-----------------|
| (1) COMMAND Code | 0xA4 |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 |
| (3) ADDRESS2 | 0 0 0 0 0 0 0 0 |

Note 84. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

3-3. Offset REG (OFREG) Write Preparation (during RUN)

| Preparation | Write data |
|------------------|---|
| (1) COMMAND Code | 0x90~0x9F (one data at 0x90, sixteen data at 0x9F) |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 |
| (3) ADDRESS2 | 0 0 0 A4 A3 A2 A1 A0 |
| (4) DATA1 | 0 0 0 0 0 0 0 0 |
| (5) DATA2 | 0 D14 D13 D12 D11 D10 D9 D8 |
| (6) DATA3 | D7~D0 |
| | Three bytes of data may be written continuously for each address. |

3-4. Offset REG (OFREG) Write Operation (during RUN)

| Execute | Write data |
|------------------|-----------------|
| (1) COMMAND Code | 0xA2 |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 |
| (3) ADDRESS2 | 0 0 0 0 0 0 0 0 |

Note 85. The COMMAND determines the length of the data. If the written data exceeds the allotted amount, the excess data is ignored.

4. Read Operation (DLRDY bit = "1")

4-1. Program RAM (PRAM) Read (during DSP Reset)

| Field | Write data | Readout data |
|--|-----------------|-------------------------|
| (1) COMMAND Code | 0x38 | |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 | |
| (3) ADDRESS2 | 0 0 0 0 0 0 0 0 | |
| (4) DATA1 | | 0 0 0 0 D35 D34 D33 D32 |
| (5) DATA2 | | D31~D24 |
| (6) DATA3 | | D23~D16 |
| (7) DATA4 | | D15~D8 |
| (8) DATA5 | | D7~D0 |
| Five bytes of data may be written continuously for each address. | | |

4-2. Coefficient RAM (CRAM) Read (during DSP Reset)

| Field | Write data | Readout data |
|---|---------------------|---------------|
| (1) COMMAND Code | 0x34 | |
| (2) ADDRESS1 | 0 0 0 0 0 A10 A9 A8 | |
| (3) ADDRESS2 | A7 ~ A0 | |
| (4) DATA1 | | D19~D12 |
| (5) DATA2 | | D11~D4 |
| (6) DATA3 | | D3~D0 0 0 0 0 |
| Three bytes of data may be written continuously for each address. | | |

4-3. Offset REG (OFREG) Read (DSP Reset)

| Field | Write data | Readout data |
|---|----------------------|-----------------------------|
| (1) COMMAND Code | 0x32 | |
| (2) ADDRESS1 | 0 0 0 0 0 0 0 0 | |
| (3) ADDRESS2 | 0 0 0 A4 A3 A2 A1 A0 | |
| (4) DATA1 | | 0 0 0 0 0 0 0 0 |
| (5) DATA2 | | 0 D14 D13 D12 D11 D10 D9 D8 |
| (6) DATA3 | | D7~D0 |
| Three bytes of data may be written continuously for each address. | | |

5. Read Operation (DLRDY bit = "1" and RUN state)

5-1. Control Register Read (during DSP Reset and RUN)

| Field | Write data | Readout data |
|------------------|------------|--------------|
| (1) COMMAND Code | 0x40~0x47h | |
| (2) DATA | | D7~D0 |

5-2. System Power Supply Register Read (during DSP Reset and RUN)

| Field | Write data | Readout data |
|------------------|------------|--------------|
| (1) COMMAND Code | 0x50~0x51 | |
| (2) DATA | | D7~D0 |

5-3. Device Identification (during DSP Reset and RUN)

| Field | Write data | Readout data | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|------------|--|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--|--|--|---|--|--|--|
| (1) COMMAND Code | 0x60 | | | | | | | | | | | | | | | | | | | | | | | | | |
| (2) DATA | | <table border="1"> <tr> <td>D7</td> <td>D6</td> <td>D5</td> <td>D4</td> <td>D3</td> <td>D2</td> <td>D1</td> <td>D0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td colspan="4">1</td> <td colspan="4">9</td> </tr> </table> | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | | 9 | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | |
| 1 | | | | 9 | | | | | | | | | | | | | | | | | | | | | | |

5-4. CRC Code Reading (during DSP Reset and RUN)

| Field | Write data | Readout data |
|------------------|------------|--------------|
| (1) COMMAND Code | 0x72 | |
| (2) DATA1 | | D15~D8 |
| (3) DATA2 | | D7~D0 |

5-5. Error and GPO statuses Reading (DSP Reset and RUN)

| Field | Write data | Output |
|------------------|------------|---|
| (1) COMMAND Code | 0x70 | |
| (2) DATA | | Active low output D7: CRCERRN 0: CRC error D6: WDTERRN 0: Watch Dog Timer error D5: CGERRN 0: Clock Generator unit lock error D4: GP0 0: clear 1: set D3: GP1 0: clear 1: set |

6. Read Operation during RUN

6-1. CRAM Write Preparation Read (during RUN)

| Field | Write data | Readout data |
|------------------|------------|---------------|
| (1) COMMAND Code | 0x24 | |
| (2) ADDRESS1 | | A15~A8 |
| (3) ADDRESS2 | | A8~A0 |
| (4) DATA1 | | D19~D12 |
| (5) DATA2 | | D11~D4 |
| (6) DATA3 | | D3~D0 0 0 0 0 |

6-2. OFREG Write Preparation Read (during RUN)

| Field | Write data | Readout data |
|------------------|------------|-----------------|
| (1) COMMAND Code | 0x24 | |
| (2) ADDRESS1 | | A15~A8 |
| (3) ADDRESS2 | | A8~A0 |
| (4) DATA1 | | 0 0 0 0 0 0 0 0 |
| (5) DATA2 | | 0 0 0 D12~D8 |
| (6) DATA3 | | D7~D0 |

6-3. MIR1/2/3/4 Read (during RUN)

| Field | Write data | Readout data |
|------------------|--|---|
| (1) COMMAND Code | 0x76(MIR1) 0x78(MIR2) 0x7A(MIR3) 0x7C(MIR4) | |
| (2) DATA1 | | D27~D20 |
| (3) DATA2 | | D19~D12 |
| (4) DATA3 | | D11~D4 |
| (5) DATA4 | | D3 D2 D1 D0 (flag3) (flag2) (flag1) (flag0) |

Note 86. Data is valid only when all flags are zero.

7. Timing (DLRDY bit = "1")

7-1. RAM Writing Timing during DSP Reset

Write to Program RAM (PRAM), Coefficient RAM (CRAM) and Offset REG (OFREG) during DSP reset in the order of command code, address and data. The PRAM start address is fixed to 0h. When writing the data to consecutive address locations, continue to input data only. PRAM address is incremented by 1 automatically.

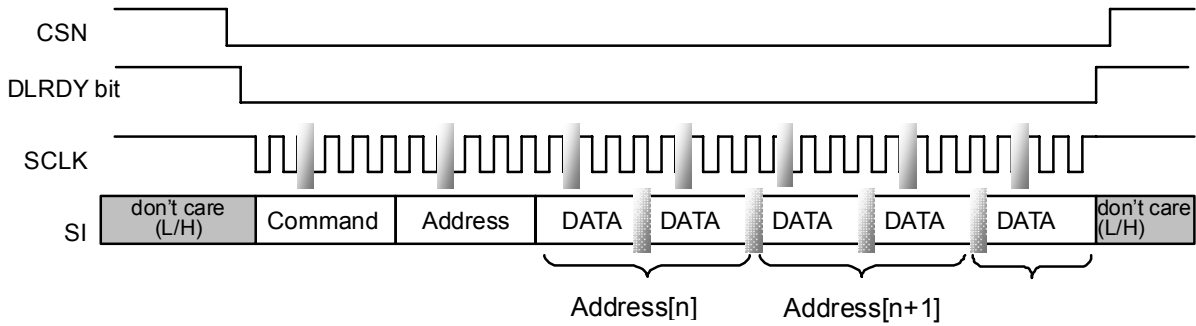


Figure 138. Writing to RAM at Consecutive Address Locations

When writing data at specified address locations, set the CSN pin to "L" from "H" and then input command code, address and data in this order.

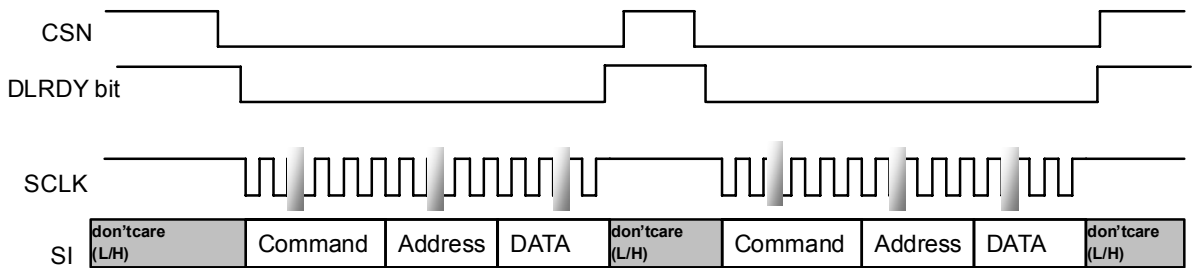


Figure 139. Writing to RAM at specified Address Locations

7-2. RAM Writing Timing during RUN

These operations are to rewrite Coefficient RAM (CRAM) and Offset REG (OFREG) during RUN. Data writing is executed in 2step; write preparation and write execution. The writing data can be confirmed by reading write preparation data.

1. Write Preparation

After inputting the assigned command code (8-bit) to select the number of data from 1 to 16, input the starting address of write (16-bit all 0) and the number of data assigned by command code in this order.

2. Write Preparation Data Confirmation

After write preparation, prepared data for writing can be confirmed. Address and Data are read in this order by write preparation data confirmation command “24h”. The data will be “0x000001” when reading more than write preparation data. Execute write preparation again when the address and data are garbled by external noise.

3. Write Execution

Upon completion of this operation, execute RAM write during RUN by inputting the corresponding command code and address (16-bit all “0”) in this order.

Note 87. Execute Write preparation before a write execution. When writing to RAM without write preparation sequence, a malfunction occurs. Access operation by microcontroller is prohibited until RDY changes to “H”.

Write modification of RAM contents is executed whenever the RAM address for modification is assigned. For example, when 5 Data are written, from RAM address “10”, it is executed as shown below.

| | | | | | | | | | | | | |
|--------------------------|---|---|---|----|----|----|----|----|----|----|----|----|
| RAM execution address | 7 | 8 | 9 | 10 | 11 | 13 | 16 | 11 | 12 | 13 | 14 | 15 |
| Write execution position | | | | ○ | ○ | ↑ | | | ○ | ○ | ○ | |

Note: Address “13” is not executed until rewriting address “12”.

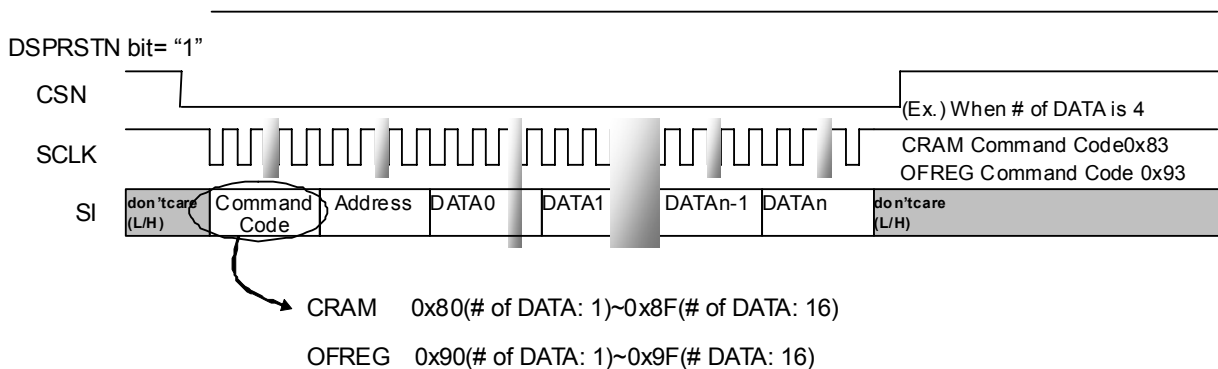


Figure 140. CRAM/OFREG Write Preparation

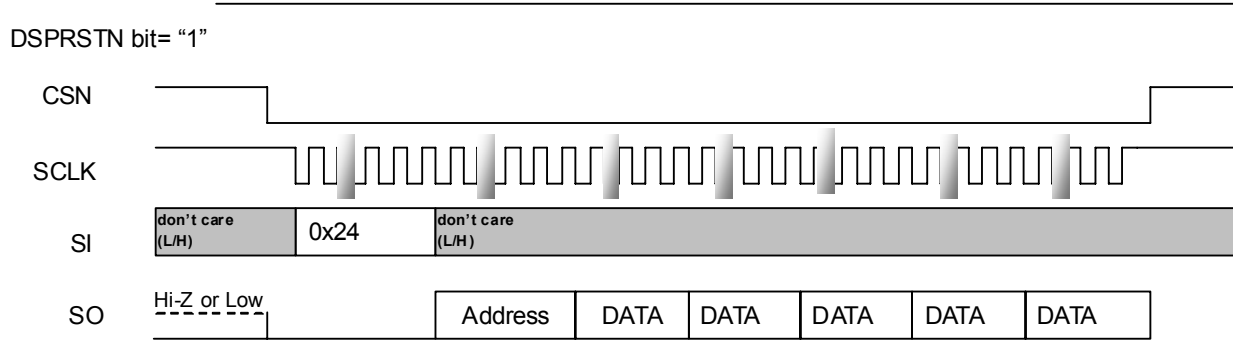


Figure 141. CRAM/OFREG Write Preparation Confirm

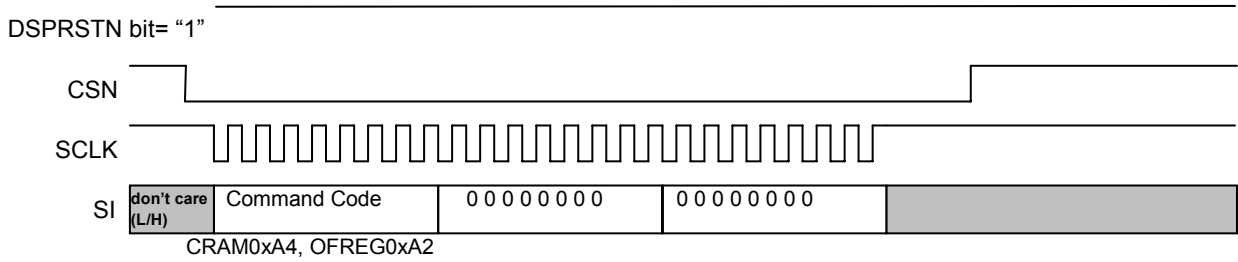


Figure 142. CRAM/OFREG Write

7-3. External Conditional Jump

External Conditional Jump Code Writing (during DSP Reset and RUN)

| | |
|-------------|-------|
| (1) COMMAND | 0xF4 |
| (2) DATA | D7~D0 |

External Conditional Jump code can be input during both DSP Reset and RUN. Input data is set to the designated register on the rising edge of SYNC. The RDY pin changes to “L” when the command code is transferred, and it changes to “H” when write operations are completed. When any single bit of “1” data in 8-bit External Jump code matches an “1” bit data in the IFCON field, a Jump instruction is executed. Then, the RDY pin changes to “H” when the rise of SYNC is captured. Access operation by microcontroller is prohibited until the RDY pin changes to “H”. IFCON field is the area where the external conditions are written. This Jump code is reset to 00h by setting the IRSTN pin to “L”, but it is not reset by DSP Reset.

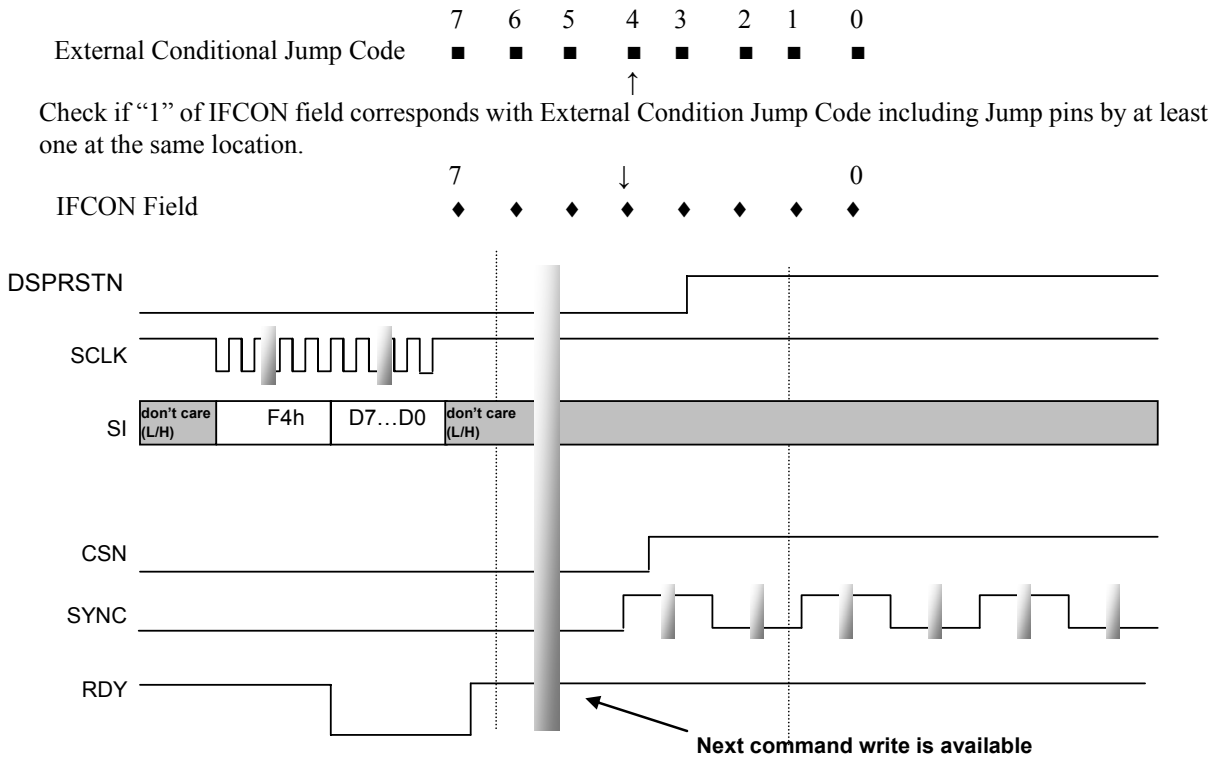


Figure 143. External Conditional Timing (in DSP Reset)

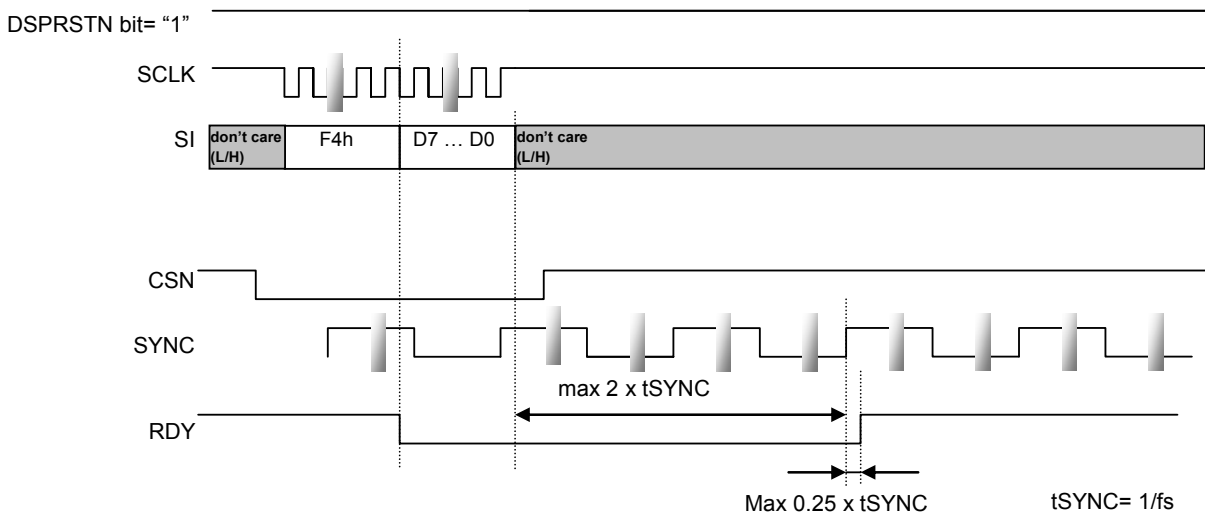


Figure 144. External Conditional Jump Timing (during RUN)

7-4. RAM Reading Timing during DSP Reset

Read Program RAM (PRAM), Coefficient RAM (CRAM) and Offset REG (OFREG) during DSP Reset in the order of input Command code and Address. PRAM address is fixed to 0h. After writing the Command, the data comes out from the SO pin synchronous with falling edge of SCLK. (The SI pin input data is “Don’t care”) When reading Data at consecutive address locations, continue to input SCLK as is.

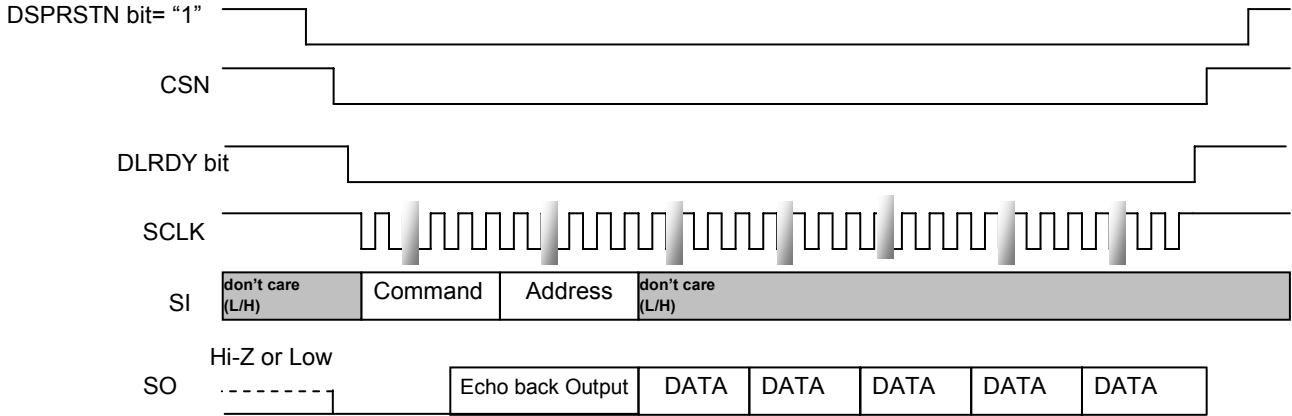


Figure 145. RAM Reading at Consecutive Address

7-5. RAM Reading Timing during DSP Reset and RUN

Input control register, device identification code, CRC result and error status during both RUN time and DSP Reset state. These codes are input in the order of Command and Address. After completing Command code write, the data comes out from the SO pin synchronous with falling edge of SCLK. (The SI pin input data is “Don’t care”)

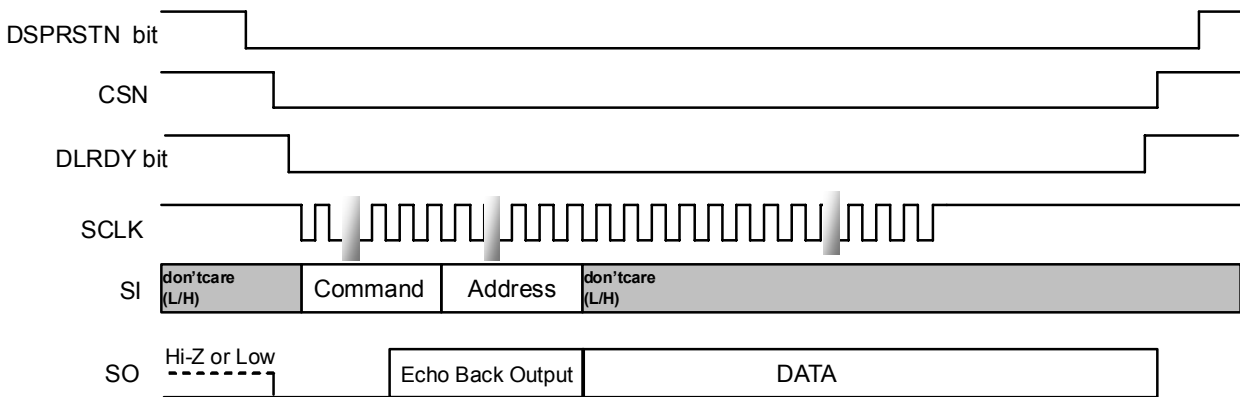
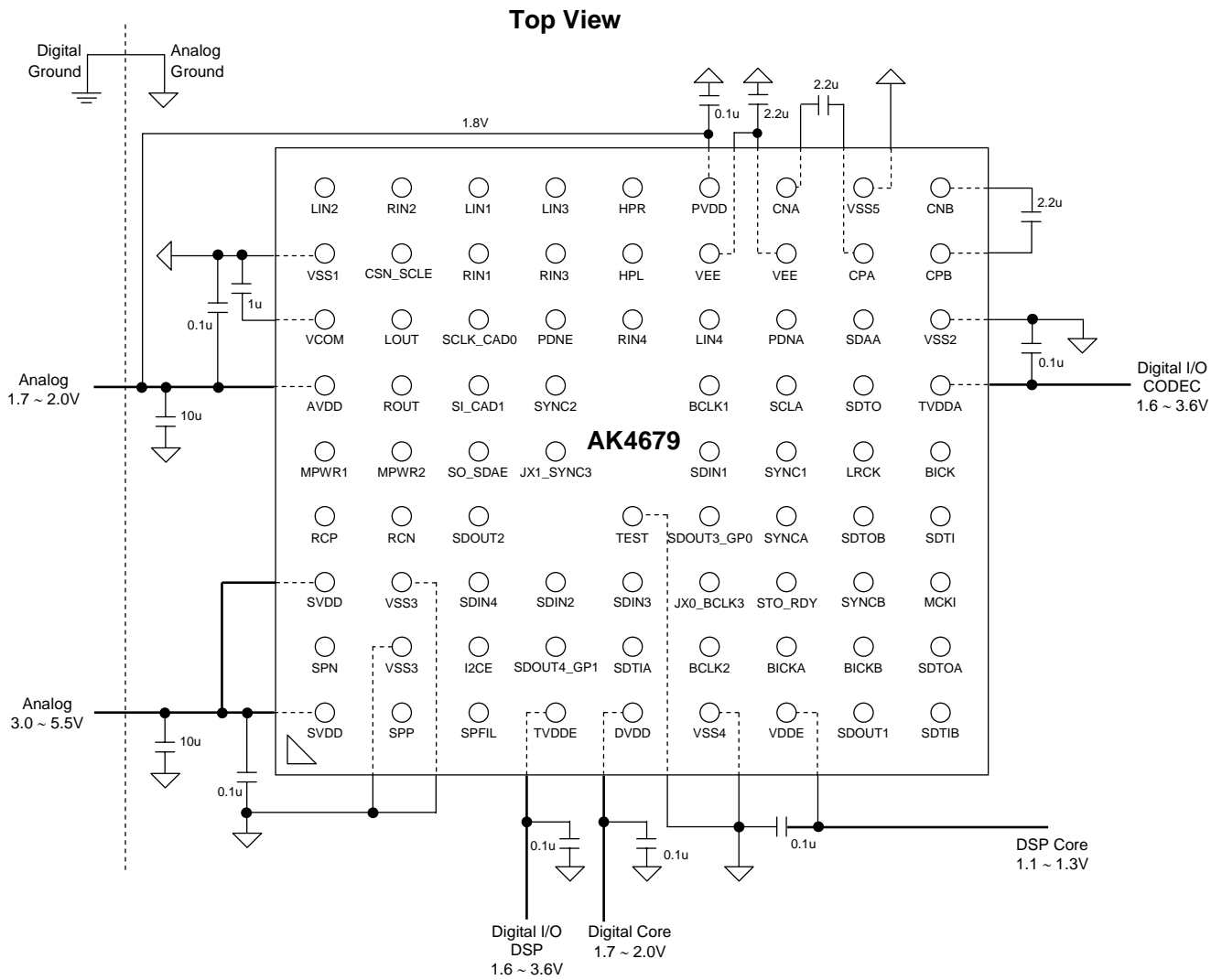


Figure 146. RAM Reading during DSP Reset and RUN

SYSTEM DESIGN

Figure 147 and Figure 148 show the system connection diagram for the AK4679. An evaluation board [AKD4679] demonstrates the optimum layout, power supply arrangements and measurement results.



Note:

- VSS1, VSS2, VSS3, VSS4 and VSS5 of the AK4679 should be distributed separately from the ground of external controllers.
- 0.1μF capacitors at power supply pins should be ceramic capacitors. 2.2μF±50% capacitors between the CPA to CNA pins, the CPB to CNB pins and the VEE to VSS5 pins should be low ESR ceramic capacitors. These capacitors must be connected as close as possible to the pins.

Figure 147. Typical Connection Diagram (Power Supply Block)

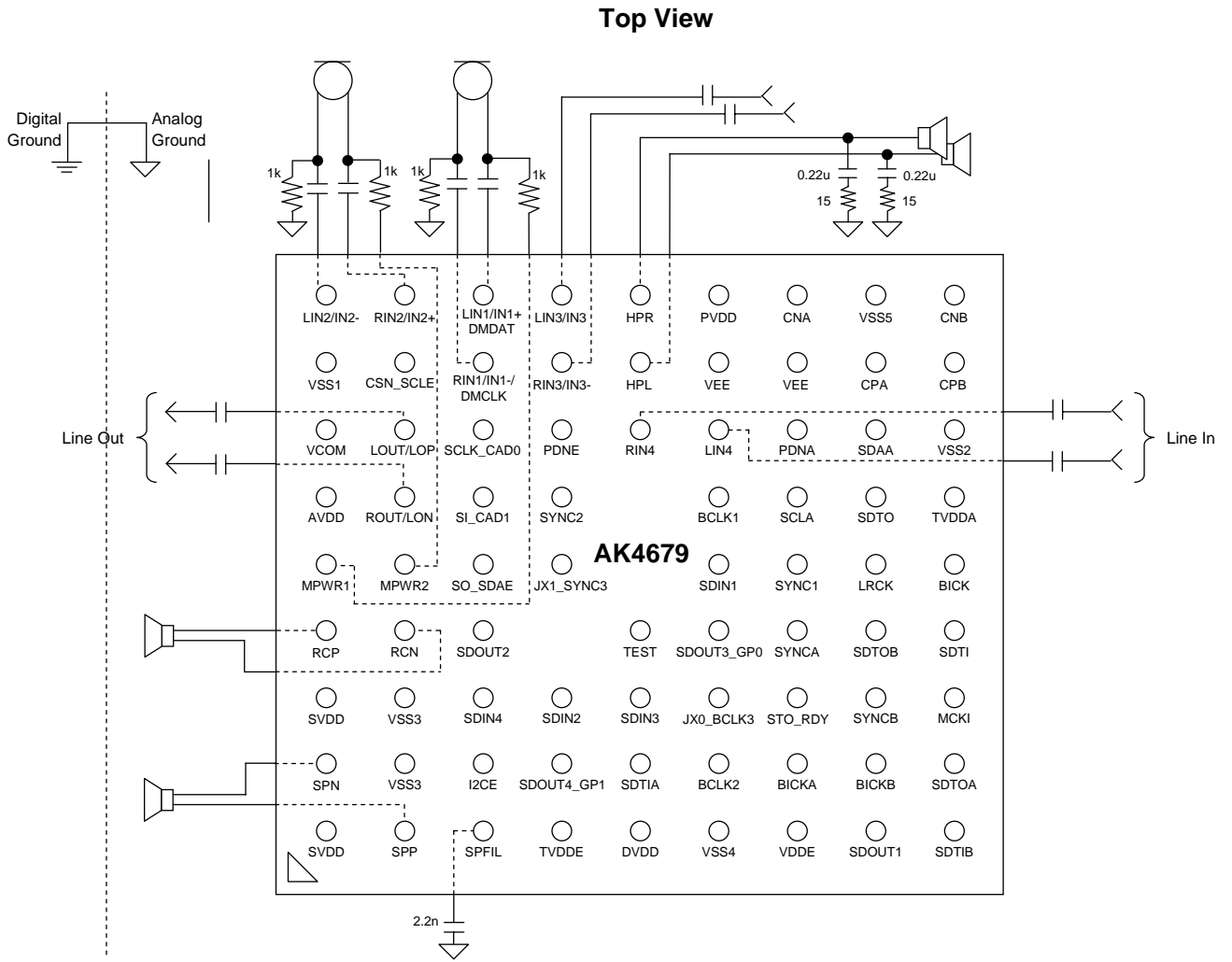


Figure 148. Typical Connection Diagram (Analog Input/Output Block)
 (In case of Internal Full-differential Mic and External pseudo differential Mic)

Typical signal connections are shown in [Figure 38](#).

1. Grounding and Power Supply Decoupling

The AK4679 requires careful attention to power supply and grounding arrangements. AVDD, PVDD and SVDD are usually supplied from the system's analog supply, and DVDD, TVDDA, TVDDE and VDDE are supplied from the system's digital power supply. The power-up sequence between supplies (AVDD, PVDD, SVDD, DVDD, TVDDA, TVDDE or VDDE) is not critical. PDNA and PDNE pins should be held "L" when power supplies are tuning on. PDNA and PDNE pins are allowed to be "H" after all power supplies are applied and settled.

To avoid pop noise at receiver output, headphone outputs, speaker output and line outputs, the AK4679 should be operated along the following recommended power-up/down sequence.

1) Power-up

- PDNA and PDNE pins should be held "L" when power supplies are turning on. The AK4679 can be reset by keeping the PDNA pin "L" for 1.5 μ s or longer after all power supplies are applied and settled.
- In the case that the power supplies are separated in two or more groups, SVDD should be powered ON first.

2) Power-down

- Each of power supplies can be powered OFF after PDNA and PDNE pins are set to "L".
- In the case that the power supplies are separated in two or more groups, SVDD should be powered OFF last.

VSS1~5 of the AK4679 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near the AK4679 as possible. Especially, the small value ceramic capacitor is to be closest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 1 μ F electrolytic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4679.

3. Charge Pump

2.2 μ F \pm 50% capacitors between the CPA to CNA pins, the CPB to CNB pins and the VEE to VSS5 pins should be low ESR ceramic capacitors. These capacitors must be connected as close as possible to the pins. No load current may be drawn from the VEE pin.

4. Analog Inputs

The input signal range scales with 1.0 x AVDD V_{pp} (typ) at MGNL=MGNR=0dB, AVDD=1.8V and single-ended input, centered around the internal common voltage (typ. 0.47 x AVDD). The input signal must be AC coupled using a capacitor. The cut-off frequency (f_c) is 1/(2 π RC).

5. Analog Outputs

Stereo Line outputs and Mono Receiver output are centered at typ. 0.8 x AVDD. Stereo line output (LOUT/ROUT pins) must be AC –coupled using a capacitor. Receiver output (RCP/RCN pins) should be connected directly to a receiver. Headphone outputs (HPL/HPR pin) are centered at 0V and should be directly connected to a headphone. Speaker output is PWM output (Class-D) and it is not necessary to add an external filter such as LC filters.

CONTROL SEQUENCE (AUDIO)

■ Clock Set-up

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied.

1. PLL Master Mode

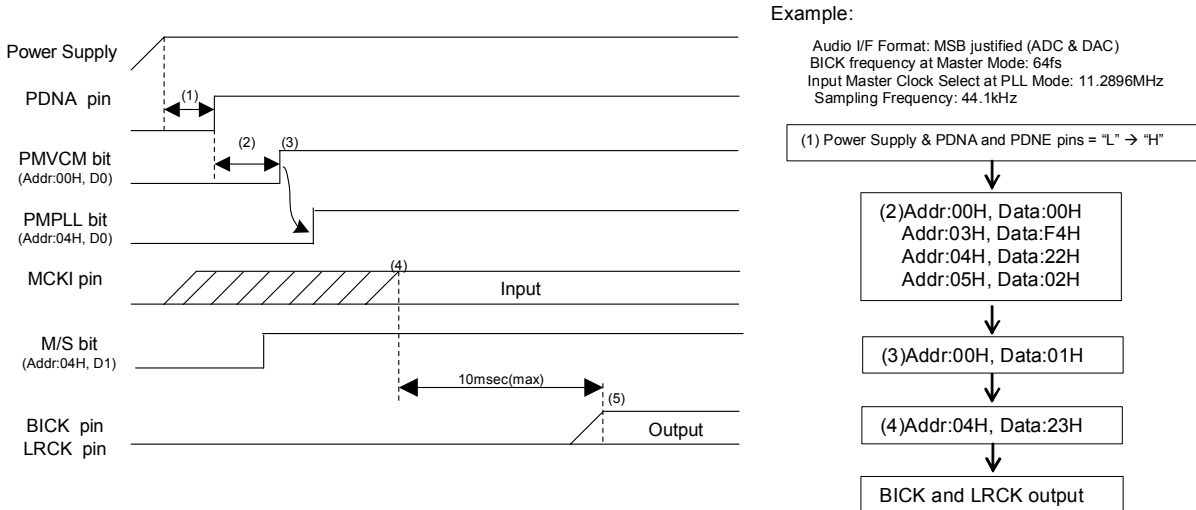


Figure 149. Clock Set Up Sequence (1)

<Example>

- (1) After Power Up, PDNA pins = "L" → "H".
"L" time of 1.5μs or more is needed to reset the AK4679.
- (2) Dummy command (Addr:00H, Data:00H) must be executed before control register is set.
DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates. Power-up time of VCOM is maximum 1.5ms when the external capacitor connected to the VCOM pin is 1μF.
- (4) PLL lock time is 10ms(max.) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
- (5) The AK4679 starts to output the LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.

2. PLL Slave Mode (BICK pin)

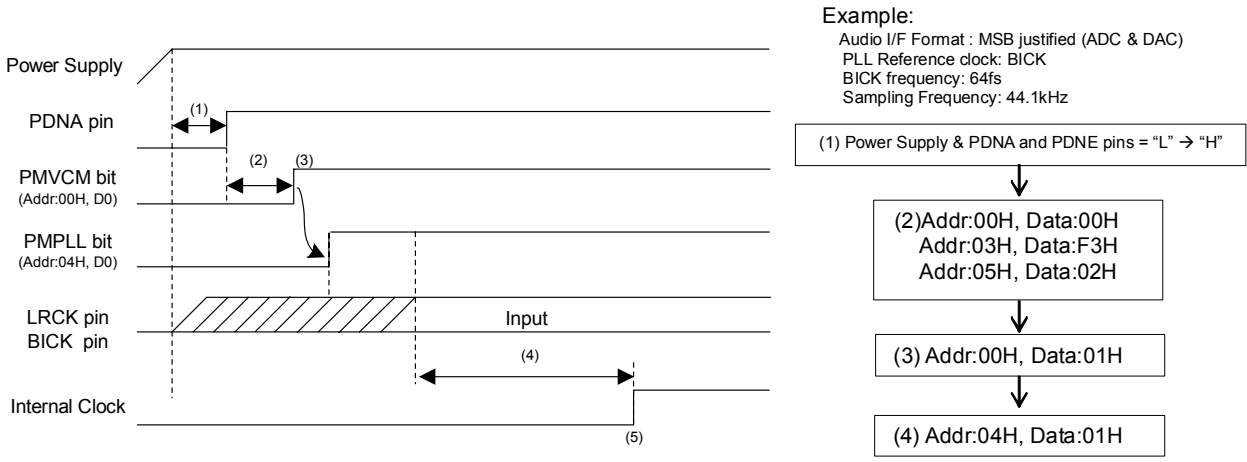


Figure 150. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up, PDNA pin = "L" → "H".
 "L" time of 1.5μs or more is needed to reset the AK4679.
- (2) Dummy command (Addr:00H, Data:00H) must be executed before control register is set. DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates. Power-up time of VCOM is maximum 1.5ms when the external capacitor connected to the VCOM pin is 1μF.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max.).
- (5) Normal operation starts after that the PLL is locked.

3. EXT Slave Mode

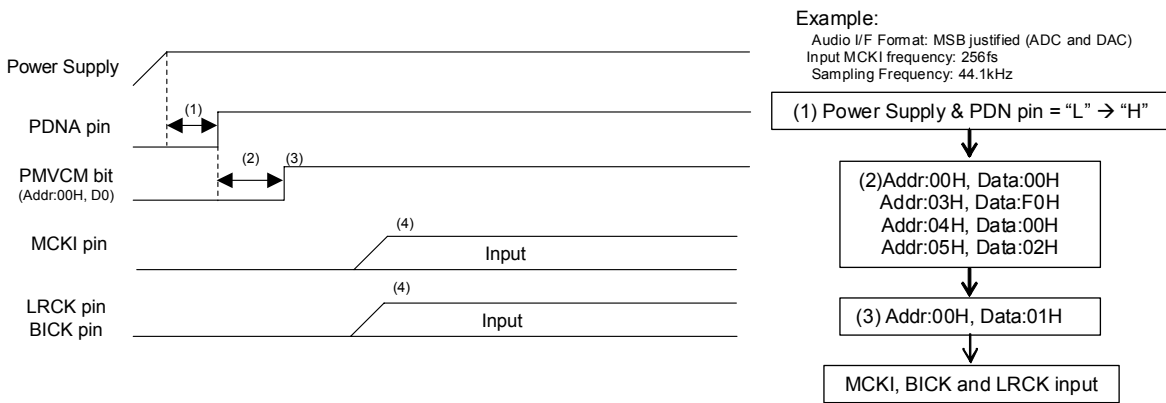


Figure 151. Clock Set Up Sequence (3)

<Example>

- (1) After Power Up, PDNA pin = "L" → "H".
 "L" time of 1.5μs or more is needed to reset the AK4679.
- (2) Dummy command (Addr:00H, Data:00H) must be executed before control register is set.
 DIF1-0, CM1-0 and FS3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates. Rise-up time of the VCOM pin is 1.5ms (max) when the external capacitance is 1μF.
- (4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

4. EXT Master Mode

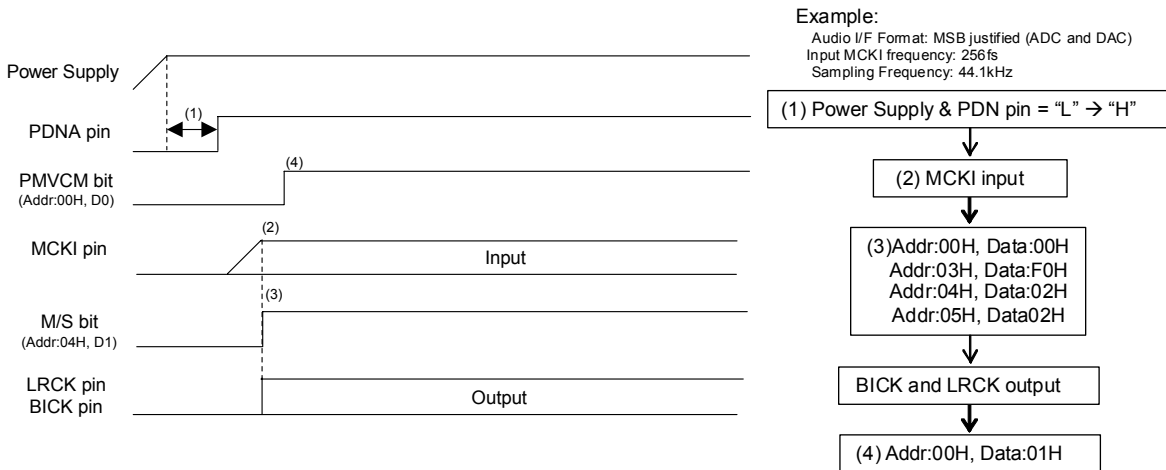


Figure 152. Clock Set Up Sequence (4)

<Example>

- (1) After Power Up, PDNA pin = "L" → "H".
 "L" time of 1.5μs or more is needed to reset the AK4679.
- (2) MCKI should be input.
- (3) Dummy command (Addr:00H, Data:00H) must be executed before control register is set.
 After DIF1-0, CM1-0 and FS3-0 bits are set, M/S bit should be set to "1". Then LRCK and BICK are output.
- (4) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates. Power-up time of VCOM is maximum 1.5ms when the external capacitor connected to the VCOM pin is 1μF.

■ MIC Input Recording (Stereo)

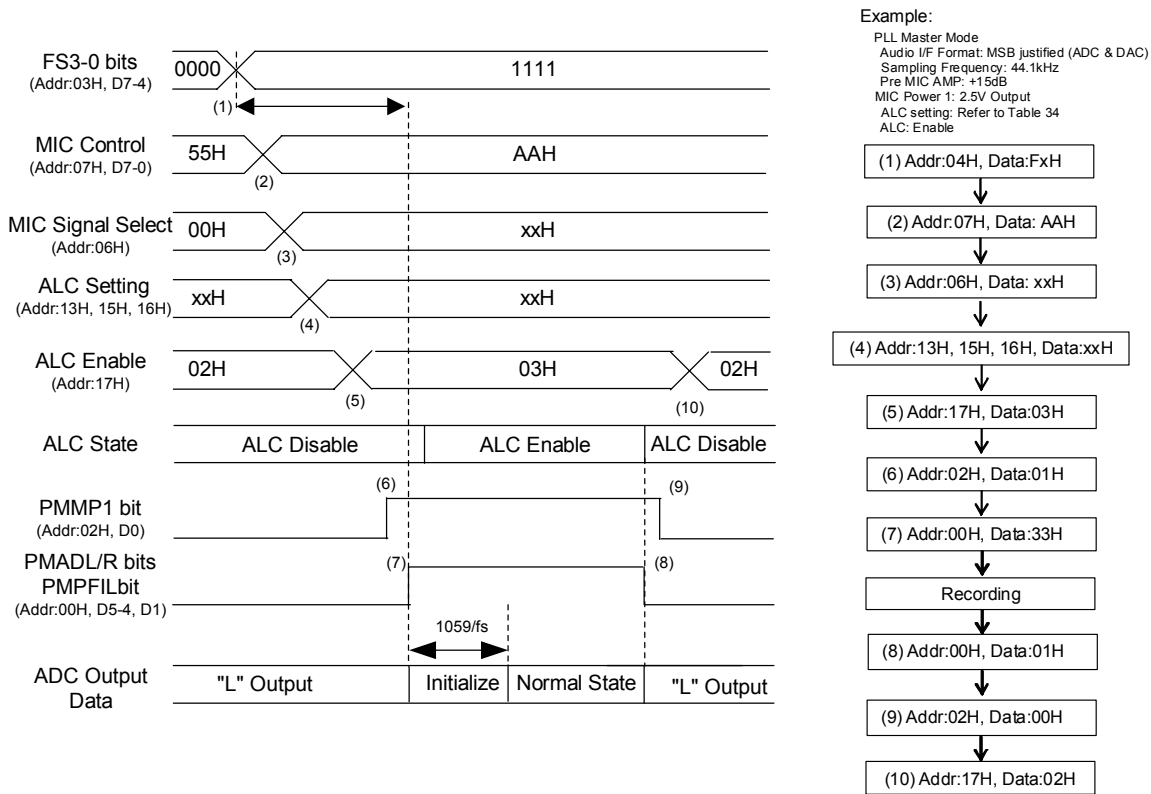


Figure 153. Stereo MIC Input Sequence
 (MIC Recording: LINx/RINx → MICL/R → ADCL/R → ALC → Audio I/F → SDTO)

<Example>

This sequence is an example of ALC setting at $f_s=44.1\text{kHz}$. If the parameter of the ALC is changed, please refer to “Example of the ALC setting (Recording Path)”.

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). MIC, ADC and Programmable Filter should be powered-up in consideration of VCOM ride time and PLL lock time after a sampling frequency is changed when the AK4679 is in PLL mode.
- (2) Set up Gain for MIC-Amp (Addr: 07H)
- (3) Set up MIC Input Selector (Addr: 06H)
- (4) Set up REF value for ALC (Addr: 13H), Timer Select for ALC (Addr: 15H) and ALC mode (Addr: 16H)
- (5) ALC Enable (Addr: 17H): ALC bit = “0” → “1”
- (6) Power Up MIC Power1: PMMP1 bit = “0” → “1”
- (7) Power Up MIC-Amp, ADC and Programmable Filter: PMADL/R = PMPFIL bits = “0” → “1”
 The initialization cycle time of ADC is $1059/f_s=24\text{ms}$ @ $f_s=44.1\text{kHz}$, ADRST bit = “0”. ADC outputs “0” data during the initialization cycle. After the ALC bit is set to “1”, the ALC operation starts from IVOL value
- (8) Power Down MIC-Amp, ADC and Programmable Filter: PMADL/R = PMPFIL bits = “1” → “0”
 When the registers for the ALC operation are not changed, ALC bit may be keeping “1”. The ALC operation is disabled because the ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK4679 goes to the manual mode (ALC bit = “0”) or ADC block is powered-down (PMADL = PMADR bits = “0”). IVOL gain is not reset when PMADL = PMADR bits = “0”, and then IVOL operation starts from the setting value when PMADL or PMADR bit is changed to “1”.
- (9) Power Down MIC Power 1: PMMP1 bit = “1” → “0”
- (10) ALC Disable: ALC bit = “1” → “0”

■ Headphone-Amp Output

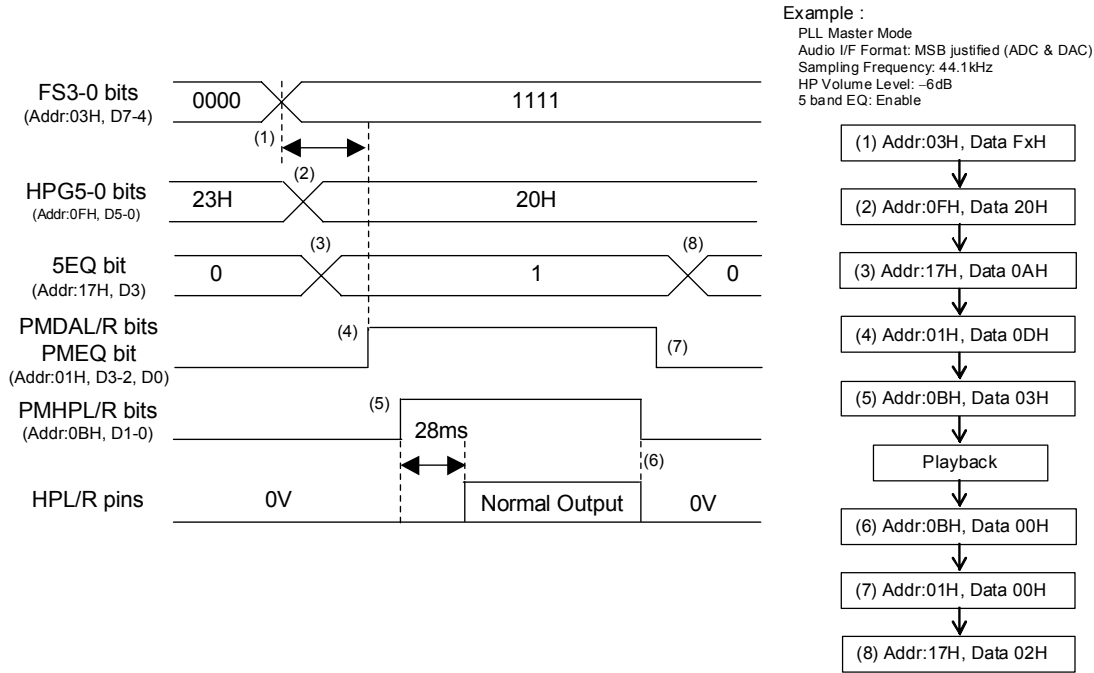


Figure 154. Headphone-Amp Output Sequence
(Headphone Playback: SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → HPL/HPR)

<Example>

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). DAC and Headphone-Amp should be powered-up in consideration of VCOM rise time and PLL lock time after a sampling frequency is changed when the AK4679 is in PLL mode.
- (2) Set up analog volume for HP-Amp (Addr: 0FH, HPG5-0 bits)
- (3) Enable 5-band Equalizer: 5EQ bit = “0” → “1” (Frequency Response and gain are selected by Addr = 50H-6EH.)
- (4) Power up DAC and EQ : PMDAL = PMDAR = PMEQ bits = “0” → “1”
- (5) Power up Headphone-Amp and charge pump circuit: PMHPL = PMHPR bits = “0” → “1”
The power-up time of HP-Amp block is 28ms. HPL and HPR pins output 0V until the power-up time of HP-Amp block passes.
- (6) Power down Headphone-Amp and charge pump circuit: PMHPL = PMHPR bits = “1” → “0”
HPL and HPR pins go to 0V.
- (7) Power down DAC and EQ: PMDAL = PMDAR = PMEQ bits = “1” → “0”
- (8) Disable 5-band Equalizer: 5EQ bit = “1” → “0”

■ Speaker-Amp Output

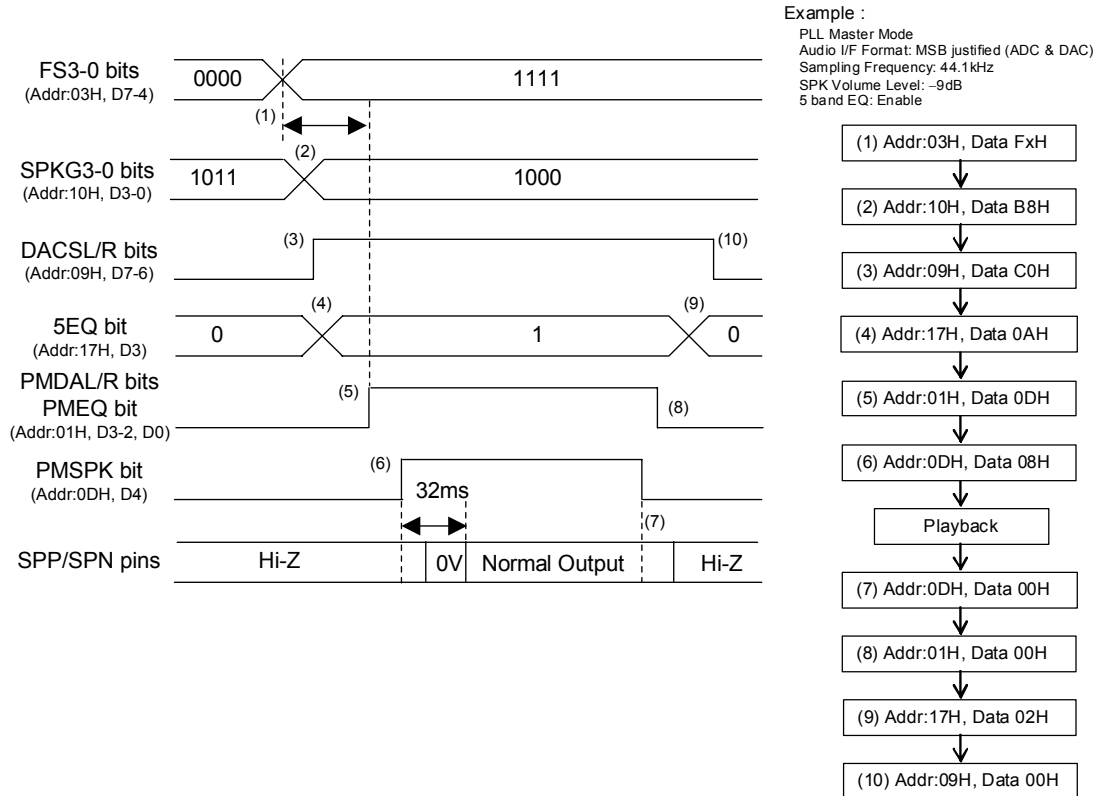


Figure 155. Speaker-Amp Output Sequence

(Headphone Playback: SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → SPP/SPN)

<Example>

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). DAC and Speaker-Amp should be powered-up in consideration of VCOM rise time and PLL lock time after a sampling frequency is changed when the AK4679 is in PLL mode.
- (2) Set up analog volume for SPK-Amp (Addr: 10H, SPKG3-0 bits)
- (3) Set up the path of “SDTI → DAC → SPK-Amp”: DACSL = DACSR bits = “0” → “1”
- (4) Enable 5-band Equalizer: 5EQ bit = “0” → “1” (Frequency Response and gain are selected by Addr = 50H-6EH.)
- (5) Power up DAC and EQ: PMDAL = PMDAR = PMEQ bits = “0” → “1”
- (6) Power up SP-Amp block: PMSPK bit = “0” → “1”
The power-up time of SPK-Amp block is 32ms. SPP and SPN pins output 0V until the power-up time of SPK-Amp block passes.
- (7) Power down SPK-Amp block: PMSPK bit = “1” → “0”
SPN and SPP pins go to 0V.
- (8) Power down DAC and EQ: PMDAL = PMDAR = PMEQ bits = “1” → “0”
- (9) Disable 5-band Equalizer: 5EQ bit = “1” → “0”
- (10) Disable the path of “DAC → Speaker-Amp”: DACSL = DACSR bits = “1” → “0”

■ Stereo Line Output

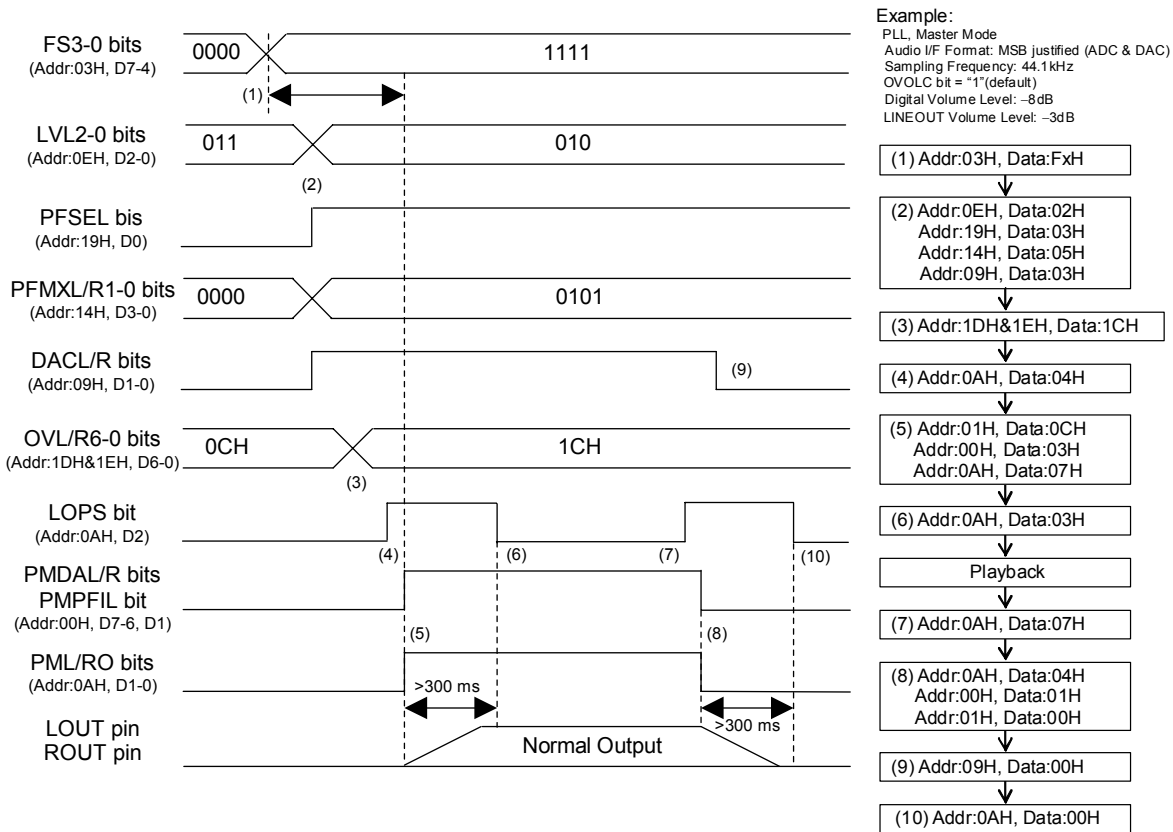


Figure 156. Stereo Lineout Sequence

(Lineout Playback: SDTI → Audio I/F → SVOLA → DATT-A → DACL/R → LOUT/ROUT)

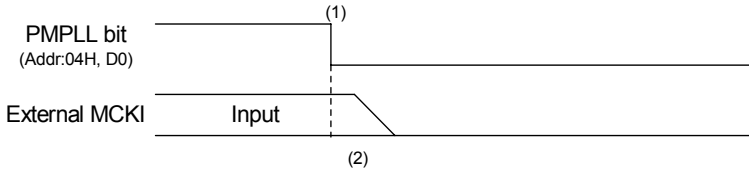
<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

- (1) Set up the sampling frequency (FS3-0 bits). DAC and Stereo Line-Amp should be powered-up in consideration of VCOM rise time and PLL lock time after the sampling frequency is changed when the AK4679 is in PLL mode.
- (2) Set up the path of "SDTI → DAC → Stereo Line-Amp": PFSEL = "0" → "1", PFMXL1-0 = PFMXR1-0 bits = "0000" → "0101", DACL = DACR bits = "0" → "1"
 Set up analog volume for Stereo Line-Amp (Addr: 0EH, LVL2-0 bits)
- (3) Set up the output digital volume (Addr: 1DH and 1EH)
 When OVOLC bit is "1" (default), OVL6-0 bits (1DH) set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (4) Enter power-save mode of Stereo Line-Amp: LOPS bit = "0" → "1"
- (5) Power-up DAC, Programmable Filter and Stereo Line-Amp: PMDAL = PMDAR = PMPFIL = PMLO = PMRO bits = "0" → "1"
 LOUT and ROUT pins rise up to VCOM voltage after PMLO and PMRO bits are changed to "1". Rise time is 300ms (max.) at C=1μF and AVDD=1.8V.
- (6) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
 LOPS bit should be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".
- (7) Enter power-save mode of Stereo Line-Amp: LOPS bit: "0" → "1"
- (8) Power-down DAC, Programmable Filter and Stereo Line-Amp: PMDAL = PMDAR = PMPFIL = PMLO = PMRO bits = "1" → "0"
 LOUT and ROUT pins fall down to VSS1. Fall time is 300ms(max.) at C=1μF and AVDD=1.8V.
- (9) Disable the path of "DAC → Stereo Line-Amp": DACL = DACR bits = "1" → "0"
- (10) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
 LOPS bit should be set to "0" after LOUT and ROUT pins fall down.

■ Stop of Clock

1. PLL Master Mode



Example:

Audio I/F Format: MSB justified (ADC & DAC)
 BICK frequency at Master Mode: 64fs
 Input Master Clock Select at PLL Mode: 11.2896MHz
 Sampling Frequency: 44.1kHz

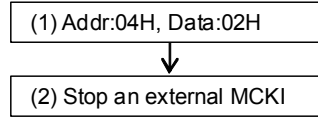
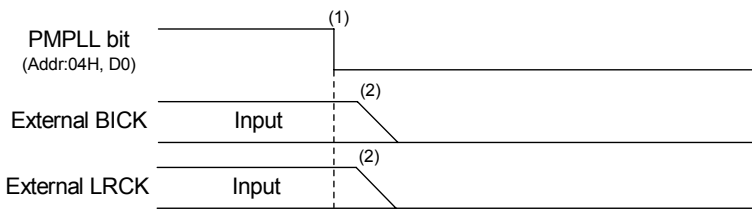


Figure 157. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLL: PMPLL bit = “1” → “0”
- (2) Stop an external MCKI clock.

2. PLL Slave Mode (BICK pin)



Example

Audio I/F Format: MSB justified (ADC & DAC)
 PLL Reference clock: BICK
 BICK frequency: 64fs
 Sampling Frequency: 44.1kHz

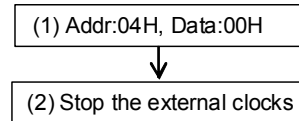


Figure 158. Clock Stopping Sequence (2)

<Example>

- (1) Power down PLL: PMPLL bit = “1” → “0”
- (2) Stop the external BICK and LRCK clocks.

3. EXT Slave Mode

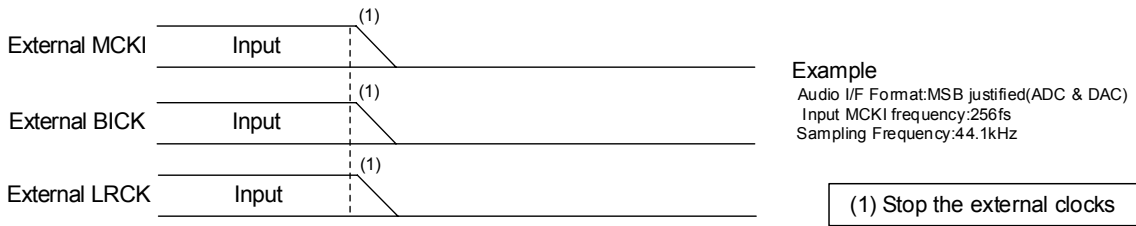


Figure 159. Clock Stopping Sequence (3)

<Example>

(1) Stop the external MCKI, BICK and LRCK clocks.

4. EXT Master Mode

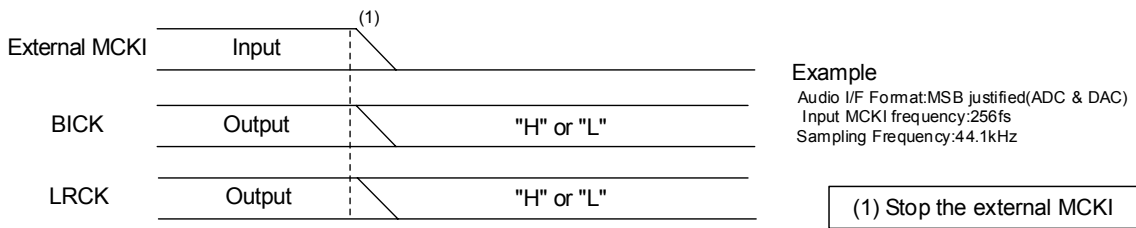


Figure 160. Clock Stopping Sequence (4)

<Example>

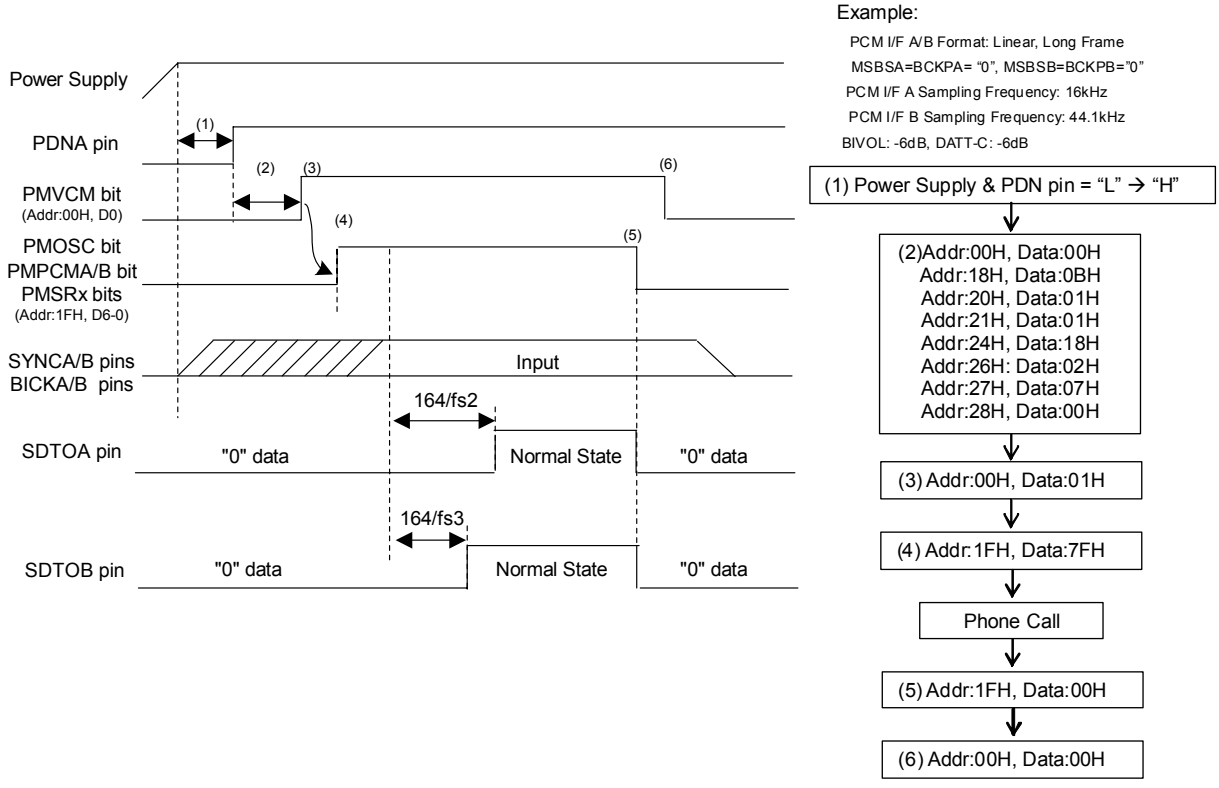
(1) Stop MCKI clock. BICK and LRCK are fixed to "H" or "L".

■ Power down

Power supply current can be shut down (typ. 50µA) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1µA) by stopping clocks and setting the PDNA pin = "L". When the PDNA pin = "L", the registers are initialized.

CONTROL SEQUENCE (PCM)

■ PCM I/F A(Baseband) to PCM I/F B(Bluetooth)



Note: PMSRx bit means PMSRAI, PMSRAO, PMSRBI and PMSRBO bits

Figure 161. Sequence of PCM I/F A to PCM I/F B

(Baseband RX to Bluetooth TX: SDTIA→PCM I/F A→SRCAI→DATT-C→MIX3→PCM I/F B→SDTOB & Bluetooth RX to Baseband TX: SDTIB→PCM I/F B→BIVOL→MIX2A→MIX2C→SRCAO→PCM I/F A→SDTOA)

<Example>

- (1) After Power Up, PDNA pin = "L" → "H". "L" time of 1.5μs or more is needed to reset the AK4679.
- (2) Dummy command (Addr:00H, Data:00H) must be executed before control register is set.
 OVTMB, BIV2-0, SDOA/BD, FMTA/B1-0, LAWA/B1-0, BCKPA/B, MSBSA/B, CVL6-0, MX2A1-0, MX2C1-0, MXSB2-0, SBMX1-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) Power Up Internal Oscillator, SRCAI, SRCAO, SRCBI, SRCBO, PCM I/F A port and PCM I/F B port.
 PMSRBO=PMSRBI=PMPCMB=PMOSC=PMSRAO=PMSRAI=PMPCMA bits: "0" → "1"
 SDTOA(SDTOB) outputs data after power-down state is released by inputting SYNCA(SYNCB). This initial of SRCAO(SRCBO) is 164/fs2(164/fs3) for SDTOA(SDTOB) output enable after power-down state is released by inputting SYNCA(SYNCB).
- (5) Power down Internal Oscillator, SRCAI, SRCAO, SRCBI, SRCBO, PCM I/F A port and PCM I/F B port.
 PMSRBO=PMSRBI=PMPCMB=PMOSC=PMSRAO=PMSRAI=PMPCMA bits: "1" → "0"
- (6) Power Down VCOM: PMVCM bit = "1" → "0"

Receiver-Amp Output

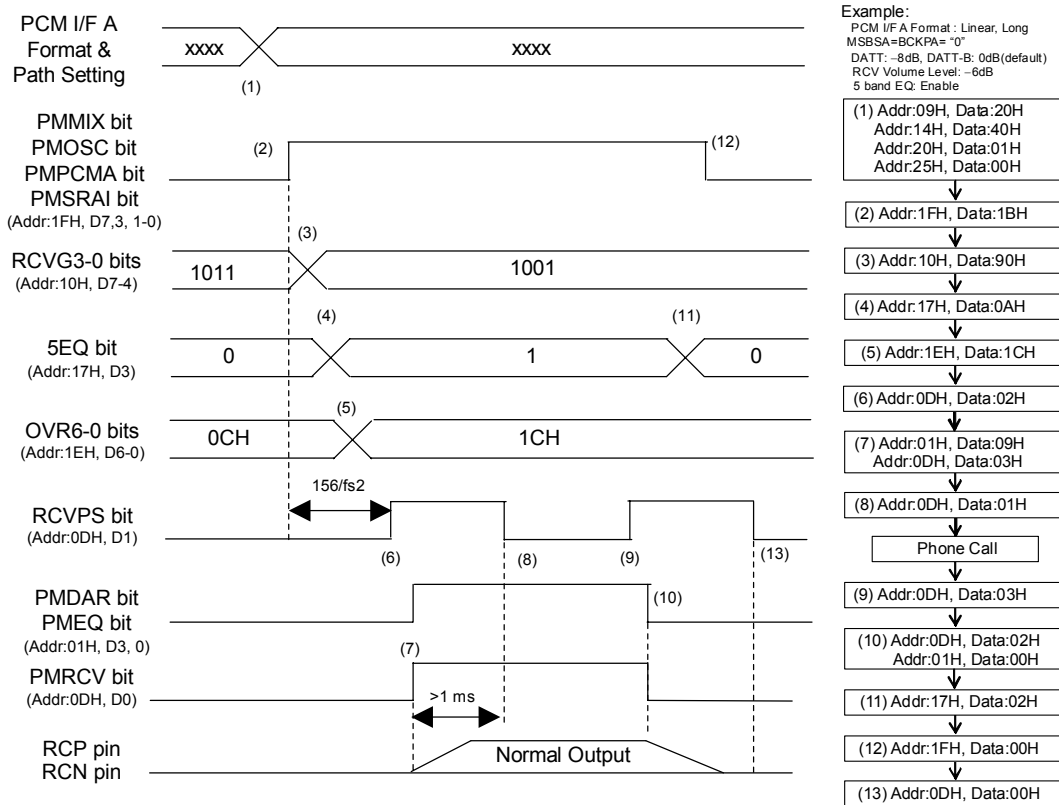


Figure 162. Receiver-Amp Output Sequence

(Baseband Rx: SDTIA→PCM I/F A→SRCAI→DATT-B→MIX1R→5-Band EQ→DATT-A→DACR→RCP/RCN)

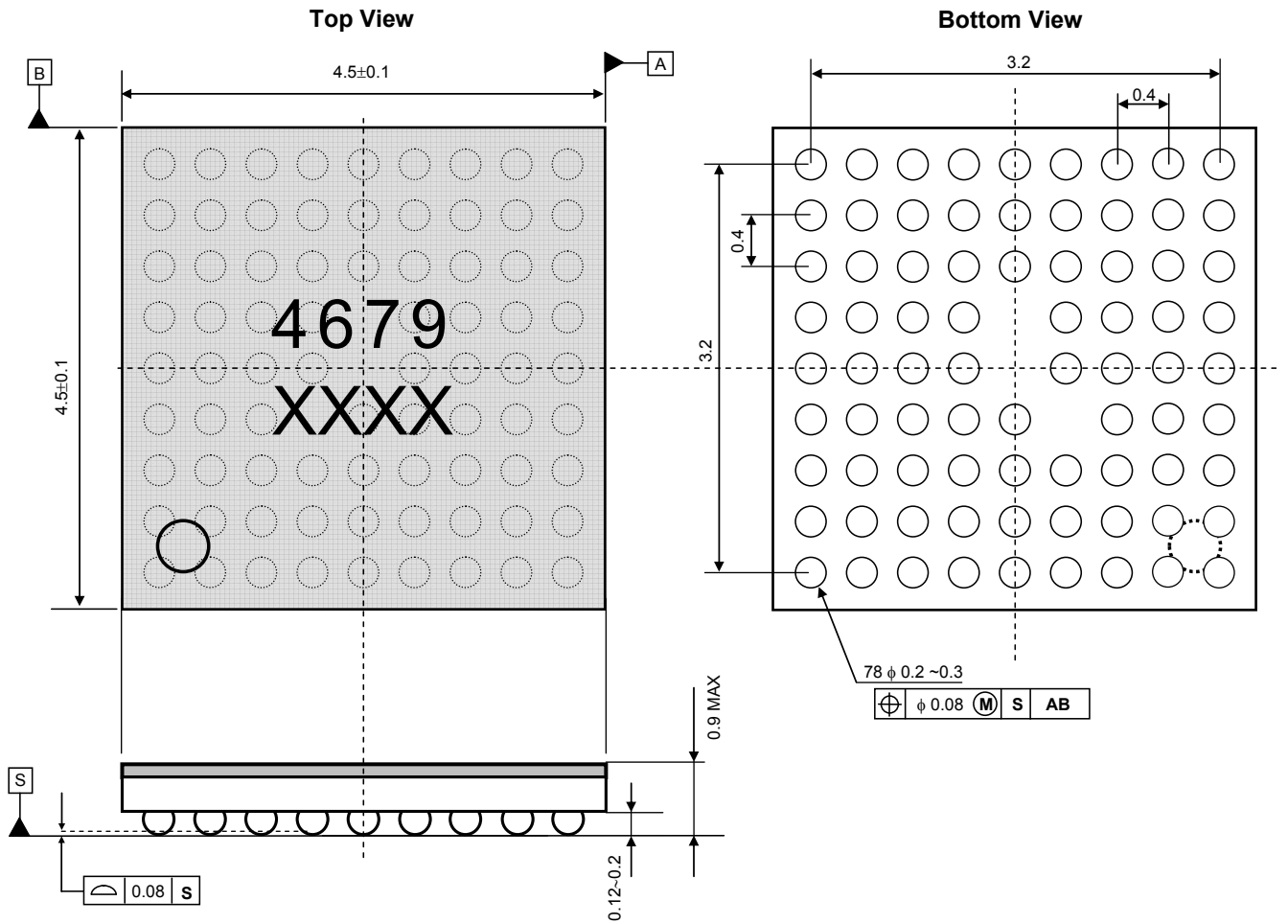
<Example>

At first, audio clocks should be supplied according to "Clock Set Up" sequence. DAC and Receiver-Amp should be powered-up in consideration of VCOM rise time

- (1) Set up the format of PCM I/F A(FMTA1-0, LAWA1-0, BCKPA, MSBSA bits) and the path of "SDTIA → DAC → Receiver-Amp"(MX1R2-0 bits = "000" → "000", SRMXR1-0 bits = "00" → "01", DACRR bit = "0" → "1")
- (2) Power-up Internal Oscillator, MIX1 block and SRCAI: PMMIX = PMOSC = PMSRAI = PMPCMA bits = "0" → "1". The initial time of SRCAI is 164/fs2 after SYNCA clock is supplied.
- (3) Set up analog volume for Receiver-Amp (Addr: 10H, RCVG3-0 bits)
- (4) Enable 5-band Equalizer: 5EQ bit = "0" → "1" (Frequency Response and gain are selected by Addr = 50H-6EH.)
- (5) Set up the output digital volume (Addr: 1EH)
 After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (6) Enter power-save mode of Receiver-Amp: RCVPS bit = "0" → "1"
 After passing the initial time of SRCAI, the Receiver-Amp should enter power-save mode.
- (7) Power-up DAC, EQ and Receiver-Amp: PMDAR = PMEQ = PMRCV bits = "0" → "1"
 The RCN pin rises up to VCOM voltage after PMRCV bit is changed to "1".
- (8) Exit power-save mode of Receiver-Amp: RCVPS bit = "1" → "0"
 RCVPS bit should be set to "0" after the RCN pin rises up. Receiver-Amp goes to normal operation by setting RCVPS bit to "0".
- (9) Enter power-save mode of Receiver-Amp: RCVPS bit: "0" → "1"
- (10) Power-down DAC, EQ and Receiver-Amp: PMDAR = PMEQ = PMRCV bit = "1" → "0"
 Receiver-Amp becomes to power-down mode.
- (11) Disable 5-band Equalizer: 5EQ bit = "1" → "0"
- (12) Power-down Internal Oscillator, MIX1 block and SRCAI: PMOSC = PMMIX = PMSRAI and PMPCMA bits = "1" → "0"
- (13) Exit power-save mode of Receiver-Amp: RCVPS bit = "1" → "0"
 RCVPS bit should be set to "0" after Receiver-Amp power-down.

PACKAGE

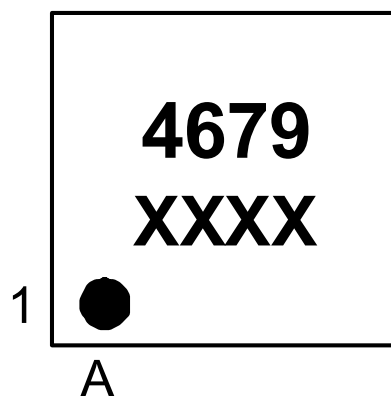
78pin BGA



■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
 Solder ball material: SnAgCu

| |
|----------------|
| MARKING |
|----------------|



XXXX: Date code (4 digit)
Pin #A1 indication

| |
|-------------------------|
| REVISION HISTORY |
|-------------------------|

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|--------------|----------|------------------|---------------------------|---|
| 12/04/23 | 00 | First Edition | | |
| 12/05/15 | 01 | Error Correction | 4, 8-12, 58, 59, 159, 201 | Pin names were corrected. LIN2/IN2+ → LIN2/IN2- RIN2/IN2- → RIN2/IN2+ |
| | | | 4 | ■ Block Diagram Figure 1 was changed. |
| | | | 59 | ■ MIC/LINE Input Selector Figure 53 was changed. |
| 12/08/30 | 02 | Error Correction | 201 | SYSTEM DESIGN Figure 148: A connection to the microphone was changed. |

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