AsahiKASEI
ASAHI KASEI EMD

AK4634

16-Bit Mono CODEC with ALC & MIC/SPK -AMP

GENERAL DESCRIPTION

The AK4634 is a 16-bit mono CODEC with Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit. Output circuits include a Speaker-Amplifier and Mono Line Output. The AK4634 is suitable for a moving picture of Digital Still Camera and etc. This speaker-Amplifier supports a Piezo Speaker. The AK4634 is housed in a space-saving 32-pin QFN 5mm x 5mm package and 29-pin CSP 2.5mm x 3mm package.

FEATURE

1. 16-Bit Delta-Sigma Mono CODEC
2. Recording Function
- **1ch Mono Input**
- **MIC Amplifier: (0dB/+3dB/+6dB/+10dB/ +17dB/+20dB/+23dB/+26dB/+29dB/+32dB)**
- **Digital ALC (Automatic Level Control)**
  (+36dB ~ -54dB, 0.375dB Step, Mute)
- **ADC Performance (MIC-Amp=+20dB)**
  - **S/(N+D): 84dB**
  - **DR, S/N: 86dB**
- **Wind-noise Reduction Filter**
- **5 band notch Filter**

3. Playback Function
- **Digital ALC (Automatic Level Control)**
  (+36dB ~ -54dB, 0.375dB Step, Mute)
- **Mono Line Output: S/(N+D): 85dB, S/N: 93dB**
- **Mono Class-D Speaker-Amp**
  - **BTL Output**
  - **Output Power: 400mW @ 8Ω (SVDD=3.3V)**
  - **S/(N+D): 55dB (150mW@8Ω)**
- **Beep Generator**

4. Power Management
5. PLL Mode:
- **Frequencies:**
  12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
  1fs (FCK pin)
  16fs, 32fs or 64fs (BICK pin)

6. EXT Mode:
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

7. Sampling Rate:
- **PLL Slave Mode (FCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Slave Mode / EXT Master Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

8. Output Master Clock Frequency: 256fs
9. Serial μP Interface: 3-wire, I^2C Bus (Ver 1.0, 400kHz High Speed Mode)

10. Master / Slave Mode
11. Audio Interface Format: MSB First, 2's complement
    - ADC: DSP Mode, 16bit MSB justified, I^2S
    - DAC: DSP Mode, 16bit MSB justified, 16bit LSB justified, I^2S
12. Ta = - 40 ~ 85°C (AK4634VN), -30 ~ 85°C (AK4634EN/ECB)
13. Power Supply
    - Analog Supply (AVDD): 2.2 ~ 3.6V
    - Digital Supply (DVDD): 1.6 ~ 3.6V
    - Speaker Supply (SVDD): 2.2 ~ 4.0V
14. Package: 32pin QFN, 5mm x 5mm, 0.5mm pitch (AK4634EN/VN)
    29pin CSP, 2.5mm x 3.0mm, 0.5mm pitch (AK4634ECB)

■ Block Diagram

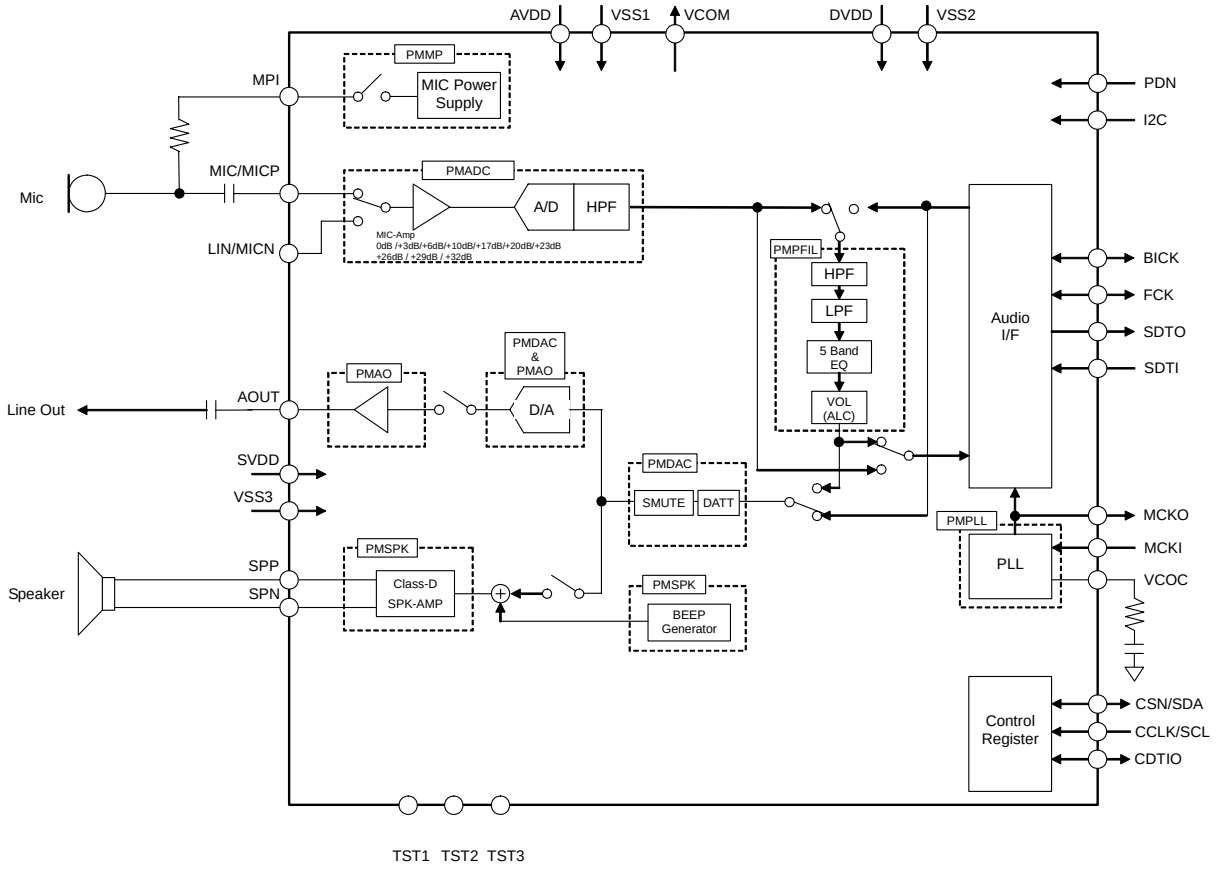


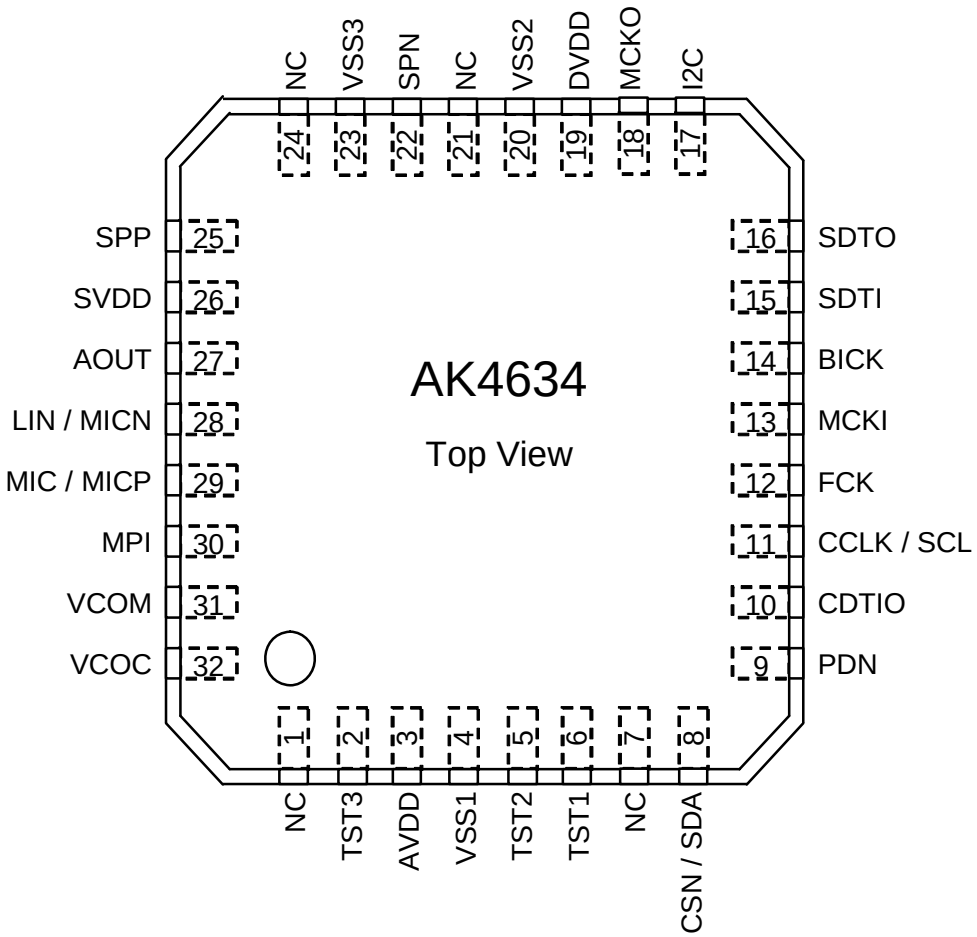
Figure 1. AK4634 Block Diagram

■ Ordering Guide

AK4634VN	–40 ~ +85°C	32pin QFN (0.5mm pitch)
AK4634EN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AK4634ECB	–30 ~ +85°C	29 pin CSP (0.5mm pitch)
AKD4634	Evaluation board for AK4634ECB	

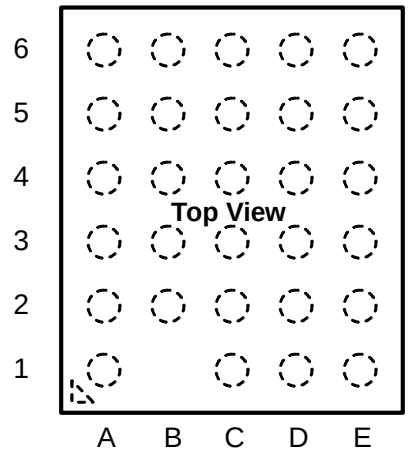
■ Pin Layout

AK4634EN/VN



AK4634EN/VN

AK4634ECB



6	**I2C**	**DVDD**	**VSS2**	**VSS3**	**NC**
5	**SDTO**	**MCKO**	**SPN**	**SVDD**	**SPP**
4	**BICK**	**SDTI**	**MCKI**	**AOUT**	**LIN/ MICN**
3	**FCK**	**CCLK/SCL**	**CDTIO**	**MPI**	**MIC/ MICP**
2	**PDN**	**CSN/SDA**	**TST2**	**VCOM**	**VCOC**
1	**TST1**		**VSS1**	**AVDD**	**TST3**
	A	**B**	**C**	**D**	**E**

■ Compatibility with AK4633

1. Function

Function	AK4633	AK4634
MIC-Amp	0dB/+6dB/+10dB/+14dB +17dB/+20dB/+26dB/+32dB	0dB/+3dB/+6dB/+10dB/+17dB/ +20dB/+23dB/+26dB/+29dB/ +32dB
Single End of Analog Input	1ch (MIC pin)	2ch (MIC pin / LIN pin)
LPF	Not Available	Available
Notch Filter (Equalizer)	2 band	5 band
SPK-Amp	Class-AB	Class-D
ALC Recovery Waiting Period	4 steps (128fs ~ 1024fs)	8 steps (128fs ~ 16384fs)
Master Clock Mode PLL Mode Frequency	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz 24MHz, 27MHz	12MHz, 13.5MHz, 24MHz, 27MHz
BEEP Output	Analog Input	Generator circuit Included
Control Interface	3-wire	3-wire, I^2C
Package	24pin QFN: 4.0mm x 4.0mm	32pin QFN : 5mm x 5mm 29 pin CSP:2.5mm x 3.0mm

PIN/FUNCTION (AK4634EN/VN)

No.	Pin Name	I/O	Function
1	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
2	TST3	-	TEST3 pin This pin must be open.
3	AVDD	-	Analog Power Supply Pin 2.2 ~ 3.6V
4	VSS1	-	Ground Pin.
5	TST2	-	TEST2 pin This pin must be open.
6	TST1	-	TEST1 pin This pin must be open.
7	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
8	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
9	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control register. AK4634 must be always reset upon power-up.
10	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L") This pin must be connected to the ground. (I2C pin = "H")
11	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
12	FCK	I/O	Frame Clock Pin
13	MCKI	I	External Master Clock Input Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	SDTI	I	Audio Serial Data Input Pin
16	SDTO	O	Audio Serial Data Output Pin
17	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
18	MCKO	O	Master Clock Output Pin
19	DVDD	-	Digital Power Supply Pin 1.6 ~ 3.6V
20	VSS2	-	Ground Pin.
21	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
22	SPN	O	Speaker Amp Negative Output Pin
23	VSS3	-	Ground Pin.
24	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
25	SPP	O	Speaker Amp Negative Output Pin
26	SVDD	-	Speaker Amp Power Supply Pin 2.2 ~4.0V
27	AOUT	O	Mono Line Output Pin
28	LIN	I	Line Input Pin for Single Ended Input (MDIF bit = "0")
	MICN	I	Microphone Negative Input Pin for Differential Input (MDIF bit = "1")
29	MIC	I	Microphone Input Pin for Single Ended Input (MDIF bit = "0")
	MICP	I	Microphone Positive Input Pin for Differential Input (MDIF bit = "1")
30	MPI	I	MIC Power Supply Pin for Microphone
31	VCOM	O	Common Voltage Output Pin, 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs.
32	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.

Note: All input pins except analog input pins (MIC/MICP, LIN/MICN pins) must not be left floating

PIN/FUNCTION (AK4634ECB)

No.	Pin Name	I/O	Function
D2	VCOM	O	Common Voltage Output Pin, 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs.
C1	VSS1	-	Ground Pin
D1	AVDD	-	Analog Power Supply Pin
E2	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.
A2	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control register. AK4634 must always be reset upon power-up.
A6	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
B2	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
B3	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
C3	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L") This pin must be connected to the ground. (I2C pin = "H")
B4	SDTI	I	Audio Serial Data Input Pin
A5	SDTO	O	Audio Serial Data Output Pin
A3	FCK	I/O	Frame Clock Pin
A4	BICK	I/O	Audio Serial Data Clock Pin
B6	DVDD	-	Digital Power Supply Pin
C6	VSS2	-	Ground Pin.
C4	MCKI	I	External Master Clock Input Pin
B5	MCKO	O	Master Clock Output Pin
E5	SPP	O	Speaker Amp Positive Output Pin
C5	SPN	O	Speaker Amp Negative Output Pin
D6	VSS3	-	Ground Pin
D5	SVDD	-	Speaker Amp Power Supply Pin
D4	AOUT	O	Mono Line Output Pin
D3	MPI	O	MIC Power Supply Pin for Microphone
E3	MIC	I	Microphone Input Pin for Single Ended Input (MDIF bit = "0")
	MICP	I	Microphone Positive Input Pin for Differential Input (MDIF bit = "1")
E4	LIN	I	Line Input Pin for Single Ended Input (MDIF bit = "0")
	MICN	I	Microphone Negative Input Pin for Differential Input (MDIF bit = "1")
E1	TST3	-	TEST3 pin This pin must be open.
C2	TST2	-	TEST2 pin This pin must be open.
A1	TST1	-	TEST1 pin This pin must be open.
E6	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.

Note: All input pins except analog input pins (MIC/MICP, LIN/MICN pins) must not be left floating

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MIC/MICP, LIN/MICN, MPI, AOUT, SPP, SPN, VCOC	These pins must be open
Digital	MCKI, SDTI	These pins must be connected to VSS2
	CDTIO	When I2C pin = "H", These pins should be connected to VSS2.
	MCKO, SDTO	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-3 =0V; Note 1)

Parameter			Symbol	min	max	Units
Power Supplies:	Analog		AVDD	–0.3	4.6	V
	Digital		DVDD	–0.3	4.6	V
	Speaker-Amp		SVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage (Note 2)			VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 3)			VIND	–0.3	DVDD+0.3	V
Ambient Temperature (power applied)		AK4634VN	Ta	–40	85	°C
		AK4634EN/ECB	Ta	–30	85	°C
Storage Temperature			Tstg	–65	150	°C
Maximum Power Dissipation (Note 4)			Pd	-	400	mW

Note 1. All voltages with respect to ground. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.
Note 2. LIN/MICN, MIC/MICP pins
Note 3. PDN, I2C, CSN/SDA, CCLK/SCL, CDTIO, SDTI, FCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.
Note 4 When PCB wiring density is 100%. This power is the AK4634 internal dissipation that does not include power of externally connected speaker.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-3=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 5)	Analog	AVDD	2.2	3.3	3.6	V
	Digital	DVDD	1.6	3.3	3.6	V
	Speaker-Amp	SVDD	2.2	3.3	4.0	V

Note 1. All voltages with respect to ground.
Note 5. The power up sequence between AVDD, DVDD and SVDD is not critical. The PDN pin must be held to "L" upon power-up. It is not permitted to power DVDD off when AVDD or SVDD is powered up. When only AVDD or SVDD is powered OFF, the AK4634must be reset by bringing the PDN pin "L" after theses power supplies are powered ON again. The power supply current of DVDD at power-down mode may be increased. DVDD should not be powered OFF while AVDD or SVDD is powered ON.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHRACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=3.3V; VSS1-3 =0V; fs=8kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; EXT Slave Mode; unless otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier: MIC, LIN pins ; MDIF bit = "0"; (Single-ended input)					
Input Resistance		20	30	40	kΩ
Gain	(MGAIN3-0 bits = "0000")	-	0	-	dB
	(MGAIN3-0 bits = "0001")	19	20	21	dB
	(MGAIN3-0 bits = "0010")	25	26	27	dB
	(MGAIN3-0 bits = "0011")	31	32	33	dB
	(MGAIN3-0 bits = "0100")	9	10	11	dB
	(MGAIN3-0 bits = "0101")	16	17	18	dB
	(MGAIN3-0 bits = "0110")	22	23	24	dB
	(MGAIN3-0 bits = "0111")	28	29	30	dB
	(MGAIN3-0 bits = "1000")	2	3	4	dB
	(MGAIN3-0 bits = "1001")	5	6	7	dB
MIC Amplifier: MICP, MICN pins ; MDIF bit = "1"; (Full-differential input)					
Input Voltage (Note 6)	(MGAIN3-0 bits = "0001")	0.168	0.198	0.228	Vpp
	(MGAIN3-0 bits = "0010")	0.084	0.099	0.114	Vpp
	(MGAIN3-0 bits = "0011")	0.042	0.050	0.057	Vpp
	(MGAIN3-0 bits = "0100")	0.532	0.626	0.720	Vpp
	(MGAIN3-0 bits = "0101")	0.238	0.280	0.322	Vpp
	(MGAIN3-0 bits = "0110")	0.119	0.140	0.161	Vpp
	(MGAIN3-0 bits = "0111")	0.060	0.070	0.080	Vpp
	(MGAIN3-0 bits = "1001")	0.843	0.992	1.14	Vpp
MIC Power Supply: MPI pin					
Output Voltage (Note 7)		2.38	2.64	2.90	V
Load Resistance		2	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: MIC/LIN → ADC, MIC Gain = 20dB, IVOL = 0dB, ALC1bit = "0"					
Resolution		-	-	16	Bits
Input Voltage (MIC Gain=20dB, Note 8)		0.168	0.198	0.228	Vpp
S/(N+D) (–1dBFS) (Note 9)		74	84	-	dB
D-Range (–60dBFS)		76	86	-	dB
S/N		76	86	-	dB
ADC Analog Input Characteristics: MIC/LIN → ADC, MIC Gain = 0dB, IVOL = 0dB, ALC1bit = "0"					
Resolution		-	-	16	Bits
Input Voltage (MIC Gain=0dB, Note 8)		-	1.98	-	Vpp
S/(N+D) (–1dBFS) (Note 9)		-	84	-	dB
D-Range (–60dBFS)		-	89	-	dB
S/N		-	89	-	dB
DAC Characteristics:					
Resolution				16	Bits
Mono Line Output Characteristics: AOUT pin, DAC → AOUT, R_L = 10kΩ					
Output Voltage (Note 10)	LOVL bit = "0"	1.78	1.98	2.18	Vpp
	LOVL bit = "1"	2.25	2.50	2.75	Vpp
S/(N+D) (0dBFS) (Note 9)		75	85	-	dB
D-Range (–60dBFS)		83	93	-	dB
S/N		83	93	-	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF

Parameter			min	typ	max	Units
Speaker-Amp Characteristics: SDTI → SPP/SPN pins, ALC2 bit = "0", SPKG bit = "0", R_L=8Ω + 10μH, BTL, SVDD=3.3V						
Output Power (0dBFS) (Note 11)			-	400	-	mW
S/(N+D)	400mW Output		-	20	-	dB
	150mW Output		-	55	-	dB
Output Noise Level			-	–80	–70	dBV
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	30	pF
Speaker-Amp Characteristics: SDTI → SPP/SPN pins, ALC2 bit = "0", SPKG bit = "0", C_L=3μF, R_{series}=10Ω x 2, BTL, SVDD=3.8V						
Output Voltage (0dBFS) (Note 11)			-	2.5	-	Vrms
S/(N+D) (Note 12)			-	20	-	dB
Output Noise Level (Note 12, Note 13)			-	–78	-	dBV
Load Impedance (Note 14)			50	-	-	Ω
Load Capacitance			-	-	3	μF
Power Supplies						
Power Up (PDN pin = "H")						
All Circuit Power-up Except Video Amp: (Note 15)						
AVDD+DVDD						
		fs = 8kHz	-	9	-	mA
		fs = 48kHz	-	12	18	mA
SVDD: Speaker-Amp Normal Operation (No Output, R_L=8Ω + 10μH)						
		SVDD = 3.3V	-	1.5	2.5	mA
Power Down (PDN pin = "L") (Note 17)						
AVDD+DVDD+SVDD			-	1	5	μA

Note 6. The voltage difference between MICP and MICN pins. AC coupling capacitor should be inserted in series at each input pin. Full-differential mic input is not available at MGAIN3-0 bits = "1000" or "0000". Maximum input voltage of MICP and MICN pins are proportional to AVDD voltage, respectively.
Vin = |(MICP) – (MICN)| = 0.069 x AVDD(max)@MGAIN3-0 bits = "0001",
0.035 x AVDD(max)@MGAIN3-0 bits = "0010", 0.017 x AVDD(max)@MGAIN3-0 bits = "0011",
0.218x AVDD(max)@MGAIN3-0 bits = "0100", 0.097x AVDD(max)@MGAIN3-0 bits = "0101",
0.048x AVDD(max)@MGAIN3-0 bits = "0110", 0.024x AVDD(max)@MGAIN3-0 bits = "0111",
0.345x AVDD(max)@MGAIN3-0 bits = "1001"
When the signal larger than above value is input to MICP or MICN pin, ADC does not operate normally.

Note 7. Output voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ)

Note 8. Input voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ)

Note 9. When a PLL reference clock is FCK pin in PLL Slave Mode, S/ (N+D) of MIC→ADC is 75dB (typ), S/ (N+D) of DAC→AOUT is 75dB (typ).

Note 10. The output voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ)@LOVL bit = "0".

Note 11. The value after passing LPF (LPF : Passband is 20kHz or less, Stopband Attenuation@250kHz is –50dB or less)

Note 12. In case of measuring at between the SPP pin and SPN pin directly.

Note 13. The output noise level is -68dB(typ) when fs=48kHz and measurement frequency = 20Hz ~ 20kHz.

Note 14. Load impedance is total impedance of series resistance (R_{series}) and piezo speaker impedance at 1kHz in Figure 44. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 15.PLL Master Mode (MCKI = 12MHz) and PMMP = PMADC = PMDAC = PMPFIL = PMSPK = PMVCM = PMPLL = MCKO = PMAO = M/S = "1". Output current from the MPI pin is 0mA.
When the AK4634 is EXT mode (PMPLL = MCKO = M/S = "0"), "AVDD+DVDD" is typically 6mA@fs=8kHz, 11mA@fs=48kHz

Note 16. In case of the resistance of class-D speaker is 8Ω+10uH. When the resistance is 3μF+10Ω x2, this value will be 3.0mA@SVDD=3.8V(typ).

Note 17. All digital inputs pins are fixed to DVDD or VSS2.

FILTER CHRACTERISTICS

(Ta = Tmin ~ Tmax; AVDD = 2.8 ~ 3.6V; DVDD = 1.6 ~ 3.6V, SVDD = 2.2 ~ 4.0V; fs=8kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 18)	±0.16dB	PB	0	-	3.0	kHz
	–0.66dB		-	3.5	-	kHz
	–1.1dB		-	3.6	-	kHz
	–6.9dB		-	4.0	-	kHz
Stopband (Note 18)		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 19)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
DAC Digital Filter (Decimation LPF):						
Passband (Note 18)	±0.16dB	PB	0	-	3.0	dB
	–0.54dB		-	3.5	-	
	–1.0dB		-	3.6	-	
	–6.7dB		-	4.0	-	
Stopband (Note 18)		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 19)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 3.4kHz		FR	-	±1.0	-	dB

Note 18. The passband and stopband frequencies are proportional to fs (system sampling rate).
For example, ADC of PB = 3.6kHz is 0.45*fs (@ –1.0dB). A reference of frequency response is 1kHz.

Note 19. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of a channel from the input register to the output register of the ADC. For the DAC, this time is from setting the 16-bit data of a channel from the input register to the output of analog signal. When there is not a phase change with the IIR filter, group delay of the programmable filter (primary HPF + primary LPF + 5-band Equalizer + ALC) increases for 2/fs than a value of an above mention.

DC CHRACTERISTICS

(Ta = Tmin ~ Tmax; AVDD = 2.8 ~ 3.6V, DVDD = 1.6 ~ 3.6V, SVDD = 2.2 ~ 4.0V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(DVDD ≥ 2.2V)	VIH	70%DVDD	-	-	V
	(DVDD < 2.2V)		80%DVDD	-	-	V
Low-Level Input Voltage	(DVDD ≥ 2.2V)	VIL	-	-	30%DVDD	V
	(DVDD < 2.2V)		-	-	20%DVDD	V
High-Level Output Voltage	(Iout = –80μA)	VOH	DVDD–0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout = 80μA)		VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ DVDD ≤ 3.6V: Iout = 3mA)		VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ DVDD < 2.0V: Iout = 3mA)		VOL2	-	-	20%DVDD	
Input Leakage Current		Iin	-	-	±10	μA

SWITING CHARACTERISTICS

(Ta = Tmin ~ Tmax; AVDD = 2.8 ~ 3.6V, DVDD = 1.6 ~ 3.6V, SVDD = 2.2 ~ 4.0V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin) (Figure 2)					
MCKI Input: Frequency	fCLK	11.2896	-	27.0	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output:					
Frequency	fMCK	-	256 x fFCK	-	kHz
Duty Cycle except fs=29.4kHz, 32kHz	dMCK	40	50	60	%
fs =29.4kHz, 32kHz (Note 20)	dMCK	-	33	-	%
FCK Output: Frequency	fFCK	8	-	48	kHz
Pulse width High (DIF1-0 bits = "00" and FCKO bit = "1")	tFCKH	-	tBCK	-	ns
Duty Cycle (DIF1-0 bits = "00" or FCKO bit = "0")	dFCK	-	50	-	%
BICK: Period (BCKO1-0 = "00")	tBCK	-	1/16fFCK	-	ns
(BCKO1-0 = "01")	tBCK	-	1/32fFCK	-	ns
(BCKO1-0 = "10")	tBCK	-	1/64fFCK	-	ns
Duty Cycle	dBCK	-	50	-	%
Audio Interface Timing					
DSP Mode: (Figure 3, Figure 4)					
FCK "↑" to BICK "↑" (Note 21)	tDBF	0.5 x tBCK –40	0.5 x tBCK	0.5 x tBCK + 40	ns
FCK "↑" to BICK "↓" (Note 22)	tDBF	0.5 x tBCK –40	0.5 x tBCK	0.5 x tBCK +40	ns
BICK "↑" to SDTO (BCKP = "0")	tBSD	-70	-	70	ns
BICK "↓" to SDTO (BCKP = "1")	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Except DSP Mode: (Figure 5)					
BICK "↓" to FCK Edge	tBFCK	–40	-	40	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Parameter	Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock: FCK pin) (Figure 6, Figure 7)					
FCK: Frequency	fFCK	7.35	8	48	kHz
DSP Mode: Pulse Width High	tFCKH	tBCK−60	-	1/fFCK−tBCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period	tBCK	1/64fFCK	-	1/16fFCK	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock: BICK pin) (Figure 6, Figure 7)					
FCK: Frequency	fFCK	7.35	8	48	kHz
DSP Mode: Pulse width High	tFCKH	tBCK−60	-	1/fFCK−tBCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period (PLL3-0 bit = “0001”)	tBCK	-	1/16fFCK	-	ns
(PLL3-0 bit = “0010”)	tBCK	-	1/32fFCK	-	ns
(PLL3-0 bit = “0011”)	tBCK	-	1/64fFCK	-	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock: MCKI pin) (Figure 8)					
MCKI Input: Frequency	fCLK	11.2896	-	27.0	MHz
Pulse Width Low	fCLKL	0.4/fCLK	-	-	ns
Pulse Width High	fCLKH	0.4/fCLK	-	-	ns
MCKO Output:					
Frequency	fMCK	-	256 x fFCK	-	kHz
Duty Cycle except fs=29.4kHz, 32kHz	dMCK	40	50	60	%
fs=29.4kHz, 32kHz (Note 20)	dMCK	-	33	-	%
FCK: Frequency	fFCK	8	-	48	kHz
DSP Mode: Pulse width High	tFCKH	tBCK−60	-	1/fFCK−tBCK	ns
Except DSP Mode: Duty Cycle	duty	45	-	55	%
BICK: Period	tBCK	1/64fFCK	-	1/16fFCK	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
Audio Interface Timing					
DSP Mode: (Figure 9, Figure 10)					
FCK “↑” to BICK “↑” (Note 21)	tFCKB	0.4 x tBCK	-	-	ns
FCK “↑” to BICK “↓” (Note 22)	tFCKB	0.4 x tBCK	-	-	ns
BICK “↑” to FCK “↑” (Note 21)	tBFCK	0.4 x tBCK	-	-	ns
BICK “↓” to FCK “↑” (Note 22)	tBFCK	0.4 x tBCK	-	-	ns
BICK “↑” to SDTO (BCKP bit= “0”)	tBSD	-	-	80	ns
BICK “↓” to SDTO (BCKP bit= “1”)	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Except DSP Mode: (Figure 12)					
FCK Edge to BICK “↑” (Note 23)	tFCKB	50	-	-	ns
BICK “↑” to FCK Edge (Note 23)	tBFCK	50	-	-	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	-	-	80	ns
BICK “↓” to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Parameter	Symbol	min	typ	max	Units
EXT Slave Mode (Figure 11)					
MCKI Frequency: 256fs	fCLK	1.8816	2.048	12.288	MHz
512fs	fCLK	3.7632	4.096	13.312	MHz
1024fs	fCLK	7.5264	8.192	13.312	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
FCK Frequency (MCKI = 256fs)	fFCK	7.35	8	48	kHz
(MCKI = 512fs)	fFCK	7.35	8	26	kHz
(MCKI = 1024fs)	fFCK	7.35	8	13	kHz
Duty Cycle	duty	45	-	55	%
BICK Period	tBCK	312.5	-	-	ns
BICK Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
Audio Interface Timing (Figure 12)					
FCK Edge to BICK "↑" (Note 23)	tFCKB	50	-	-	ns
BICK "↑" to FCK Edge (Note 23)	tBFCK	50	-	-	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Parameter	Symbol	min	typ	max	Units
EXT Master Mode (Figure 2)					
MCKI Frequency: 256fs	fCLK	1.8816	2.048	12.288	MHz
512fs	fCLK	3.7632	4.096	13.312	MHz
1024fs	fCLK	7.5264	8.192	13.312	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
FCK Frequency (MCKI = 256fs)	fFCK	7.35	8	48	kHz
(MCKI = 512fs)	fFCK	7.35	8	26	kHz
(MCKI = 1024fs)	fFCK	7.35	8	13	kHz
Duty Cycle	dFCK	-	50	-	%
BICK: Period (BCKO1-0 bit = "00")	tBCK	-	1/16fFCK	-	ns
(BCKO1-0 bit = "01")	tBCK	-	1/32fFCK	-	ns
(BCKO1-0 bit = "10")	tBCK	-	1/64fFCK	-	ns
Duty Cycle	dBCK	-	50	-	%
Audio Interface Timing					
DSP Mode: (Figure 3, Figure 4)					
FCK "↑" to BICK "↑" (Note 21)	tDBF	0.5 x tBCK–40	0.5 x tBCK	0.5 x tBCK + 40	ns
FCK "↑" to BICK "↓" (Note 22)	tDBF	0.5 x tBCK–40	0.5 x tBCK	0.5 x tBCK +40	ns
BICK "↑" to SDTO (BCKP bit = "0")	tBSD	–70	-	70	ns
BICK "↓" to SDTO (BCKP bit = "1")	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Except DSP Mode: (Figure 5)					
BICK "↓" to FCK Edge	tBFCK	–40	-	40	ns
FCK to SDTO (MSB) (Except I^2S mode)	tFSD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 20. Duty Cycle = (the width of "L")/(the period of clock)*100
Note 21. MSBS, BCKP bits = "00" or "11"
Note 22. MSBS, BCKP bits = "01" or "10"
Note 23. BICK rising edge must not occur at the same time as FCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN edge to CCLK "↑" (Note 25)	tCSS	50	-	-	ns
CCLK "↑" to CSN edge (Note 25)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command) (Note 26)	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 27)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Reset Timing					
PDN Pulse Width (Note 28)	tPD	150	-	-	ns
PMADC "↑" to SDTO valid (Note 29)					
ADRST bit = "0"	tPDV	-	1059	-	1/fs
ADRST bit = "1"	tPDV	-	291	-	1/fs

Note 24. I^2C is a registered trademark of Philips Semiconductors.
Note 25. CCLK rising edge must not occur at the same time as CSN edge.
Note 26. R_L = 1kΩ/10% change (Pull-up to DVDD)
Note 27. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 28. The AK4634 can be reset by the PDN pin = "L"
Note 29. This is the count of FCK "↑" from the PMADC = "1".

■ Timing Diagram

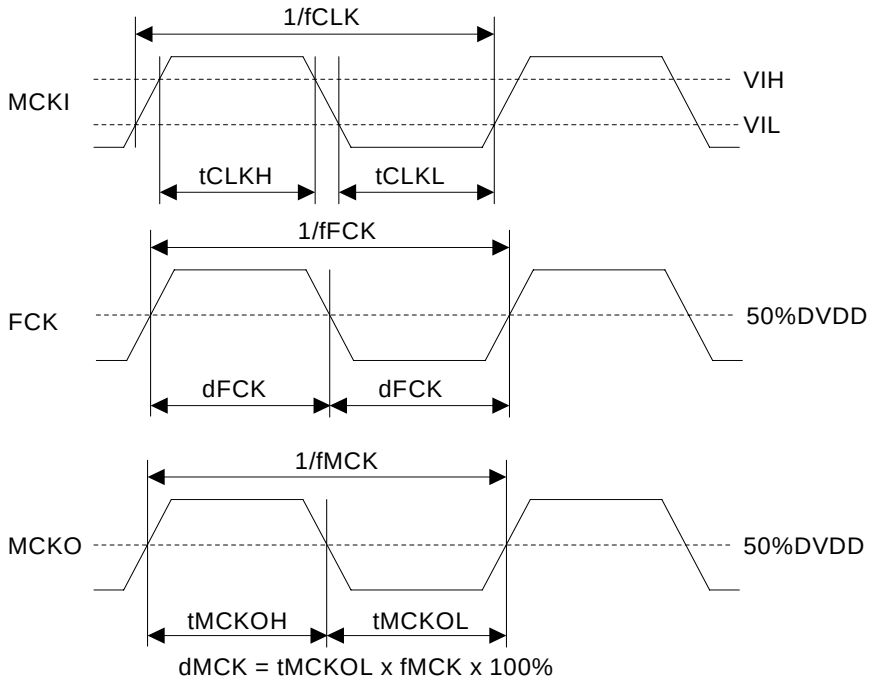


Figure 2. Clock Timing (PLL/EXT Master mode) (MCKO is not available at EXT Master Mode)

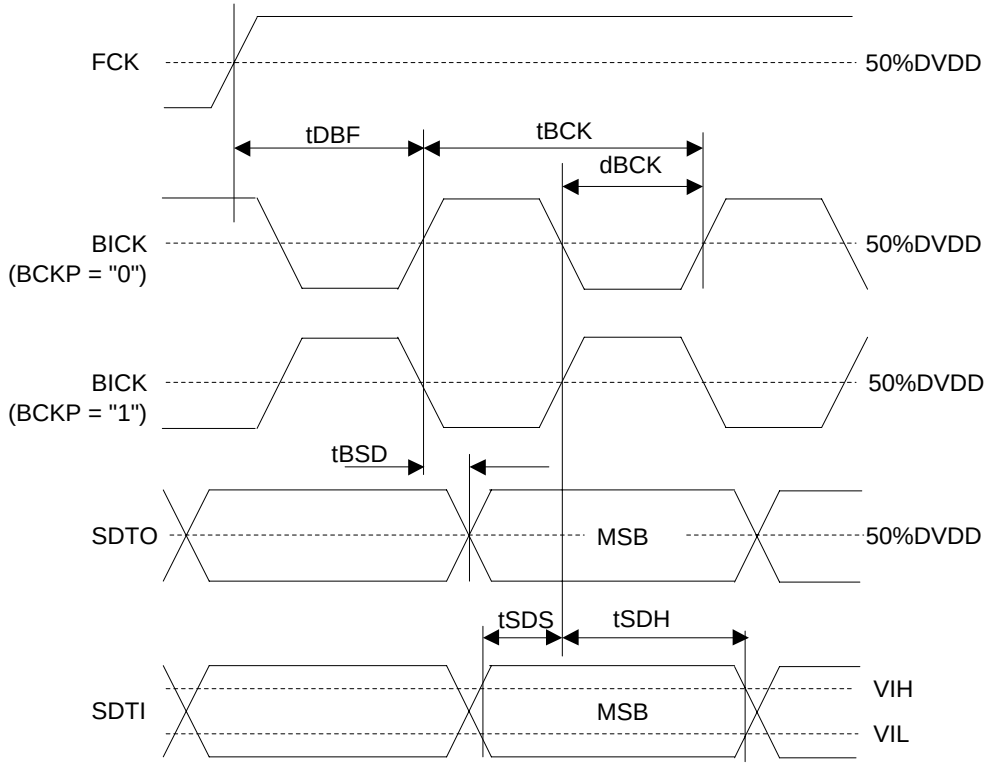


Figure 3. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = “0”)

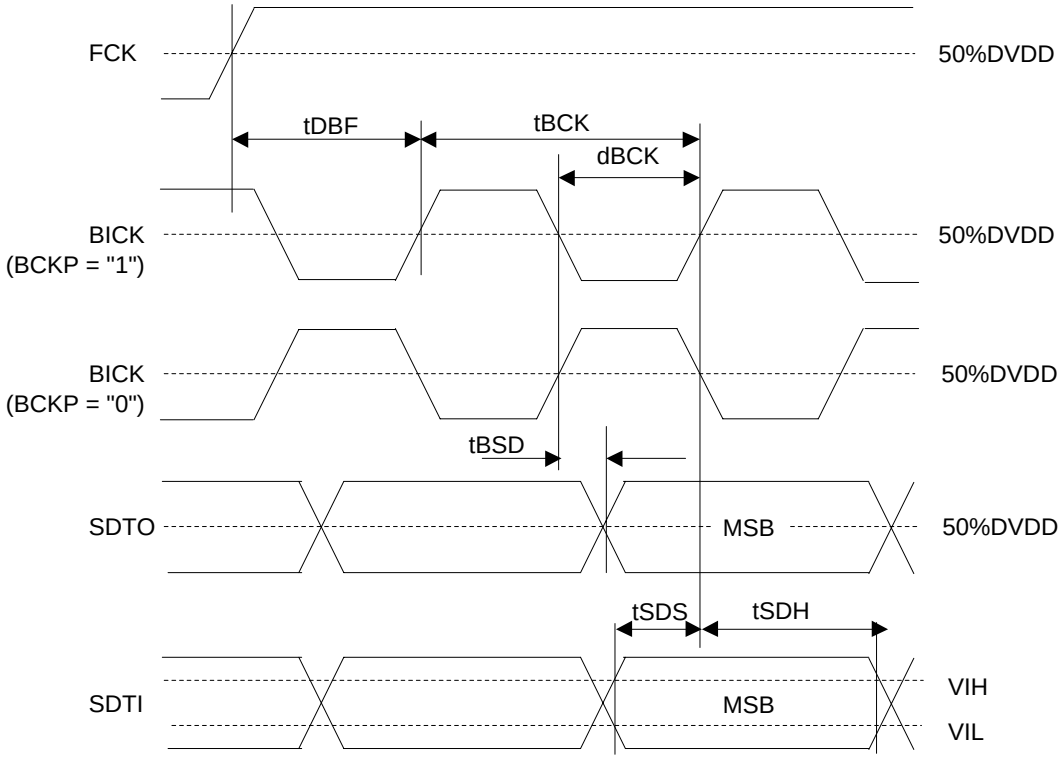


Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = "1")

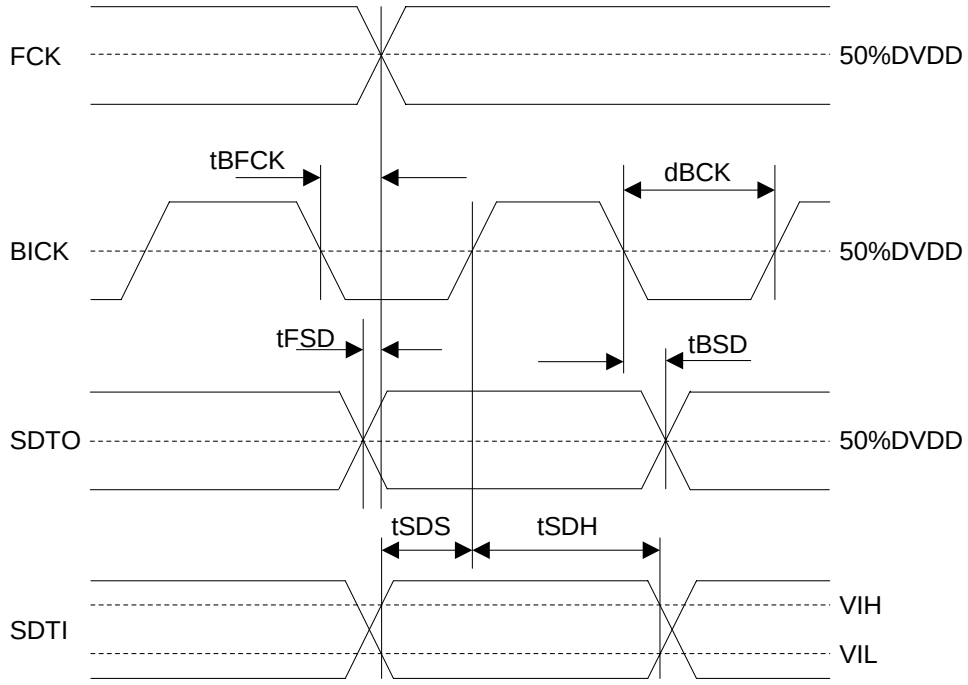


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Except DSP mode)

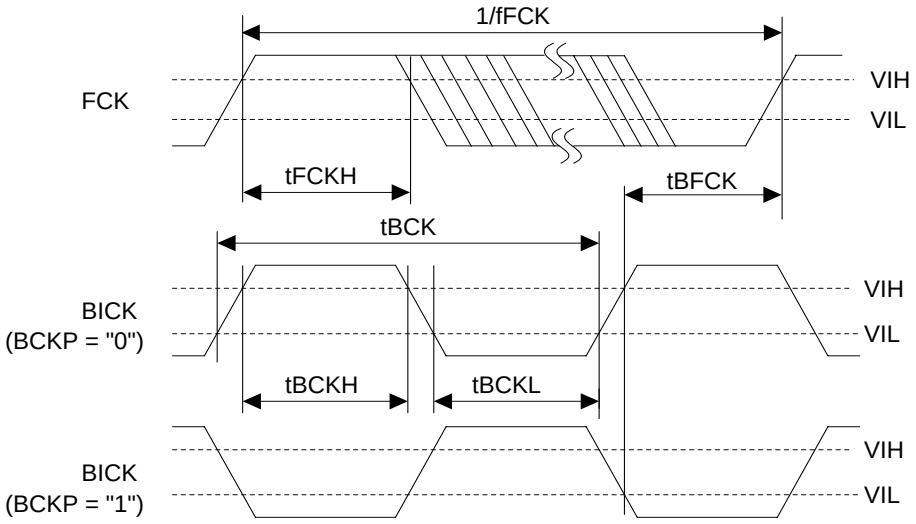


Figure 6. Clock Timing (PLL Slave mode; PLL Reference clock = FCK or BICK pin & DSP mode; MSBS = 0)

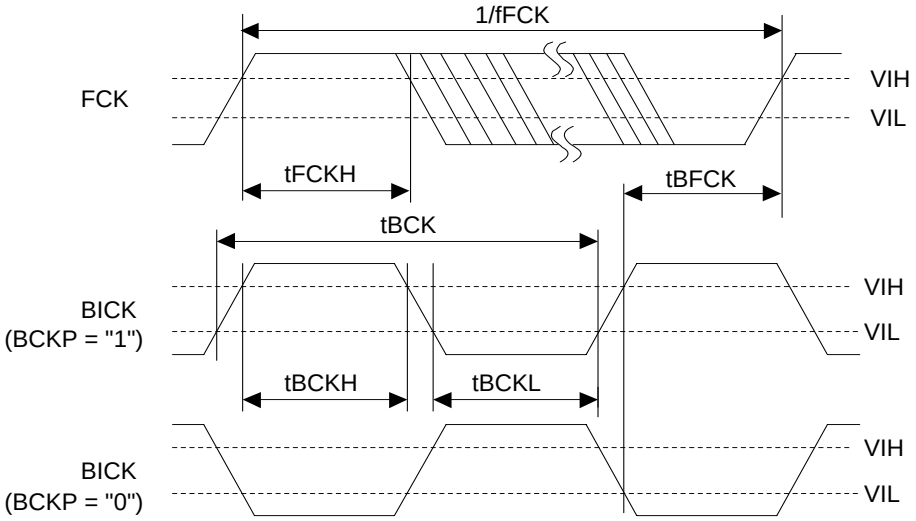


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = FCK or BICK pin & DSP mode; MSBS = 1)

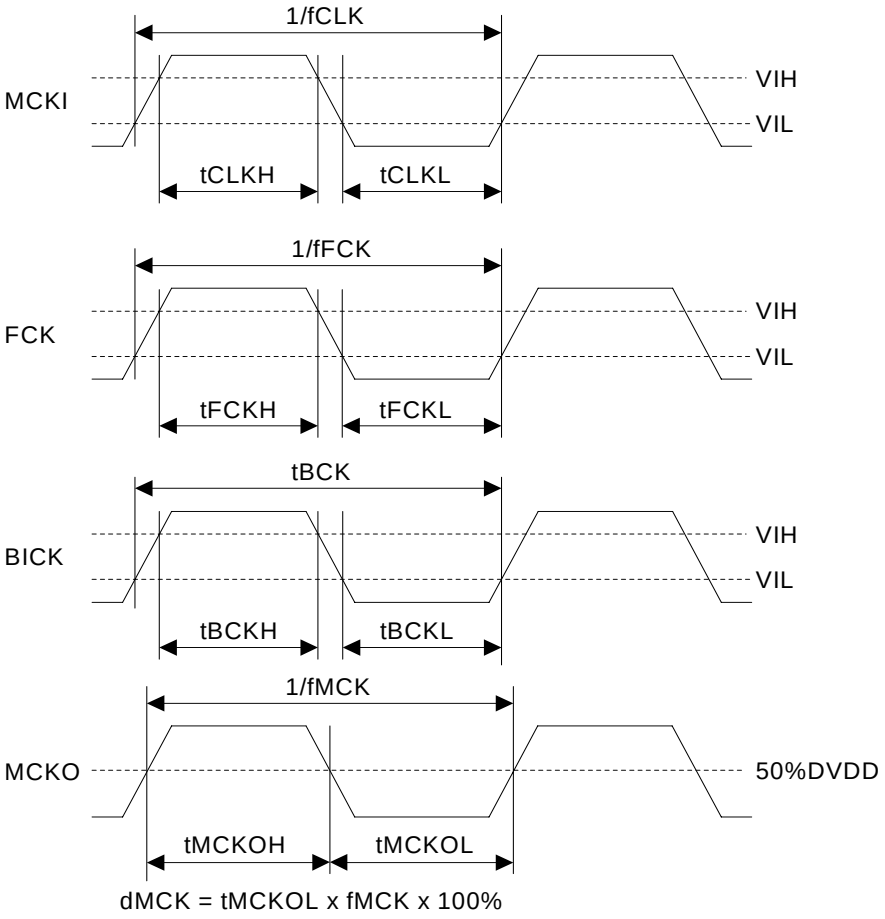


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

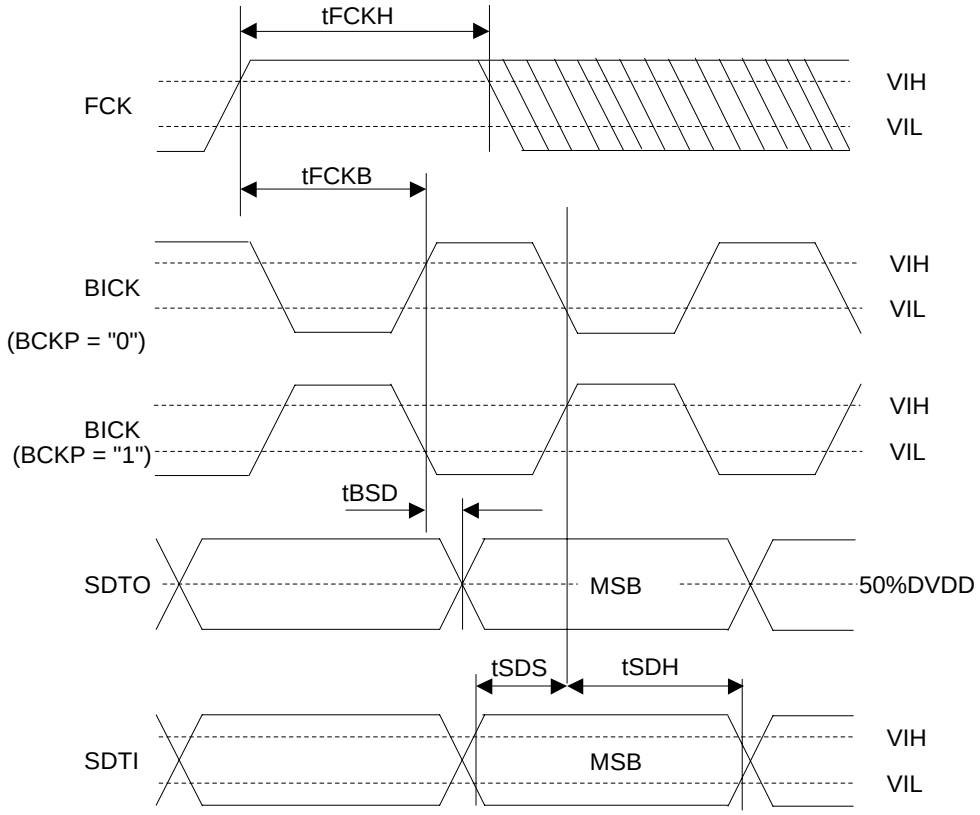


Figure 9. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)

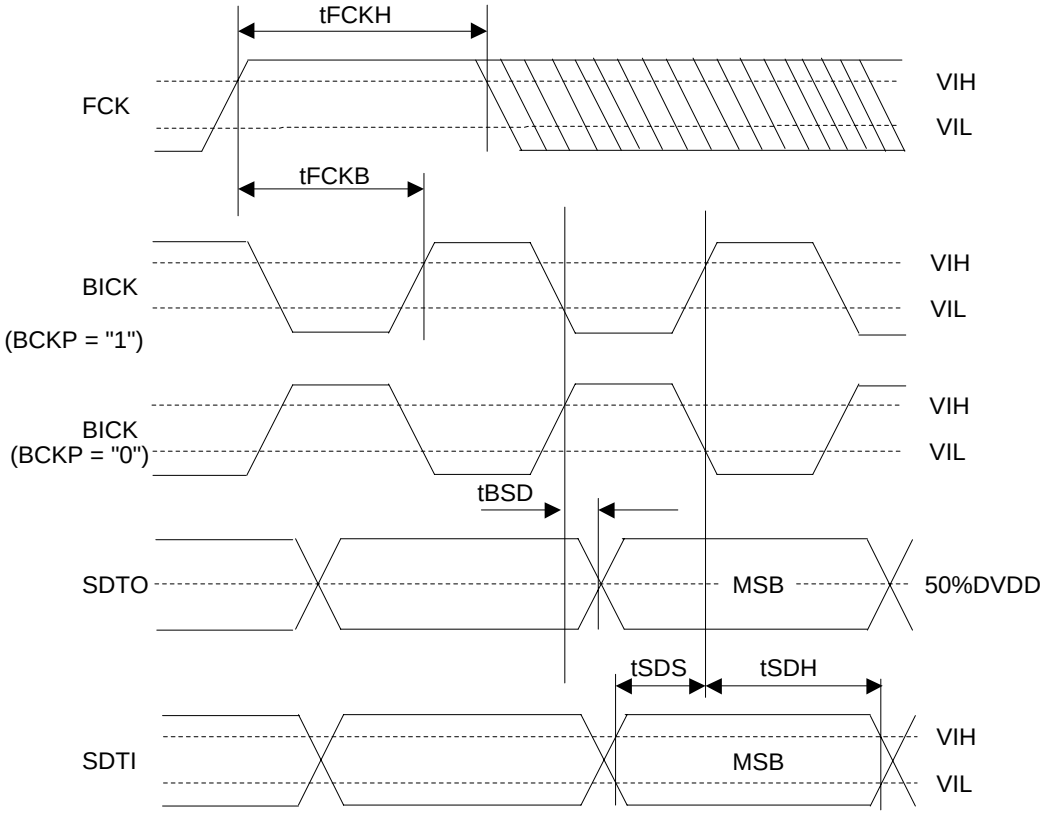


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = 1)

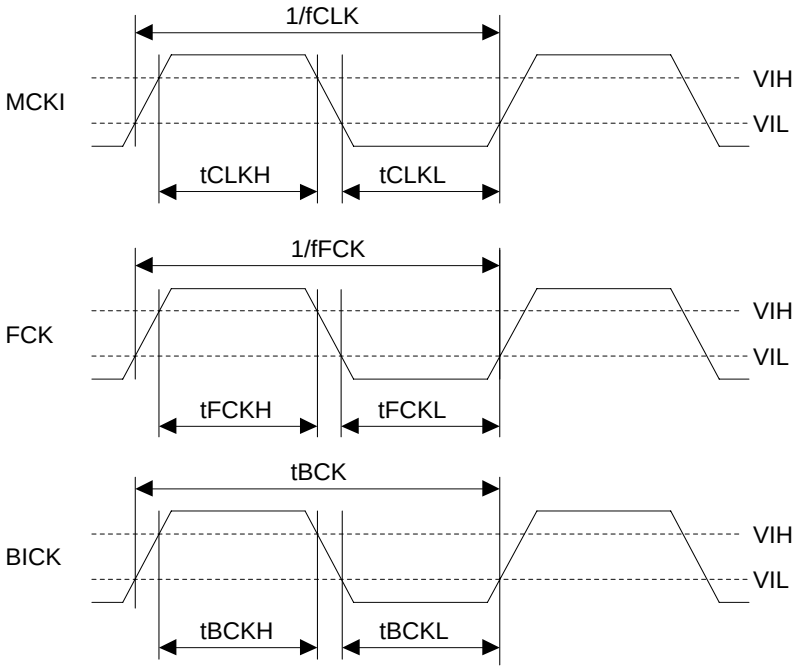


Figure 11. Clock Timing (EXT Slave mode)

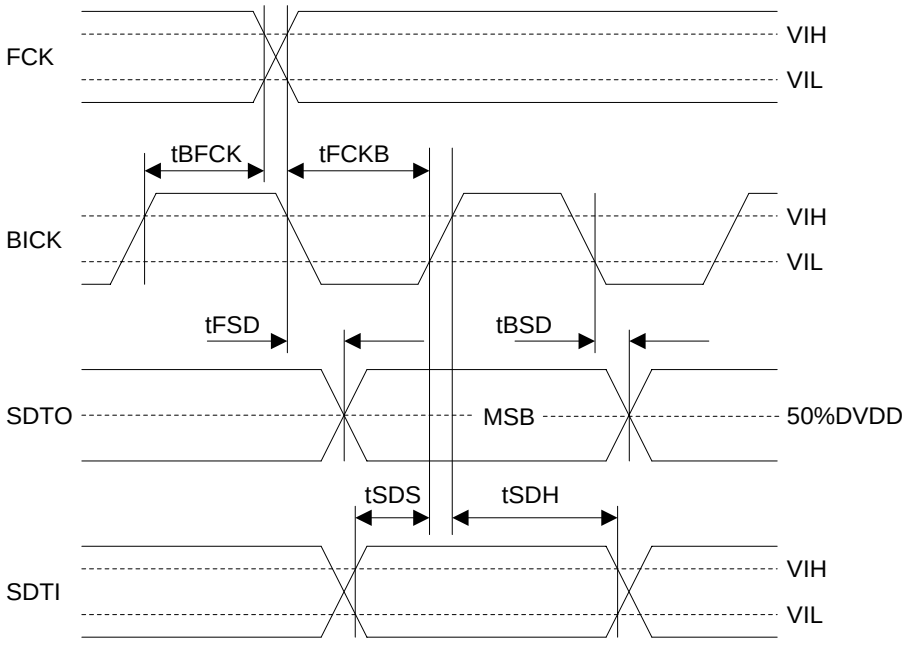


Figure 12. Audio Interface Timing (PLL, EXT Slave mode & Except DSP mode)

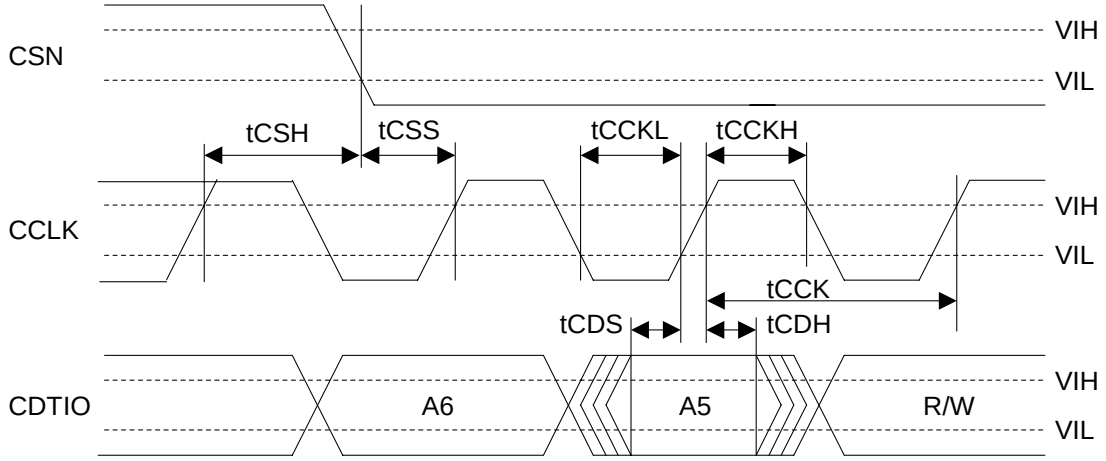


Figure 13. WRITE Command Input Timing

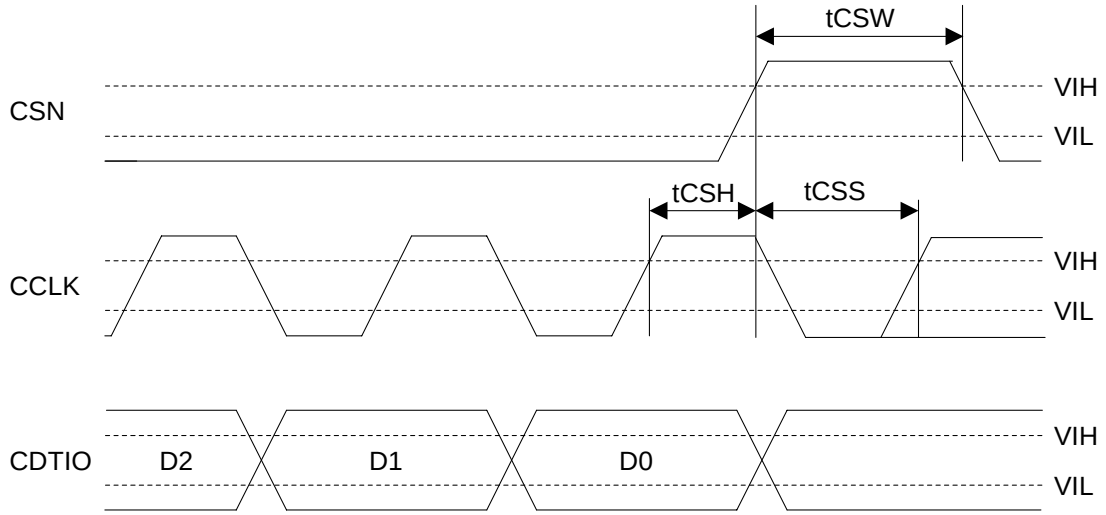


Figure 14. WRITE Data Input Timing

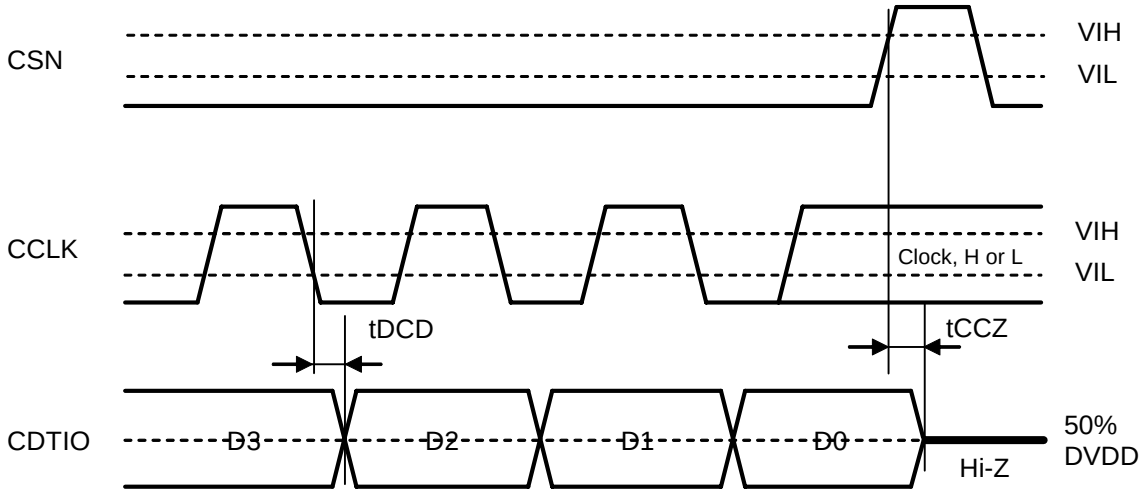


Figure 15. Read Data Output Timing

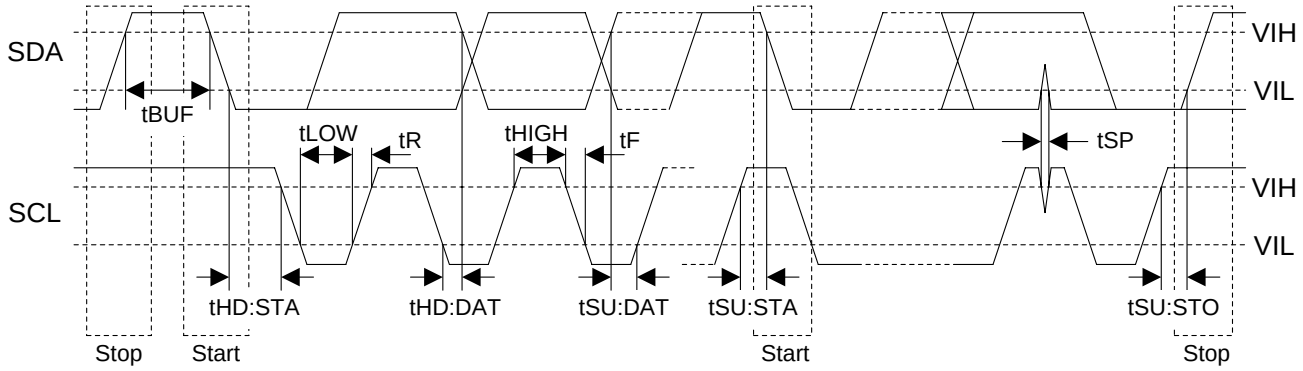


Figure 16. I^{2}C Bus Mode Timing

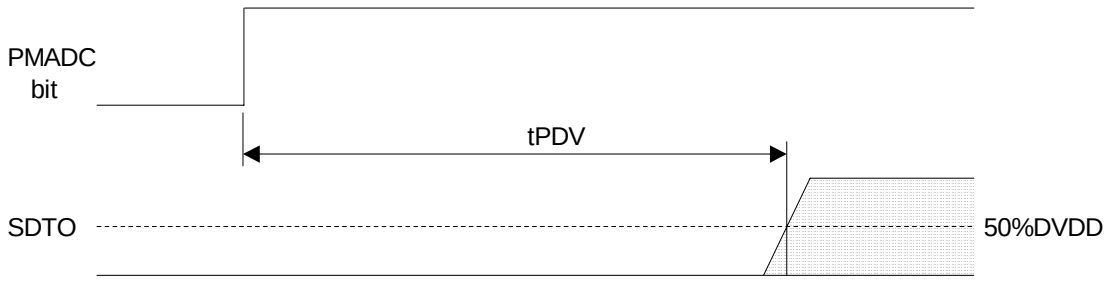


Figure 17. Power Down & Reset Timing 1

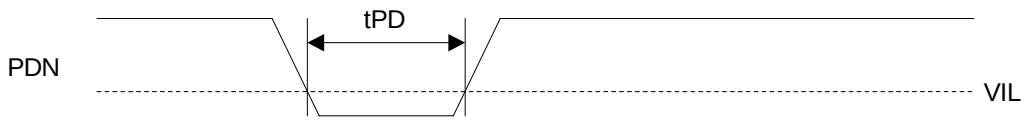


Figure 18. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices. (Table 1 and Table 2)

Mode	PMPLL bit	M/S bit	PLL3-0 bit	Figure
PLL Master Mode	1	1	Table 4	Figure 19
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 20
PLL Slave Mode 2 (PLL Reference Clock: FCK or BICK pin)	1	0	Table 4	Figure 21 Figure 22
EXT Slave Mode	0	0	x	Figure 23
EXT Master Mode	0	1	x	Figure 24

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	FCK pin
PLL Master Mode	0	"L" Output	Master Clock Input for PLL (Note 30)	16fs/32fs/64fs Output	1fs Output
	1	256fs Output			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	"L" Output	Master Clock Input for PLL (Note 30)	≥ 16fs Input	1fs Input
	1	256fs Output			
PLL Slave Mode 2 (PLL Reference Clock: FCK or BICK pin)	0	"L" Output	GND	16fs/32fs/64fs Input	1fs Input
EXT Slave Mode	0	"L" Output	256fs/ 512fs/ 1024fs Input	≥ 32fs Input	1fs Input
EXT Master Mode	0	"L" Output	256fs/ 512fs/ 1024fs Input	32fs/64fs Output	1fs Output

Note 30. 12MHz/13.5MHz/24MHz/27MHz

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave modes. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4634 is power-down mode (PDN pin = "L") and exits reset state, the AK4634 is slave mode. After exiting reset state, the AK4634 changes to master mode by bringing M/S bit = "1".

When the AK4634 is in master mode, FCK and BICK pins are a floating state until M/S bit becomes "1". The FCK and BICK pins of the AK4634 should be pulled-down or pulled-up by about 100kΩ resistor externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Salve Mod

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4. Ether when the AK4634 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or when the sampling frequency changes, the PLL lock time is the same.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin (Note 31)		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	FCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	BICK pin	16fs	10k	4.7n	2ms	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	20ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	20ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	20ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	20ms	
Others	Others				N/A					

Note 31. the tolerance of R is ±5%, the tolerance of C is ±30%

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode.

When PLL2 bit is "1" (PLL reference clock input is the MCKI pin), the sampling frequency is selected by FS2-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (N/A: Not available)

When PLL2 bit is "0" (PLL reference clock input is FCK or BICK pin), the sampling frequency is selected by FS3-2 bits. (Table 6)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

(x: Don't care, N/A: Not available)

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1"

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, irregular frequency clocks are output from FCK, BICK and MCKO pins after PMPLL bit = "0" → "1" or sampling frequency is changed. After that PLL is unlocked, the BICK and FCK pins output "L" for a moment, and invalid frequency clock is output from the MCKO pin at MCKO bit = "1". If the MCKO bit is "0", the MCKO pin is output to "L".
(Table 7)

When sampling frequency is changed, BICK and FCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	FCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	256fs Output	See Table 9	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin after PMPLL bit = "0" → "1" or sampling frequency is changed. After that, 256fs is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACA and DACS bits in Addr=02H.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

When an external clock (12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and FCK clocks are generated by an internal PLL circuit. The MCKO output frequency is fixed to 256fs, the output is enabled by MCKO bit. The BICK is selected among 16fs, 32fs or 64fs, by BCKO1-0 bits. (Table 9)

In DSP mode, FCK output can select Duty 50% or High-output only during 1 BICK cycle (Table 10). Except DSP mode, FCKO bit should be set “0”.

When BICK output frequency is 16fs, the audio interface format supports Mode 0 only (DSP Mode).

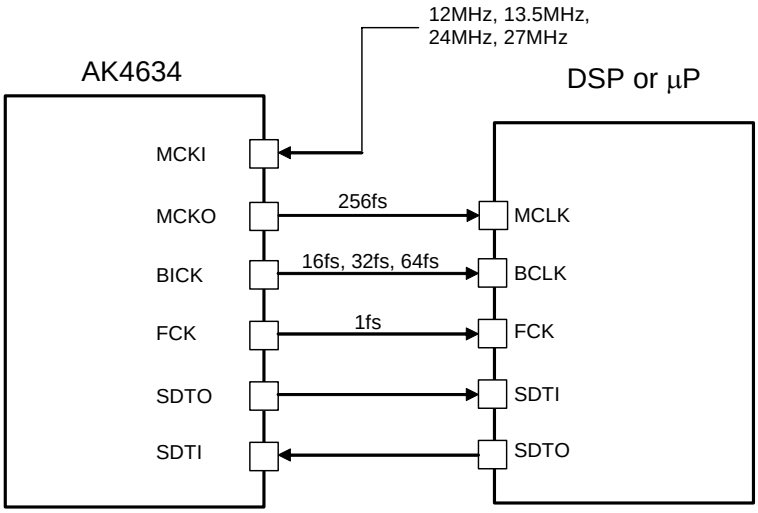


Figure 19. PLL Master Mode

Mode	BCKO1	BCKO0	BICK Output Frequency	
0	0	0	16fs	(default)
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 9. BICK Output Frequency at Master Mode

Mode	FCKO	FCK Output	
0	0	Duty = 50%	(default)
1	1	High Width = 1/fBCK	

Note 32. fBCK is BICK Output Frequency.

Table 10. FCK Output at PLL Master Mode and DSP Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or FCK pin. The required clock to the AK4634 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits. When BICK input frequency is 16fs, the audio interface format supports Mode 0 only (DSP Mode).

a) PLL reference clock: MCKI pin

BICK and FCK inputs should be synchronized with MCKO output. The phase between MCKO and FCK is not important. The MCKO pin outputs the frequency selected by FS3-0 bits (Table 5)

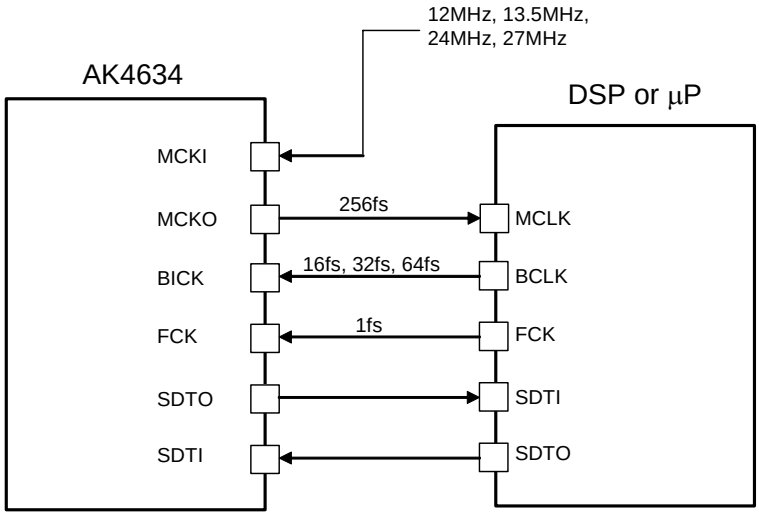


Figure 20. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits. (Table 6)

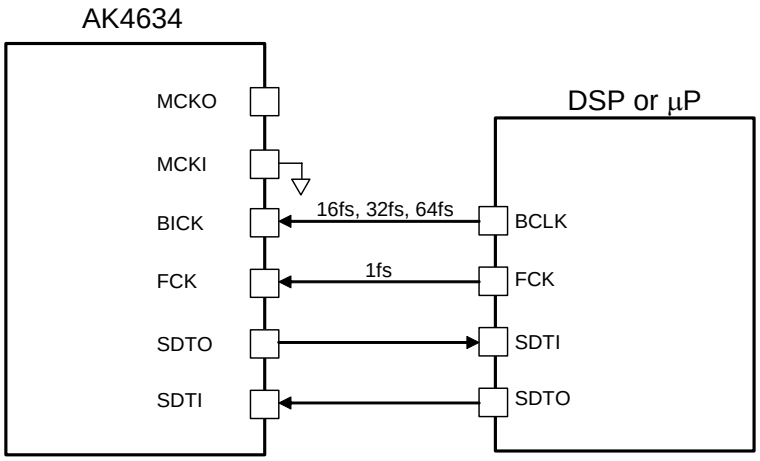


Figure 21 PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

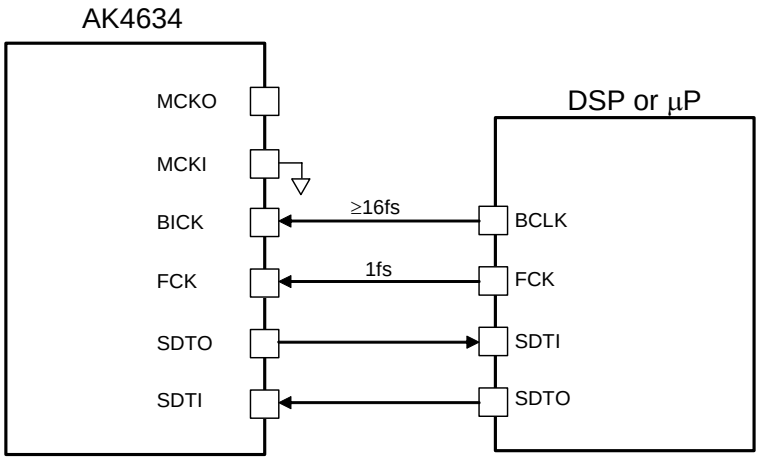


Figure 22. PLL Slave Mode 2 (PLL Reference Clock: FCK pin)

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC or SPK or Programmable Filter is in operation (PMADC bit = "1", PMDAC bit = "1", PMSPK bit = "1", PMPFIL bit = "1"). If these clocks are not provided, the AK4634 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC, DAC, SPK and Programmable Filter should be in the power-down mode.(PMADC = PMDAC = PMSPK = PMPFIL bits = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4634 becomes EXT Slave mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), FCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with FCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits. (Table 11)

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ≤ fs ≤ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ≤ fs ≤ 13kHz	
2	x	1	0	512fs	7.35kHz ≤ fs ≤ 26kHz	
3	x	1	1	256fs	7.35kHz ≤ fs ≤ 48kHz	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0") (x: Don't care)

External Slave Mode does not support Mode 0 (DSP Mode) of Audio Interface Format.

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. (Table 12, Table 13)

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
	DAC →AOUT
256fs	84dB
512fs	92dB
1024fs	92dB

Table 12. Relationship between MCKI and S/N of AOUT and SPK-Amp

MCKI	Output Noise Level (SVDD=3.3V,fs=8kHz, 20kHzLPF + A-weighted)
	SDTI → SPK-Amp
256fs	-58dBV
512fs	-72dBV
1024fs	-80dBV

Table 13. Relationship between MCKI and Output Noise Level of SPK-Amp

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC or SPK or Programmable Filter is in operation (PMADC = PMDAC = PMSPK bit = PMPFIL bits = "1"). If these clocks are not provided, the AK4634 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC, DAC, SPK and Programmable Filter should be in the power-down mode (PMADC = PMDAC = PMSPK bit = PMPFIL bits = "0").

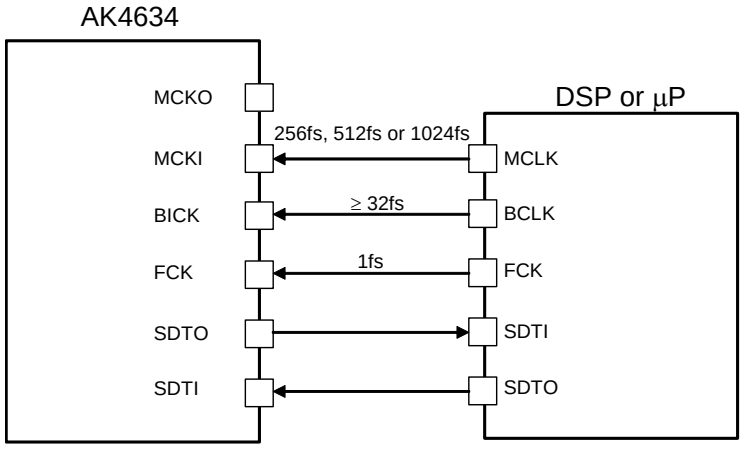


Figure 23. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4634 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 14). The BICK is selected among 32fs or 64fs, by BCKO1-0 bits (Table 15). FCK bit should be set to "0".

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ≤ fs ≤ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ≤ fs ≤ 13kHz	
2	x	1	0	512fs	7.35kHz ≤ fs ≤ 26kHz	
3	x	1	1	256fs	7.35kHz ≤ fs ≤ 48kHz	

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1") (x: Don't care)

External Master Mode does not support Mode 0 (DSP Mode) of Audio Interface Format.

MCKI should always be present whenever the ADC, DAC, SPK or Programmable Filter is in operation (PMADC = PMDAC = PMSPK bit = PMPFIL bits = "1"). If MCKI is not provided, the AK4634 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC, DAC, SPK and Programmable Filter should be in the power-down mode (PMADC = PMDAC = PMSPK = PMPFIL bits = "0").

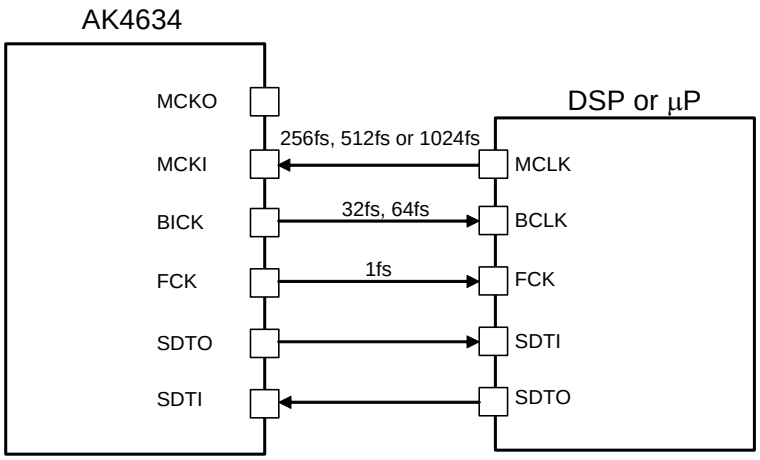


Figure 24. EXT Master Mode

Mode	BCKO1	BCKO0	BICK Output Frequency	
0	0	0	N/A	(default)
1	0	1	32fs	
2	1	0	64fs	
3	1	1	N/A	

Table 15. BICK Output Frequency at Master Mode (N/A: Not available)

■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits. (Table 16) In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. FCK and BICK are output from the AK4634 in master mode, but must be input to the AK4634 in slave mode.

In Mode 1-3, the SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 16fs	Table 17	
1	0	1	MSB justified	MSB justified	≥ 32fs	Figure 25	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 26	(default)
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 27	

Table 16. Audio Interface Format

In Mode0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is "0", SDTO data is output by rising edge of BICK, SDTI data is latched by falling edge of BICK.
When BCKP bit is "1", SDTO data is output by falling edge of BICK, SDTI data is latched by rising edge of BICK.

MSB data position of SDTO and SDTI can be shifted by MSBS bit. The shifted period is a half of BICK.

MSBS bit	BCKP bit	Audio Interface Format	
0	0	Figure 28	(default)
0	1	Figure 29	
1	0	Figure 30	
1	1	Figure 31	

Table 17. Audio Interface Format in Mode 0

If 16-bit data, the output of ADC, is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

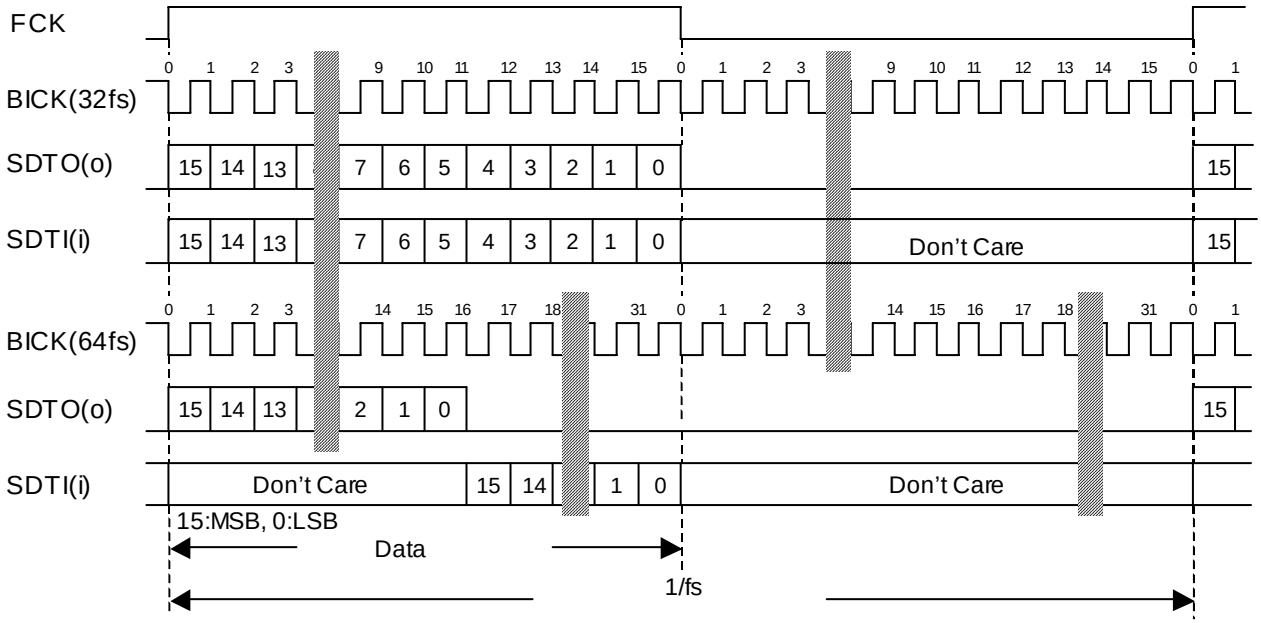


Figure 25. Mode 1 Timing

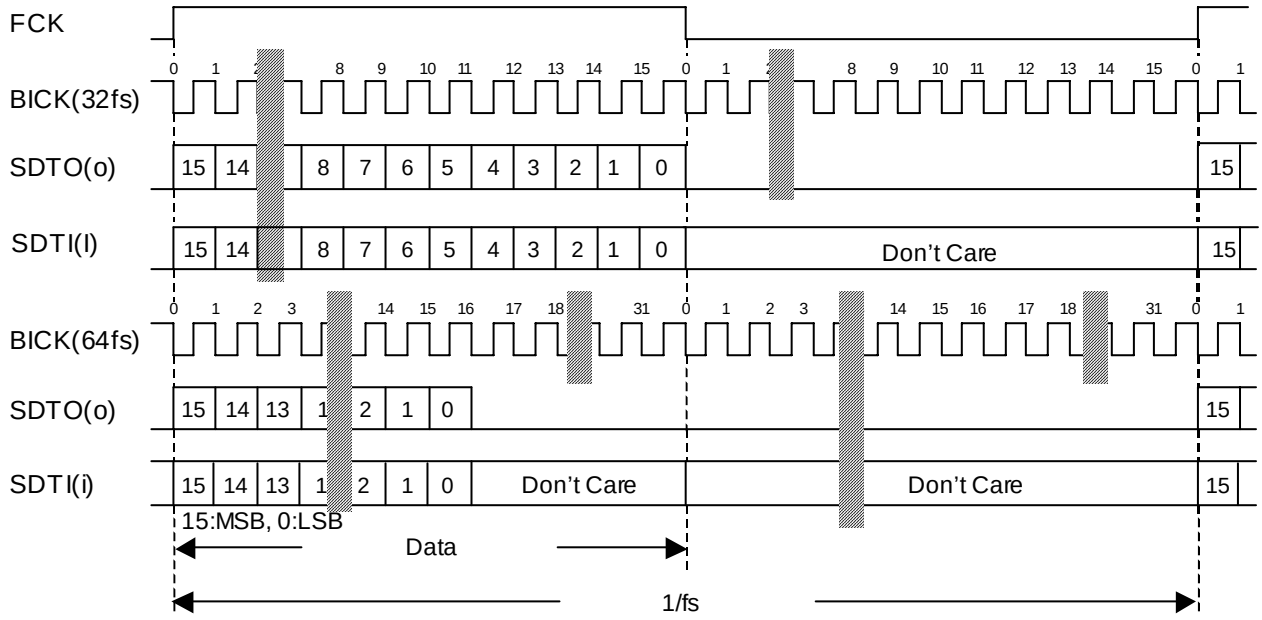


Figure 26. Mode 2 Timing

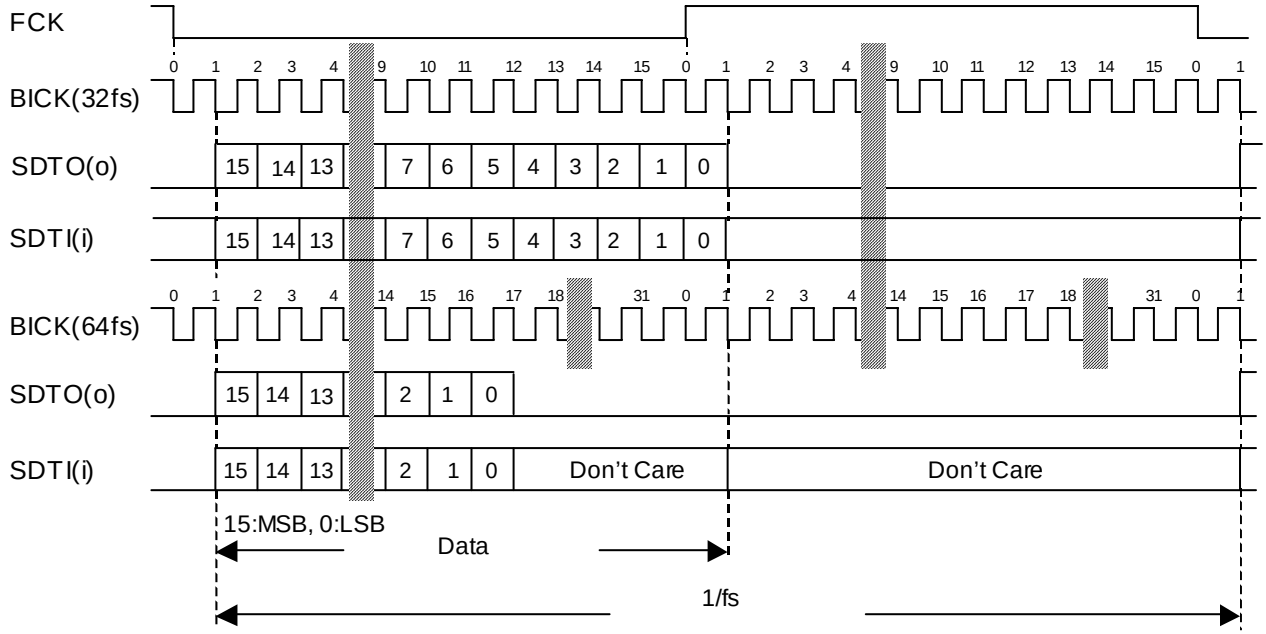


Figure 27. Mode 3 Timing

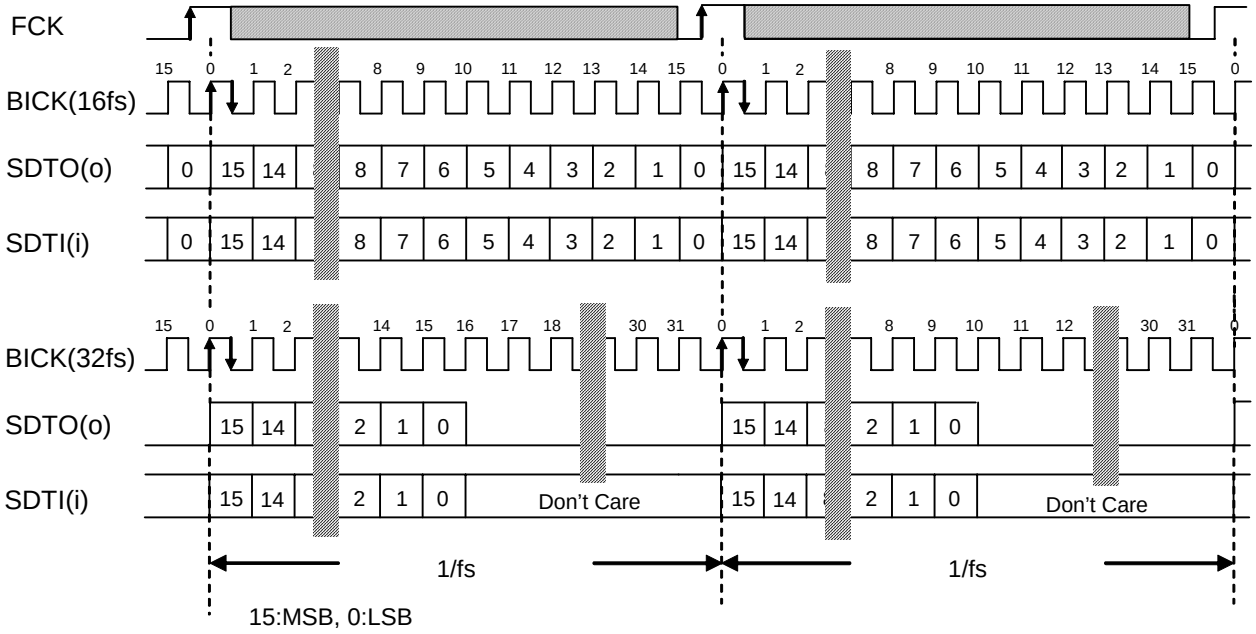


Figure 28. Mode 0 Timing (BCKP = "0", MSBS = "0")

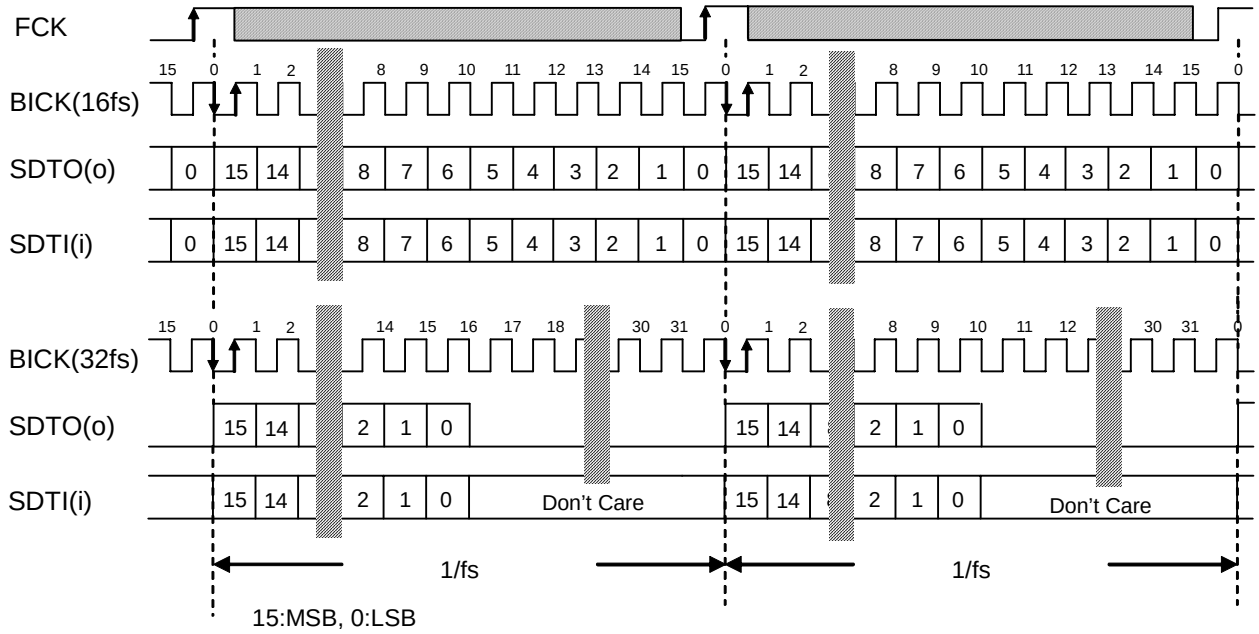


Figure 29. Mode 0 Timing (BCKP = "1", MSBS = "0")

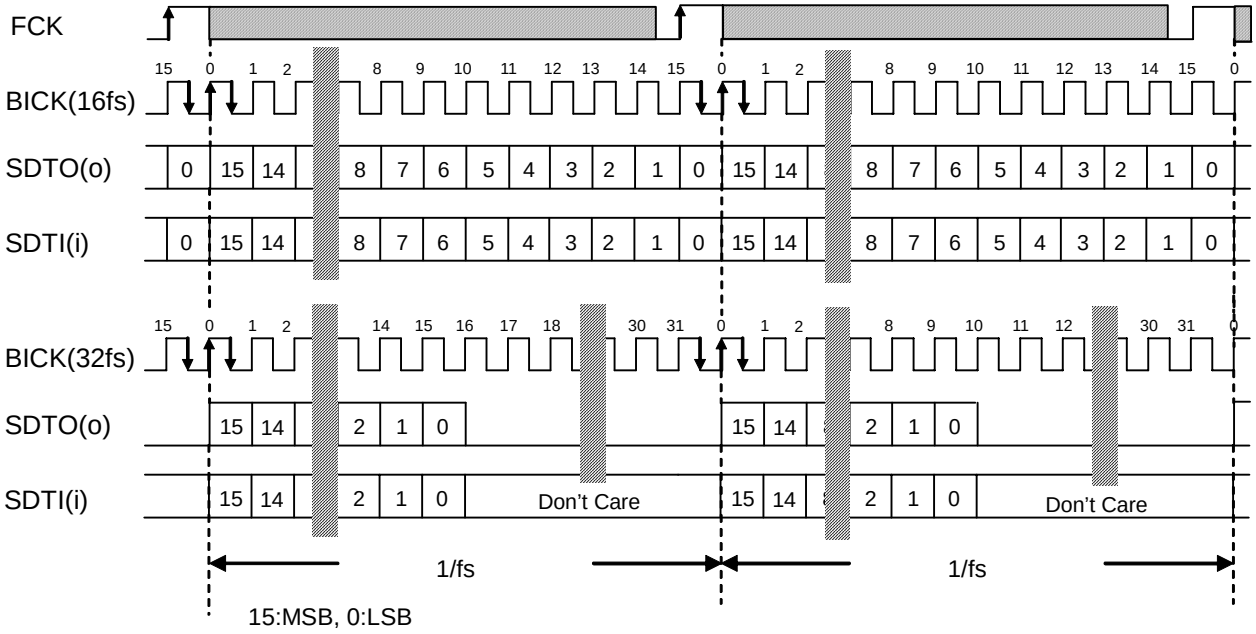


Figure 30. Mode 0 Timing (BCKP = "0", MSBS = "1")

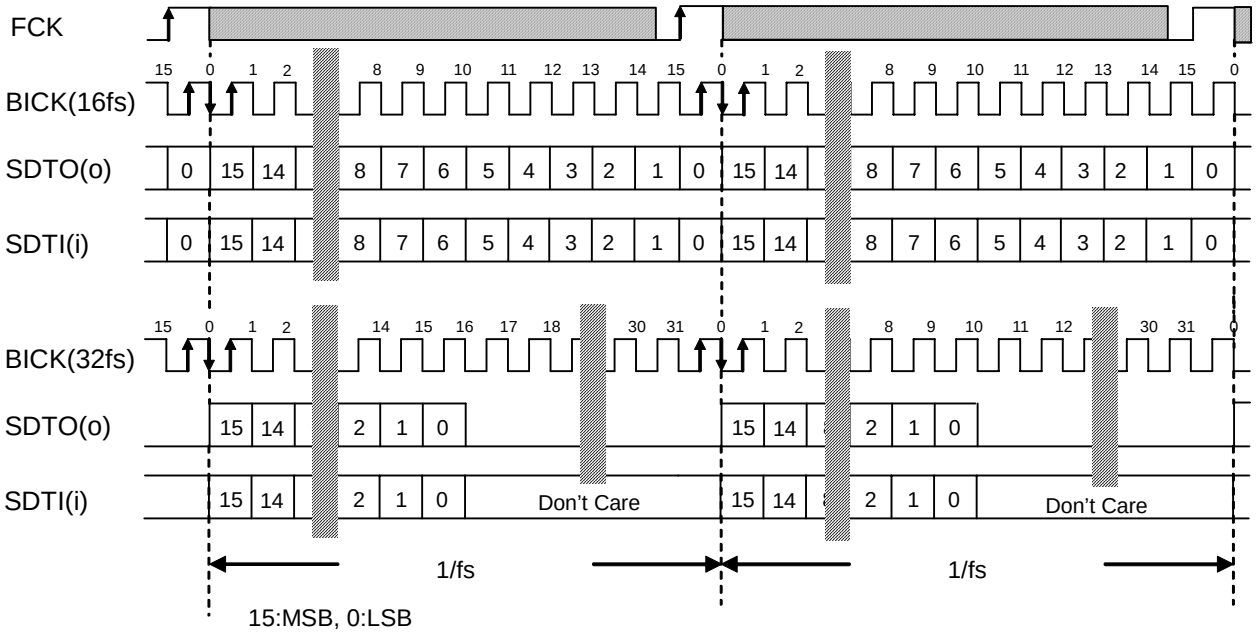


Figure 31. Mode 0 Timing (BCKP = "1", MSBS = "1")

■ System Reset

When power-up, the PDN pin should be "L" and change to "H" after all powers are supplied. "L" time of 150ns or more is needed to reset the AK4634.

The ADC enters an initialization cycle when the PMADC bit is changed from "0" to "1". The initialization cycle time is 1059/fs, or 133ms@fs = 8kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. The DAC does not require an initialization cycle.

(Note) Off-set occurs in the initial data depending on the conditions of a microphone and cut-off frequency of HPF. When Off-set becomes a problem, lengthen initialization time of ADC as ADRST bit = "0" or do not use initial output data of ADC.

	Init Cycle			
ADRST bit	Cycle	fs = 8kHz	fs = 16kHz	fs = 48kHz
0	1059/fs	132.4ms	66.2ms	22.1ms
1	291/fs	36.4ms	18.2ms	6.1ms

Table 18 Initialization cycle of ADC

■ Thermal Shut Down

When the internal device temperature rises up irregularly (e.g. output pins of speaker amplifier are shortened), the AK4634 is powered down automatically and then THDET bit becomes "1". The powered-down speaker amplifier do not return to normal operation unless SPK-Amp blocks of the AK4634 are reset by the PDN pin "L". The device status can be monitored by THDET bit.

■ MIC/LINE Input Selector

The AK4634 has an input selector. When MDIF bit is "0", LIN bit selects the MIC pin or LIN pin. When MDIF bit is "1", full-differential input is available.

MDIF bit	LIN bit	Input circuit	Input pin	
0	0	Single-End	MIC pin	(default)
0	1	Single-End	LIN pin	
1	x	Differential	MICP/MICN pin	

Table 19. Input Select (x: Don't care)

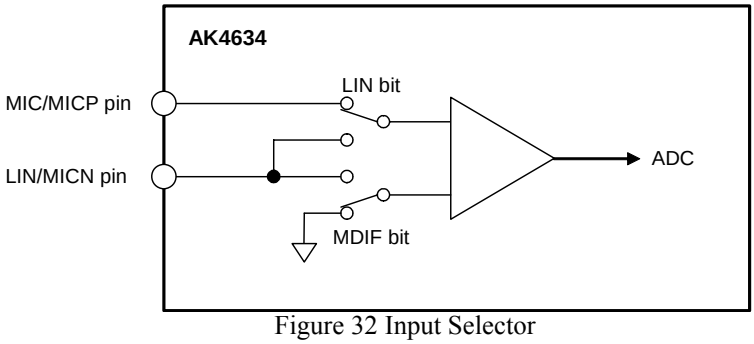


Figure 32 Input Selector

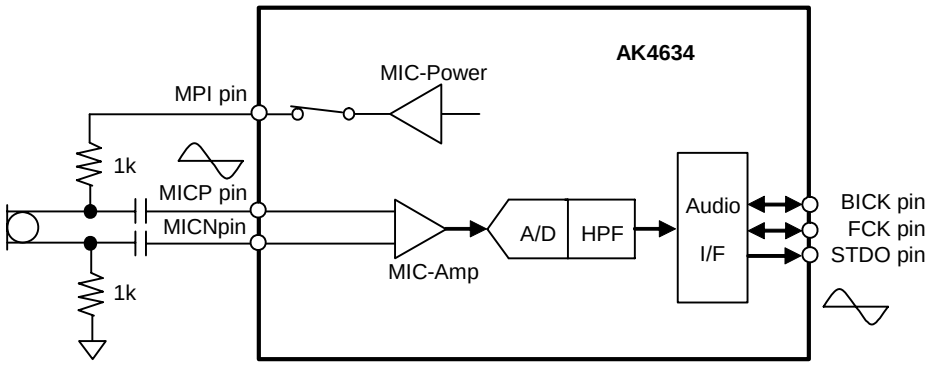


Figure 33. MIC Differential Input Circuit

■ MIC Gain Amplifier

The AK4634 has a Gain Amplifier for Microphone input. These gains are selected by the MGAIN3-0 bit. The typical input impedance is 30kΩ.

MGAIN3 bit	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0	0dB	
0	0	0	1	+20dB	(default)
0	0	1	0	+26dB	
0	0	1	1	+32dB	
0	1	0	0	+10dB	
0	1	0	1	+17dB	
0	1	1	0	+23dB	
0	1	1	1	+29dB	
1	0	0	0	+3dB	
1	0	0	1	+6dB	
Others				N/A	

Table 20. Input Gain (N/A: Not available)

■ MIC Power

The MPI pin supplies power for a Microphone. This output voltage is proportional to 0.8 x AVDD typically and the load resistance is minimum 2kΩ. Any capacitor must not be connected to the MPI pin directly. (Figure 34)

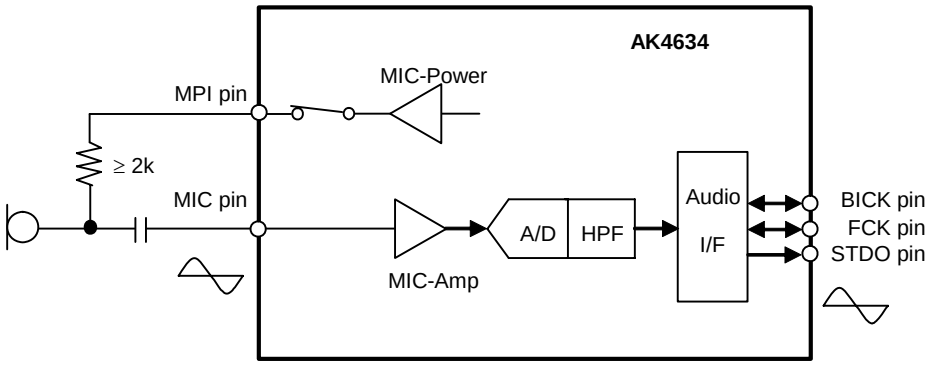
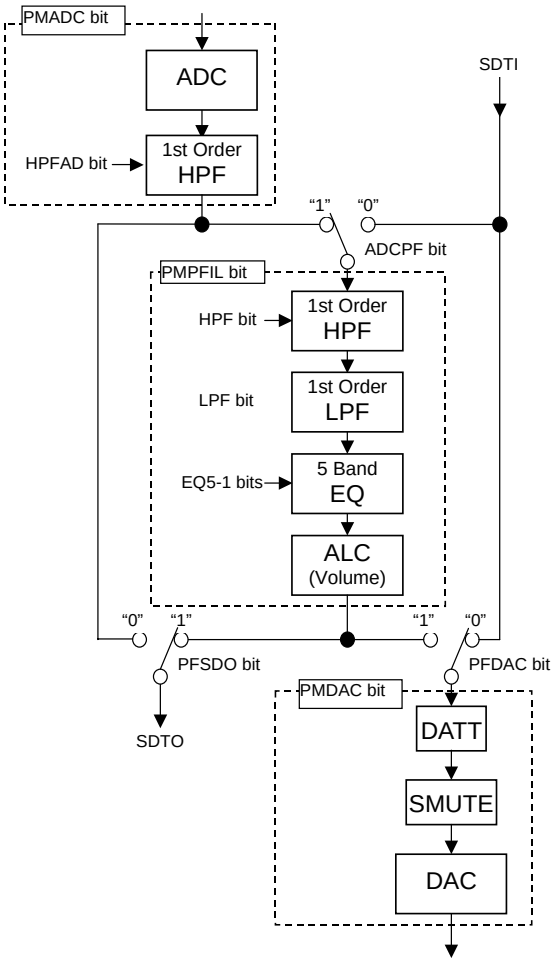


Figure 34. MIC Block Circuit

■ Digital Block

The digital block consists of block diagram as shown in Figure 35. The AK4634 can choose various signal processing on a recording path or a playback path by setting ADCPF bit, PFDAC bit and PFSDO bit. (Figure 35 ~ Figure 38, Table 21)



(1) ADC: Include a Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) DAC: Include a Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(3) HPF: High Pass Filter. Applicable to use as Wind-Noise Reduction Filter. (See "Programmable Filter".)
(4) LPF: Low Pass Filter (See "Digital Programmable Filter".)
(5) 5-Band EQ: Applicable to use as Equalizer or Notch Filter. (See "Digital Programmable Filter".)
(6) ALC: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC".)
(7) DATT: 4-step Digital Volume for recording path. (See "Digital Volume 2")
(8) SMUTE: Soft mute. (See "Soft Mute".)

Figure 35. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	Figure
Recording Mode	1	0	1	Figure 36
Reproduction Mode	0	1	0	Figure 37
Loop Back Mode	1	1	1	Figure 38

Table 21 Recording Reproduction Mode

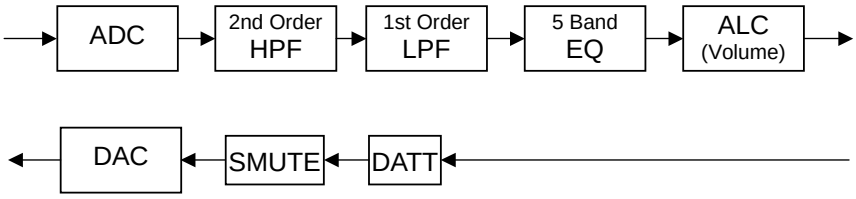


Figure 36. Path at Recording Mode (default)

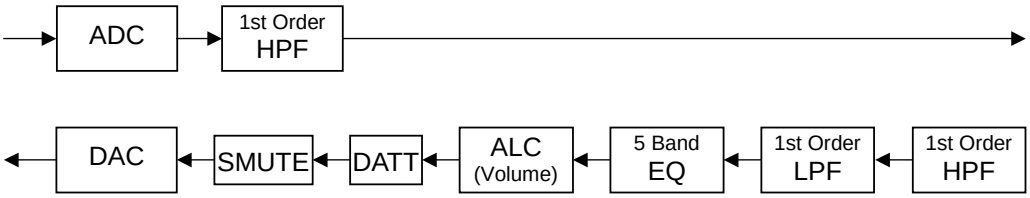


Figure 37. Path at Playback Mode

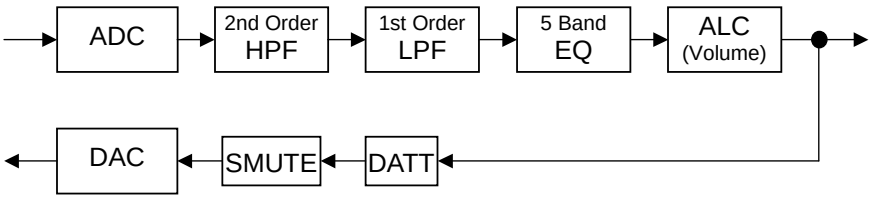


Figure 38. Path at Recording & Playback Mode

■ Digital Programmable Filter Circuit

The AK4634 has 2 steps of 1st order HPF, 1st order LPF and 5-band Equalizer built-in in a recording/playback path.

(1) High Pass Filter (HPF)

Normally, this HPF is used as a Wind-Noise Reduction Filter. This is composed with 2 steps of 1st order HPF. The coefficient of both HPF is the same and set by F1A13-0 bits and F1B13-0 bits. HPFAD bit controls ON/OFF of the 1st step HPF and HPF bit controls ON/OFF of the 2nd step HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when HPFAD = HPF bits = "0" or PMADC = PMPFIL bits = "0".

fs : Sampling frequency
fc : Cut-off frequency

Register setting (Note 33)
HPF: F1A[13:0] bits = A, F1B[13:0] bits = B
(MSB = F1A13, F1B13; LSB = F1A0, F1B0)

$$A = \frac{1}{1 + \tan(\pi fc/fs)}, \quad B = \frac{1 - \tan(\pi fc/fs)}{1 + \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 - Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 1.6Hz at fs=16kHz)

(2) Low Pass Filter(LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when LPF bit = "0" or PMPFIL bits = "0".

fs : Sampling frequency
fc : Cut-off frequency

Register setting (Note 33)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1/\tan(\pi fc/fs)}, \quad B = \frac{1 - 1/\tan(\pi fc/fs)}{1 + 1/\tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at fs=44.1kHz)

(3) 5-band Equalizer

This block can be used as Equalizer or Notch Filter. ON/OFF 5-band Equalizer (EQ1, EQ2, EQ3, EQ4 and EQ5) can be controlled independently by EQ1, EQ2, EQ3, EQ4 and EQ5 bits. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5.

fs : The Sampling frequency
$fo_1 \sim fo_5$: The Center frequency
$fb_1 \sim fb_5$: The Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: The Gain ($-1 \leq K_n < 3$)

Register setting (Note 33)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer Function

$$H(z) = (1 + h_1(z) + h_2(z) + h_3(z) + h_4(z) + h_5(z))$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency should be set as below
$fo_n / fs < 0.497$

When gain of K is set to "–1", the equalizer becomes notch filter. The central frequency of a real notch filter deviates from the above calculation, if the central frequency of each band is near. The control soft that is attached to the evaluation board has a function that revises a gap of frequency, and calculates the coefficient. When the central frequency of each band is near, revise the central frequency and confirm the frequency response.

Note 33.
[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ Input Digital Volume (Manual Mode)

When ADCPF bit = "1" and ALC1 bit = "0", ALC block becomes an input digital volume (manual mode). The digital volume's gain is set by IVOL7-0 bits as shown in Table 22. The IVOL value is changed at zero cross or zero cross time out. The zero crossing timeout period is set by ZTM1-0 bits.

IVOL7-0bits	GAIN(0dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 22. Input Digital Volume Setting

When writing to the IVOL7-0 bits continually, the control register should be written in an interval more than zero crossing timeout. If not, a zero crossing counter is reset at each time and the volume will not be changed. However, it could be ignored when writing the same register value as the last time. At this time, zero crossing counter is not reset, so it can be written in an interval less than zero crossing timeout.

■ Output Digital volume (Manual mode)

When ADCPF bit = "0" and ALC2 bit = "0", ALC block become an output digital volume (manual mode). The digital volume's gain is set by OVOL7-0 bits as shown in Table 23. The OVOL7-0 bits value are reflected to this output volume at zero cross or zero cross time out. The zero crossing timeout period is set by ZTM1-0 bits.

OVOL7-0bits	GAIN(0dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 23 Output Digital Volume Setting

When writing to the OVOL7-0 bits continually, the control register should be written in an interval more than zero crossing timeout. If not, a zero crossing counter is reset at each time and the volume will not be changed. However, It could be ignored when writing a same register value as the last time. At this time, zero crossing counter is not reset, so it can be written by an interval less than zero crossing timeout.

■ Output Digital Volume2

AK4634 has 4 steps output volume in addition to the volume setting by OVOL7-0 bits. This volume is set by DATT1-0 bits as shown in Table 24.

DATT1-0bits	GAIN(0dB)	Step	
0H	0.0	6.0dB	(default)
1H	-6.0		
2H	-12.0		
3H	-18.1		

Table 24. Output Digital Volume2 Setting

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit = "1", ALC operation is enable at recording path. When ADCPF bit = "0", ALC operation is enable at playback path. ON/OFF switching of ALC operation is controlled by ALC1 bit for recording and ALC2 bit for playback.

1. ALC Limiter Operation

During the ALC limiter operation, if the output data exceeds the ALC limiter detection level (Table 25), the volume value is automatically attenuated by the amount defined in LMAT1-0 bits (Table 26).

When ZELMN bit = "0" (zero cross detection valid), the IVL and VOL value is changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 27). When ALC output level exceeds full-scale at LFST bit = "1", VOL value is immediately (Period: 1/fs) changed in 1 step. When ALC output level is less than full-scale, VOL value is changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = "1" (zero cross detection invalid), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds the ALC limiter detection level.

LMTH1	LMTH0	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	(default)
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 25. ALC Limiter Detection Level / Recovery Waiting Counter Reset Level

LMAT1	LMAT0	ALC1 Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 26. ALC Limiter ATT Step Setting

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 27. ALC Zero Crossing Timeout Period Setting

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 28) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 25) during the wait time, the ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 29) up to the set reference level (Table 30, Table 31) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 27). The ALC recovery operation is executed in a period set by WTM2-0 bits.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01"(2 steps), VOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (IREF7-0 or OREF5-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits (Table 32).

WTM2	WTM1	WTM0		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 28. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1	0.375dB	(default)
0	1	2	0.750dB	
1	0	3	1.125dB	
1	1	4	1.500dB	

Table 29. ALC Recovery GAIN Step

IREF7-0bits	GAIN(0dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
C5H	+19.5		
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 30. Reference Level at ALC Recovery operation for recoding

OREF5-0bits	GAIN(0dB)	Step	
3CH	+36.0	1.5dB	(default)
3BH	+34.5		
3AH	+33.0		
:	:		
28H	+6.0		
:	:		
25H	+1.5		
24H	0.0		
23H	-1.5		
:	:		
2H	-51.0		
1H	-52.5		
0H	-54.0		

Table 31. Reference Level at ALC Recovery operation for playback

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	4 times	(default)
0	1	8 times	
1	0	16times	
1	1	N/A	

Table 32. First Recovery Speed Setting (N/A: Not available)

3. The Volume at the ALC Operation

The current volume value at the ALC operation is reflected in VOL7-0 bits. It is enable to check the current volume value by reading the register value of VOL7-0 bits.

This function is available only in 3-wire mode. The volume value at the ALC operation can not be read in I^2C mode.

VOL7-0bits	GAIN(0dB)
F1H	+36.0
F0H	+35.625
EFH	+35.25
:	:
C5H	+19.5
:	:
92H	+0.375
91H	0.0
90H	–0.375
:	:
2H	–53.625
1H	–54.0
0H	MUTE

Table 33. Value of VOL7-0 bits

4. Example of the ALC Operation for Recording Operation

Table 34 shows the examples of the ALC setting for microphone recording.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELM	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	23.2ms
WTM2-0	Recovery waiting period *WTM1-0 bits should be more than or equal to ZTM1-0 bits	000	16ms	011	23.2ms
IREF7-0	Maximum gain at recovery operation	C5H	19.5dB	C5H	19.5dB
IVOL7-0	Gain of IVOL	C5H	19.5dB	C5H	19.5dB
LMAT1-0	Limiter ATT step	00	1step	00	1step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
ALC1	ALC enable	1	Enable	1	Enable
FRSL1-0	Speed of Fast Recovery	00	4 times	00	4times

Table 34. Example of the ALC Setting (Recording)

5. Example of ALC for Playback Operation

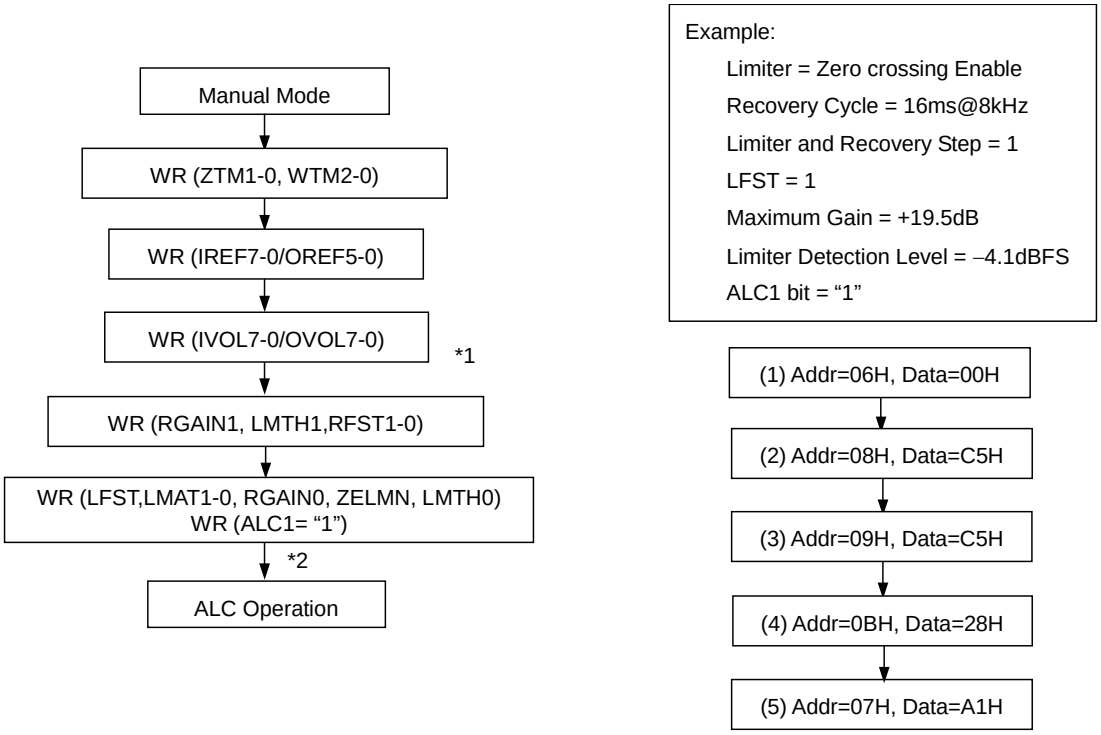
Table 35 shows the example of the ALC setting for playback.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELM	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	01	23.2ms
WTM2-0	Recovery waiting period *WTM1-0 bits should be more than or equal to ZTM1-0 bits	000	16ms	011	23.2ms
OREF5-0	Maximum gain at recovery operation	28	+6dB	28	+6dB
OVOL7-0	Gain of IVOL	91	0dB	91	0dB
LFST	Fast Limiter Operation	1	ON	1	ON
LMAT1-0	Limiter ATT step	00	1step	00	1step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
ALC2	ALC enable	1	Enable	1	Enable
FRSL1-0	Speed of Fast Recovery	00	4 times	00	4 times

Table 35. Examples of the ALC Setting (Play back)

The following registers must not be changed during the ALC operation. These bits should be changed, after the ALC operation is finished by ALC1 bit = ALC2 bit = "0" or PMPFIL bit = "0". When ALC is restarted, after ALC1 bit and ALC2 bit set to "0" or PMPFIL bit sets to "0", the waiting time of zero crossing timeout is not needed.

LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, IREF7-0/OREF7-0, ZELM, RFST1-0, LFST



Note : WR : Write

*1: The value of volume at starting should be the same or smaller than REF's.
*2: When setting ALC1 bit or ALC2 bit to "0", the operation is shifted to manual mode after passing the zero crossing time set by ZTM1-0 bits.

Figure 39. Registers set-up sequence at the ALC operation

■ SOFTMUTE

Soft mute operation is performed in the digital input domain. When the SMUTE bit changes to "1", the input signal is attenuated by –∞ ("0") in 245/fs cycles (31msec@fs=8kHz). When the SMUTE bit is returned to "0", the mute is cancelled and the input attenuation gradually changes to 0dB in 245/fs cycles (31msec@fs=8kHz). If the soft mute is cancelled within the 245/fs cycles (31msec@fs=8kHz), the attenuation is discontinued and returned to 0dB. The soft mute for Playback operation is effective for changing the signal source without stopping the signal transmission.

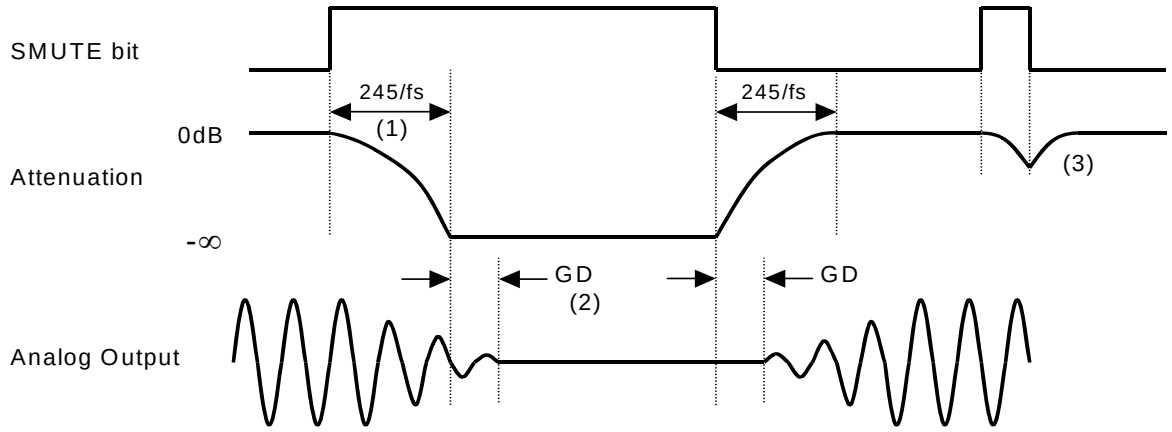


Figure 40. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") in 245/fs cycles (31msec@fs=8kHz).
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled within the 245/fs cycles (31msec@fs=8kHz), the attenuation is discounted and returned to 0dB within the same cycle.

■ MONO LINE OUTPUT (AOUT pin)

A signal of DAC is output from the AOUT pin. When the DACA bit is "0", this output is OFF. When the LOVL bit is "1", this gain changes to +2dB. The load resistance is 10kΩ(min). When PMAO bit is "0" and AOPSN bit is "0", the mono line output enters power-down mode and is pulled down by 100Ω(typ). If PMAO bit is controlled when AOPS bit = "1", POP noise will be reduced at power-up and down. Then, this line should be pulled down by 20kΩ of resister after C-coupling shown in Figure 41. This rising and falling time is max 300 ms at C = 1.0μF . When PMAO bit is "1" and AOPS bit is "0", the mono line output enters power-up state.

LOVL bits	Gain	
0	0dB	(default)
1	+2dB	

Table 36. Mono line output volume setting

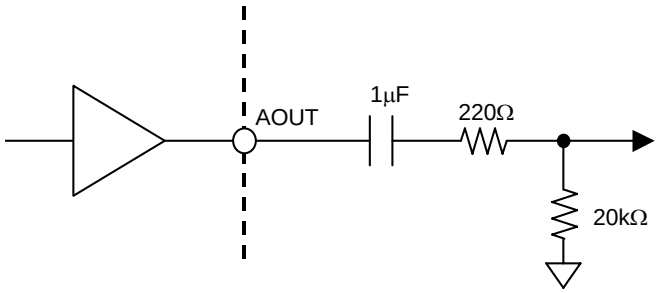


Figure 41. AOUT external circuit when using POP Reduction function

AOUT Control Sequence in case of using POP Reduction Circuit

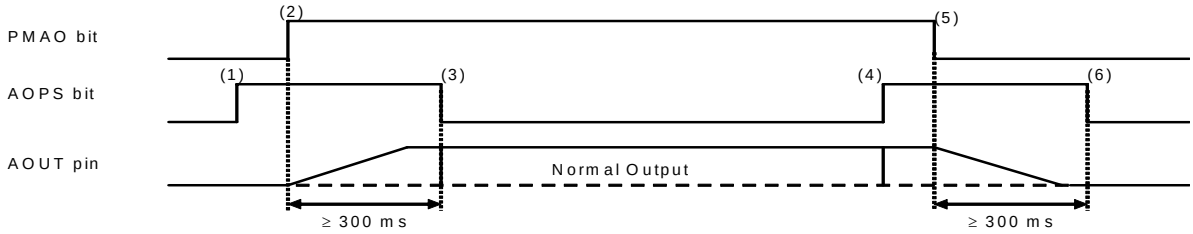


Figure 42. Mono Line Output Control Sequence when using POP Reduction function

(1) Set AOPS bit = "1". Mono line output enters the power-save mode.
(2) Set PMAO bit = "1". Mono line output exits the power-down mode.
AOUT pin rises up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set AOPS bit = "0" after AOUT pin rises up. Mono line output exits the power-save mode.
Mono line output is enabled.
(4) Set AOPS bit = "1". Mono line output enters power-save mode.
(5) Set PMAO bit = "1". Mono line output enters power-down mode.
AOUT pin falls down to VSS1. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set AOPS bit = "0" after AOUT pin falls down. Mono line output exits the power-save mode.

■ Speaker Output

AK4634 has a Mono Class-D Speaker-Amp. Power supply for Speaker-Amp(SVDD) can be set from 2.2V up to 4.0V.

The Speaker is mono and BTL output, and can drive dynamic speaker and piezo speaker without LPF (filter-less). This speaker can output 400W@8Ω at SVDD = 3.3V, SPKG bit = "0". This gain is set by SPKG bit (Table 37). The output level of speaker amp is depended on voltage of SVDD and SPKG bit.

SPKG bit	Gain
0	0dB
1	+2dB (Note 34)

Note 34. The signals more than -2dBFS clip.
Table 37. SPK- Amp Gain

The power up/down speaker amp is controlled by PMSPK bit. When PMSPK bit is "0", the SPP and SPN pins output VSS3 level. ON/OFF of the speaker amp output is controlled by SPOUTE bit. When SPOUTE bit is "0", the SPP and SPN pins are in VSS3-state forcibly. When outputting from the DAC to the speaker, PMDAC bit should be set to "1".

Follow the following sequence.

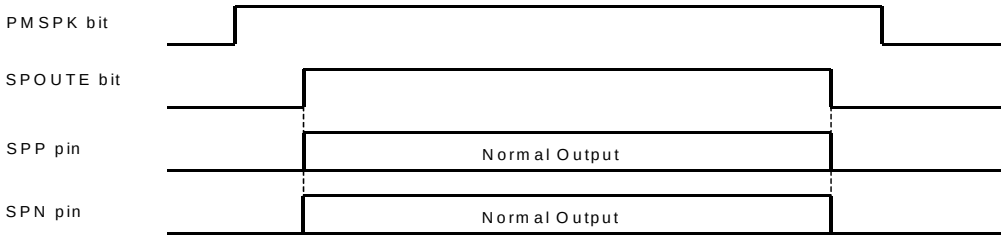


Figure 43. Power-up/Power-down Timing for Speaker-Amp

<Caution for using Piezo Speaker>

When a piezo speaker is used, resistances more than 10Ω should be connected between the SPP/SPN pins and speaker in series respectively as shown in Figure 44. Zener diodes should be connected between speaker and GND as shown in Figure 44, in order to protect SPK-Amp of the AK4634 from the power that is the piezo speaker output when the speaker is pressured. Zener diodes of the following Zener voltage should be used.

92% of SVDD ≤ Zener voltage of Zener diodo(ZD of Figure 44) ≤ SVDD+0.3V
Ex) In case of SVDD = 3.8V :3.5V ≤ ZD ≤ 4.1V
For example, Zener diode which Zener voltage is 3.9V(Min 3.7V, Max 4.1V) can be used.

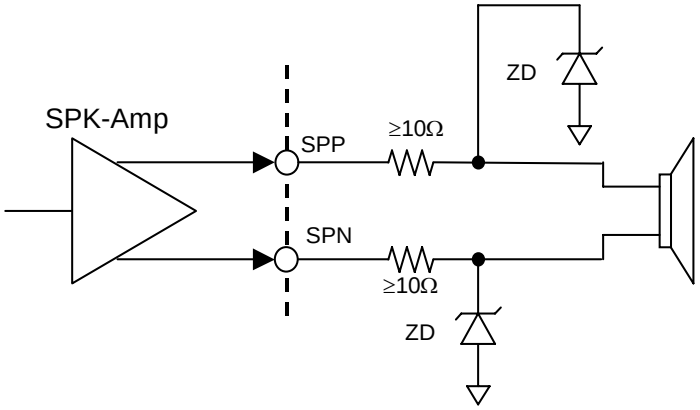


Figure 44. Circuit of Speaker Output (using a piezo speaker)

■ BEEP Generate

The AK4634 generates and output square wave from speaker amp. After outputting the signal during the time set by BPON6-0 bits, the AK4634 stops the output signal during the time set by BPOFF6-0 bits (Figure 46). The repeat count is set by BPTM6-0 bit, and the output level is set by BPLVL2-0 bits. When BPCNT bit is "0", if BPOUT bit is written "1", the AK4634 outputs the beep for the times of repeat count. When the output finish, BPOUT bit is set to "0" automatically. When BPCNT bit is set to "1", it outputs the beep in succession regardless of repeat count, on-time and off-time.

< Setting parameter >

1) Output Frequency (Table 38 ~ Table 40)
2) ON Time (Table 41)
3) OFF Time (Table 42)
4) Repeat Count (Table 43)
5) Output Level (Table 44)

BPFR1-0, BPON7-0, BPOFF7-0, BPTM6-0 and BPLVL3-0 bits should be set when BPOUT =BPCNT = "0".
BPCNT bit is given priority in BPOUT bit. When BPOUT bit be set to "1", if BPCNT bit is set to "0", BPOUT bit is set to "0" forcibly.

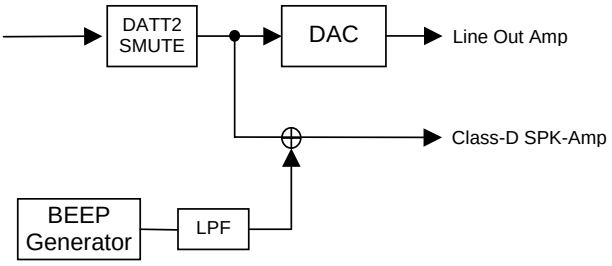


Figure 45. BEEP signal output path

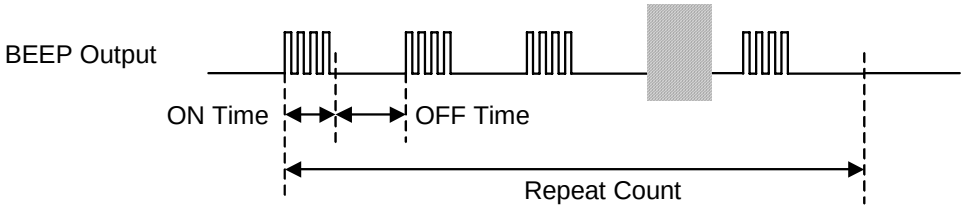


Figure 46. Beep output

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]		
	fs = 48kHz system (Note 35)	fs = 44.1kHz system (Note 36)	
00	4000	4009	(default)
01	2000	2005	
10	1000	1002	
11	N/A		

Note 35. Sampling frequency is 8kHz, 16kHz, 32kHz or 48kHz.
Note 36. Sampling frequency is 11.025kHz, 22.05kHz or 44.1kHz.

Table 38. Beep signal frequency (PLL Master/Slave Mode: reference clock: MCKI) (N/A: Not available)

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]			
	FS3-2 bits = "00"	FS3-2 bits = "01"	FS3-2 bits = "10"	
00	fs/2.75	fs/5.5	fs/11	(default)
01	fs/5.5	fs/11	fs/22	
10	fs/11	fs/22	fs/44	
11	N/A			

Table 39. Beep signal frequency (PLL Slave Mode: reference clock : FCK/BICK) (N/A: Not available)

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]				
	FS1-0 bits = "00"	FS1-0 bits = "01"	FS1-0 bits = "10"	FS1-0 bits = "11"	
00	fs/11	fs/2.75	fs/55	fs/11	(default)
01	fs/22	fs/5.5	fs/11	fs/22	
10	fs/44	fs/11	fs/22	fs/44	
11	N/A				

Table 40. Beep signal frequency (EXT Slave/Master Mode) (N/A: Not available)

BPON7-0 bits	ON Time of BEEP Generator [msec]		Step [msec]		
	fs = 48kHz system (Note 35)	fs = 44.1kHz system (Note 36)	fs = 48kHz system (Note 35)	fs = 44.1kHz system (Note 36)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.86			
2H	24.0	23.95			
3H	32.0	31.93			
4H	40.0	39.9			
:	:				
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 35. Sampling frequency is 8kHz, 16kHz, 32kHz or 48kHz.
Note 36. Sampling frequency is 11.025kHz, 22.05kHz or 44.1kHz.

Table 41. Beep output ON-time (PLL Master/Slave Mode reference clock: MCKI)

BPOFF7-0 bits	OFF Time of BEEP Generator [msec]		Step [msec]		
	fs = 48kHz system (Note 35)	fs = 44.1kHz system (Note 36)	fs = 48kHz system (Note 35)	fs = 44.1kHz system (Note 36)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.86			
2H	24.0	23.95			
3H	32.0	31.93			
4H	40.0	39.9			
:	:	:			
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 35. Sampling frequency is 8kHz, 16kHz, 32kHz or 48kHz.
Note 36. Sampling frequency is 11.025kHz, 22.05kHz or 44.1kHz.

Table 42. Beep output OFF-time (PLL Master/Slave Mode reference clock: MCKI)

BPTM6-0 bits	Repeat Count	
0H	1	(default)
1H	2	
2H	3	
3H	4	
:	:	
7DH	126	
7EH	127	
7FH	128	

Table 43. Beep output Repeat Count

BPLVL2-0 bits	.Beep Output Level	STEP	
0H	0dB	3dB	(default)
1H	–3dB		
2H	–6dB		
3H	–9dB		
4H	–12dB		
5H	–18dB	6dB	
6H	–24dB		
7H	–30dB		

Note 37. Power supply is 3.3V
Note 38. Beep output amplitude as 0dB setting is 4.4Vpp@ load resistance = 8Ω + 10μH, SVDD=3.3V

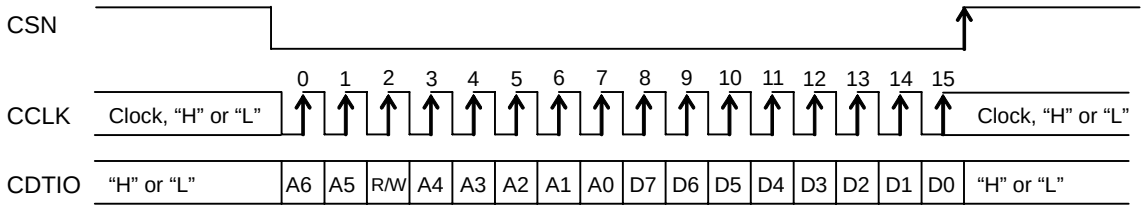
Table 44. Beep output level

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written and read by the 3-wire μP interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. Data writing is valid on the rising edge of the 16th CCLK after the falling edge of CSN. CSN should be set to "H" every after a data writing for each address. In reading operation, the CDTIO pin changes to output mode at the falling edge of 8th CCLK and outputs D7-D0. The output finishes on the rising edge of CSN. However this reading function is available only at READ bit = "1". When READ bit = "0", the CDTIO pin stays as Hi-Z even after the falling edge of 8th CCLK. The CDTIO pin is placed in a Hi-Z state except outputting data at read operation mode. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at the PDN pin = "L".

Note 39. A read operation is available at 00H ~ 11H, 20H ~ 24H and 30H addresses. When reading the address 12H ~ 1FH, 25H ~ 2FH and 31H ~ 4FH, the register values are invalid.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data

Figure 47. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4634 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 48 shows the data transfer sequence for I²C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 54). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010010" (Figure 49). If the slave address matches that of the AK4634, the AK4634 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 55). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4634. The format is MSB first, and those most significant 1-bits are fixed to zeros (Figure 50). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 51). The AK4634 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 54).

The AK4634 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4634 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 56) except for the START and STOP conditions.

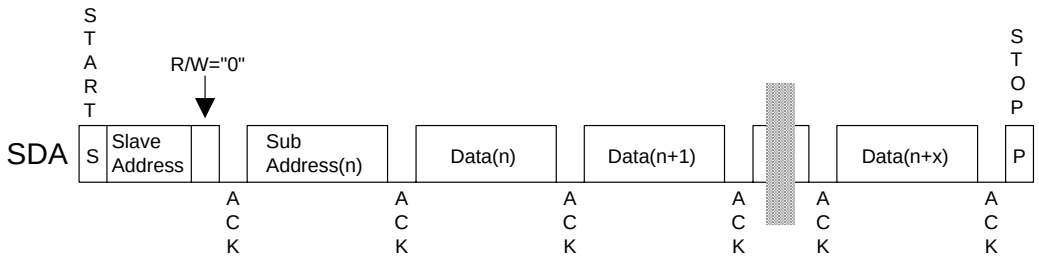


Figure 48. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	1	0	R/W

Figure 49. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 50. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 51. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for READ operation of the AK4634. After a transmission of data, if the master generates an acknowledge instead of terminating a write cycle, the internal 7-bit address counter of the AK4634 is incremented by one, and the next data is automatically taken into the next address so that the data can be read from the AK4634. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

Note 39. A read operation is available at 00H ~ 11H, 20H ~ 24H and 30H addresses. When reading the address 12H ~ 1FH, 25H ~ 2FH and 31H ~ 4FH, the register values are invalid.

The AK4634 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4634 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4634 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates stop condition, the AK4634 ceases transmission.

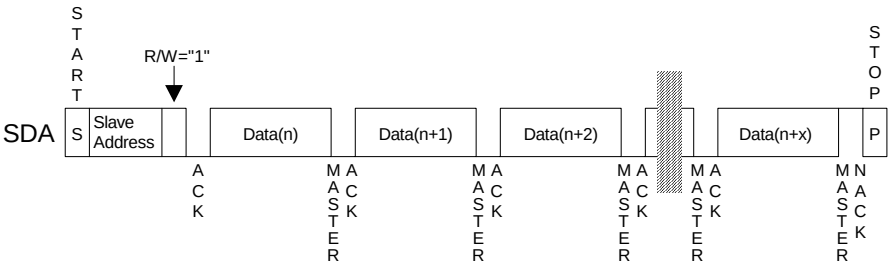


Figure 52. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4634 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates stop condition, the AK4634 ceases transmission.

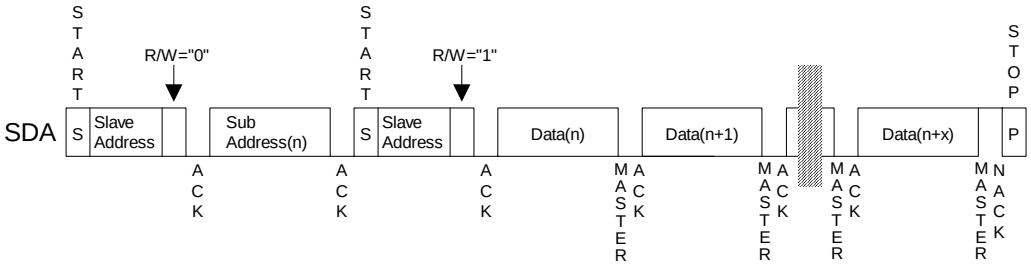


Figure 53. RANDOM ADDRESS READ

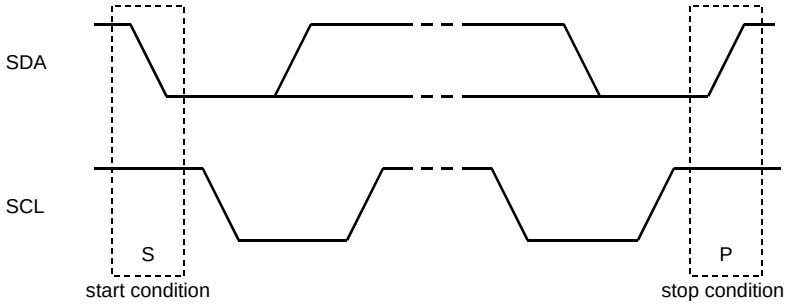


Figure 54. START and STOP Conditions

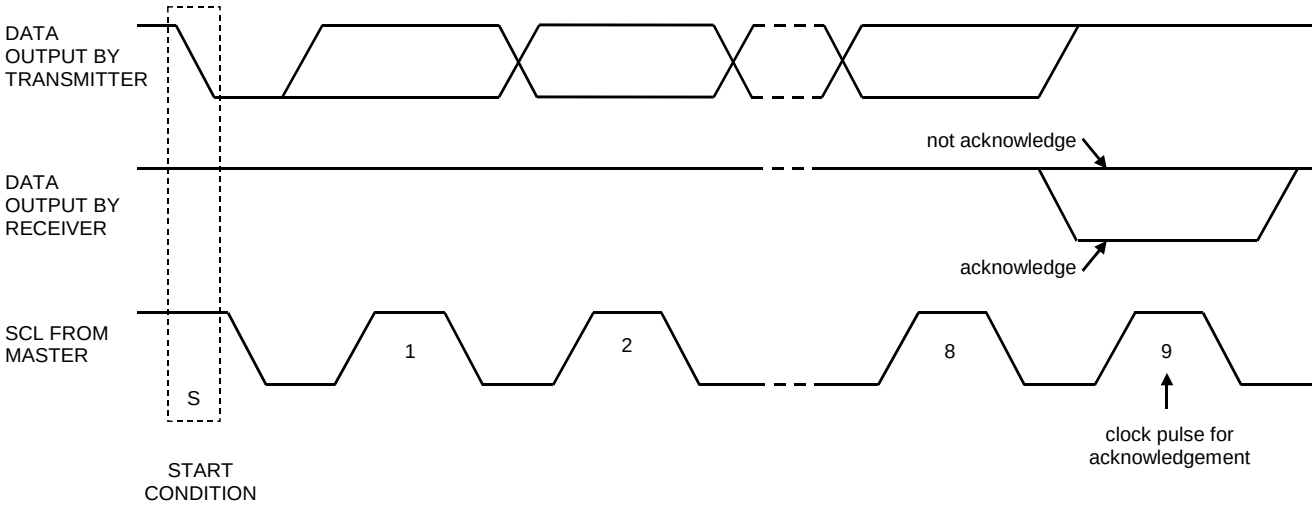


Figure 55. Acknowledge on the I^2C-Bus

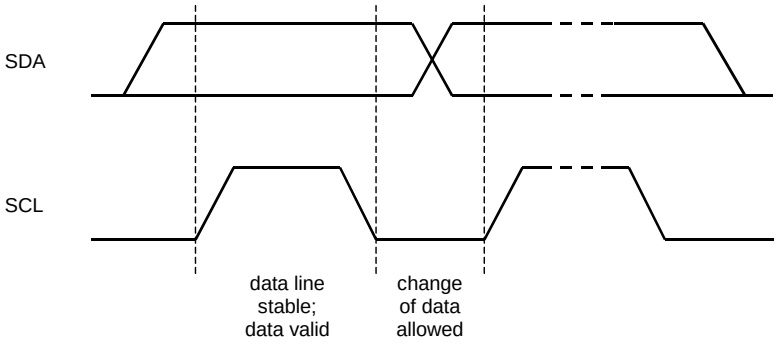


Figure 56. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	0	PMSPK	PMAO	PMDAC	0	PMADC
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPOUTE	0	DACS	DACA	MGAIN3	PMMP	MGAIN2	MGAIN0
03H	Signal Select 2	PFSDO	AOPS	MGAIN1	0	SPKG	0	PFDAC	ADCPF
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
05H	Mode Control 2	ADRST	FCKO	FS3	MSBS	BCKP	FS2	FS1	FS0
06H	Timer Select	0	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
09H	Digital Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
0AH	Digital Volume Control	OVOL7	OVOL6	OVOL5	OVOL4	OVOL3	OVOL2	OVOL1	OVOL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0CH	Reserved	0	0	0	0	0	0	1	0
0DH	ALC LEVEL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0EH	Signal Select 3	DATT1	DATT0	SMUTE	MDIF	1	0	1	READ
0FH	Thermal Shutdown	THDET	0	0	0	0	0	0	0
10H	Signal Select 4	0	LOVL	0	0	0	0	LIN	0
11H	Digital Filter Select 1	0	0	LPF	HPF	0	0	0	1
12H	Reserved	0	0	0	0	0	0	0	0
13H	Reserved	0	0	0	0	0	0	0	0
14H	Reserved	0	0	0	0	0	0	0	0
15H	Reserved	0	0	0	0	0	0	0	0
16H	Reserved	0	0	0	0	0	0	0	0
17H	Reserved	0	0	0	0	0	0	0	0
18H	Reserved	0	0	0	0	0	0	0	0
19H	Reserved	0	0	0	0	0	0	0	0
1AH	Reserved	0	0	0	0	0	0	0	0
1BH	Reserved	0	0	0	0	0	0	0	0
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
21H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
22H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
23H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
24H	BEEP VOL/Control	BPOUT	0	0	0	0	BPLVL2	BPLVL1	BPLVL0
25H	Reserved	0	0	0	0	0	0	0	0
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

The PDN pin = "L" resets the registers to their default values.

Note 40. "0" bits must contain a "0" value. "1" bits must contain a "1" value.
Note 41. Reading of address 12H ~ 1FH, 25H ~ 2FH and 31H ~ 4FH are not possible.
Note 42. 0FH and 0DH are for address read only. However, 0DH address cannot be read at I^2C –bus control mode. Writing access to 0DH and 0FH does not effect the operation.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	0	PMSPK	PMAO	PMDAC	0	PMADC
R/W		R/W	R/W	R	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	0

PMADC: ADC Block Power Control
0: Power down (default)
1: Power up
When the PMADC bit changes from "0" to "1", the initialization cycle (1059/fs=133ms@8kHz) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Block Power Control
0: Power down (default)
1: Power up

PMAO: Mono Line Out Power Control
0: Power down (default)
1: Power up

PMSPK: Speaker Block Power Control
0: Power down (default)
1: Power up

PMVCM: VCOM Block Power Control
0: Power down (default)
1: Power up

PMPFIL: Programmable Filter Block (HPF/ LPF/ 5-Band EQ/ ALC) Power Control
0: Power down (default)
1: Power up

Each block can be powered-down respectively by writing "0" to each bit. When the PDN pin is "L", all blocks are powered-down.

When PMPLL and MCKO bits and all bits in 00H address are "0", all blocks are powered-down.

When any of the blocks are powered-up, the PMVCM bit must be set to "1". When PMPLL and MCKO bits and all bits in 00H address are "0", PMVCM bit can be "0".

When any block of ADC, DAC, SPK, or Programmable digital filter is powered-up (PMADC bit = "1"or PMDAC bit = "1" or PMSPK bit = "1" PMPFIL bit = "1"), the clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
R/W		R	R	R	R	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Block Power Control Select
0: PLL is Power down and External is selected. (default)
1: PLL is Power up and PLL Mode is selected.

MCKO: Master Clock Output Enable
0: "L" Output (default)
1: 256fs Output

M/S: Select Master/ Slave Mode
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPOUTE	0	DACS	DACA	MGAIN3	PMMP	MGAIN2	MGAIN0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

MGAIN3-2: MIC-amp Gain control (Table 20)
MGAIN1 bit is located at D5 bit of 03H. Default: "0001" (+20.0dB)

PMMP: MPI pin Power Control
0: Power down (default)
1: Power up
When PMADC bit is "1", PMMP bit is enabled.

DACA: Switch Control from DAC to mono line amp
0: OFF (default)
1: ON
When PMAO bit is "1", DACA bit is enabled. When PMAO bit is "0", the AOUT pin goes VSS1.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

SPOUTE: Speaker output signal Enable
0: Disable (default)
1: Enable
When SPOUTE bit is "0", the SPP and SPN pins output VSS3.
When SPOUTE bit is "1", the SPP and SPN pins output signal.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	PFSDO	AOPS	MGAIN1	0	SPKG	0	PFDAC	ADCPF
	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W
	Default	1	0	0	0	0	0	0	1

ADCPF: Select of Input signal to Programmable Filter/ALC.
0: SDTI
1: Output of ADC (default)

PFDAC: Select of Input signal to DAC.
0: SDTI (default)
1: Output of Programmable Filter/ALC

SPKG: Select Speaker-Amp Output Gain
0: 0dB (default)
1: +2dB

MGAIN1: Mic-Amplifier Gain Control (Table 20)
MGAIN3-2 and MGAIN0 bits are D3, D2 and D0 of 02H. Default: "0001" (+20.0dB)

AOPS: Mono Line Output Power-Save Mode
0: Normal Operation (default)
1: Power-Save Mode
Power-save mode is enable at AOPS bit = "1". POP noise at power-up/down can be reduced by changing at PMAO bit = "1". (Figure 42)

PFSDO: Select of signal from SDTO
0: Output of ADC (1st - HPF)
1: Output of Programmable Filter/ALC (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO1	BCKO0	DIF1	DIF0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 16)
Default: "10" (MSB justified)

BCKO1-0: Select BICK output frequency at Master Mode (Table 9)
Default: "00" (16fs)

PLL3-0: Select input frequency at PLL mode (Table 4)
Default: "0000" (FCK pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	ADRST	FCKO	FS3	MSBS	BCKP	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Setting of Sampling Frequency (Table 5 and Table 6) and MCKI Frequency (Table 11)
These bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.
Default: "0000"

BCKP, MSBS: "00" (default) (Table 17)

FCKO: Select FCK output frequency at Master Mode (Table 10)
Default: "0"

ADRST: Initialization cycle setting of ADC
0: 1059/fs (default)
1: 291/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	0	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

WTM2-0: ALC1 Recovery Waiting Period (Table 28)
A period of recovery operation when any limiter operation does not occur during the ALC1 operation.
Default is "000".

ZTM1-0: ALC1, ALC2, IVOL and OVOL Zero crossing timeout Period (Table 27)
The gain is changed by the manual volume controlling (ALC off) or the recovery operation (ALC on) only at Zero crossing or timeout. The default value is "00".

RFST1-0 : ALC First recovery Speed (Table 32)
Default: "00" (4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

LMTH1-0: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level (Table 25)
LMTH1 bit is located at D6 bit of 0BH. Default: "01"

RGAIN1-0: ALC Recovery GAIN Step (Table 29)
RGAIN1 bit is located at D7 bit of 0BH. Default: "00"

LMAT1-0: ALC Limiter ATT Step (Table 26)
Default: "00"

ZELMN: Zero crossing detection enable at ALC Limiter operation
0: Enable (default)
1: Disable

ALC1: ALC of recoding path Enable
0: Disable (default)
1: Enable

ALC2: ALC2 of playback path Enable
0: Disable (default)
1: Enable

LFST: Limiter function of ALC when the output was bigger than Fs.
0: The volume value is changed at zero crossing or timeout. (default)
1: When output of ALC is bigger than FS, VOL value is changed instantly.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	0	0	0	1	0	1

IREF7-0: Reference value at ALC Recovery operation for recoding. (0.375dB step, 242 Level) (Table 30)
Default: "C5H" (+19.5dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Input Digital Volume Control	IVOL7	IVOL6	IVOL5	IVOL4	IVOL3	IVOL2	IVOL1	IVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

IVOL7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 22)
Default: "91H" (0.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Digital Volume Control	OVOL7	OVOL6	OVOL5	OVOL4	OVOL3	OVOL2	OVOL1	OVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVOL7-0: Output Digital Volume; 0.375dB step, 242 Level (Table 23)
Default: "91H" (0.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

OREF5-0: Reference value at ALC Recovery operation for playback. 1.5dB step, 60 Level (Table 31)
Default: "28H" (+6.0dB)

LMTH1-0: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level
Default: "01" (-4.1dBFS > ALC Output ≥ -6.0dBFS)

RGAIN1-0: ALC Recovery GAIN Step (Table 29)
RGAIN1 bit is located at D1 bit of 07H. Default: "00"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Input Digital Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: The current volume of ALC; 0.375dB step, 242 Level, Read only (Table 33)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Mode Control 3	DATT1	DATT0	SMUTE	MDIF	1	0	1	READ
R/W		R/W	R/W	R/W	R/W	R	R	R	R/W
Default		0	0	0	0	1	0	1	0

READ: Read function Enable
0: Disable (default)
1: Enable

MDIF: Single-ended / Full-differential Input Select
0: Single-ended input (MIC pin or LIN pin: Default)
1: Full-differential input (MICP and MICN pins)

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

DATT1-0: Output Digital Volume2; 6dB step, 4 Level (Table 24)
Default: "00H" (0.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Thermal Shutdown	THDET	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

THDET: Thermal Shutdown Detection
0: Normal Operation (default)
1: Thermal Shutdown

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Signal Select 4	0	LOVL	0	0	0	0	LIN	0
R/W		R	R/W	R	R	R	R	R/W	R
Default		0	0	0	0	0	0	0	0

LIN: Select Input data of ADC
0: MIC pin (default)
1: LIN pin

LOVL: Lineout Gain Setting
0: 0dB(default)
1: +2dB

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Digital Filter Select 1	0	0	LPF	HPF	0	0	0	1
R/W		R	R	R/W	R/W	R	R	R	R
Default		0	0	0	1	0	0	0	1

HPF: HPF Enable in Filter block.

0: Disable

1: Enable (default)

When HPF bit is "0", HPF block is bypassed (0dB).

When HPF bit is "1", F1A13-0, F1B13-0 bits are enabled.

LPF: LPF Coefficient Setting Enable

0: Disable (default)

1: Enable

When LPF bit is "0", LPF block is bypassed (0dB).

When LPF bit is "1", F2A13-0, F2B13-0 bits are enabled.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		W	W	W	W	W	W	W	W
Default		F1A13-0 bits = 0x1F16, F1B13-0 bits = 0x1E2B							

F1A13-0, F1B13-0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)

Default: F1A13-0 bits = 0x1F16, F1B13-0 bits = 0x1E2B

fc = 75Hz@fs = 8kHz, 150Hz@fs = 16kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
R/W		R/W	R	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPFR1-0: BEEP Signal Output Frequency Setting (Table 38 ~ Table 40)

Default: "00"

BPCNT: BEEP Signal Output Mode Setting

0: Once Output Mode (default)

1: Continuous Mode

In continuous mode, the BEEP signal is output while BPCNT bit is "1".

In once output mode, the BEEP signal is output by only the frequency set with BPTM6-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPON7-0: Setting ON-time of BEEP signal output (Table 41)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPOFF7-0: Setting OFF-time of BEEP signal output (Table 42)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
23H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPTM6-0: Setting the number of times that BEEP signal repeats (Table 43)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	BEEP VOL/Control	BPOUT	0	0	0	0	BPLVL2	BPLVL1	BPLVL0
R/W		R/W	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL2-0: Setting Output Level of BEEP signal (Table 44)
Default: "0H" (0dB)

BPOUT: BEEP Signal Control
0: OFF (default)
1: ON
At the time of BPCNT = "0", when BPOUT bit is "1", the beep signal starts outputting. The Beep signal stops after the number of times that was set in BPTM6-0 bit, and BPOUT bit is set to "0" automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is “1”, E1A15-0, E1B15-0, E1C15-0 bits are enabled. When EQ1 bit is “0”, EQ block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is “1”, E2A15-0, E2B15-0, E2C15-0 bits are enabled. When EQ2 bit is “0”, EQ block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is “1”, E3A15-0, E3B15-0, E3C15-0 bits are enabled. When EQ3bit is “0”, EQ block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is “1”, E4A15-0, E4B15-0, E4C15-0 bits are enabled. When EQ4 bit is “0”, EQ block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is “1”, E5A15-0, E5B15-0, E5C15-0 bits are enabled. When EQ5 bit is “0”, EQ block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

SYSTEM DESIGN

Figure 57 and Figure 59 show the system connection diagram. The evaluation board [AKD4634] demonstrates the optimum layout, power supply arrangements and measurement results.

AK4634EN/VN < MIC Single-end Input >

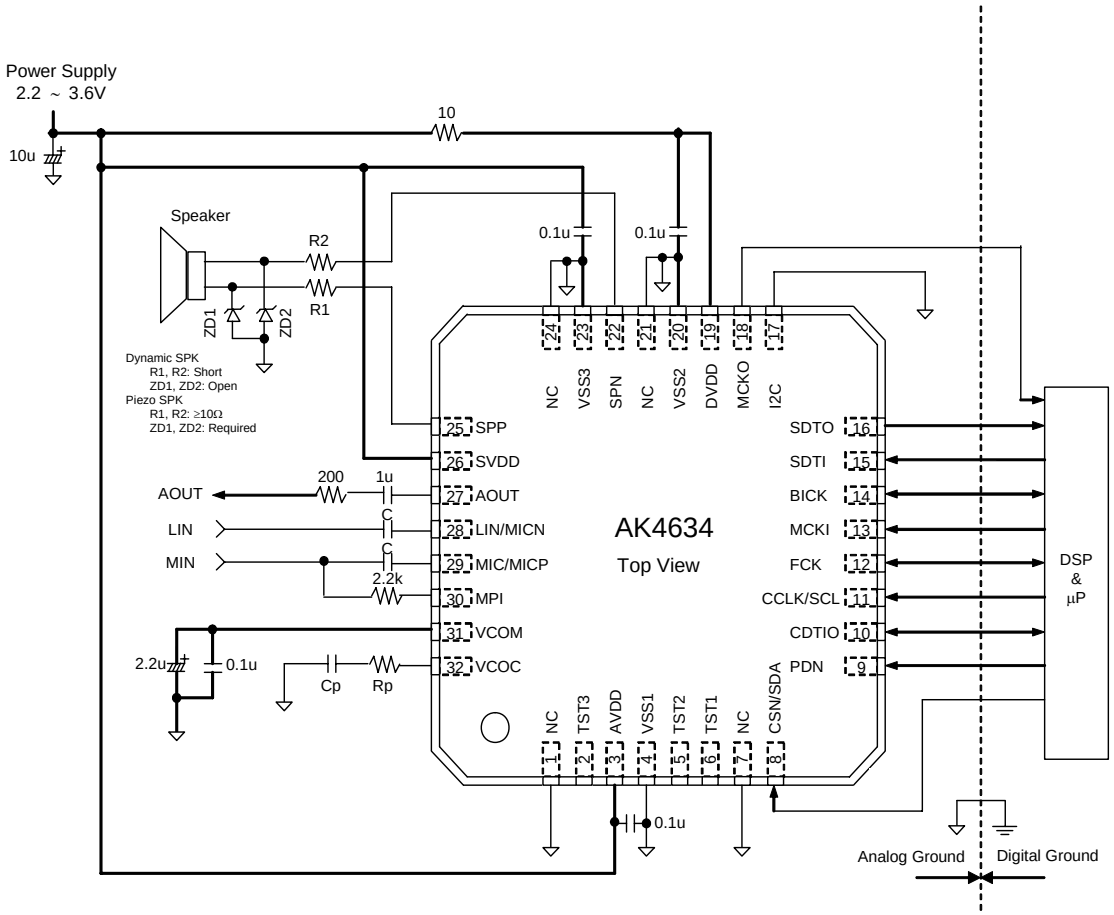


Figure 57. Typical Connection Diagram (3-wire Mode, AK4634EN/VN)

Notes:

- VSS1, VSS2 and VSS3 of the AK4634 must be distributed separately from the ground of external controllers.
- All digital input pins except pull-down pin must not be left floating.
- In EXT mode (PMPLL bit = "0"), Rp and Cp of the VCOC pin can be open.
- In PLL mode (PMPLL bit = "1"), Rp and Cp of the VCOC pin should be connected as shown in Table 4.
- When the AK4634 is used at master mode, FCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up resistor with around 100Ω must be connected to LRCK and BICK pins of the AK4634.
- When AVDD, DVDD and SVDD were distributed, DVDD = 1.6 ~ 3.6 V, SVDD = 2.2 ~ 4.0 V.
- 1st-oder HPF consists of the input impedance of the LIN pin and MIC pin (R = typ 30 kΩ) and the LIN, MIC pin capacitors "C" before MIC-Amp. The cut-off frequency of the HPF(fs) is calculated by the following formula.

$$fc = 1 / (2\pi R C)$$

AK4634ECB < MIC Single-end Input >

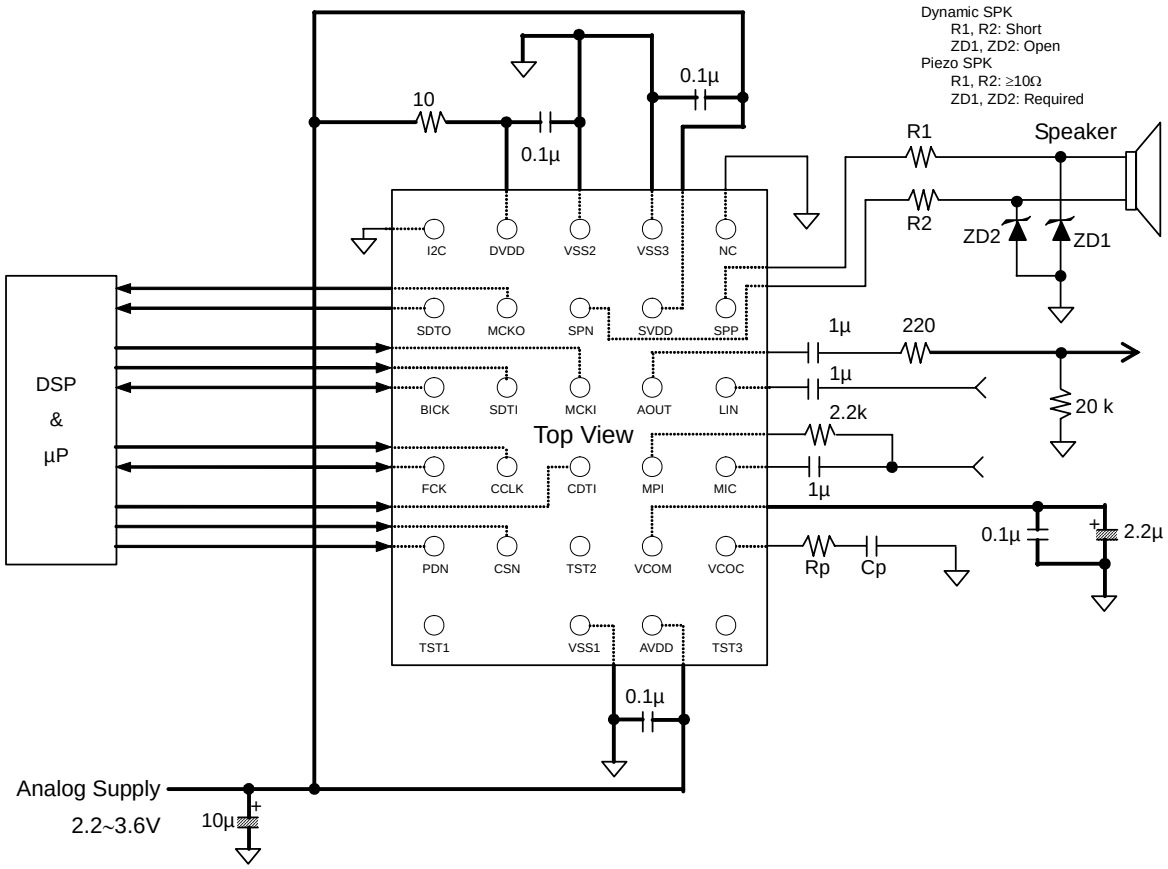


Figure 58. Typical Connection Diagram (3-wire Mode, AK4634ECB)

Notes:

- VSS1, VSS2 and VSS3 of the AK4634 must be distributed separately from the ground of external controllers.
- All digital input pins except pull-down pin must not be left floating.
- In EXT mode (PMPLL bit = "0"), Rp and Cp of the VCOC pin can be open.
- In PLL mode (PMPLL bit = "1"), Rp and Cp of the VCOC pin must be connected as shown in Table 4.
- When the AK4634 is used at master mode, FCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up resistor with around 100Ω must be connected to LRCK and BICK pins of the AK4634.
- When AVDD, DVDD and SVDD were distributed, DVDD = 1.6 ~ 3.6 V, SVDD = 2.2 ~ 4.0 V.
- 1st-oder HPF consists of the input impedance of the LIN pin and MIC pin (R = typ 30 kΩ) and the LIN, MIC pin capacitors "C" before MIC-Amp. The cut-off frequency of the HPF(fs) is calculated by the following formula.

$$fc = 1 / (2\pi R\, C)$$

AK4634EN/VN < MIC differential Input >

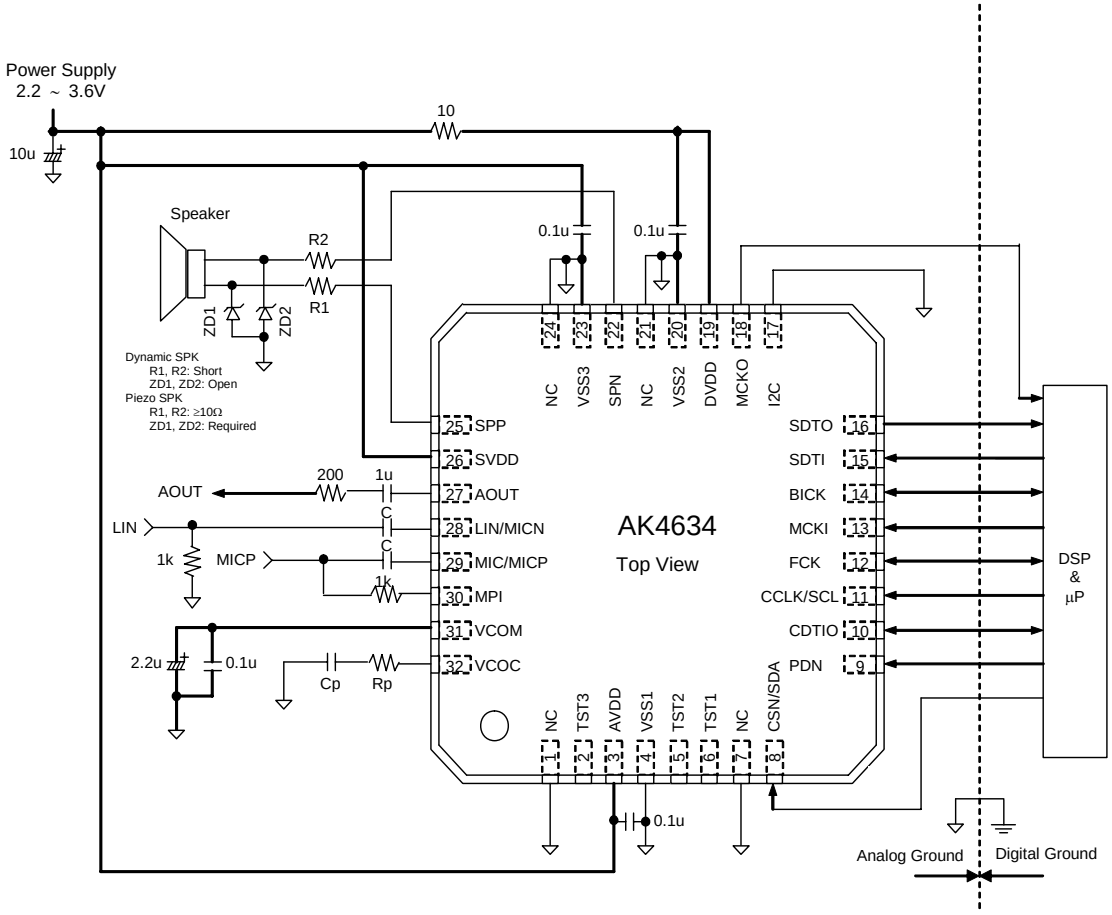


Figure 59. Typical Connection Diagram (3-wire Mode, AK4634EN/VN)

Notes:

- VSS1, VSS2 and VSS3 of the AK4634 must be distributed separately from the ground of external controllers.
- All digital input pins except pull-down pin must not be left floating.
- In EXT mode (PMPLL bit = "0"), Rp and Cp of the VCOC pin can be open.
- In PLL mode (PMPLL bit = "1"), Rp and Cp of the VCOC pin should be connected as shown in Table 4.
- When the AK4634 is used at master mode, FCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up resistor with around 100Ω must be connected to LRCK and BICK pins of the AK4634.
- When AVDD, DVDD and SVDD were distributed, DVDD = 1.6 ~ 3.6 V, SVDD = 2.2 ~ 4.0 V.
- 1st-oder HPF consists of the input impedance of the MICP pin and MICN pin (R = typ 30 kΩ) and the MICP, MICN pin capacitors "C" before MIC-Amp. The cut-off frequency of the HPF(fs) is calculated by the following formula.

$$fc = 1 / (2\pi R\, C)$$

AK4634ECB < MIC differential Input >

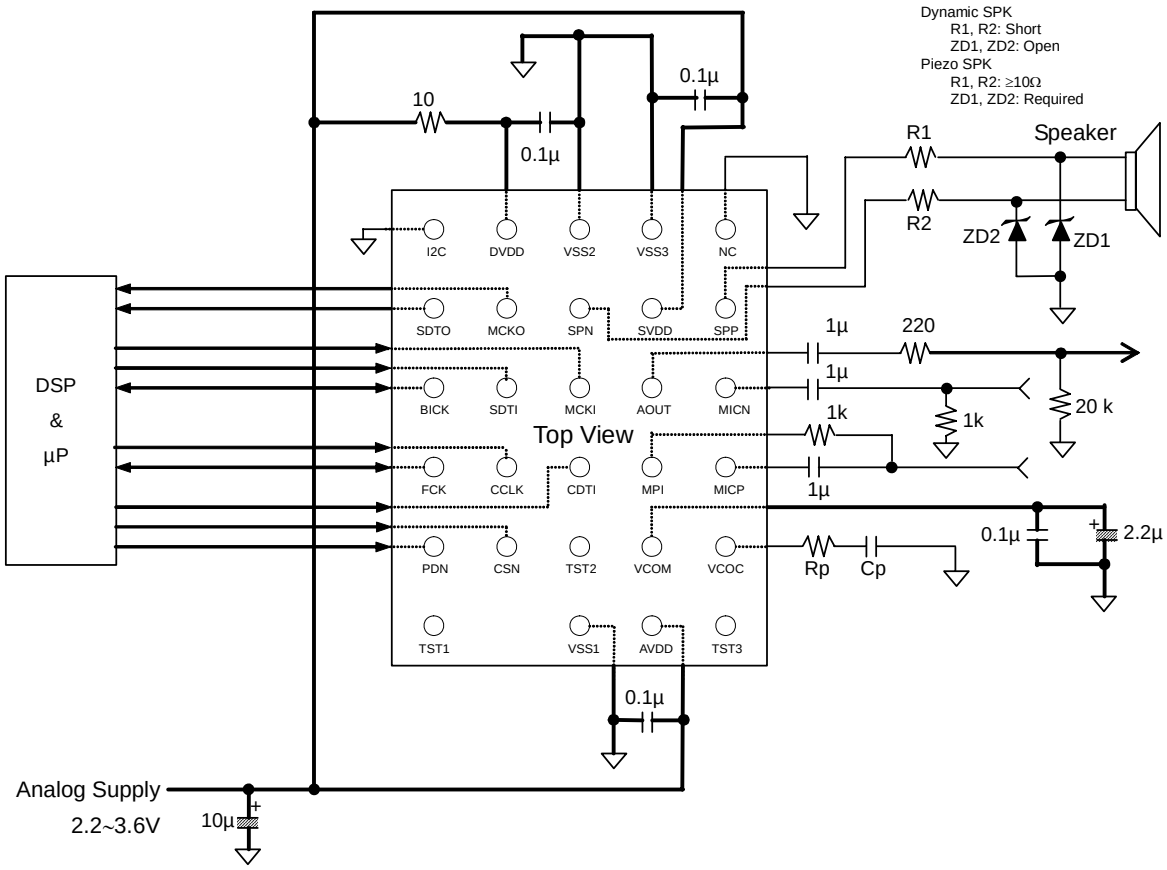


Figure 60. Typical Connection Diagram (3-wire Mode, AK4634ECB)

Notes:

- VSS1, VSS2 and VSS3 of the AK4634 must be distributed separately from the ground of external controllers.
- All digital input pins except pull-down pin must not be left floating.
- In EXT mode (PMPLL bit = "0"), Rp and Cp of the VCOC pin can be open.
- In PLL mode (PMPLL bit = "1"), Rp and Cp of the VCOC pin must be connected as shown in Table 4.
- When the AK4634 is used at master mode, FCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up resistor with around 100Ω must be connected to LRCK and BICK pins of the AK4634.
- When AVDD, DVDD and SVDD were distributed, DVDD = 1.6 ~ 3.6 V, SVDD = 2.2 ~ 4.0 V.
- 1st-oder HPF consists of the input impedance of the MICP pin and MICN pin (R = typ 30 kΩ) and the MICP, MICN pin capacitors "C" before MIC-Amp. The cut-off frequency of the HPF(fs) is calculated by the following formula.

$$fc = 1 / (2\pi R\,C)$$

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	FCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	BICK pin	16fs	10k	4.7n	2ms	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	20ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	20ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	20ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	20ms	
Others	Others				N/A					

Note 31. the tolerance of R is ±5%, the tolerance of C is ±30%

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

1. Grounding and Power Supply Decoupling

The AK4634 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and SVDD are usually supplied from the system's analog supply. If AVDD, DVDD and SVDD are supplied separately, the correct power up sequence should be observeVSS21, VSS2 and VSS3 of the AK4634 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4634 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4634.

3. Analog Inputs

The Mic and Line inputs supports single-ended and differential. The input signal range scales with nominally at 0.06 x AVDD Vpp@MIC-amp gain 20dB for the Mic input and 0.6 x AVDD Vpp@MIC-amp gain 20dB for the Beep input, centered around the internal common voltage (approx. 0.45 x AVDD). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is fc = 1 (/2πRC). The AK4634 can accept input voltages from VSS1 to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The theoretical figure for 0000H (@16bit) is VCOM voltage. Mono Line Output from the AOUT pin is centered at 0.45 x AVDD (typ).

CONTROL SEQUENCE

■ Clock Set up

When ADC, DAC, SPK-amp and Programmable Filter are used, the clocks must be supplied.

1. PLL Master Mode

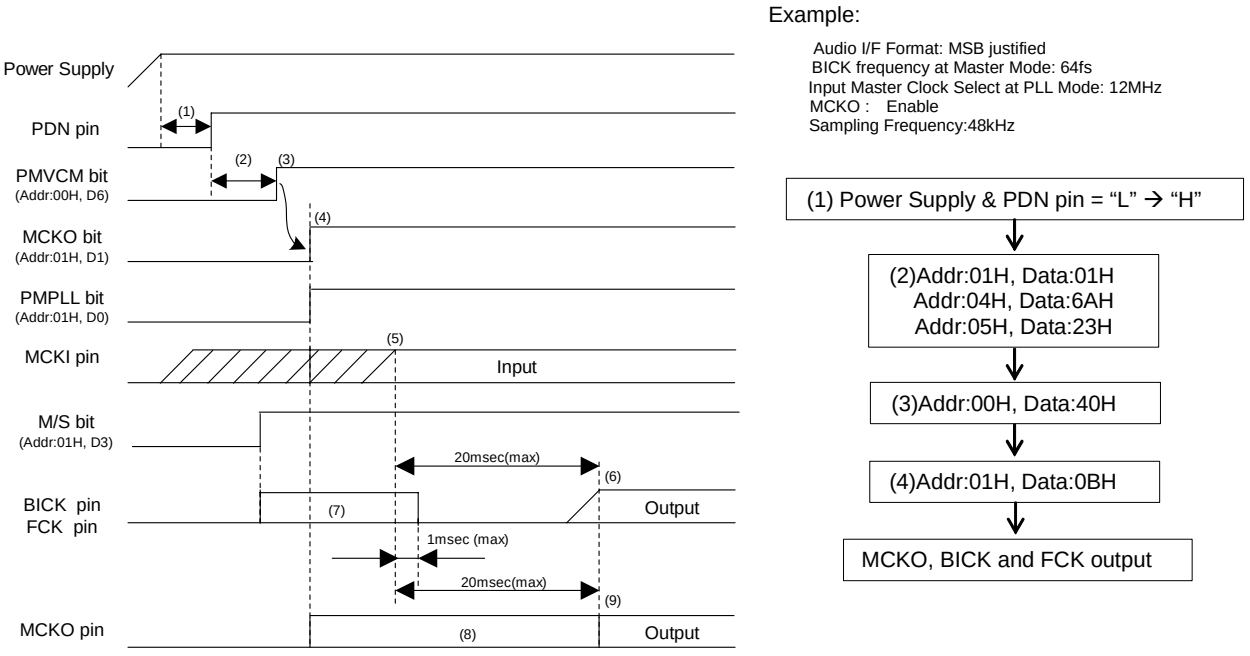


Figure 61. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4634.

(1) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits must be set during this period.

(2) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.

(2) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(3) PLL lock time is 20ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.

(4) The AK4634 starts to output the FCK and BICK clocks after the PLL becomes stable and the normal operation starts.

(5) The invalid frequencies are output from FCK and BICK pins during this period.

(6) The invalid frequency is output from the MCKO pin during this period.

(7) The normal clock is output from the MCKO pin after the PLL is locked.

2. When the external clock (FCK or BICK pin) is used in PLL Slave mode.

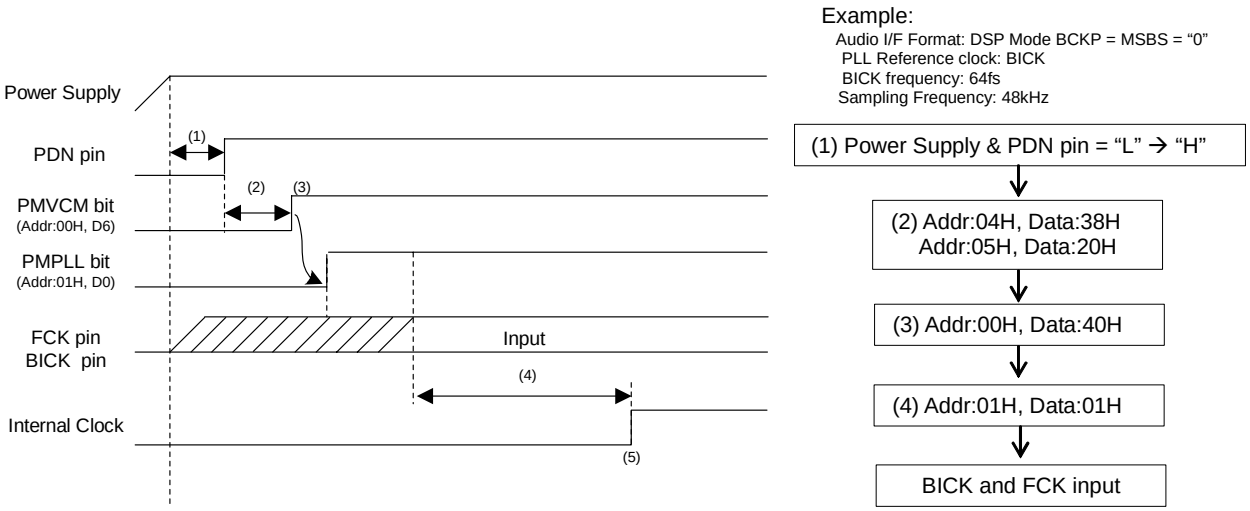


Figure 62. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4634.

(2) DIF1-0, FS3-0, PLL3-0, MSBS and BCKP bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clocks (FCK or BICK pin) are supplied. PLL lock time is 160ms(max) when PLL reference clock is FCK, and PLL lock time is 2ms(max) when PLL reference clock is BICK.

(5) Normal operation starts after the PLL is locked.

3. When the external clock (MCKI pin) is used in PLL Slave mode.

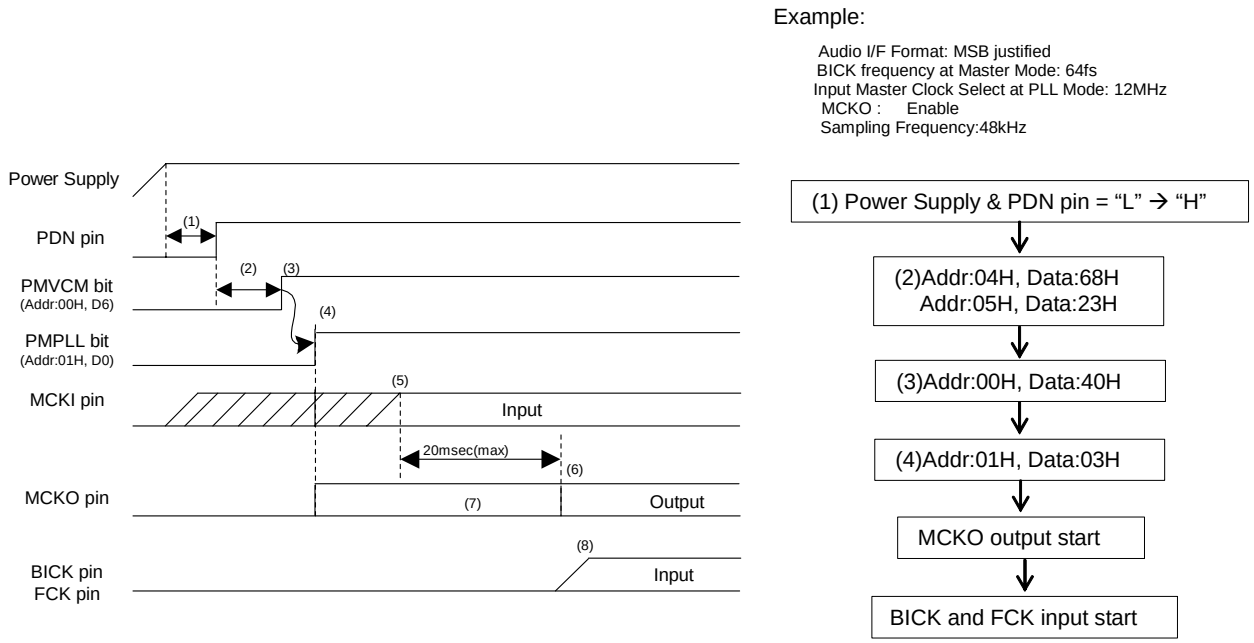


Figure 63. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4634.

(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL Power Up: PMPLL bit "0" → "1"

(5) PLL lock time is 20ms(max) after the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.

(6) Normal clock is output from the MCKO pin after PLL is locked.

(7) The invalid frequency is output from the MCKO pin during this period.

(8) BICK and FCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

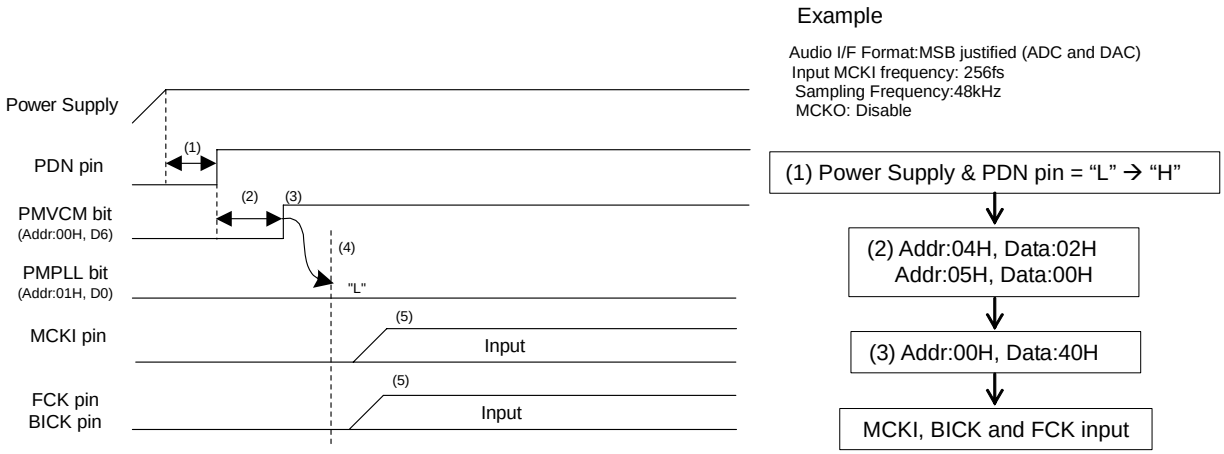


Figure 64. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4634.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Power down PLL: PMPLL bit = "0"

(5) Normal operation starts after the MCKI, FCK and BICK are supplied.

■ MIC Input Recording

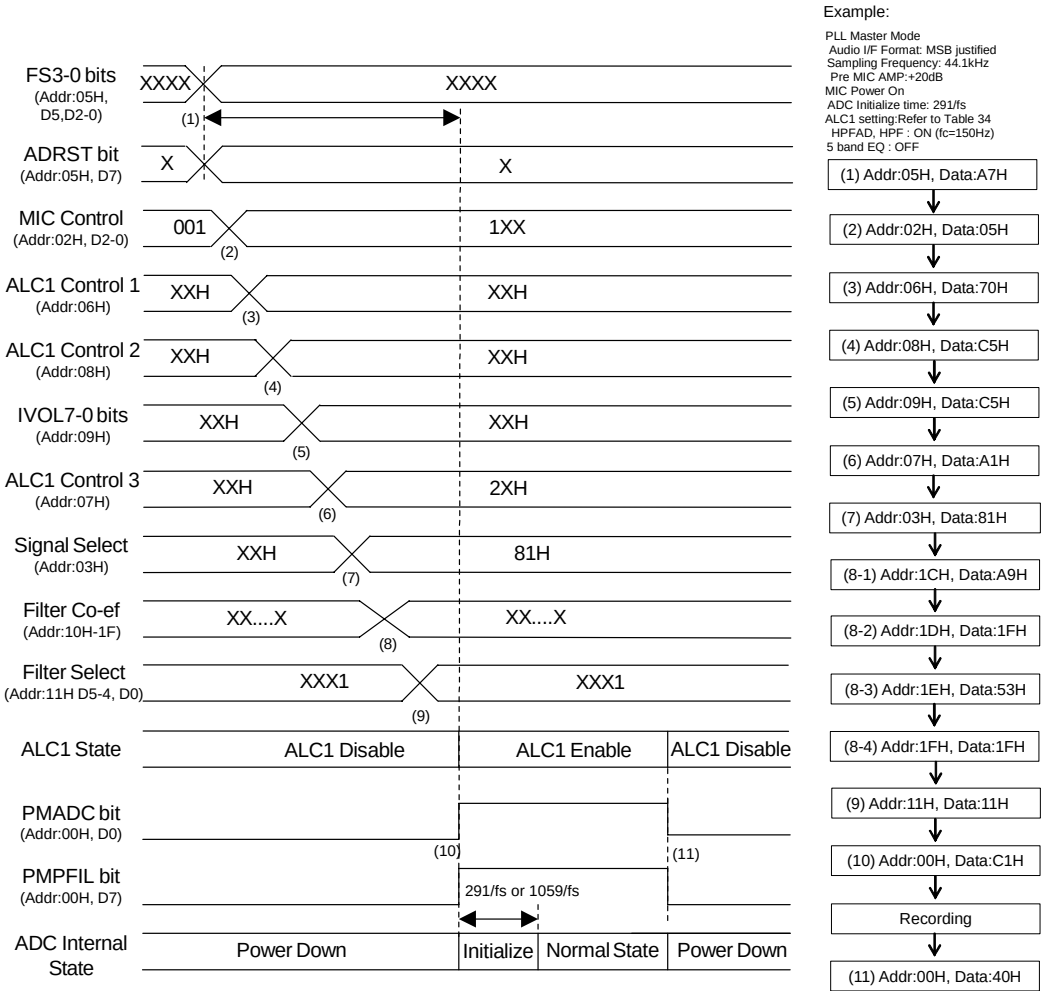


Figure 65. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=44.1kHz. If the parameter of the ALC1 is changed, please refer to the Table 34.

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK4634 is in PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up MIC input (Addr: 02H)
(3) Set up Timer Select for ALC1 (Addr: 06H)
(4) Set up REF value for ALC1 (Addr: 08H)
(5) Set up IVOL value for ALC1 (Addr: 09H)
(6) Set up LMTH0, RGAIN0, LMAT1-0, ZELM and ALC1 bits (Addr: 07H)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1"
(8) Set up Coefficient of the Programmable Filter (HPF/EQ) Addr: 1CH ~ 1FH, 2CH ~ 2FH, 32H ~ 4FH
(9) Switch ON/OFF of the Programmable Filter
HPFAD bit must be "1".
(10) Power-up of the ADC and Programmable Filter: PMPFIL bit = PMADC bit = "0" → "1"
The initialization cycle of the ADC is 1059/fs=24ms@fs=44.1kHz when ADRST bit = "0",
291/fs=18ms@fs=16kHz when ADRST bit= "1". ALC starts operating at the value set by IVOL (5).
(11) Power-down of the ADC and Programmable Filter: PMPFIL bit = PMADC bit = "1" → "0"

■ Mono Lineout

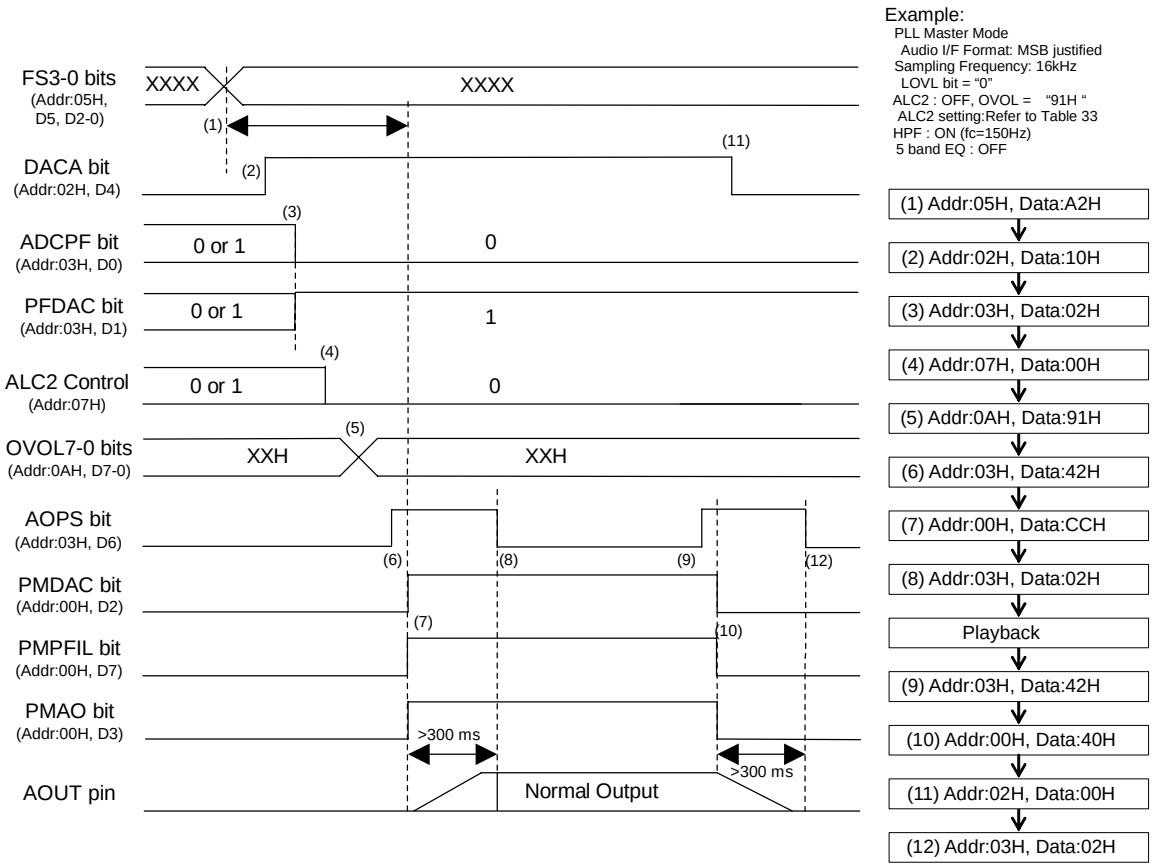


Figure 66. Mono Lineout Sequence

<Example>
In case of using digital volume in manual mode

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4634 is PLL mode, DAC, Programmable Filter and Mono Line Amp should be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the path of "DACA → Mono Line Amp"
DACA bit: "0" → "1"
(3) Set up the path: ADCPF bit = "0", PFDAC bit = "1"
(4) ALC2 Disable: ALC2 bit = "0"
(5) Set up the digital volume (Addr: 0AH)
(6) AOUT power save mode: AOPS bit: "0" → "1"
(7) Power-up of DAC, Programmable Filter and Mono Line Amp:
PMDAC bit = PMPFIL bit = PMAO bit = "0" → "1"
AOUT pin goes to "H". It takes 300ms (max) when C = 1μF
(8) Exit power save mode of AOUT: AOPS bit = "1" → "0"
Set up AOPS bit after AOUT became "H", then the AOUT pin starts outputting data.
(9) Enter power save mode of AOUT: AOPS bit= "0" → "1"
(10) Power –down the DAC, Programmable Filter and Mono Line Amp:
PMDAC bit = PMPFIL bit = PMAO bit = "1" → "0"
The AOUT pin starts going to "L". It takes 300ms(max) when C = 1μF.
(11) Disable the path of "DAC → Mono Line Amp": DACA bit= "1" → "0"
(12) Exit power save mode of AOUT: AOPS bit="1" → "0"
Set up AOPS bit after AOUT became "L".

■ Speaker-amp Output

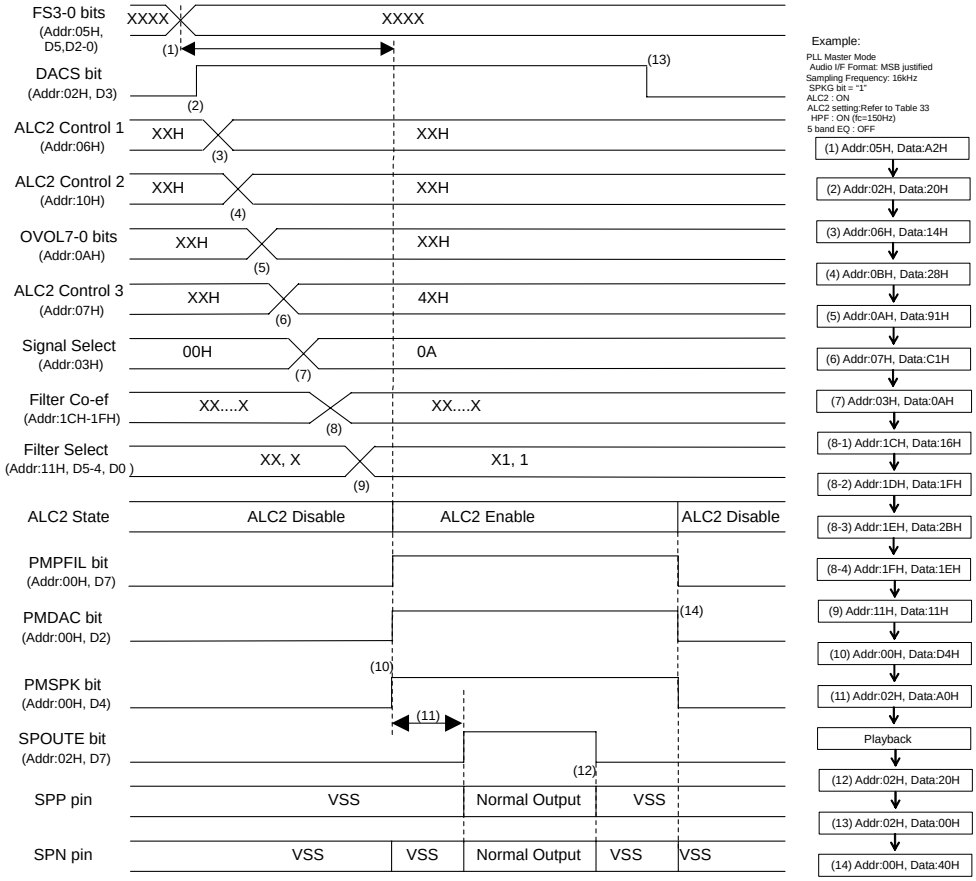


Figure 67. Speaker-Amp Output Sequence

<Example>

In case of fs=16kHz. Refer to the Table 35 for changing ALC2 parameter.

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4634 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of "DAC → SPK-Amp": DACS bit = "0" → "1"
(3) Set up Timer Select for ALC2 (Addr: 06H)
(4) Set up REF value for ALC2 (Addr: 08H)
(5) Set up OVOL value, RGAIN1 and LMTH1 for ALC2 (Addr: 10H)
(6) Set up LMTH0, RGAIN0, LMAT1-0, ZELM and ALC2 bit (Addr: 07H)
(7) Set up the Programmable Filter Path and SPK-Amp Gain:
PFDAC bit = "1", ADCPF bit = "0", SPKG bit = "X"
(8) Set up Coefficient of the Programmable Filter (HPF/EQ) Addr: 1C ~ 1FH, 2CH ~ 2FH, 32H ~ 4FH
(9) Switch ON/OFF of the Programmable Filter
It is recommended that HPF bit ="1".
(10) Power-up of the DAC, SPK-Amp and Programmable Filter:
PMDAC bit = PMSPK bit = PMPFIL bit = "0" → "1"
(11) Enable Speaker Output: SPOUTE bit = "0" → "1"
1ms or more time is needed before setting SPOUTE bit = "1"after setting PMSPK bit = "1".
(12) Disable Speaker Output: SPOUTE bit = "1" → "0"
(13) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0".
(14) Power down of the DAC, SPK-Amp and Programmable Filter:
PMDAC bit = PMSPK bit = PMPFIL bit = "1"→ "0"

■ BEEP signal output from Speaker-Amp

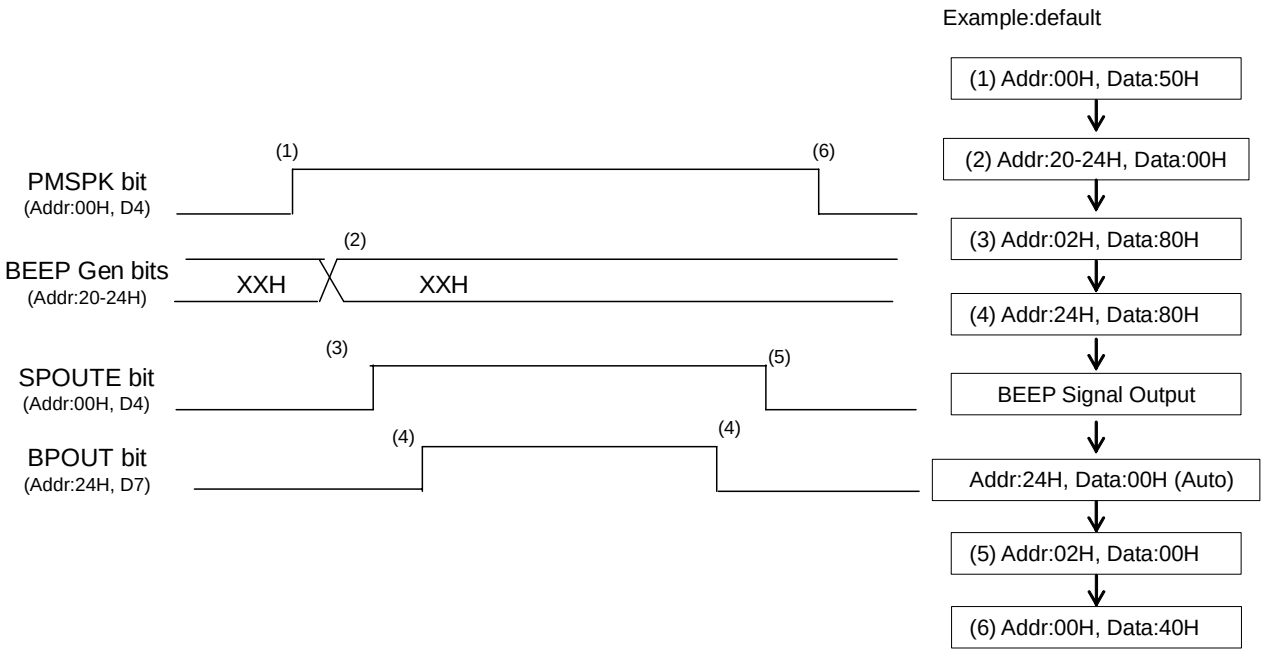


Figure 68. "BEPP Generator → Speaker-Amp" Output Sequence

<Example>
At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Power Up BEEP-Generator and Speaker-Amp: PMSPK bit = "0" → "1"
(2) Set up BEEP Generator (Addr: 20H ~ 24H)(When repeat output time BPCNT bit = "0")
(3) Enable SPK-Amp Output: SPOUTE bit = "0" → "1"
(4) BEEP Output: BPOUT bit= "0" → "1" (after outputting data particular set times, BPOUT bit automatically goes to "0")
(5) Disable Speaker Output: SPOUTE bit bit = "1" → "0"
(6) Power down of the SPK-Amp: PMSPK bit = "1" → "0"

■ Stop of Clock

Master clock can be stopped when ADC, DAC and Programmable Filter are not in operation.

1. PLL Master Mode

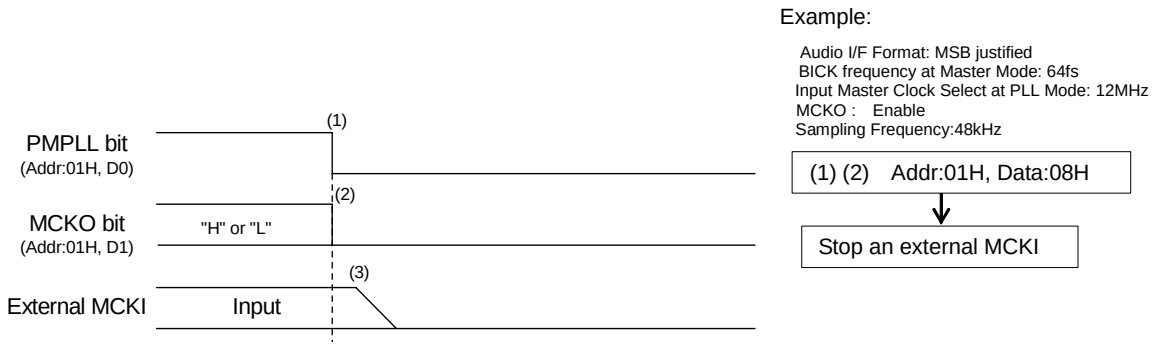


Figure 69. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock

2. PLL Slave Mode (FCK, BICK pin)

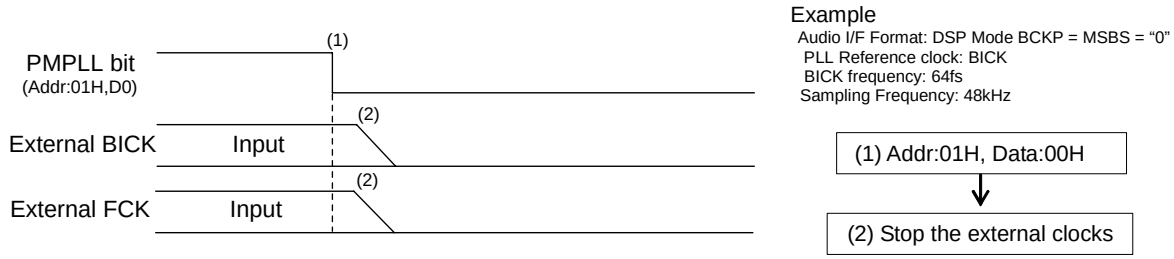


Figure 70. Clock Stopping Sequence (2)

<Example>
(1) Power down of the PLL: PMPLL bit = "1" → "0"
(2) Stop an external master clock

3. PLL Slave Mode (MCKI pin)

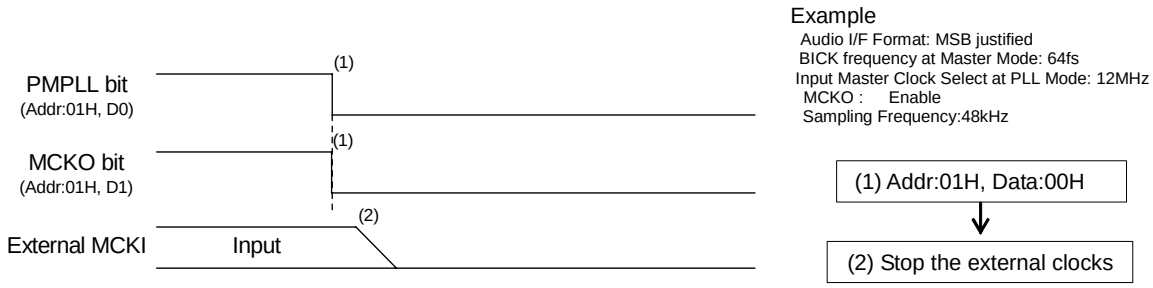


Figure 71. Clock Stopping Sequence (3)

<Example>
(1) Power down of the PLL: PMPLL bit = "1" → "0"
Stop the MCKO output: MCKO bit = "1" → "0"
(2) Stop an external master clock

4. EXT Slave Mode

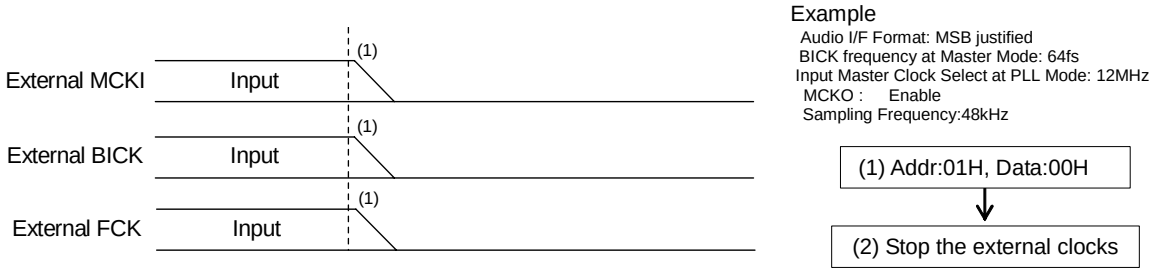


Figure 72. Clock Stopping Sequence (4)

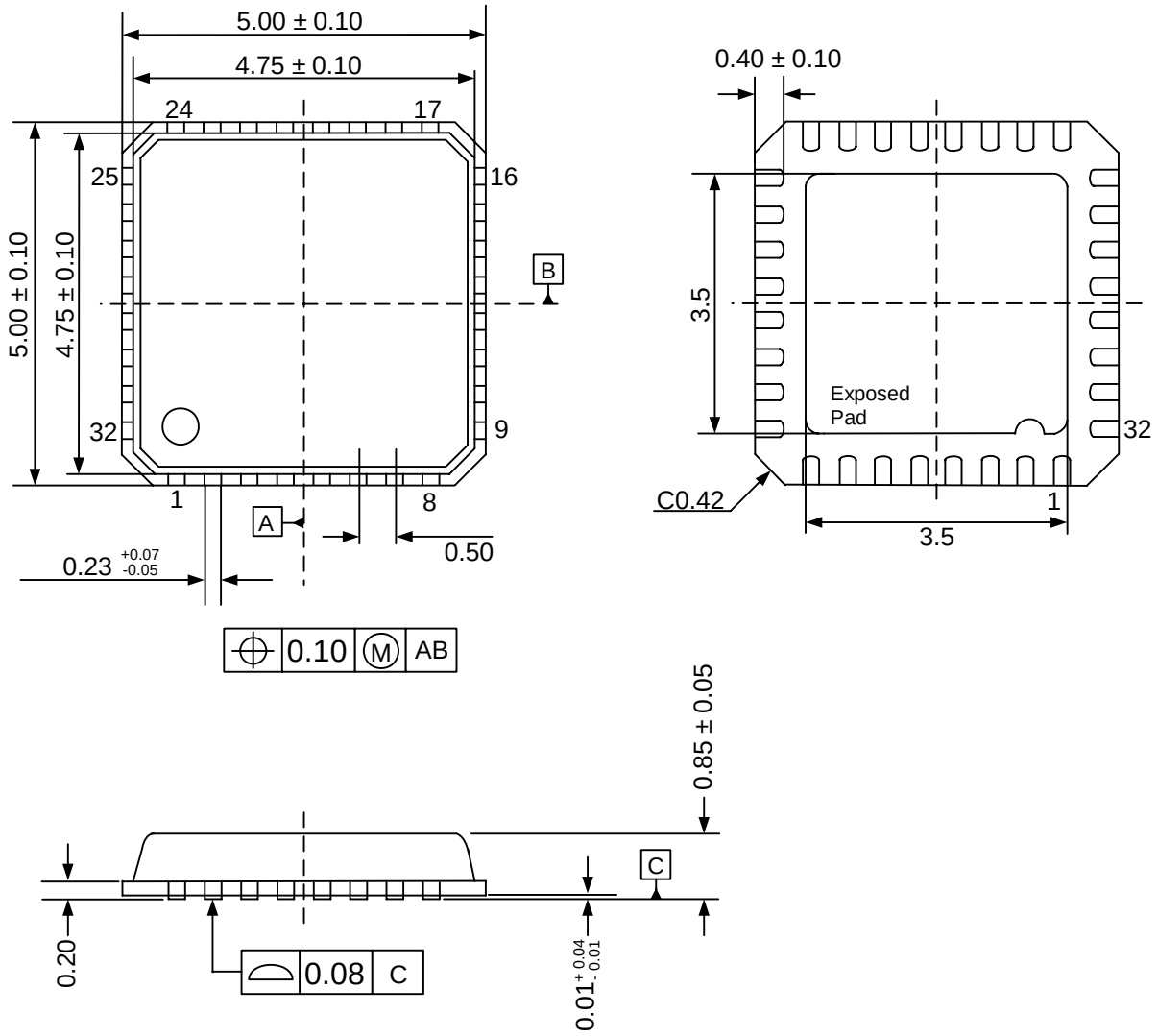
<Example>
(1) Stop an external master clock

■ Power Down

VCOM should be powered-down after the master clock is stopped if clocks are supplied when all blocks except for VCOM are powered-down. The AK4634 is also powered-down by the PDN pin = "L". In this case, the registers are initialized.

PACKAGE (AK4634EN, AK4634VN)

32pin QFN (Unit: mm)



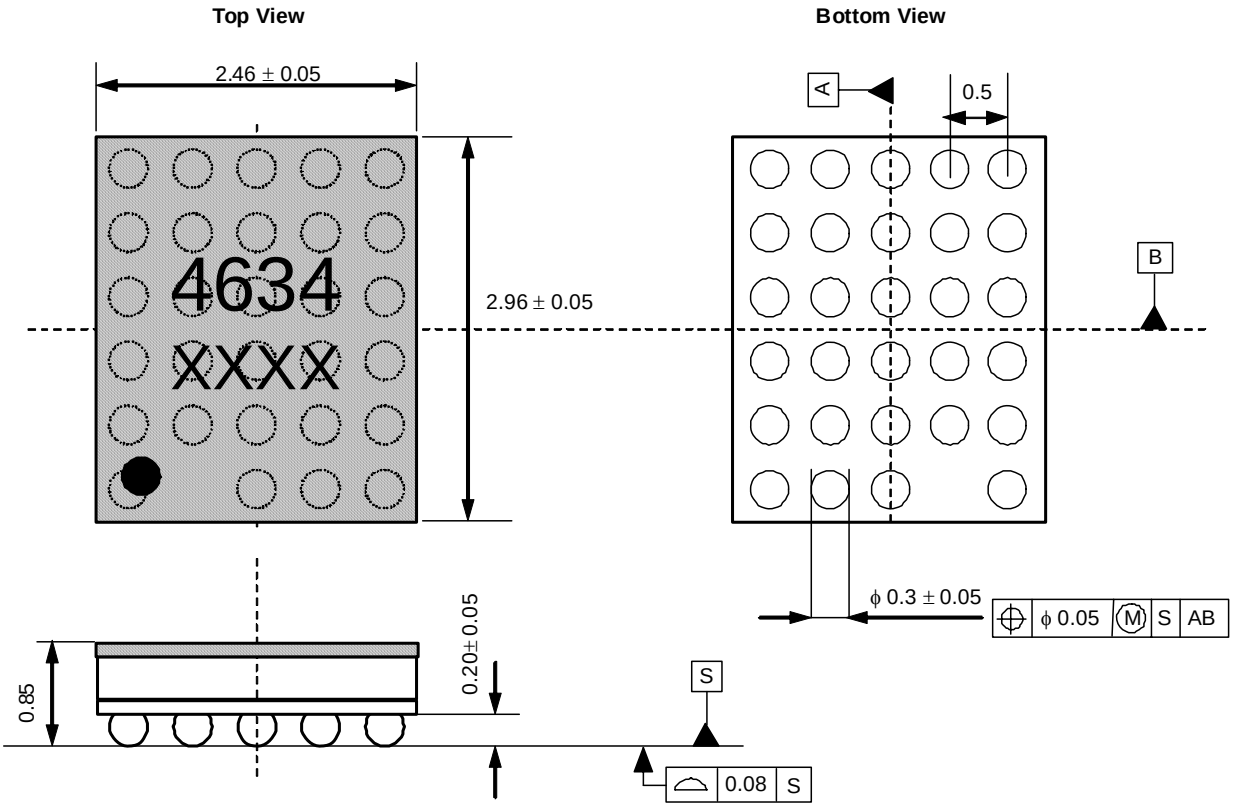
Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ Material & Lead finish

Package molding compound:	Epoxy resin, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

PACKAGE (AK4634ECB)

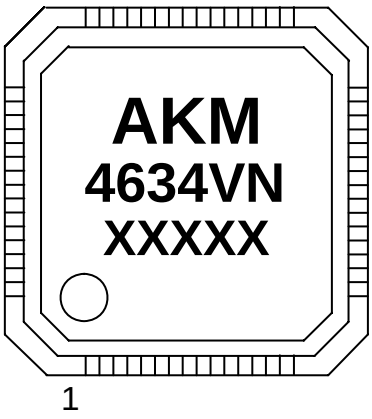
29pin CSP: 2.5mm x 3.0mm



■ Material & Lead finish

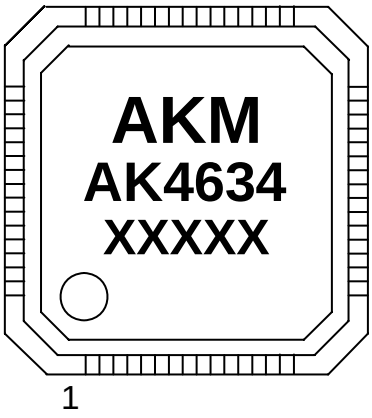
Package material: Epoxy resin, Halogen (bromine and chlorine) free
Solder ball material: SnAgCu

MARKING (AK4634VN)



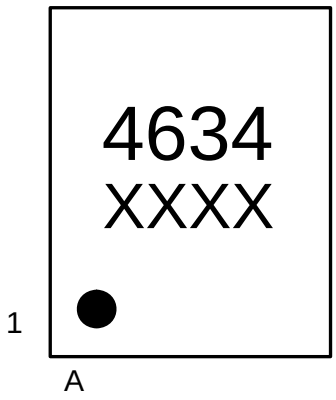
XXXXX: Date code identifier (5 digit)

MARKING (AK4634EN)



XXXXX: Date code identifier (5 digit)

MARKING (AK4634ECB)



XXXX: Date code (4 digit)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/07/09	00	First Edition		
08/10/28	01	Comment Addition		AK4634VN and AK4634ECB were added.