AK4186

Low Power Touch Screen Controller with I²C Interface

GENERAL DESCRIPTION

The AK4186 is a 4-wire/ 5-wire resistive touch screen controller that incorporates 12bit SAR A/D converter. The AK4186 can detect the pressed screen location with two A/D conversions and it can also measure touch pressure. The AK4186 has both an automatic continuous measurement and a measurement data calculation function. The functions that normally require external processing, such as calculating the average screen input value, are processed by the AK4186. In addition, a new sequential mode achieves short coordinate measurement time while greatly reducing the microprocessor overhead. The AK4186 operates off of supply voltage down to 1.6V in order to connect a low voltage microprocessor. The AK4186 is the best fit for cellular phone, DSC, DVC, smart phone and other portable devices.

FEATURES

- **4-wire or 5-wire Touch Screen Interface**
- **I²C Serial Interface**
- **12bit SAR A/D Converter with S/H circuit**
- **Sampling Rate: 22.2kHz**
- **Pen Pressure Measurement (4-wire)**
- **Continuous Read Function**
- **Integrated Internal Osc (Sequence Mode)**
- **Integrated Median Averaging Filter**
- **Low Voltage Operation: VDD = 1.6V ~ 3.6V**
- **PENIRQN Buffer Output**
- **Low Power Consumption: 60µA at 1.8V**
- **Auto Power Down**
- **Package: 12pin CSP (1.7mm x 1.3mm, pitch 0.4mm)**
  16pin QFN (3mm x 3mm, pitch 0.5mm)

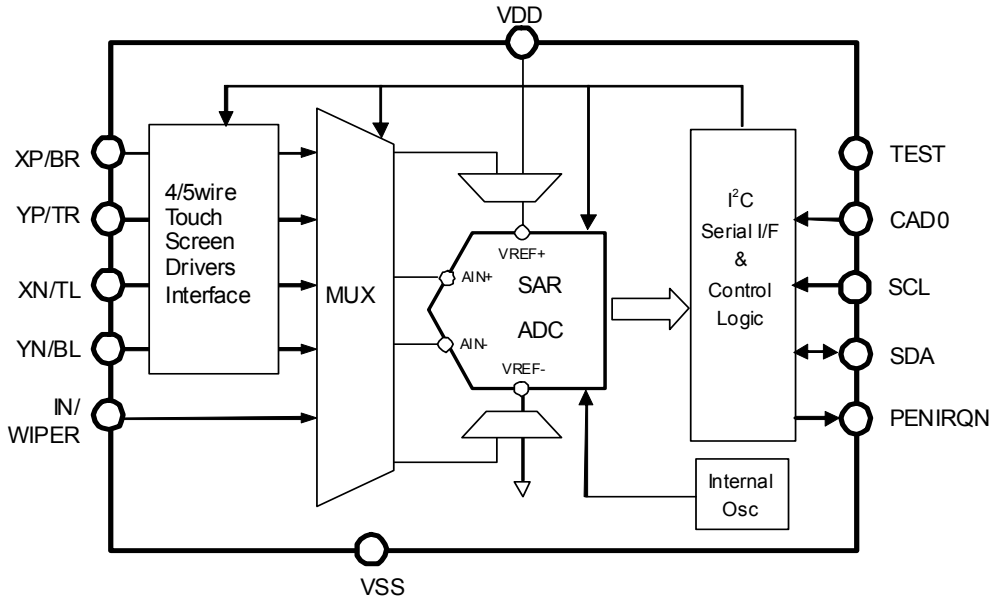


Figure 1. Block Diagram

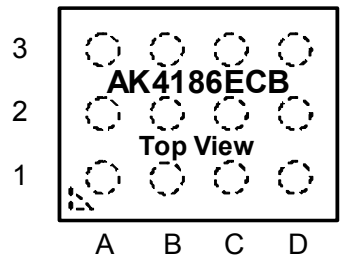
I²C-bus is a trademark of NXP B.V.

■ Ordering Guide

AK4186ECB	–40 ~ +85°C	12pin CSP (1.66mm x 1.26mm, 0.4mm pitch)	Black Type
AK4186EN	–40 ~ +85°C	16pin QFN (3mm x 3mm, 0.5mm pitch)	
AKD4186	AK4186ECB Evaluation Board		
AKD4186EN	AK4186EN Evaluation Board		

■ Pin Layout

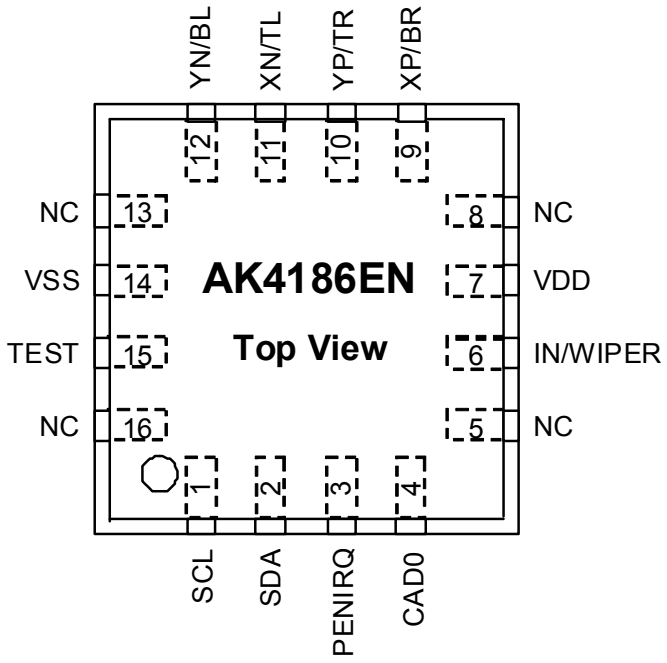
AK4186ECB



3	XP/BR	YP/TR	XN/TL	YN/BL
2	VDD	CAD0	TEST	VSS
1	IN/WIPER	PENIRQN	SDA	SCL
	A	B	C	D

TOP View

AK4186EN



PIN/FUNCTION

Pin No. ECB	Pin No. EN	Pin Name	I/O	Function
D1	1	SCL	I	I^2C Serial Clock Input
C1	2	SDA	I/O	I^2C Serial Data Input/ Output
B1	3	PENIRQN	O	Pen Interrupt Output (CMOS output) The PENIRQN pin is "L" when touch-screen press is detected. This pin is always "L" irrespective of touch-screen press when pen interrupt is not enabled.
B2	4	CAD0	I	I^2C Slave Address bit 0
-	5	NC	-	No Connection. No internal bonding. This pin must be connected to VSS.
A1	6	IN	I	Auxiliary Analog Input (4-wire, PANEL bit = "0")
		WIPER	I	Top Touch Panel Input (5-wire, PANEL bit = "1")
A2	7	VDD	-	Power Supply and External Reference Input: 1.6V ~ 3.6V
-	8	NC	-	No Connection. No internal bonding. This pin must be connected to VSS.
A3	9	XP	I/O	Touch Panel X+ Input (4-wire, PANEL bit = "0")
		BR	I/O	Touch Panel Bottom Right Input (5-wire, PANEL bit = "1")
B3	10	YP	I/O	Touch Panel Y+ Input (4-wire, PANEL bit = "0")
		TR	I/O	Touch Panel Top Right Input (5-wire, PANEL bit = "1")
C3	11	XN	I/O	Touch Panel X- Input (4-wire, PANEL bit = "0")
		TL	I/O	Touch Panel Top Left Input (5-wire, PANEL bit = "1")
D3	12	YN	I/O	Touch Panel Y- Input (4-wire, PANEL bit = "0")
		BL	I/O	Touch Panel Bottom Left Input (5-wire, PANEL bit = "1")
-	13	NC	-	No Connection. No internal bonding. This pin must be connected to VSS.
D2	14	VSS	-	Ground
C2	15	TEST	I	TEST pin This pin must be connected to VSS.
-	16	NC	-	No Connection. No internal bonding. This pin must be connected to VSS.

Note 1. All digital input pins (CAD0, SCL, SDA) must not be left floating.

■ Handling of Unused Pin

The unused I/O pin must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	IN/WIPER	This pin must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS = 0V (Note 2))

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	4.6	V
Input Current, Any Pins except for supply	IIN	-	±10	mA
Touch Panel Drive Current	IOUTDRV	-	50	mA
Input Voltage (Note 3)	VIN	–0.3	VDD+0.3 or 4.6	V
Ambient Temperature (power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground.
Note 3. XP/BR, XN/TL, YP/TR, YN/TL, IN/WIPER, CAD0, SCL and SDA pins. Max is smaller value between (VDD+0.3)V and 4.6V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS = 0V (Note 2))

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	1.6	1.8	3.6	V

Note 2. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = -40°C to 85°C, VDD = 1.8V, I²C bus SCL=400kHz)

Parameter		min	typ	max	Units
A/D Converter					
Resolution		-	12	-	Bits
No Missing Codes		11	12	-	Bits
Integral Nonlinearity (INL) Error		-	-	±2	LSB
Differential Nonlinearity (DNL) Error		-2	±1	+3	LSB
Offset Error	AK4186ECB	-	-	±6	LSB
	AK4186EN	-4	-	+8	LSB
Gain Error	AK4186ECB	-	-	±4	LSB
	AK4186EN	-4.5	-	+3.5	LSB
Throughput Rate		-	-	22.2	kHz
Touch Panel Drivers Switch On-Resistance					
XP, YP		-	6	-	Ω
XN, YN		-	6	-	Ω
PENIRQ Pull Up Resistor R_{IRQ}		-	50	-	kΩ
Auxiliary IN Input					
Input Voltage Range		0	-	VDD	V
Power Supply Current					
Normal Mode (Single mode, PD0 bit = "0")	VDD=1.8V	-	60	-	μA
(Note 4)	VDD=3.6V	-	-	220	μA
Normal Mode (Sequence mode, 10kHz equal rate) (Note 5)		-	25	-	μA
Full Power Down (SDA = SCL = "H")		-	0	3	μA

Note 4. Continuous ADC data read (fs = 22.2kHz). Expect for Power Consumption of Touch Panel driver.

Note 5. COUNT bit = "1", INTERVAL2-0 bits = 000. Write command cycle = 1kHz. Expect for Power Consumption of Touch Panel driver.

DC CHARACTERISTTICS (Logic I/O)

(Ta=-40°C to 85°C, VDD =1.6V to 3.6V)

Parameter	Symbol	min	typ	max	Units
"H" level input voltage	VIH	0.8xVDD	-	-	V
"L" level input voltage	VIL	-	-	0.2xVDD	V
Input Leakage Current	IILK	-10	-	10	μA
"H" level output voltage (PENIRQN pin @ Iout = -250μA)	VOH	VDD-0.3	-	-	V
"L" level output voltage (PENIRQN pin @ Iout = 250μA) (SDA pin @ Iout = 3mA)	VOL	-	-	0.3	V
Tri-state Leakage Current (Note 6)	IOLK				
All pins expect for XP, YP, XN, YN pins		-10		10	μA
XP, YP, XN, YN pins		-10		10	μA

Note 6. Expect for TEST pin. TEST pin has internal pull-down device, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=-40°C to 85°C, VDD=1.6V to 3.6V)

Parameter	Symbol	min	typ	max	Units
Internal OSCILATOR					
Clock Frequency	f_{OSC}	2.5	3.6	5.1	MHz
Touch Panel (A/D Converter)					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 7)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

Note 7: Data must be held for sufficient time to bridge the 300ns transition time of SCL.

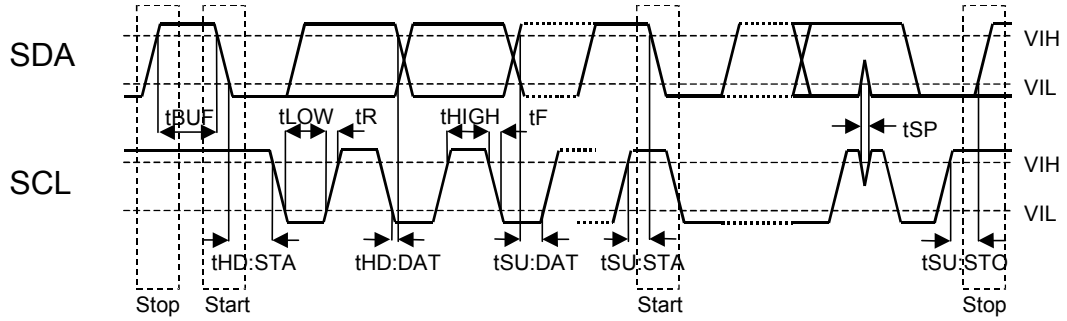


Figure 2. Timing Diagram

OPERATION OVERVIEW

■ Function Overview

The AK4186 consists of the following blocks:

- 1.6V Successive Approximation Resister (SAR) A/D converter
- 4-wire or 5-wire resistive touch screen controller interface
- Single or Continuous A/D conversion
- Internal Clock for SAR A/D Converter
- I^2C^{TM} I/F

■ A/D Converter for Touch Screen

The AK4186 integrates a 12bit successive approximation resistor (SAR) A/D converter for position measurement, temperature, and auxiliary input. The architecture is based on capacitive redistribution algorithm, and an internal capacitor array functions as the sample/hold (S/H) circuit.

The SAR A/D converter output is a straight binary format as shown below:

Input Voltage	Output Code
(ΔVREF-1.5LSB)~ ΔVREF	FFFH
(ΔVREF-2.5LSB) ~ (ΔVREF-1.5LSB)	FFEH
---------	---------
0.5LSB ~ 1.5LSB	001H
0 ~ 0.5LSB	000H

ΔVREF: (VREF+) – (VREF-)

Table 1. Output Code

The f_{OSC} clock of an internal oscillator is used for A/D conversion. The full scale (ΔVREF) of the A/D converter depends on the input mode. Position and pen pressure are measured in differential mode, and then IN is measured in single-ended mode. The AK4186 is controlled by 8bit serial command. A/D conversion result is 12bit data output on the SDA pin.

■ Analog Inputs

The analog input channel is automatically selected in sequential measurement mode. When position detection (X-axis and Y-axis) and pen pressure are selected as analog inputs in differential mode, the full scale (ΔVREF) is the voltage difference between the non-inverting terminal and the inverting terminal of the measured axis (e.g. X-axis measurement: (XP) – (XN)). Analog input to A/D converters (ΔAIN) is the voltage difference between the non-inverting terminal of the non-measured axis and the inverting terminal of the measured axis. At single-ended mode, the full scale of A/D converter (ΔVREF) is the voltage difference between the VDD and the VSS. The analog input of A/D converter (ΔAIN) is the voltage difference between the selected channel (IN) and the VSS.

If the source of analog input is high impedance, longer tracking time is required. Then A/D conversion should be started.

Channel Selection	Status of Driver Switch		ADC input (ΔAIN)		Reference Voltage (ΔVREF)		Ref. Mode
	X-Driver	Y-Driver	AIN+	AIN-	VREF+	VREF-	
AIN Measure	OFF	OFF	IN	GND	VREF	GND	SER
X-axis Measure	ON	OFF	YP	XN	XP	XN	DFR
Y-axis Measure	OFF	ON	XP	YN	YP	YN	DFR
Z1 Measure (Pressure)	XN-ON	YP-ON	XP	XN	YP	XN	DFR
Z2 Measure (Pressure)	XN-ON	YP-ON	YN	XN	YP	XN	DFR

Table 2. Measurement Mode (4-wire)

Channel Selection	Status of Driver Switch		ADC input (ΔAIN)		Reference Voltage (ΔVREF)		Ref. Mode
	TL-Driver	BR-Driver	AIN+	AIN-	VREF+	VREF-	
X-axis Measure	ON	OFF	WIPER	TL	BR	TL	DFR
Y-axis Measure	OFF	ON	WIPER	BR	TL	BR	DFR

Table 3. Measurement Mode (5-wire)

■ Position Detection of Touch Screen

1. The Position Detection for 4-wire Touch Screen

The position on the touch screen is detected by taking the voltage of one axis when the voltage is supplied between the two terminals of another axis. At least two A/D conversions are needed to get the two-dimensions (X/Y-axis) position.

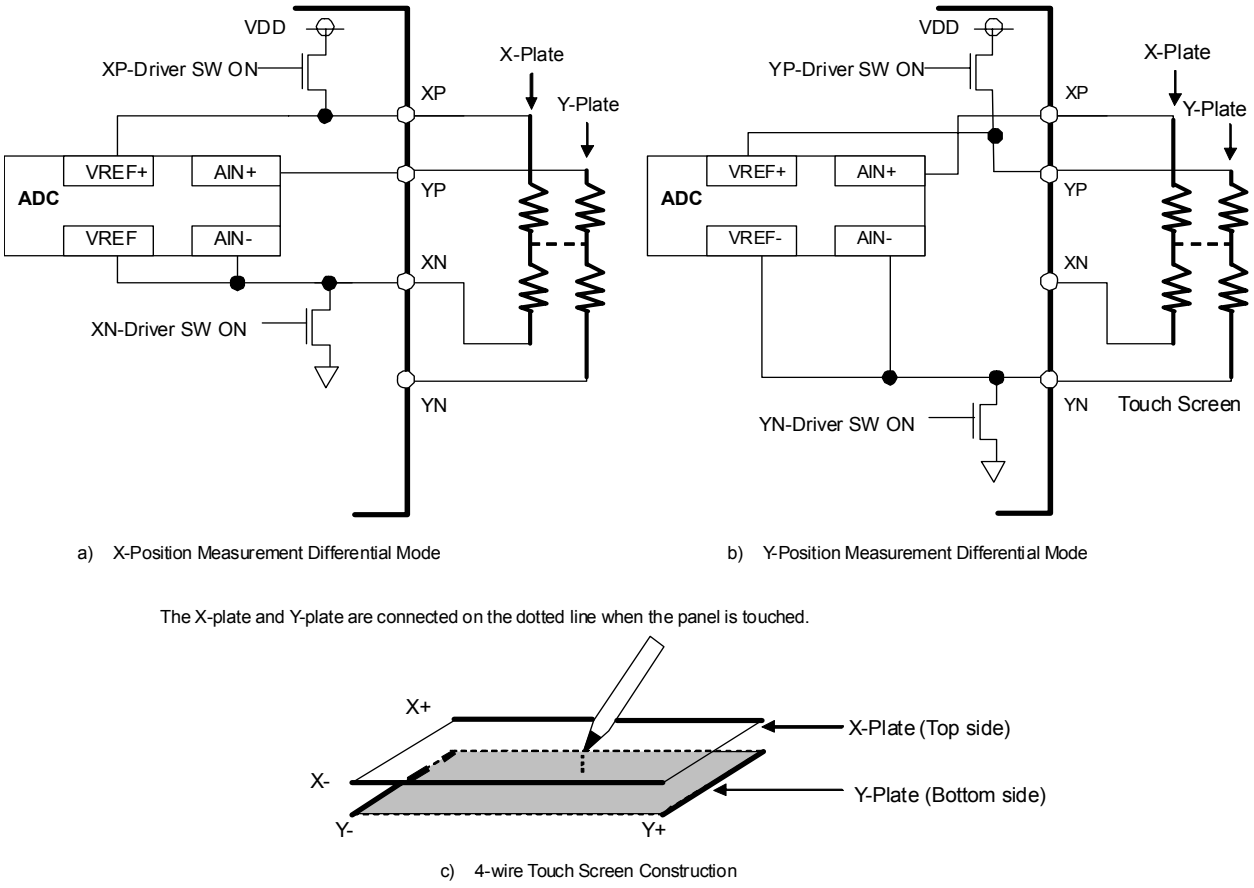


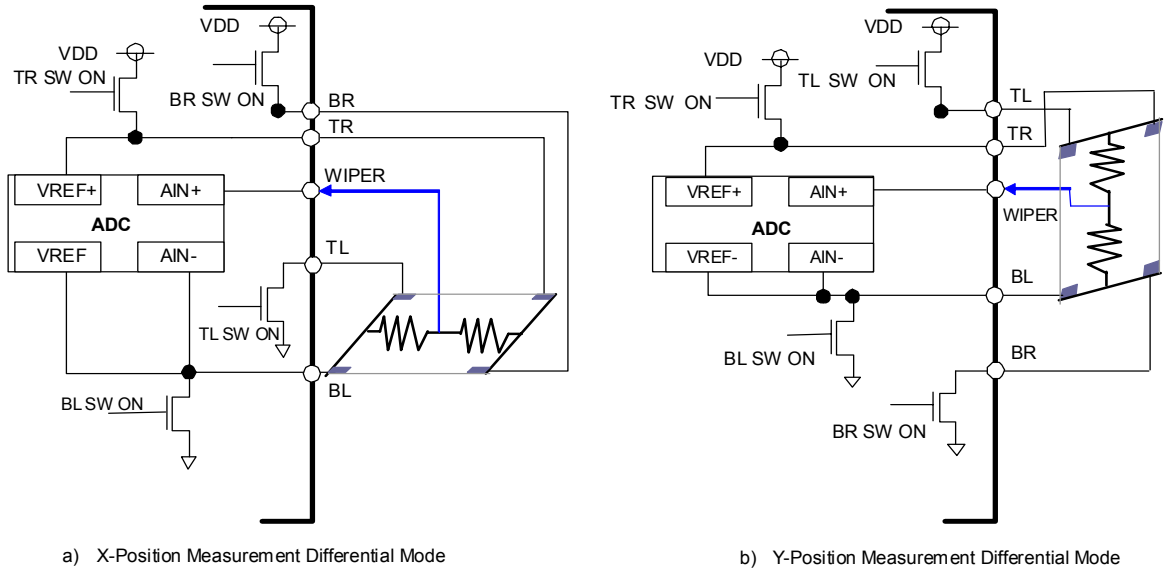
Figure 3. Axis Measurements for 4-wire Touch Screen

2. The Position Detection for 5-wire Touch Screen

A 5-wire touch panel consists of one transparent resistive layer and a top metal contact area separated by insulating spacers. The top layer acts only as a voltage measuring probe, the position detection uses the bottom resistive layer that had metal contacts at the 4 corners. When the top layer is pressed by a pen or stylus, the top layer contacts with the bottom layer. Then the X and Y coordinates is detected. The 5-wire touch screen works properly even with damages or scratches on the top layer, therefore the 5-wire touch panel has higher durability than the 4-wire touch panel. Connect the metal contact of the top layer to the WIPER pin to measure the Y-axis of current position at AIN+. The top right and top left contacts at the 4 corners are connected to VDD and the bottom right and bottom left contacts connected to VSS. Then the AK4186 initiates A/D conversion of AIN+ input voltage, and Y-axis position is determined.

Terminal	TL	TR	BL	BR
X-axis	VSS	VDD	VSS	VDD
Y-axis	VDD	VDD	VSS	VSS
SW	Switch VDD/VSS	VDD ON/OFF	VSS ON/OFF	Switch VDD/VSS

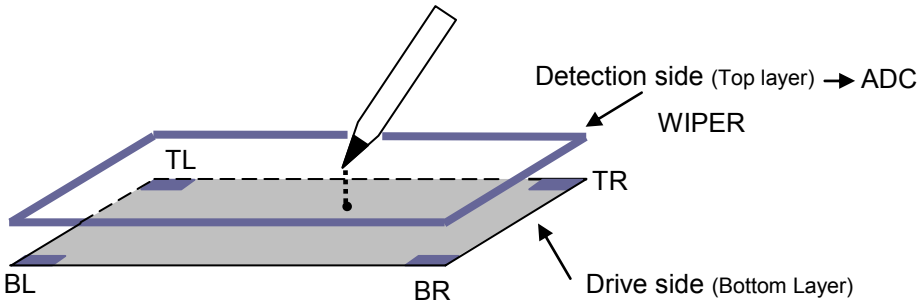
Table 4. Driver SW configuration



a) X-Position Measurement Differential Mode

b) Y-Position Measurement Differential Mode

The Top layer and Bottom layer are connected on the dotted line when the panel is touched.



5-wire Touch Screen Construction

Figure 4. Axis Measurements for 5-wire Touch Screen

■ Pen Pressure Measurement (Only 4-wire Touch Screen)

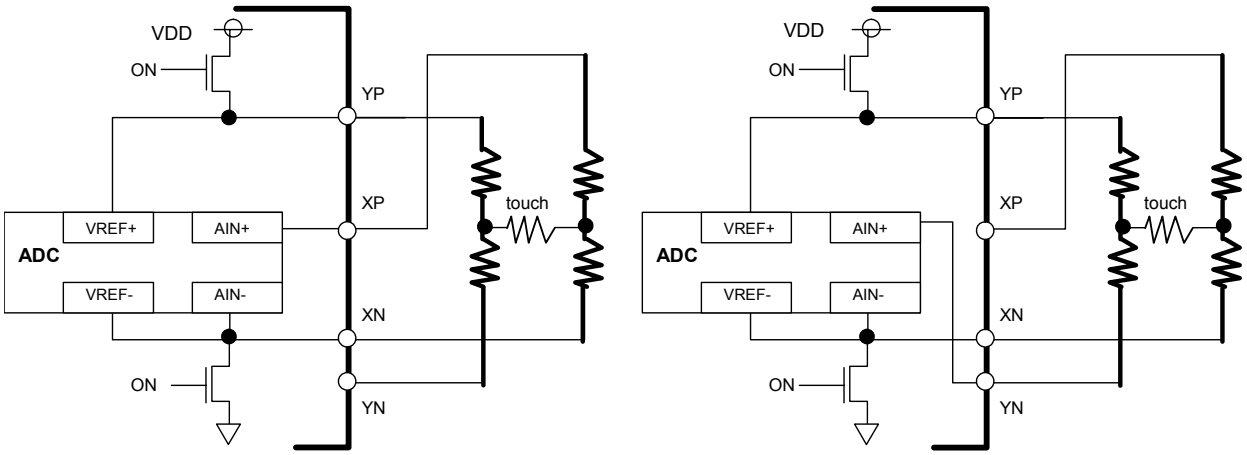
The touch screen pen pressure can be derived from the measurement of the contact resistor between two plates. The contact resistance depends on the size of the depressed area and the pressure. The area of the spot is proportional to the contact resistance.

This resistance (Rtouch) can be calculated using two different methods. The first method is that when the total resistance of the X-plate sheet is already known. The resistance, Rtouch, is calculated from the results of three conversions, X-position, Z1-position, and Z2-position, and then using following formula:

$$R_{TOUCH} = R_{X\text{-plate}} \cdot \frac{X_{Position}}{4096} \left(\frac{Z_2}{Z_1} - 1 \right)$$

The second method is that when both the resistances of the X-plate and Y-plate are known. The resistance, Rtouch, is calculated from the results of three conversions, X-position, Y-position, and Z1-position, and then using the following formula:

$$R_{TOUCH} = \frac{R_{X\text{-plate}} \cdot X_{Position}}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y\text{-plate}} \cdot \left(1 - \frac{Y_{Position}}{4096} \right)$$



a) Z1-Position Measurement Differential Mode

b) Z2-Position Measurement Differential Mode

Figure 5. Pen Pressure Measurements

■ Digital I/F

The AK4186 is controlled by a microprocessor via I^2C bus and supports standard mode (100kHz) and fast mode (400kHz). Note that the AK4186 operates in those two modes and does not support a High speed mode I^2C-bus system (3.4MHz). The AK4186 can operate as a slave device on the I^2C bus network. The AK4186 operates off of supply voltage down to 1.6V in order to connect a low voltage microprocessor.

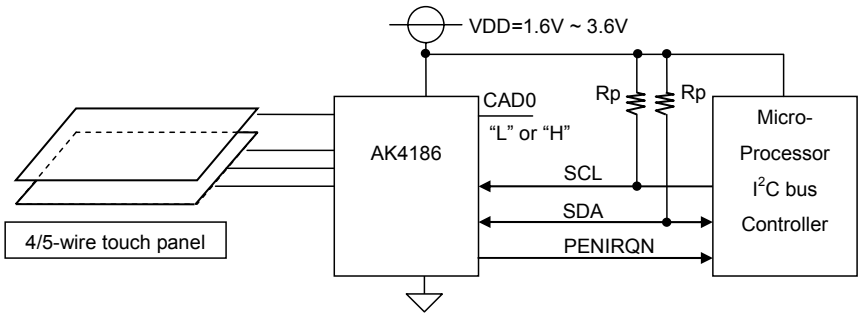


Figure 6. Digital I/F

1. WRITE Operations

Figure 7 shows the data transfer sequence for the I^2C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 11). After the START condition, a slave address is sent. This address is 6 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "100100". The next bit is CAD0 (device address bit). This bit identify the specific device on the bus. The hard-wired input pin (CAD0 pin) set this device address bit (Figure 8). If the slave address matches that of the AK4186, the AK4186 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 12). R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4186. The format is MSB first, and those most significant two bits are fixed to zeros (Figure 9). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 10). The AK4186 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 11).

The AK4186 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4186 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1FH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 13) except for the START and STOP conditions.

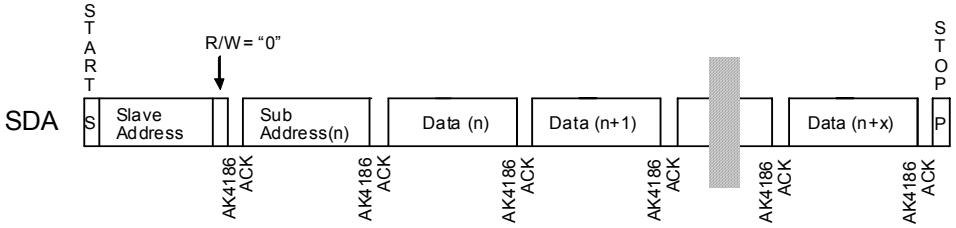


Figure 7. Data Transfer Sequence at the I²C-Bus Mode

1	0	0	1	0	0	CAD0	R/W

(This CAD0 should match with CAD0 pin.)

Figure 8. The First Byte

0	0	A5	A4	A3	A2	A1	A0

Figure 9. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 10. Byte Structure after the second byte

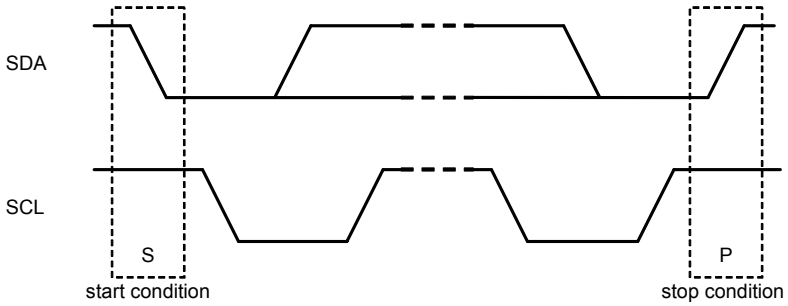


Figure 11. START and STOP Conditions

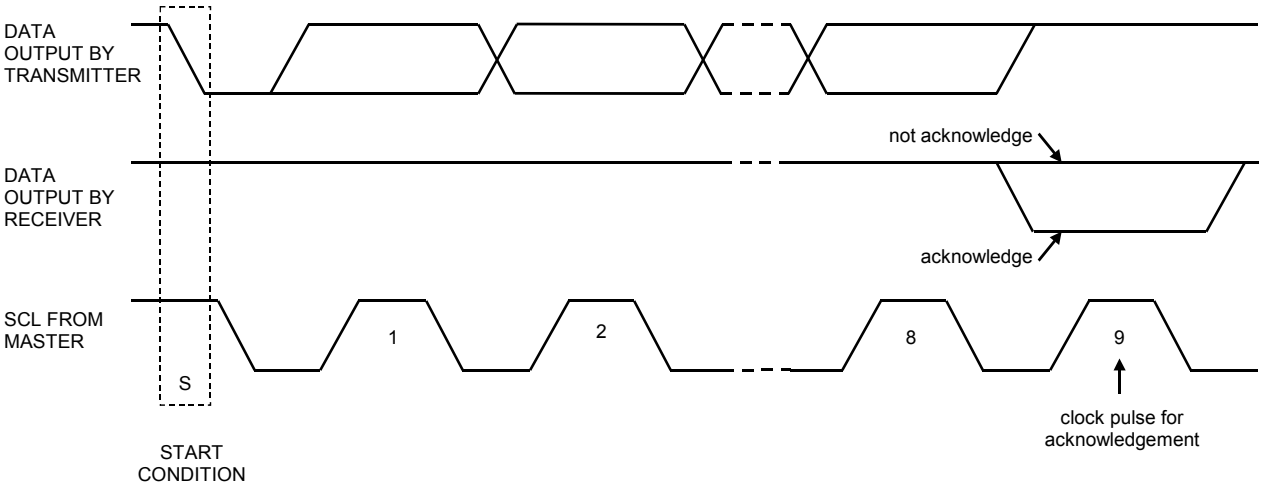


Figure 12. Acknowledge on the I²C-Bus

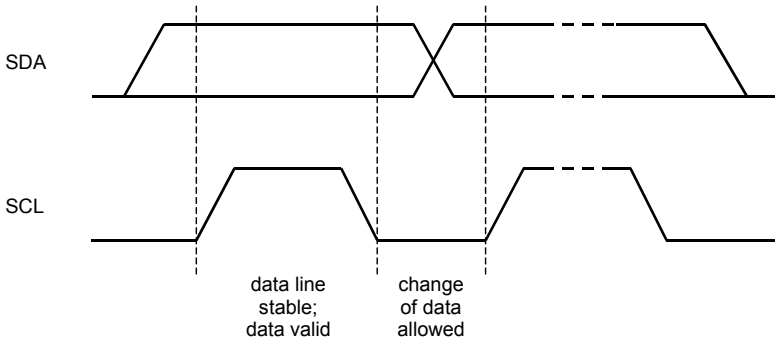


Figure 13. Bit Transfer on the I²C-Bus

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4186.

(1) Register READ Operation

After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out. The register read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4186 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4186 ceases transmission. A/D conversion data in sequence mode can be read when the data is available.

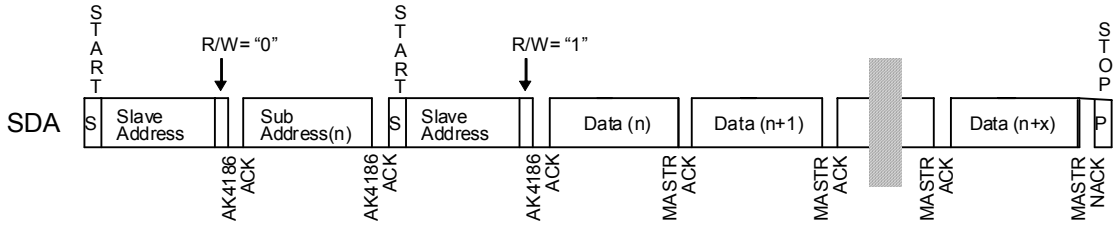


Figure 14. Register Address Read

(2) A/D Measurement Operation

When the master send a READ command after sending a control register address for a measurement channel by a WRITE operation, the AK4186 starts A/D conversion in single mode. The master issues the slave address with the R/W bit "1". The AK4186 then generates an acknowledge, and outputs ADC data. The ADC data is 2 bytes format (MSB first), and upper 12-bit are valid and lower 4-bit are filled with "0". (Figure 17, Figure 18) The master receives the first byte, and generates an acknowledge. Then the master receives the second byte and does not generate an acknowledge, the AK4186 ceases transmission. (Figure 15) If the master generates an acknowledge, the AK4186 newly repeats A/D conversion to set the channel every read cycle, and the master can receive update ADC data on each read operation. The AK4186 repeats A/D conversion and continuously outputs ADC data until the master does not generate an acknowledge but generates a stop condition instead. (Figure 16) This continuous read mode enables the higher sampling rate and lower processor load than a single ADC data read.

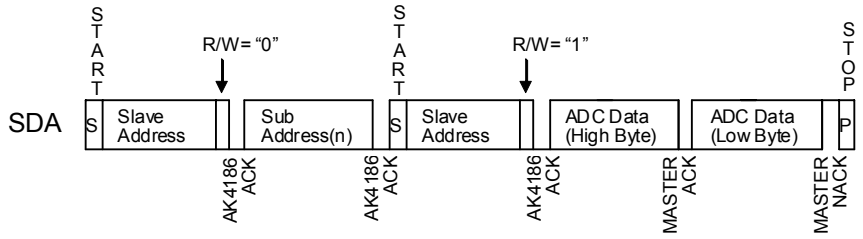


Figure 15. Single ADC Data Read

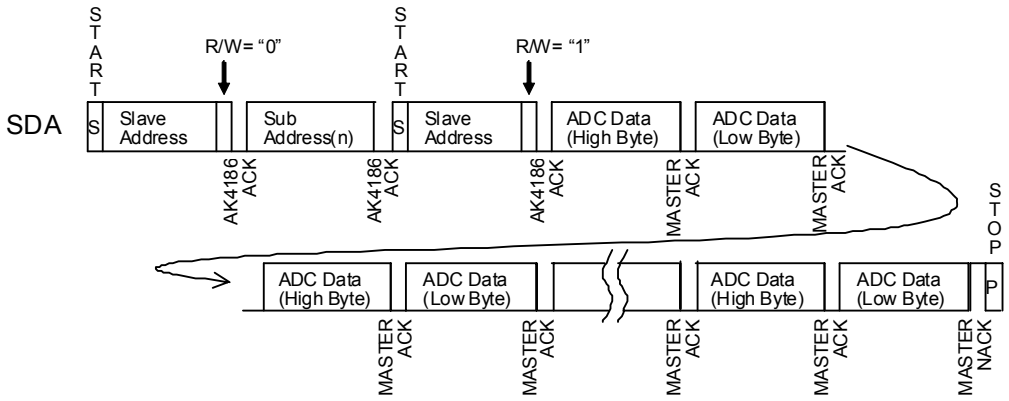


Figure 16. Continuous ADC Data Read

D11	D10	D9	D8	D7	D6	D5	D4

Figure 17. ADC Data (High Byte)

D3	D2	D1	D0	0	0	0	0

Figure 18. ADC Data (Low Byte)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	System Reset	0	0	0	0	0	0	0	SRST
01H	Setup Command	PANEL	0	SLEEP1	SLEEP0	0	0	0	PD0
02H	Sequence Command	0	SEQM2	SEQM1	SEQM0	COUNT	INTERVAL2	INTERVAL1	INTERVAL0
03H -0FH	Reserved	0	0	0	0	0	0	0	0
10H	Status	CHST3	CHST2	CHST1	CHST0	SEQST3	SEQST2	SEQST1	SEQST0
11H	Sequence Data 1H	D1T11	D1T10	D1T9	D1T8	D1T7	D1T6	D1T5	D1T4
12H	Sequence Data 1L	D1T3	D1T2	D1T1	D1T0	0	0	0	0
13H	Sequence Data 2H	D2T11	D2T10	D2T9	D2T8	D2T7	D2T6	D2T5	D2T4
14H	Sequence Data 2L	D2T3	D2T2	D2T1	D2T0	0	0	0	0
15H	Sequence Data 3H	D3T11	D3T10	D3T9	D3T8	D3T7	D3T6	D3T5	D3T4
16H	Sequence Data 3L	D3T3	D3T2	D3T1	D3T0	0	0	0	0
17H	Sequence Data 4H	D4T11	D4T10	D4T9	D4T8	D4T7	D4T6	D4T5	D4T4
18H	Sequence Data 4L	D4T3	D4T2	D4T1	D4T0	0	0	0	0
19H -1FH	Reserved	0	0	0	0	0	0	0	0
20H	Single XH	XS11	XS10	XS9	XS8	XS7	XS6	XS5	XS4
21H	Single XL	XS3	XS2	XS1	XS0	0	0	0	0
22H	Single YH	YS11	YS10	YS9	YS8	YS7	YS6	YS5	YS4
23H	Single YL	YS3	YS2	YS1	YS0	0	0	0	0
24H	Single Z1H	Z1S11	Z1S10	Z1S9	Z1S8	Z1S7	Z1S6	Z1S5	Z1S4
25H	Single Z1L	Z1S3	Z1S2	Z1S1	Z1S0	0	0	0	0
26H	Single Z2H	Z2S11	Z2S10	Z2S9	Z2S8	Z2S7	Z2S6	Z2S5	Z2S4
27H	Single Z2L	Z2S3	Z2S2	Z2S1	Z2S0	0	0	0	0
28H	Single INH	INS11	INS10	INS9	INS8	INS7	INS6	INS5	INS4
29H	Single INL	INS3	INS2	INS1	INS0	0	0	0	0

Table 5. AK4186 Register Map

■ System Reset

Upon power-up, the AK4186 must be reset by writing the reset command. (Refer to the "■ Power-up Sequence" for details) This ensures that all internal register reset to their initial values (00H) and set the channel to X-axis (auto driver = OFF). The System reset can also stop a sequential measurement forcibly, but all data will be cleared.

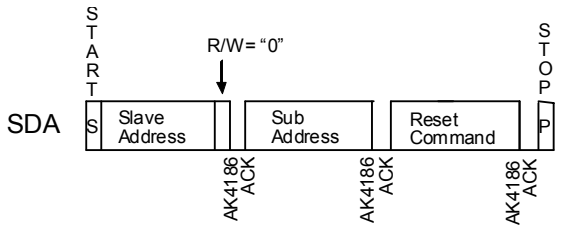


Figure 19. Data Transfer Sequence at the System Reset

1	0	0	1	0	0	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins.)
Figure 20. The First Byte

0	0	0	0	0	0	0	0

Figure 21. The Second Byte

0	0	0	0	0	0	0	1

Figure 22. Byte Structure at Reset Command

■ Setup Function of Touch Panel

1. Setup Command Configuration

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Setup Command	PANEL	0	SLEEP1	SLEEP0	0	0	0	PD0

Table 6. Setup Command Register Format

Bits	Name	Description
D7	PANEL	Panel type Selection 0: 4-wire (default) 1: 5-wire
D6	Reserved	Must write "0"
D5-D4	SLEEP1-0	Sleep Command bits (refer to "■ Sleep Mode") 00: Normal Mode (default) 01: Sleep Mode 1 (PENIRQN disabled and output "H". Touch Panel is open.) 10: Sleep Mode 2 (PENIRQN disabled and open. Touch Panel is open.) 11: Reserved
D3	Reserved	Must write "0"
D2	Reserved	Must write "0"
D1	Reserved	Must write "0"
D0	PD0	Power-down Mode (refer to "■ Power-down Control") 0: Auto Power-down Mode (default) 1: Driver ON Mode

Table 7. Setup Command description

SLEEP1-0, PD0 bits can be written during a sequential measurement but PANEL bit will not be changed.

2. Sequence Command Configuration

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Sequence Command	0	SEQM2	SEQM1	SEQM0	COUNT	INTERVAL2	INTERAVAL1	INTERVAL0

Table 8. Sequence Command Register Format

The AK4186 starts A/D conversion in sequence mode by setting the COUNT, SEQM2-0, INTERVAL2-0 bits of the register address to 02H. The AK4186 makes six or ten measurements by setting the COUNT bit. The results are used to calculate the average value, discarding the minimum and maximum values, and the result sets the data register of sequence mode. If the address 02H is set again during a sequential measurement, this setting is ignored and the AK4186 continues the measurement. The master executes the register read operation to read the measurement data of sequence mode after confirming the PENIRQN pin turns to "H" (Data Available).

Bits	Name	Description
D7	Reserved	Must write "0"
D6-D4	SEQM2-0	Sequence Mode 000: X → Y → Z1 → Z2 Scan (only 4-wire Touch Screen) (default) 001: X → Y Scan 010: X Scan 011: Y Scan 100: Z1 → Z2 Scan (only 4-wire Touch Screen) 101: Reserved 110: A-IN (only 4-wire Touch Screen) 111: Reserved
D3	COUNT	A/D Conversion count 0: 6 times A/D Conversion (default) 1: 10 times A/D Conversion
D2-D0	INTERVAL2-0	Sampling interval times. 000: 0μs (default) 001: 5μs 010: 10μs 011: 20μs 100: 50μs 101: 100μs 110: 200μs 111: 500μs

Table 9. Sequence Command description

■ Data Register

1. Sequence Mode Data Register

The AK4186 starts A/D conversion in sequence mode by setting the COUNT, SEQM2-0, INTERVAL2-0 bits of the register address 02H. The AK4186 makes six or ten measurements by setting the COUNT bit. The results are used to calculate the average value, discarding the minimum and maximum values, and the result sets the data register of sequence mode. The AK4186 registers data from address 11H in order of setting the SEQM2-0 bits. The master can read the ADC data by the register read operation after confirming the PENIRQN pin turns to "H" or a register status SEQST3-0 = 02H (Data Available). The data register is Read Clear so that data will be deleted once it is read. Do not read data during a sequential measurement.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Status	CHST3	CHST2	CHST1	CHST0	SEQST3	SEQST2	SEQST1	SEQST0
11H	Sequence Data 1H	D1T11	D1T10	D1T9	D1T8	D1T7	D1T6	D1T5	D1T4
12H	Sequence Data 1L	D1T3	D1T2	D1T1	D1T0	0	0	0	0
13H	Sequence Data 2H	D2T11	D2T10	D2T9	D2T8	D2T7	D2T6	D2T5	D2T4
14H	Sequence Data 2L	D2T3	D2T2	D2T1	D2T0	0	0	0	0
15H	Sequence Data 3H	D3T11	D3T10	D3T9	D3T8	D3T7	D3T6	D3T5	D3T4
16H	Sequence Data 3L	D3T3	D3T2	D3T1	D3T0	0	0	0	0
17H	Sequence Data 4H	D4T11	D4T10	D4T9	D4T8	D4T7	D4T6	D4T5	D4T4
18H	Sequence Data 4L	D4T3	D4T2	D4T1	D4T0	0	0	0	0

Table 10. Data Register for Sequence Mode (Read Only)

BIT	Name	Description
D7-D4	CHST3-0	Last Measurement Channel for Single Mode 0011: AIN 0100: X-axis 0101: Y-axis 0110: Z1 0111: Z2 others: Reserved
D3-D0	SEQST3-0	Status Bits for Sequence Mode 0000: Not Busy 0001: Sequence Busy 0010: Data Available others: Reserved

Table 11. Status Register description (Read Only)

2. Single Mode Data Register

The AK4186 starts A/D conversion in single mode by receiving a single measurement command, and then outputs MSB first 12bit A/D data.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	Single XH	XS11	XS10	XS9	XS8	XS7	XS6	XS5	XS4
21H	Single XL	XS3	XS2	XS1	XS0	0	0	0	0
22H	Single YH	YS11	YS10	YS9	YS8	YS7	YS6	YS5	YS4
23H	Single YL	YS3	YS2	YS1	YS0	0	0	0	0
24H	Single Z1H	Z1S11	Z1S10	Z1S9	Z1S8	Z1S7	Z1S6	Z1S5	Z1S4
25H	Single Z1L	Z1S3	Z1S2	Z1S1	Z1S0	0	0	0	0
26H	Single Z2H	Z2S11	Z2S10	Z2S9	Z2S8	Z2S7	Z2S6	Z2S5	Z2S4
27H	Single Z2L	Z2S3	Z2S2	Z2S1	Z2S0	0	0	0	0
28H	Single INH	INS11	INS10	INS9	INS8	INS7	INS6	INS5	INS4
29H	Single INL	INS3	INS2	INS1	INS0	0	0	0	0

Table 12. Data Register for Single Mode (Read Only)

■ Power-down Control

Power-down and pen interrupt function are controlled by PD0 bit. In order to achieve minimum current, it is recommended to set PD0 bit = “0” for automatic power down of the touch screen driver after A/D conversion. It is possible to reduce the variation in data by setting PD0 bit = “1” during measurements. A/D converter keeps power up state after every measurement completed.

When the register data of address 01H is written, PD0 bit is updated at the rising edge of the 27th SCL. The last PD0 bit is valid until this timing.

The A/D converter and internal oscillator are automatically powered up at the start of the conversion, and automatically powered down at the end of the conversion, regardless of the PD0 bit setting.

PD0	PENIRQN	Function
0	Enable	Auto Power-down Mode In power-down state, the touch screen driver switches are powered down. (Only YN or BL driver switch is turned ON and forced to VSS.) PEN interrupt function is enabled except when in the sampling time and converting time.
1	Disable	Driver ON Mode If X-axis or Y-axis is selected as analog input, touch screen driver switches are always powered up. This is effective when more settling time is required to suppress the electrical bouncing of touch plate. PEN interrupt function is disabled and PENIRQN is forced to “L” state.

Table 13. Power-down Control

■ Sleep Mode

The AK4186 supports sleep mode that puts touch panel to open state and disables pen interrupt function, effective for reducing power consumption caused by unnecessary pen touch.

Sleep mode is controlled by SLEEP1-0 bits. The AK4186 changes to sleep mode on the rising edge of 27th SCL after the micro-controller writes “01” or “10” to SLEEP1-0 bits of AK4186’s register. All touch screen driver switches and A/D converter are powered down in this sleep mode, and it reduces power consumption to the minimum value. The PENIRQN output is shown below. (Table 14)

The AK4186 returns to normal operation out of sleep mode when the micro-controller writes “00” to SLEEP1-0 bits. The timing of going back to normal operation mode is the rising edge of the 27th SCL. The initial state after system reset is in normal operation mode.

SLEEP1-0	PENIRQN	Touch Panel
00	Normal Operation	Normal Operation
01	Disable (PENIRQN=H)	Open
10	Disable (PENIRQN=Hi-z)	Open
11	N/A	N/A

Table 14. Sleep Mode

A/D conversion is available during sleep mode by issuing an ADC executing command (sequential). The AK4186 returns to sleep mode after completing an A/D conversion.

CONTROL SEQUENCE

■ Power-up Sequence

To fix the I^2C interface statement, send a dummy command when first power up. After the dummy command, send a reset command to initialize internal registers.

1	0	0	1	0	0	CAD0	R/W

Figure 23. Slave Address Construction (CAD0 is set by a pin)

1	1	1	1	1	1	1	1

Figure 24. Dummy Address Construction

1	1	1	1	1	1	1	1

Figure 25. Dummy Command Construction

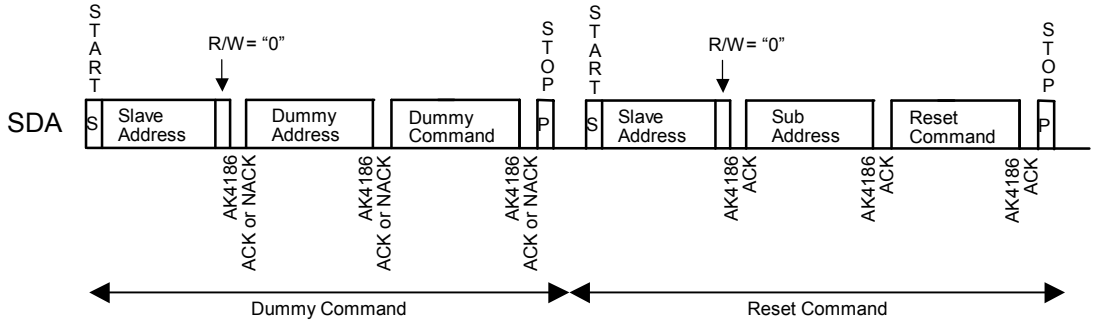


Figure 26. Power-up Sequence

■ Touch Screen Controller Control Sequence (Single Mode)

(1) Setup Sequence

In case of the single measurement mode, this touch panel configuration register sets the measurement mode of the AK4186. Touch screen driver switches are turned ON at Driver ON mode (PD0 bit = "1") on the rising edge of the 27th SCL. It is possible to have longer tracking time even if the source of analog input impedance is high, because the actual sampling is executed at the read operation. If a current measurement is made by the same setting of PD0 bit as the last time, the setup sequence is unnecessary.

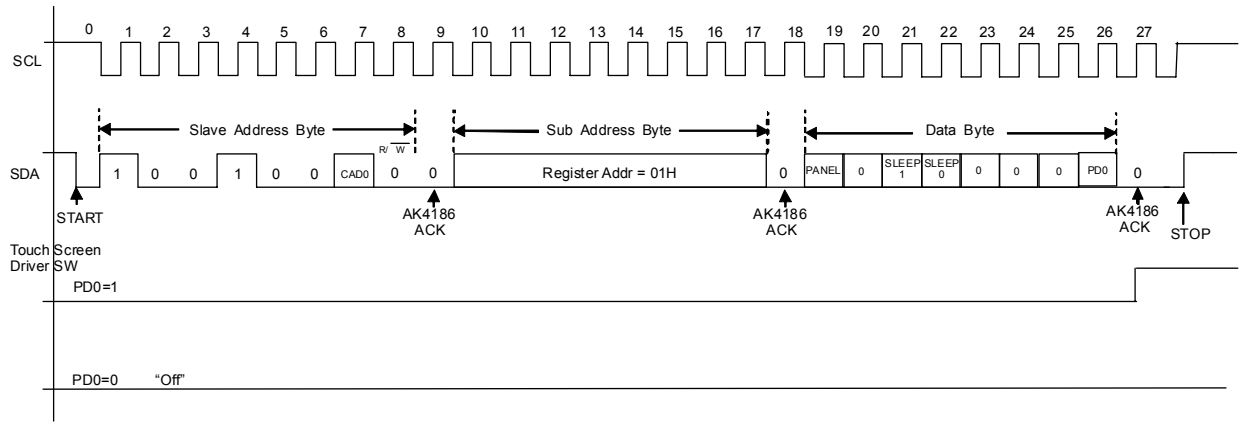


Figure 27. Setup operation and Driver SW timing

(2) Single Measurement Sequence

When the master send a READ command after sending a control register address for a measurement channel by a WRITE operation, the AK4186 starts A/D conversion in single mode. This A/D conversion is synchronized with the internal clock. The internal oscillator of the AK4186 is automatically powered up on the falling edge of 25th SCL after writing the register address, and the AK4186 samples the analog input and completes A/D conversion after the rising edge of 26th SCL. The master receives the first byte of serial data (D11-D4, MSB first), and generates an acknowledge. Then the master receives the second byte of serial data (D3-D0, followed by four 0 bits). When the master continuously reads ADC data, the master repeats read operation after generating an acknowledge. If the master does not generate an acknowledge but generates stop condition instead, the AK4186 ceases continuous operation.

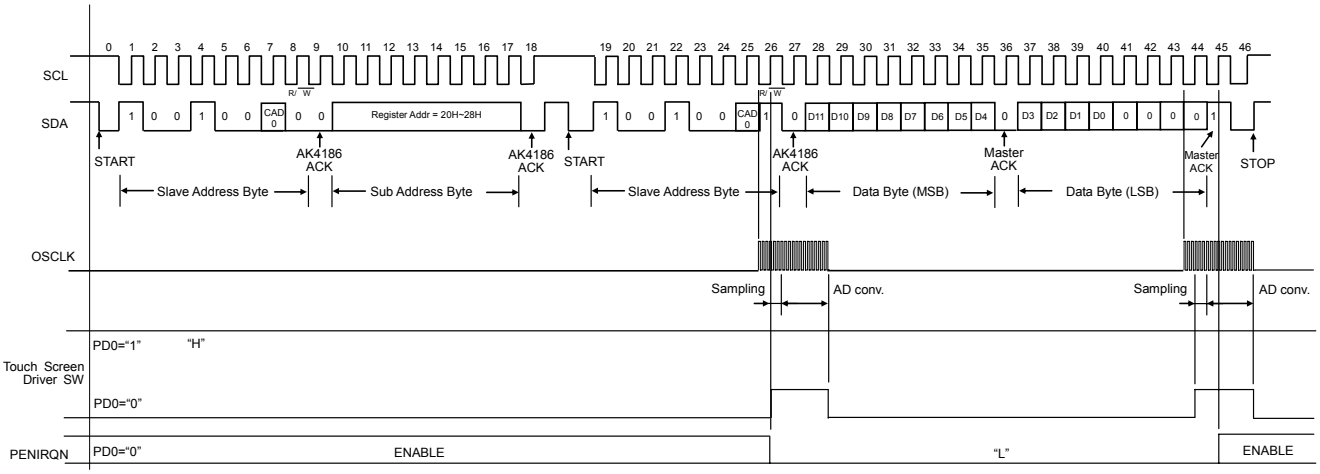


Figure 28. Single Measurement operation and Driver SW timing

■ Touch Screen Controller Control Sequence (Sequence Mode)

The AK4186 starts A/D conversion in sequence mode by setting the COUNT, SEQM2-0, INTERVAL2-0 bits of the register address 02H. PENIRQN is forced to "L" state, and internal oscillator is automatically powered up. The AK4186 makes six or ten measurements by setting the COUNT bit. The results are used to calculate the average value, discarding the minimum and maximum values, and the result sets the data register of sequence mode. When the sequence is finished, the AK4186 sets the PENIRQN pin to "H" and notifies that sequence is ended. After 20μs (typ.) is passed from the rising edge of the PENIRQN pin, the internal oscillator is powered down and PEN interrupt function is enabled.

The master executes the register read operation to read the measurement data of sequence mode after confirming Data availability. The master can confirm Data availability by PENIRQN↑ or SEQST3-0 = 03H.

This sequence data can be read in register read operation one by one (Address 11H). Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4186 then generates an acknowledge, 1 byte of ADC data, and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4186 ceases transmission. The A/D data is cleared after reading all the A/D data.

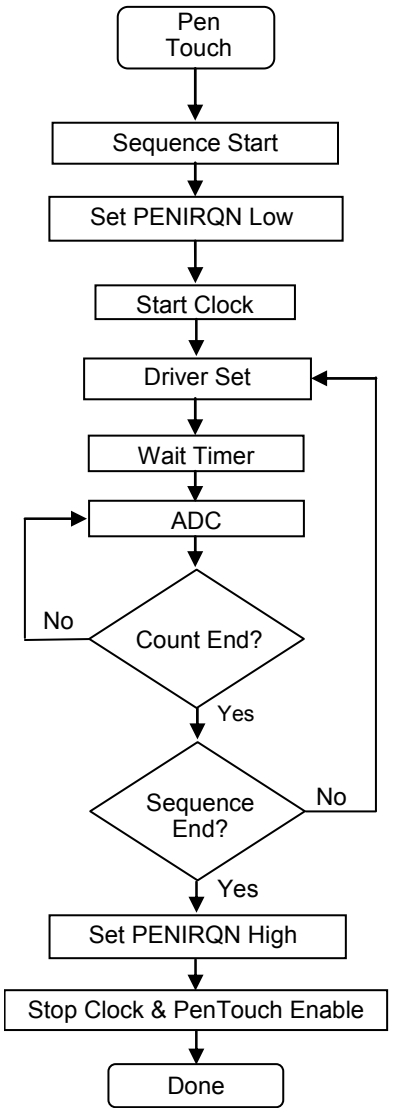


Figure 29. Internal Clock Mode Control Flowchart

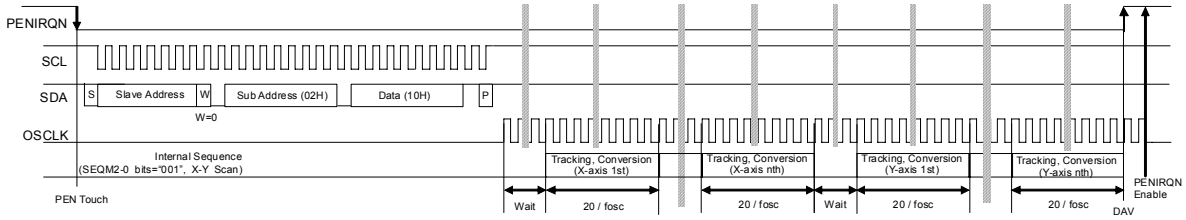


Figure 30. Sequence Mode Control Sequence (X-Y Scan: SEQM bits = "001")
(Sequence Mode Start → Internal Sequence Processing → Data Available)

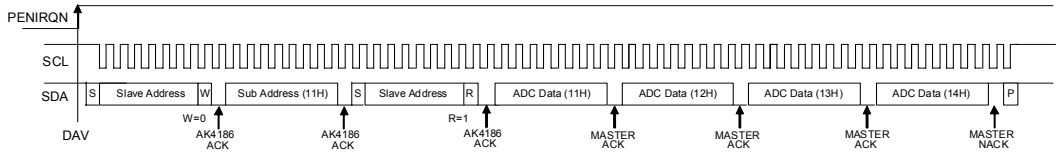


Figure 31. Sequence Mode Control Sequence (X-Y Scan: SEQM bits = "001")
(Data Available → A/D Data Read)

D11 (MSB)	D10	D9	D8	D7	D6	D5	D4

Figure 32. ADC Data (High Byte)

D3	D2	D1	D0 (LSB)	0	0	0	0

Figure 33. ADC Data (Low Byte)

■ Pen Interrupt

The AK4186 has pen interrupt function to detect pen touches. Pen interrupt function is enabled at power-down state and PD0 bit = "0" (Figure 34). The YN pin (4-wire) or BL pin (5-wire) is connected to VSS at the PEN interrupt enabled state. The XP pin (4-wire) or WIPER pin (5-wire) is pulled up via an internal resistor (R_{IRQ}: typ.50kΩ). PENIRQN is connected to the XP pin (4-wire) or WIPER pin (5-wire) inside. If touch plate is pressed by a pen, the current flows via <VDD> - <Ri> - <X+> - <Y-> (4-wire). If 5-wire, via <VDD> - <Ri> - <WIPER> - <BL>. The resistance of the plate is generally 1kΩ or less, PENIRQN is forced to "L" level. If the pen is released, PENIRQN returns "H" level because two plates are disconnected, and the current does not flow via two plates.

During an A/D conversion or Sequence measurement or when PD0 bit is set to "1", the PENIRQN is "L" for all the time in this period regardless of the touched/non-touched state.

While in single measurement mode, the pen interrupt function is disabled from the rising edge of 26th SCL to the end of the measurement. (Figure 28)

It is recommended that the micro controller mask the pseudo-interrupts while the control command is issued or A/D data is output.

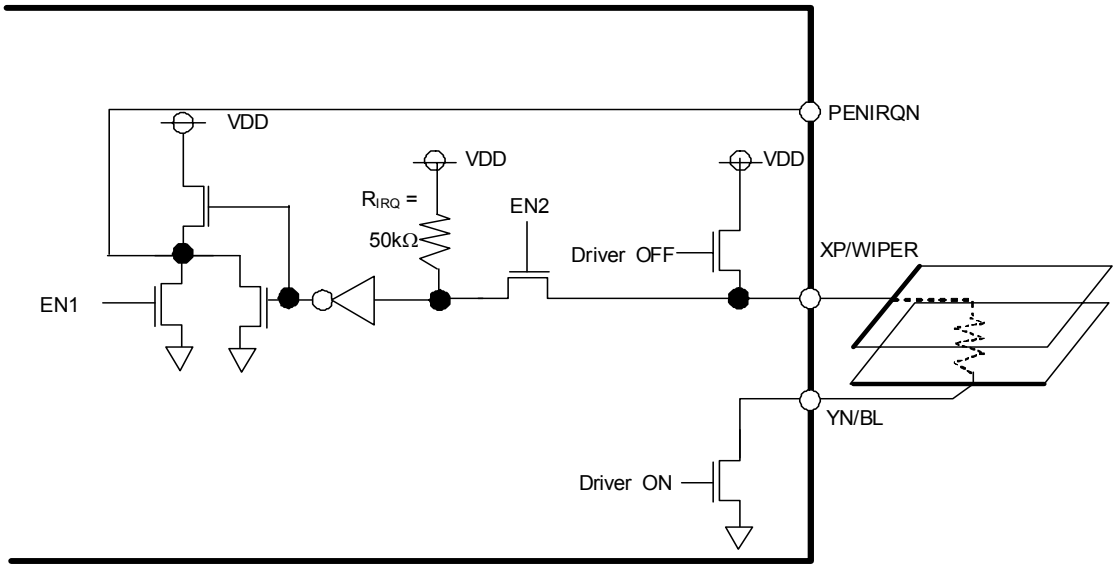


Figure 34. PENIRQN Functional Block Diagram (WIPER does not have a driver.)

SYSTEM DESIGN

Figure 35, Figure 36, Figure 37, Figure 38 shows the system connection diagram for the AK4186. The evaluation board [AKD4186] demonstrates the optimum layout, power supply arrangements and measurement results.

AK4186ECB <4-wire Touch Screen Input>

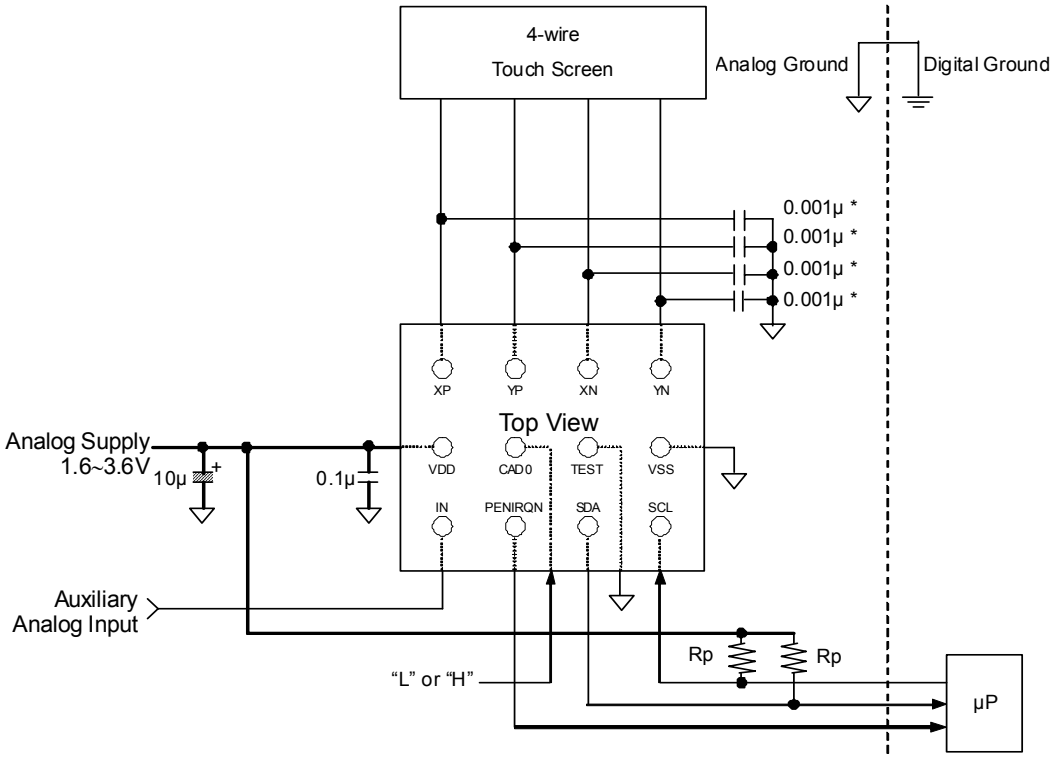


Figure 35. Typical Connection Diagram (4-wire, AK4186ECB)

Notes:
- VSS of the AK4186 should be distributed separately from the ground of external controllers.
- All digital input pins (SCL, SDA, CAD0 pins) must not be left floating.

AK4186EN <4-wire Touch Screen Input>

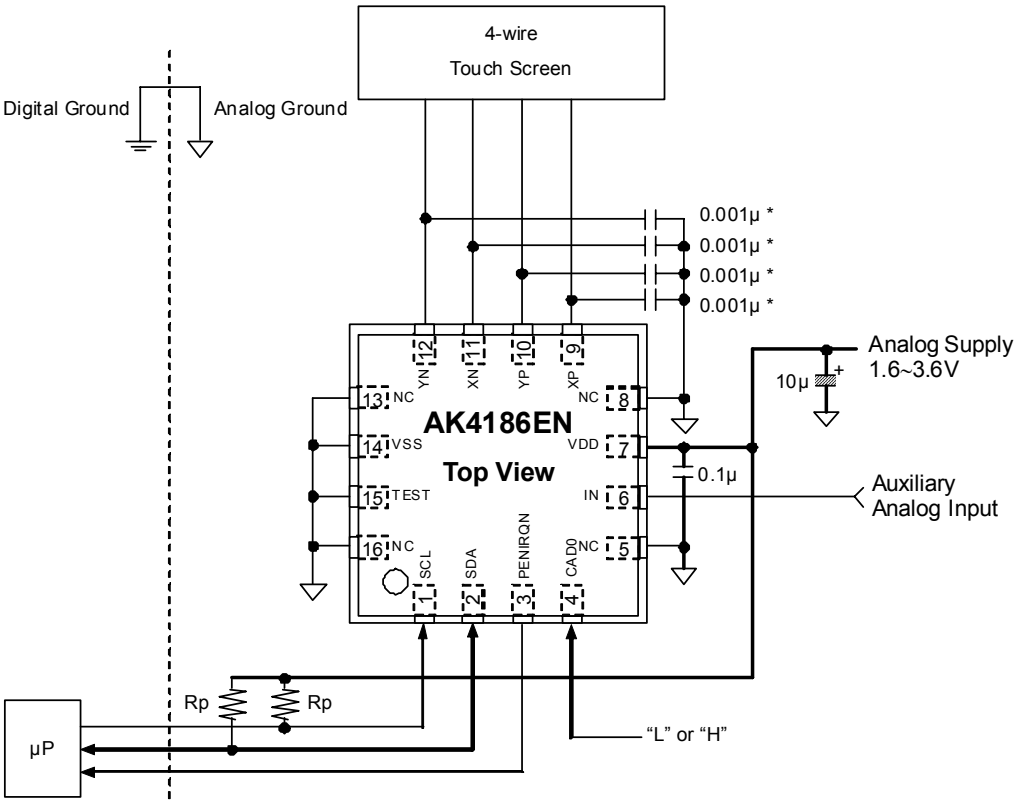


Figure 36. Typical Connection Diagram (4-wire, AK4186EN)

Notes:
- VSS of the AK4186 should be distributed separately from the ground of external controllers.
- All digital input pins (SCL, SDA, CAD0 pins) must not be left floating.

AK4186ECB <5-wire Touch Screen Input>

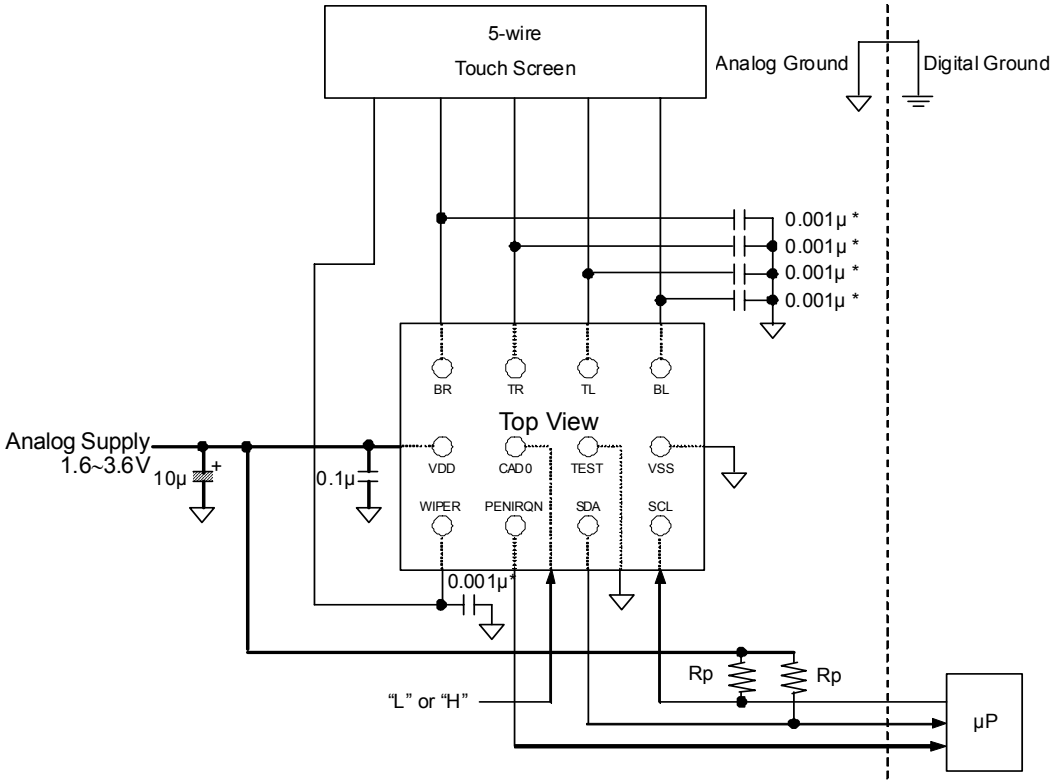


Figure 37. Typical Connection Diagram (5-wire, AK4186ECB)

Notes:

- VSS of the AK4186 should be distributed separately from the ground of external controllers.
- All digital input pins (SCL, SDA, CAD0 pins) must not be left floating.

AK4186EN <5-wire Touch Screen Input>

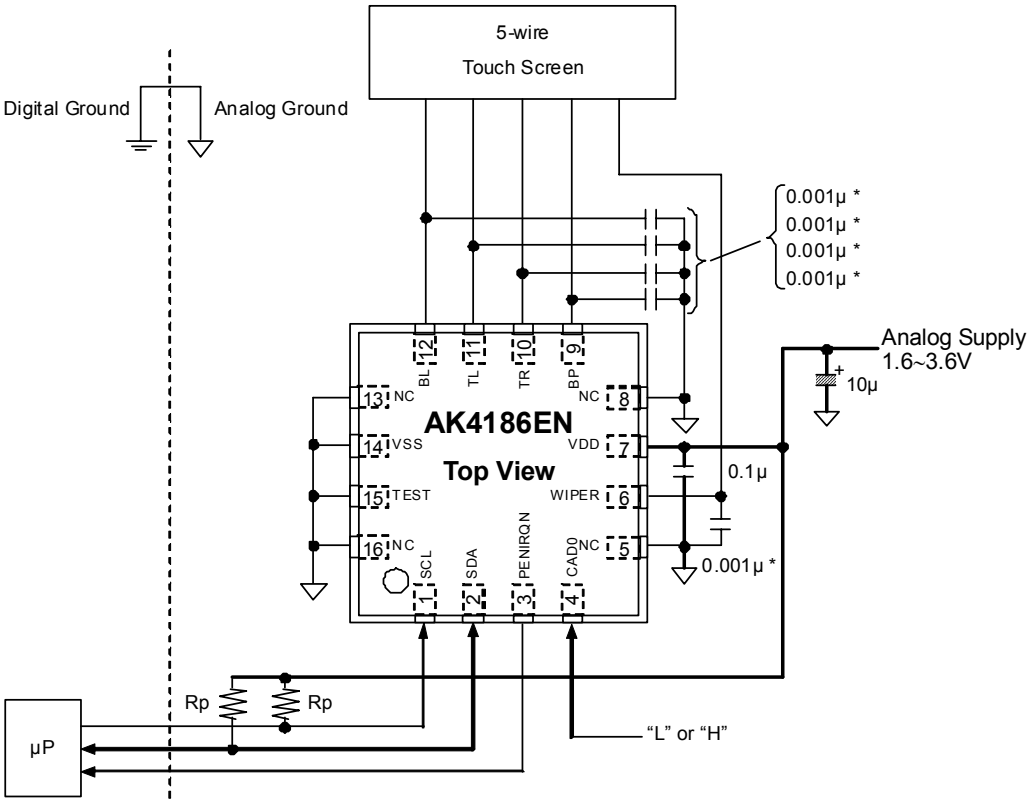


Figure 38. Typical Connection Diagram (5-wire, AK4186EN)

Notes:
- VSS of the AK4186 should be distributed separately from the ground of external controllers.
- All digital input pins (SCL, SDA, CAD0 pins) must not be left floating.

3. Grounding and Power Supply Decoupling

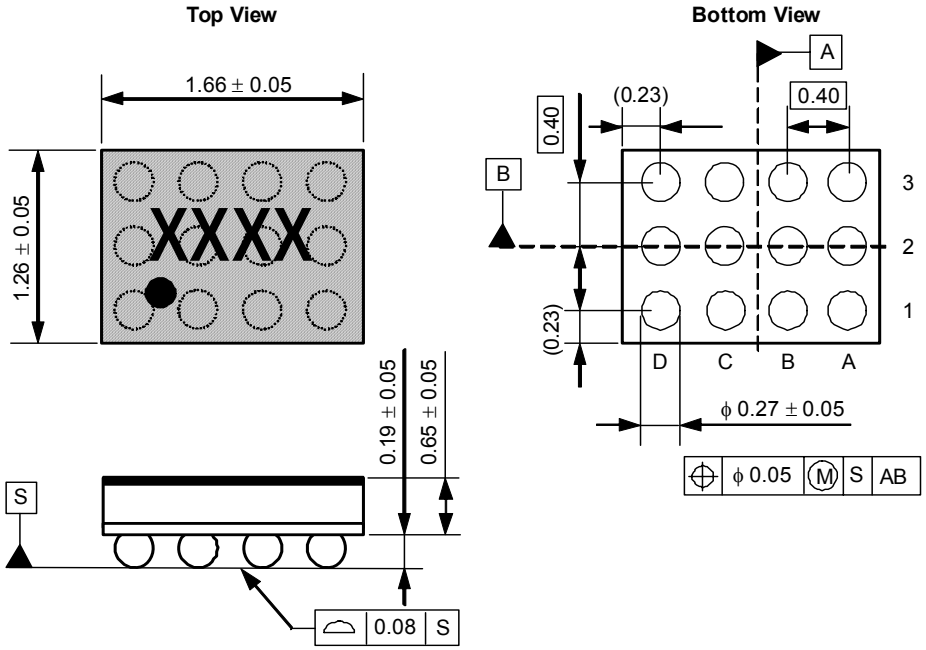
The AK4186 requires careful attention to power supply and grounding arrangements. VDD is usually supplied from the system's analog supply. VSS of the AK4186 must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4186 as possible, with the small value ceramic capacitor being the nearest.

4. Analog Inputs

When an EMI source is close to the touch panel analog signal line, EMI noise affects analog characteristics performance. Connect noise canceling capacitors (*) as close as possible to each pin (XP, XN, YP, YN pins) of the AK4186 to avoid this noise. (Figure 35, Figure 36, Figure 37, Figure 38)

PACKAGE (AK4186ECB)

12pin CSP (Unit: mm)

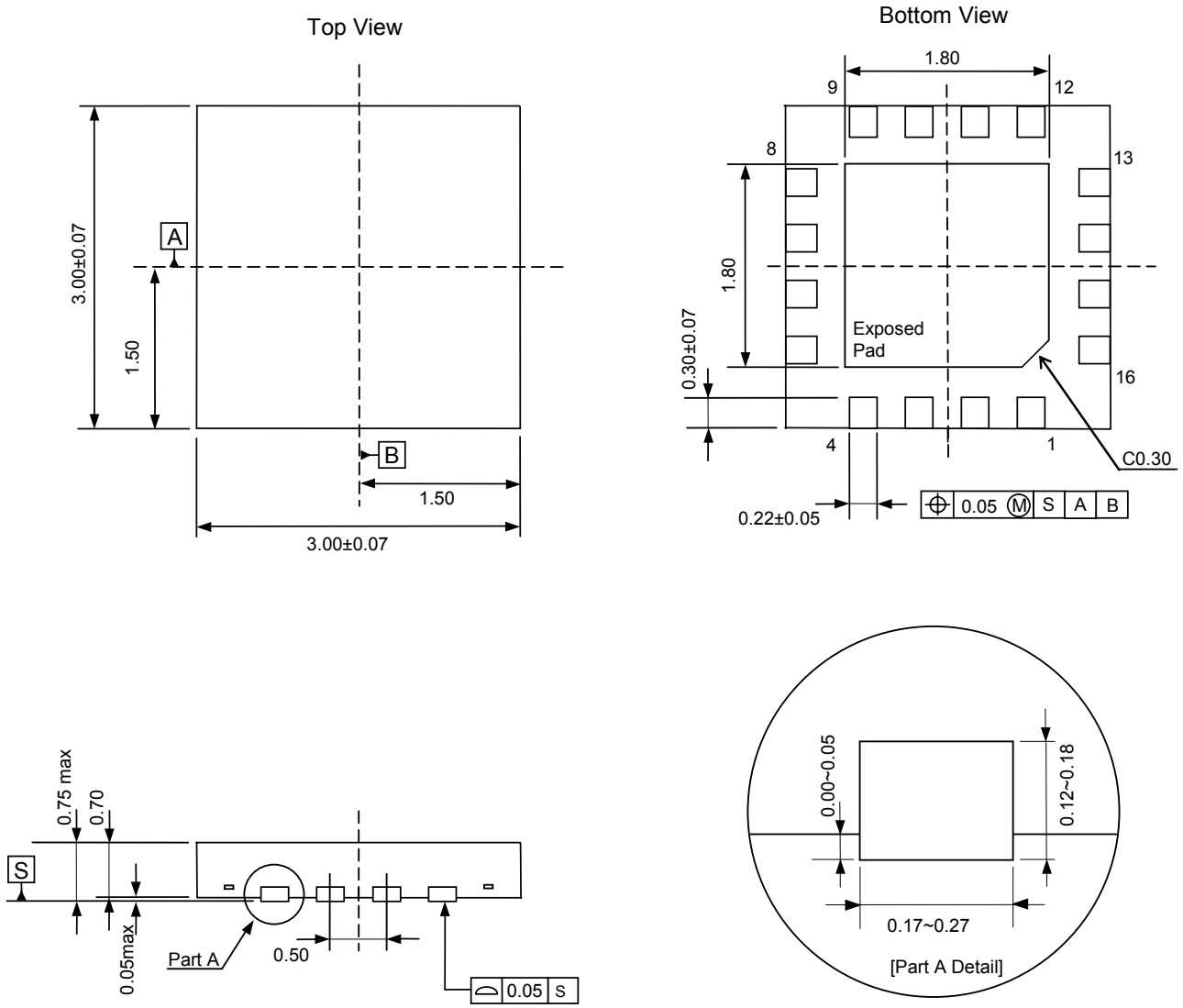


■ Material & Lead finish

Package molding compound: Epoxy resin, Halogen (bromine and chlorine) free
Solder ball material: SnAgCu

PACKAGE (AK4186EN)

16pin QFN (Unit: mm)

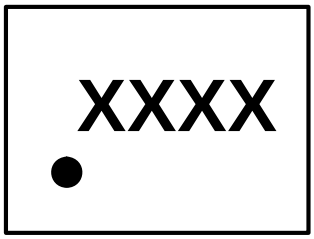


Note: The thermal die pad must be open or connected to the ground.

■ Package & Lead frame material

Package molding compound: Epoxy Resin, Halogen (bromine and chlorine) free
Lead frame material: Cu Alloy
Lead frame surface treatment: Palladium Plate

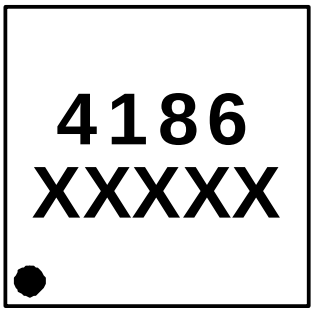
MARKING (AK4186ECB)



A1

Date Code: XXXX(4 digits)
Pin #A1 indication

MARKING (AK4186EN)



Date Code: XXXXX (5 digits)
Pin #1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page/Line	Contents
09/03/30	00	First Edition		
09/10/22	01	Error Correction	18 /2 /6	Sequence Mode Data Register "register address 03H" →"register address 02H" SEQST7-0 = 03H → SEQST3-0 = 02H
			22	Setup Sequence Figure 27 was changed.
10/07/02	02	Product Addition		AK4186EN was added.
10/12/15	03	Spec Change	5	ANALOG CHARACTERISTICS Gain Error (AK4186EN): -6 → -4.5 (min) +2 → +3.5 (max)
11/03/30	04	Error Correction	3	PIN/FUNCTION Pin No. D3, 12: BL "Touch Panel Bottom Right Input" → "Touch Panel Bottom Left Input"