



# **AK4122A**

## **24-Bit 96kHz SRC with DIR**

### **GENERAL DESCRIPTION**

The AK4122A is a digital sample rate converter (SRC) with the digital audio receiver (DIR). The input sample rate ranges from 8kHz to 96kHz. The output sample rate is 32kHz, 44.1kHz, 48kHz or 96kHz. By using the AK4122A, the system can take very simple configuration because the AK4122A has an internal PLL and does not need any master clock at slave mode. Then the AK4122A is suitable for the application interfacing to different sample rates like Car Audio, DVD recorder, etc.

### **FEATURES**

#### **1. SRC**

- Asynchronous Sample Rate Converter
- Input Sample Rate Range (fsi) : 8kHz ~ 96kHz
- Output Sample Rate (fso) : 32kHz, 44.1kHz, 48kHz, 96kHz
- Input to Output Sample Rate Ratio : 0.33 to 6
- THD+N : -113dB
- I/F format : MSB justified, LSB justified (16/24bit) and I<sup>2</sup>S compatible
- Clock for Master mode : 256/384/512/768fs
- SRC Bypass mode
- Soft Mute Function

#### **2. DIR**

- 4-Channel Inputs Selector & 1-Channel Through Output
- AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible
- Low Jitter Analog PLL
- PLL Lock Range : 32kHz ~ 96kHz
- Auto detection
  - Non-PCM Bit Stream
  - DTS-CD Bit Stream
  - Validity Flag
  - Sampling Frequency (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz)
  - Unlock & Parity Error
  - DAT Start ID
- 40-bit Channel Status Buffer
- Burst Preamble bit Pc, Pd Buffer for Non-PCM bit streams
- Q-subcode Buffer for CD bit streams

#### **3. 4-wire Serial $\mu$ P Interface**

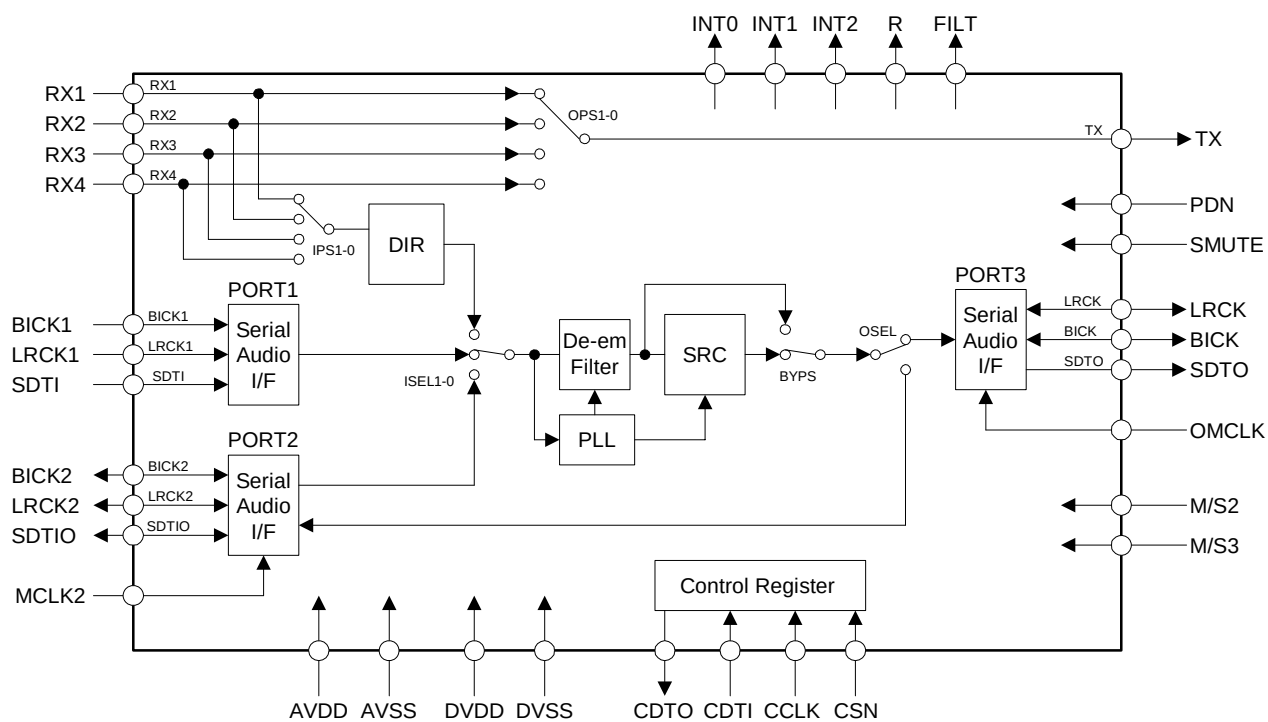
#### **4. Power Supply**

- AVDD: 3.0 ~ 3.6V (typ. 3.3V)
- DVDD: 3.0 ~ 3.6V (typ. 3.3V)

#### **5. Ta = -10 ~ 70°C**

#### **6. Package : 48pin LQFP**

## ■ Block Diagram



Block diagram

## ■ Ordering Guide

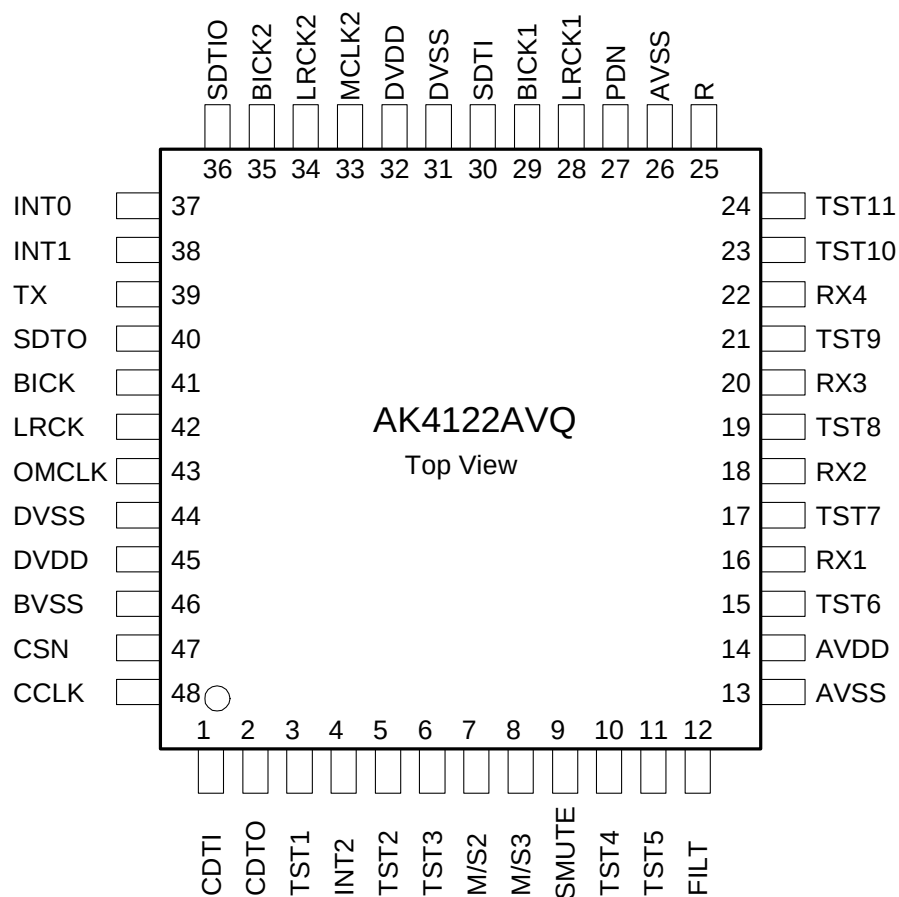
AK4122AVQ  
AKD4122A

-10 ~ +70°C

48pin LQFP (0.5mm pitch)

Evaluation Board for AK4122A

## ■ Pin Layout



## PIN/FUNCTION

| No. | Pin Name | I/O | Function                                                                                                                                                          |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | CDTI     | I   | Control Data Input Pin                                                                                                                                            |
| 2   | CDTO     | O   | Control Data Output Pin                                                                                                                                           |
| 3   | TST1     | O   | Test 1 Pin                                                                                                                                                        |
| 4   | INT2     | O   | Interrupt 2 Pin                                                                                                                                                   |
| 5   | TST2     | O   | Test 2 Pin                                                                                                                                                        |
| 6   | TST3     | I   | Test 3 Pin<br>This pin should be connected to DVSS.                                                                                                               |
| 7   | M/S2     | I   | Master / Slave Mode Pin for PORT2<br>“H” : Master mode, “L” : Slave Mode                                                                                          |
| 8   | M/S3     | I   | Master / Slave Mode Pin for PORT3<br>“H” : Master mode, “L” : Slave Mode                                                                                          |
| 9   | SMUTE    | I   | Soft Mute Pin<br>“H” : Soft Mute, “L” : Normal Operation                                                                                                          |
| 10  | TST4     | I   | Test 4 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 11  | TST5     | I   | Test 5 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 12  | FILT     | O   | PLL Loop Filter Pin<br>470Ω±5% resistor and 2.2μF±50% ceramic capacitor in parallel with a<br>2.2nF±50% ceramic capacitor should be connected to AVSS externally. |
| 13  | AVSS     | -   | Analog Ground Pin                                                                                                                                                 |
| 14  | AVDD     | -   | Analog Power Supply Pin, 3.0 ~ 3.6V                                                                                                                               |
| 15  | TST6     | I   | Test 6 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 16  | RX1      | I   | Receiver Input 1 Pin with Amp for 0.2Vpp (Internal Biased Pin)                                                                                                    |
| 17  | TST7     | I   | Test 7 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 18  | RX2      | I   | Receiver Input 2 Pin with Amp for 0.2Vpp (Internal Biased Pin)                                                                                                    |
| 19  | TST8     | I   | Test 8 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 20  | RX3      | I   | Receiver Input 3 Pin with Amp for 0.2Vpp (Internal Biased Pin)                                                                                                    |
| 21  | TST9     | I   | Test 9 Pin<br>This pin should be connected to AVSS.                                                                                                               |
| 22  | RX4      | I   | Receiver Input 4 Pin with Amp for 0.2Vpp (Internal Biased Pin)                                                                                                    |
| 23  | TST10    | I   | Test 10 Pin<br>This pin should be connected to AVSS.                                                                                                              |
| 24  | TST11    | O   | Test 11 Pin                                                                                                                                                       |

Note: All input pins except internal biased pins should not be left floating.

|    |       |     |                                                                                                   |
|----|-------|-----|---------------------------------------------------------------------------------------------------|
| 25 | R     | -   | External Resistor Pin<br>12k $\Omega$ ±5% resistor should be connected to AVSS externally.        |
| 26 | AVSS  | -   | Analog Ground Pin                                                                                 |
| 27 | PDN   | I   | Power-Down Mode Pin<br>“H”: Power up, “L”: Power down reset and initializes the control register. |
| 28 | LRCK1 | I   | Input Channel Clock Pin                                                                           |
| 29 | BICK1 | I   | Audio Serial Data Clock Pin                                                                       |
| 30 | SDTI  | I   | Audio Serial Data Input Pin                                                                       |
| 31 | DVSS  | -   | Digital Ground Pin                                                                                |
| 32 | DVDD  | -   | Digital Power Supply Pin, 3.0 ~ 3.6V                                                              |
| 33 | MCLK2 | I   | Master Clock Input Pin                                                                            |
| 34 | LRCK2 | I/O | Input / Output Channel Clock Pin                                                                  |
| 35 | BICK2 | I/O | Audio Serial Data Clock Pin                                                                       |
| 36 | SDTIO | I/O | Audio Serial Data Input / Output Pin                                                              |
| 37 | INT0  | O   | Interrupt 0 Pin                                                                                   |
| 38 | INT1  | O   | Interrupt 1 Pin                                                                                   |
| 39 | TX    | O   | Transmitter Output Pin                                                                            |
| 40 | SDTO  | O   | Audio Serial Data Output Pin                                                                      |
| 41 | BICK  | I/O | Audio Serial Data Clock Pin                                                                       |
| 42 | LRCK  | I/O | Output Channel Clock Pin                                                                          |
| 43 | OMCLK | I   | Master Clock Input Pin                                                                            |
| 44 | DVSS  | -   | Digital Ground Pin                                                                                |
| 45 | DVDD  | -   | Digital Power Supply Pin, 3.0 ~ 3.6V                                                              |
| 46 | BVSS  | -   | Substrate Ground Pin<br>This pin should be connected to AVSS.                                     |
| 47 | CSN   | I   | Chip Select Pin                                                                                   |
| 48 | CCLK  | I   | Control Data Clock Pin                                                                            |

Note: All input pins except internal biased pins should not be left floating.

## ■ Handling of Unused pins

The unused digital I/O pins should be processed appropriately as below.

| Classification | Pin Name                                  | Setting                                                                      |
|----------------|-------------------------------------------|------------------------------------------------------------------------------|
| PORT1          | BICK1, LRCK1, SDTI                        | These pins should be connected to DVSS.                                      |
| PORT2          | MCLK2                                     | This pin should be connected to DVSS.                                        |
|                | BICK2, LRCK2                              | These pins should be connected to DVSS in slave mode or open in master mode. |
|                | SDTIO                                     | This pin should be connected to DVSS.                                        |
|                | M/S2                                      | This pin should be connected to DVDD or DVSS.                                |
| PORT3          | OMCLK                                     | This pin should be connected to DVSS.                                        |
|                | BICK, LRCK                                | These pins should be connected to DVSS in slave mode or open in master mode. |
|                | SDTO                                      | This pin should be open.                                                     |
|                | M/S3                                      | This pin should be connected to DVDD or DVSS.                                |
| DIR            | RX1, RX2, RX3, RX4                        | These pins should be open.                                                   |
|                | INT0, INT1, INT2, TX                      | These pins should be open.                                                   |
| Control PORT   | CCLK, CDTI, CSN                           | These pins should be connected to DVSS.                                      |
|                | CDTO                                      | This pin should be open.                                                     |
| Other          | SMUTE                                     | This pin should be connected to DVSS.                                        |
| TEST           | TST1, TST2, TST11                         | These pins should be open.                                                   |
|                | TST3                                      | This pin should be connected to DVSS.                                        |
|                | TST4, TST5, TST6, TST7, TST8, TST9, TST10 | These pins should be connected to AVSS.                                      |
|                |                                           |                                                                              |
|                |                                           |                                                                              |

**ABSOLUTE MAXIMUM RATINGS**(AVSS=BVSS=DVSS=0V; [Note 1](#))

| Parameter                                   |                                         | Symbol | min  | max      | Units |
|---------------------------------------------|-----------------------------------------|--------|------|----------|-------|
| Power Supplies:                             | Analog                                  | AVDD   | -0.3 | 4.6      | V     |
|                                             | Digital                                 | DVDD   | -0.3 | 4.6      | V     |
|                                             | BVSS – DVSS  ( <a href="#">Note 2</a> ) | ΔGND   | -    | 0.3      | V     |
| Input Current, Any Pin Except Supplies      |                                         | IIN    | -    | ±10      | mA    |
| Digital Input Voltage 1 (Except RX1-4 pins) |                                         | VIND1  | -0.3 | DVDD+0.3 | V     |
| Digital Input Voltage 2 (RX1-4 pins)        |                                         | VIND2  | -0.3 | AVDD+0.3 | V     |
| Ambient Temperature (Power applied)         |                                         | Ta     | -10  | 70       | °C    |
| Storage Temperature                         |                                         | Tstg   | -65  | 150      | °C    |

Note 1. All voltages with respect to ground.

Note 2. AVSS, BVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**(AVSS=BVSS=DVSS=0V; [Note 1](#))

| Parameter                                    |         | Symbol | min | typ | max  | Units |
|----------------------------------------------|---------|--------|-----|-----|------|-------|
| Power Supplies<br>( <a href="#">Note 3</a> ) | Analog  | AVDD   | 3.0 | 3.3 | 3.6  | V     |
|                                              | Digital | DVDD   | 3.0 | 3.3 | AVDD | V     |

Note 1. All voltages with respect to ground.

Note 3. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

**SRC CHARACTERISTICS**

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=BVSS=DVSS=0V; data = 24bit; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

| Parameter                                                 | Symbol  | min  | typ  | max  | Units |
|-----------------------------------------------------------|---------|------|------|------|-------|
| <b>SRC Characteristics:</b>                               |         |      |      |      |       |
| Resolution (Note 4)                                       |         |      |      | 24   | Bits  |
| Input Sample Rate                                         | FSI     | 8    |      | 96   | kHz   |
| Output Sample Rate                                        | FSO     | 32   |      | 96   | kHz   |
| THD+N (Input = 1kHz, 0dBFS, Note 5)                       |         |      |      |      |       |
| FSO/FSI = 44.1kHz/48kHz                                   |         | -    | -113 | -    | dB    |
| FSO/FSI = 48kHz/44.1kHz                                   |         | -    | -113 | -    | dB    |
| FSO/FSI = 32kHz/48kHz                                     |         | -    | -114 | -    | dB    |
| FSO/FSI = 96kHz/32kHz                                     |         | -    | -111 | -    | dB    |
| Worst Case (FSO/FSI = 48kHz/8kHz)                         |         | -    | -    | -103 | dB    |
| Dynamic Range (Input = 1kHz, -60dBFS, Note 5)             |         |      |      |      |       |
| FSO/FSI = 44.1kHz/48kHz                                   |         | -    | 114  | -    | dB    |
| FSO/FSI = 48kHz/44.1kHz                                   |         | -    | 115  | -    | dB    |
| FSO/FSI = 32kHz/48kHz                                     |         | -    | 115  | -    | dB    |
| FSO/FSI = 96kHz/32kHz                                     |         | -    | 116  | -    | dB    |
| Worst Case (FSO/FSI = 32kHz/44.1kHz)                      |         | 112  | -    | -    | dB    |
| Dynamic Range (Input = 1kHz, -60dBFS, A-weighted, Note 5) |         |      |      |      |       |
| FSO/FSI = 44.1kHz/48kHz                                   |         | -    | 117  | -    | dB    |
| Ratio between Input and Output Sample Rate (Note 6)       | FSO/FSI | 0.33 |      | 6    | -     |

Note 4. Input data for SRC corresponds to 24bit data. When LSB 4bit data is input, the AK4122A calculates the data as "0" because SRC is 20bit calculation. Therefore, SRC outputs "0" data.

Note 5. Measured by ROHDE & SCHWARZ UPD04, Rejection Filter = wide, 8192point FFT.

Note 6. The "0.33" is the ratio of FSO/FSI when FSI is 96kHz and FSO is 32kHz. The "6" is the ratio of FSO/FSI when FSI is 8kHz and FSO is 48kHz.

**S/PDIF RECEIVER CHARACTERISTICS**

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

| Parameter              | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|-------|
| Input Resistance       | Zin    | -   | 10  | -   | kΩ    |
| Input Voltage          | VTH    | 200 |     |     | mVpp  |
| Input Sample Frequency | fs     | 32  | -   | 96  | kHz   |



### FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; DEM=OFF)

| Parameter             |                                        | Symbol | min       | typ  | max       | Units |
|-----------------------|----------------------------------------|--------|-----------|------|-----------|-------|
| <b>Digital Filter</b> |                                        |        |           |      |           |       |
| Passband -0.001dB     | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | PB     | 0         |      | 0.4583FSI | kHz   |
|                       | $0.905 \leq \text{FSO/FSI} < 0.985$    | PB     | 0         |      | 0.4167FSI | kHz   |
|                       | $0.714 \leq \text{FSO/FSI} < 0.905$    | PB     | 0         |      | 0.3195FSI | kHz   |
|                       | $0.656 \leq \text{FSO/FSI} < 0.714$    | PB     | 0         |      | 0.2852FSI | kHz   |
|                       | $0.536 \leq \text{FSO/FSI} < 0.656$    | PB     | 0         |      | 0.2245FSI | kHz   |
|                       | $0.492 \leq \text{FSO/FSI} < 0.536$    | PB     | 0         |      | 0.2003FSI | kHz   |
|                       | $0.452 \leq \text{FSO/FSI} < 0.492$    | PB     | 0         |      | 0.1781FSI | kHz   |
|                       | $0.333 \leq \text{FSO/FSI} < 0.452$    | PB     | 0         |      | 0.1092FSI | kHz   |
| Stopband              | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | SB     | 0.5417FSI |      |           | kHz   |
|                       | $0.905 \leq \text{FSO/FSI} < 0.985$    | SB     | 0.5021FSI |      |           | kHz   |
|                       | $0.714 \leq \text{FSO/FSI} < 0.905$    | SB     | 0.3965FSI |      |           | kHz   |
|                       | $0.656 \leq \text{FSO/FSI} < 0.714$    | SB     | 0.3643FSI |      |           | kHz   |
|                       | $0.536 \leq \text{FSO/FSI} < 0.656$    | SB     | 0.2974FSI |      |           | kHz   |
|                       | $0.492 \leq \text{FSO/FSI} < 0.536$    | SB     | 0.2732FSI |      |           | kHz   |
|                       | $0.452 \leq \text{FSO/FSI} < 0.492$    | SB     | 0.2510FSI |      |           | kHz   |
|                       | $0.333 \leq \text{FSO/FSI} < 0.452$    | SB     | 0.1822FSI |      |           | kHz   |
| Passband Ripple       |                                        | PR     |           |      | ±0.01     | dB    |
| Stopband Attenuation  |                                        | SA     | 96        |      |           | dB    |
| Group Delay           | (Note 7)                               | GD     | -         | 58.5 | -         | 1/fs  |

Note 7. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

### DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

| Parameter                 |               | Symbol | min      | typ | max     | Units |
|---------------------------|---------------|--------|----------|-----|---------|-------|
| High-Level Input Voltage  |               | VIH    | 70%DVDD  | -   | -       | V     |
| Low-Level Input Voltage   |               | VIL    | -        | -   | 30%DVDD | V     |
| High-Level Output Voltage | (Iout=-400μA) | VOH    | DVDD-0.4 | -   | -       | V     |
| Low-Level Output Voltage  | (Iout=400μA)  | VOL    | -        | -   | 0.4     | V     |
| Input Leakage Current     |               | Iin    | -        | -   | ±10     | μA    |

| Parameter                                    |  | min | typ | max | Units |
|----------------------------------------------|--|-----|-----|-----|-------|
| Power Supply Current                         |  |     |     |     |       |
| Normal operation (PDN pin = "H") (Note 8)    |  |     |     |     |       |
| FSI=FSO=48kHz at Slave Mode: AVDD=DVDD=3.3V  |  |     | 15  | -   | mA    |
| FSI=FSO=96kHz at Master Mode: AVDD=DVDD=3.3V |  |     | 29  | -   | mA    |
| FSI=FSO=96kHz at Master Mode: AVDD=DVDD=3.6V |  |     | -   | 45  | mA    |
| Power down (PDN pin = "L") (Note 9)          |  |     |     |     |       |
| AVDD+DVDD                                    |  |     | 10  | 100 | μA    |

Note 8. Typ and max values are the value of AVDD+DVDD in each power supply voltage.

Power supply current of each path@Slave Mode, AVDD=DVDD=3.3V, FSI=FSO=48kHz

1. PORT1 → SRC → PORT3: AVDD=5mA(typ), DVDD=10mA(typ)
2. PORT2 → SRC → PORT3: AVDD=5mA(typ), DVDD=10mA(typ)
3. DIR → SRC → PORT3: AVDD=6mA(typ), DVDD=9mA(typ)

Note 9. All digital input pins are held DVSS.

## SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; CL=20pF)

| Parameter                                           | Symbol | min      | typ | max    | Units |
|-----------------------------------------------------|--------|----------|-----|--------|-------|
| <b>Master Clock Timing</b>                          |        |          |     |        |       |
| Frequency                                           | fCLK   | 8.192    |     | 36.864 | MHz   |
| Pulse Width Low                                     | tCLKL  | 0.4/fCLK |     |        | ns    |
| Pulse Width High                                    | tCLKH  | 0.4/fCLK |     |        | ns    |
| <b>LRCK for Input data (LRCK1, LRCK2)</b>           |        |          |     |        |       |
| Frequency                                           | fs     | 8        |     | 96     | kHz   |
| Duty Cycle                                          | Duty   | 48       | 50  | 52     | %     |
| <b>LRCK for Output data (LRCK, LRCK2)</b>           |        |          |     |        |       |
| Frequency (Note 10)                                 | fs     | 32       |     | 96     | kHz   |
| Duty Cycle Slave Mode                               | Duty   | 48       | 50  | 52     | %     |
| Duty Cycle Master Mode                              | Duty   |          | 50  |        | %     |
| <b>S/PDIF Clock Recover Frequency</b>               | fPLL   | 32       |     | 96     | kHz   |
| <b>Audio Interface Timing</b>                       |        |          |     |        |       |
| <b>Input for PORT1</b>                              |        |          |     |        |       |
| BICK1 Period                                        | tBCK   | 1/64fs   |     |        | ns    |
| BICK1 Pulse Width Low                               | tBCKL  | 65       |     |        | ns    |
| Pulse Width High                                    | tBCKH  | 65       |     |        | ns    |
| LRCK1 Edge to BICK1 “↑” (Note 11)                   | tLRB   | 30       |     |        | ns    |
| BICK1 “↑” to LRCK1 Edge (Note 11)                   | tBLR   | 30       |     |        | ns    |
| SDTI Hold Time from BICK1 “↑”                       | tSDH   | 30       |     |        | ns    |
| SDTI Setup Time to BICK1 “↑”                        | tSDS   | 30       |     |        | ns    |
| <b>Input for PORT2 (Slave mode)</b>                 |        |          |     |        |       |
| BICK2 Period                                        | tBCK   | 1/64fs   |     |        | ns    |
| BICK2 Pulse Width Low                               | tBCKL  | 65       |     |        | ns    |
| Pulse Width High                                    | tBCKH  | 65       |     |        | ns    |
| LRCK2 Edge to BICK2 “↑” (Note 11)                   | tLRB   | 30       |     |        | ns    |
| BICK2 “↑” to LRCK2 Edge (Note 11)                   | tBLR   | 30       |     |        | ns    |
| SDTIO Hold Time from BICK2 “↑”                      | tSDH   | 30       |     |        | ns    |
| SDTIO Setup Time to BICK2 “↑”                       | tSDS   | 30       |     |        | ns    |
| <b>Output for PORT2 (Slave mode)</b>                |        |          |     |        |       |
| BICK2 Period                                        | tBCK   | 1/64fs   |     |        | ns    |
| BICK2 Pulse Width Low                               | tBCKL  | 65       |     |        | ns    |
| Pulse Width High                                    | tBCKH  | 65       |     |        | ns    |
| LRCK2 Edge to BICK2 “↑” (Note 11)                   | tLRB   | 30       |     |        | ns    |
| BICK2 “↑” to LRCK2 Edge (Note 11)                   | tBLR   | 30       |     |        | ns    |
| LRCK2 to SDTIO (MSB) (Except I <sup>2</sup> S mode) | tLRS   |          |     | 30     | ns    |
| BICK2 “↓” to SDTIO                                  | tBSD   |          |     | 30     | ns    |

Note 10. Min value is 8kHz at BYPASS mode.

Note 11. BICK1 rising edge must not occur at the same time as LRCK1 edge.

BICK2 rising edge must not occur at the same time as LRCK2 edge.

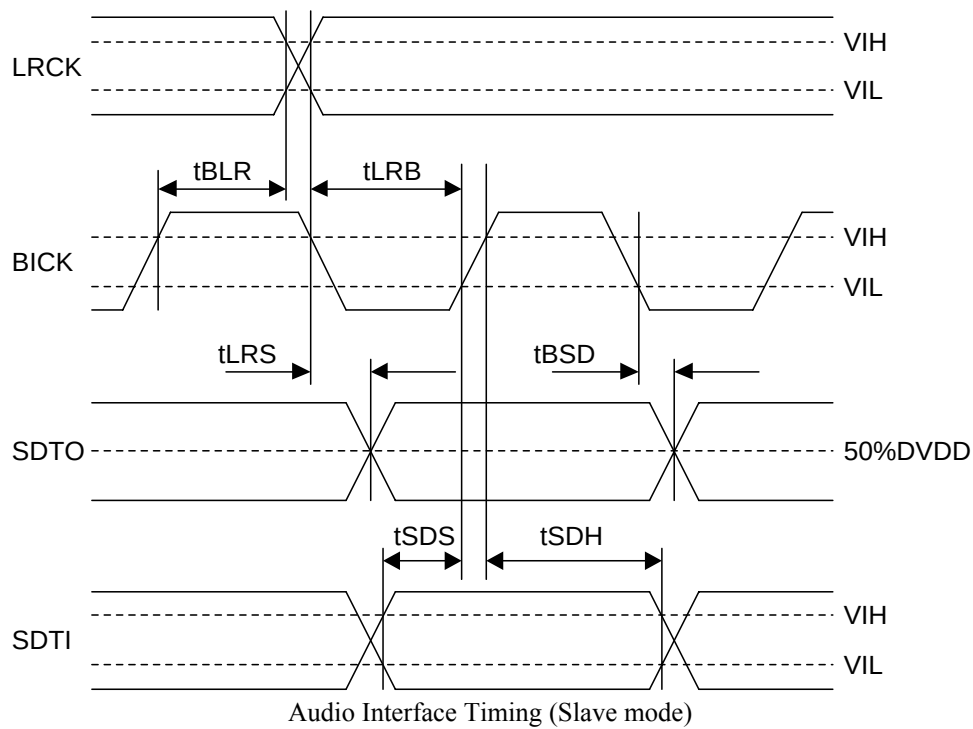
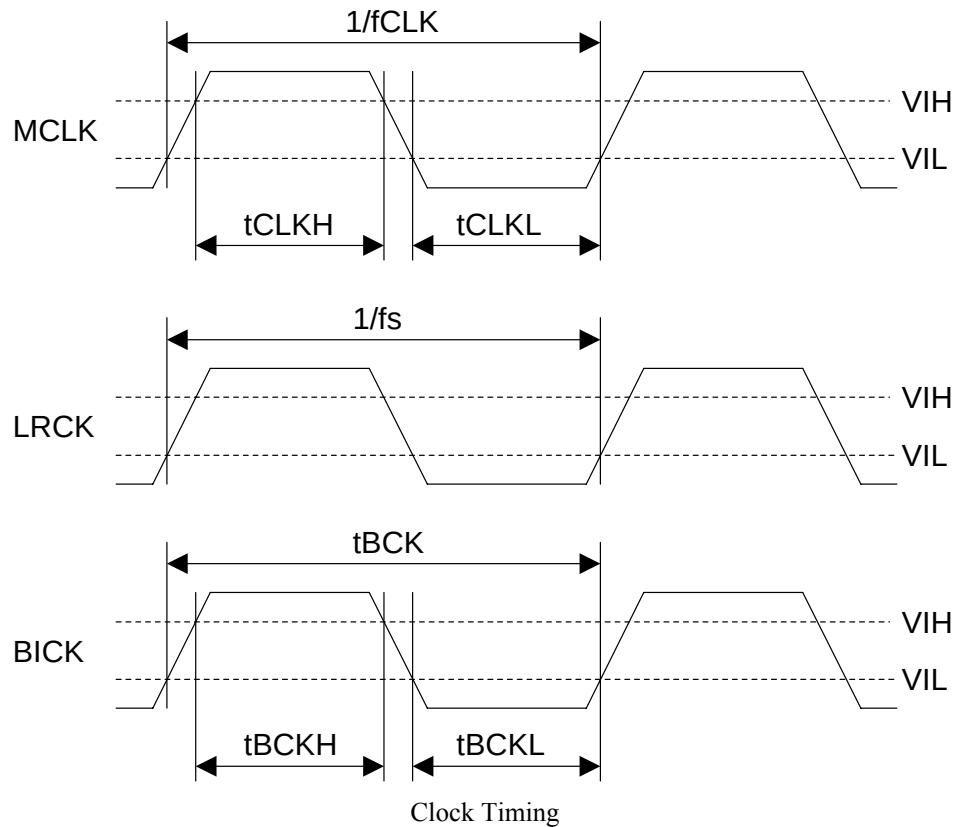
| Parameter                                         | Symbol | min    | typ  | max  | Units |
|---------------------------------------------------|--------|--------|------|------|-------|
| <b>Output for PORT3 (Slave mode)</b>              |        |        |      |      |       |
| BICK Period                                       | tBCK   | 1/64fs |      |      | ns    |
| BICK Pulse Width Low                              | tBCKL  | 65     |      |      | ns    |
| Pulse Width High                                  | tBCKH  | 65     |      |      | ns    |
| LRCK Edge to BICK “↑” (Note 11)                   | tLRB   | 30     |      |      | ns    |
| BICK “↑” to LRCK Edge (Note 11)                   | tBLR   | 30     |      |      | ns    |
| LRCK to SDTO (MSB) (Except I <sup>2</sup> S mode) | tLRS   |        |      | 30   | ns    |
| BICK “↓” to SDTO                                  | tBSD   |        |      | 30   | ns    |
| <b>Output for PORT2 (Master mode)</b>             |        |        |      |      |       |
| BICK2 Frequency                                   | fBCK   |        | 64fs |      | Hz    |
| BICK2 Duty                                        | dBCK   |        | 50   |      | %     |
| BICK2 “↓” to LRCK2                                | tMBLR  | −20    |      | 20   | ns    |
| BICK2 “↓” to SDTIO                                | tBSD   | −20    |      | 30   | ns    |
| <b>Output for PORT3 (Master mode)</b>             |        |        |      |      |       |
| BICK Frequency                                    | fBCK   |        | 64fs |      | Hz    |
| BICK Duty                                         | dBCK   |        | 50   |      | %     |
| BICK “↓” to LRCK                                  | tMBLR  | −20    |      | 20   | ns    |
| BICK “↓” to SDTO                                  | tBSD   | −20    |      | 30   | ns    |
| <b>Control Interface Timing</b>                   |        |        |      |      |       |
| CCLK Period (Note 12)                             | tCCK   | 200    |      | 1000 | ns    |
| CCLK Pulse Width Low                              | tCCKL  | 80     |      |      | ns    |
| Pulse Width High                                  | tCCKH  | 80     |      |      | ns    |
| CDTI Setup Time                                   | tCDS   | 40     |      |      | ns    |
| CDTI Hold Time                                    | tCDH   | 40     |      |      | ns    |
| CSN “H” Time                                      | tCSW   | 150    |      |      | ns    |
| CSN “↓” to CCLK “↑”                               | tCSS   | 50     |      |      | ns    |
| CCLK “↑” to CSN “↑”                               | tCSH   | 50     |      |      | ns    |
| CDTO Delay                                        | tDCD   |        |      | 45   | ns    |
| CSN “↑” to CDTO Hi-Z                              | tCCZ   |        |      | 70   | ns    |
| <b>Reset Timing</b>                               |        |        |      |      |       |
| PDN Pulse Width (Note 13)                         | tPD    | 150    |      |      | ns    |

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

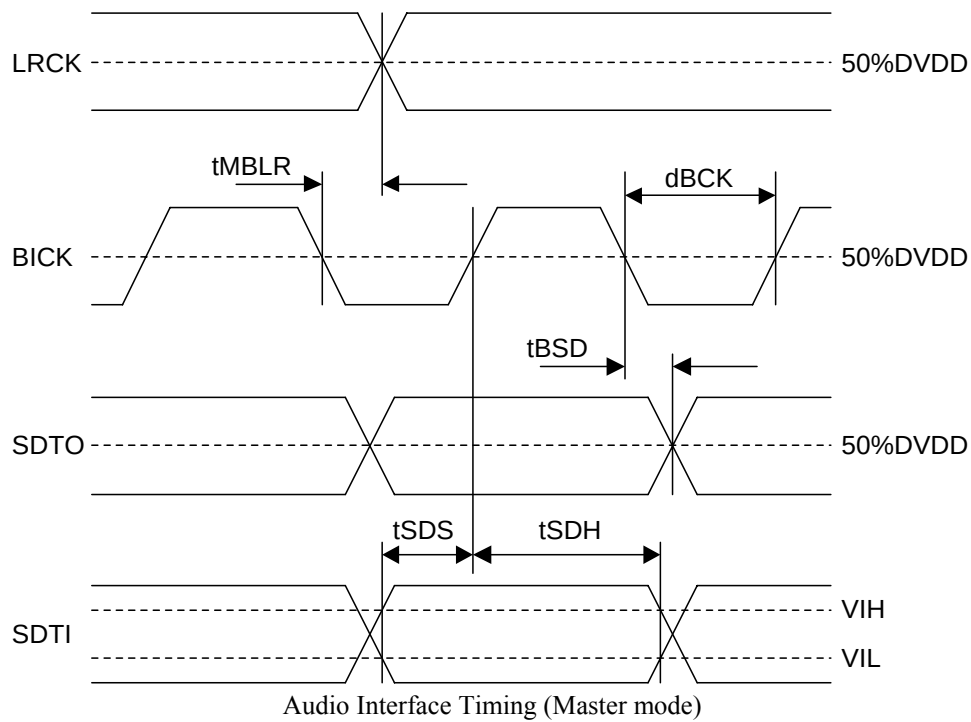
Note 12. In case of using INT2. When INT2 is not used, the max value is not limited.

Note 13. The AK4122A can be reset by bringing the PDN pin = “L”.

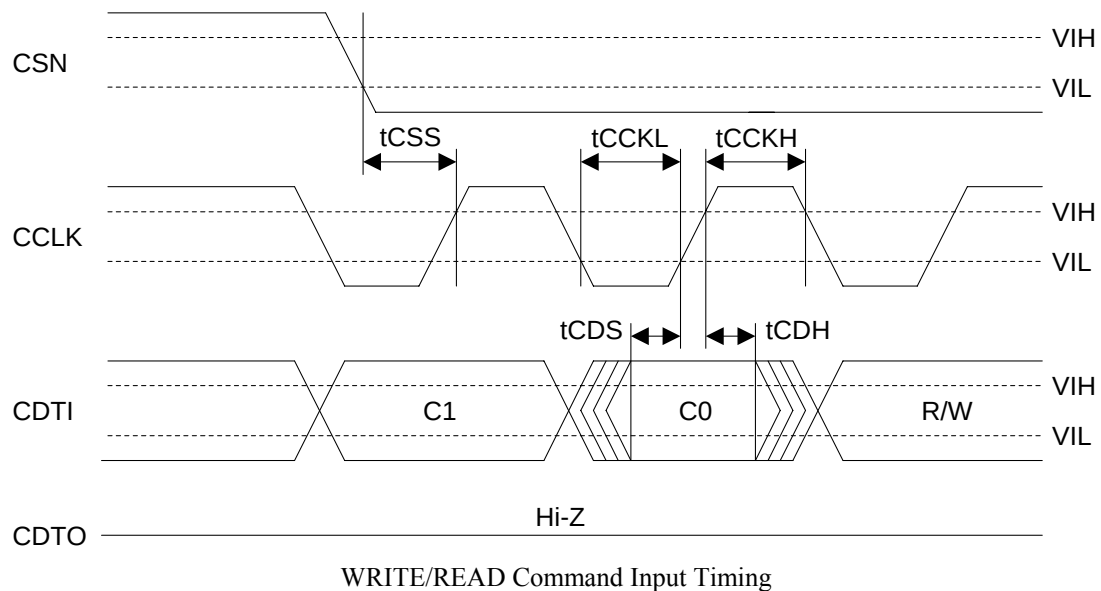
## ■ Timing Diagram

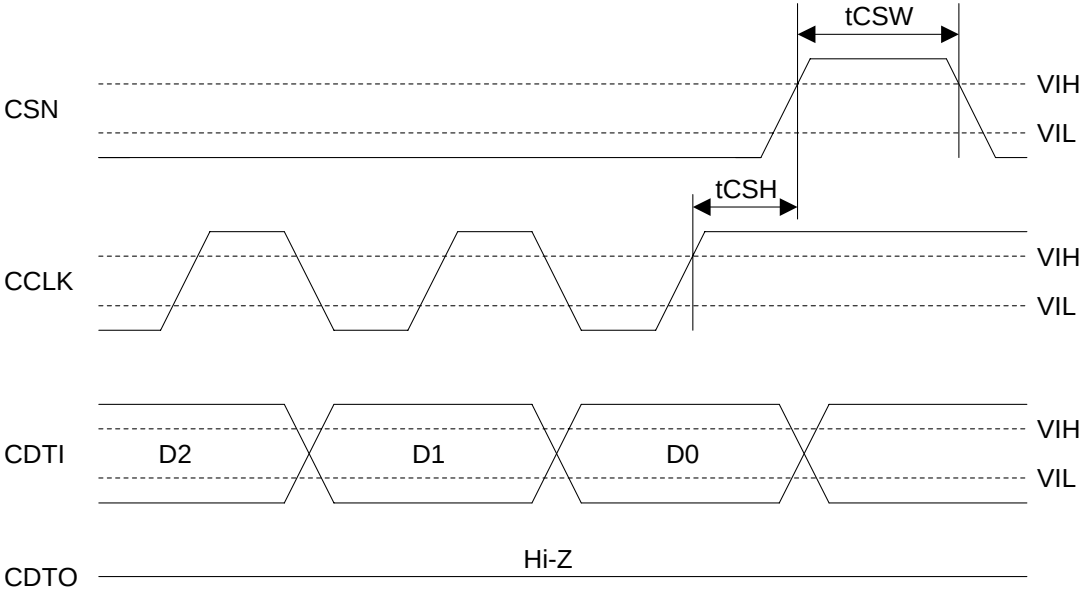


Note : BICK shows BICK1 of PORT1, BICK2 of PORT2 and BICK of PORT3. LRCK shows LRCK1 of PORT1, LRCK2 of PORT2 and LRCK of PORT3. SDTI shows SDTI of PORT1 or SDTIO of PORT2 that is used as input port. SDTO shows SDTO of PORT3 or SDTIO of PORT2 that is used as output port.

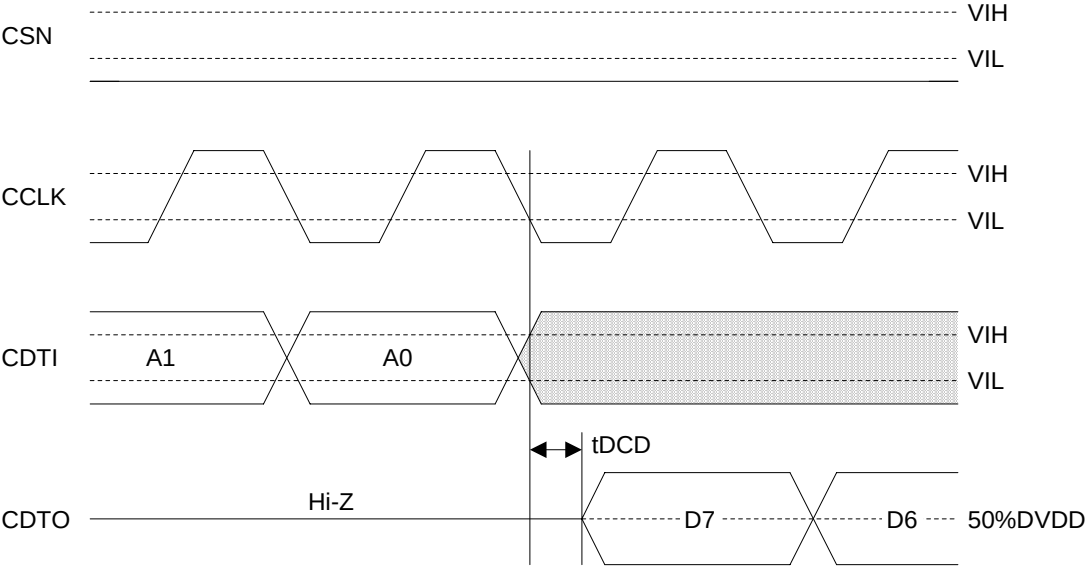


Note : BICK shows BICK1 of PORT1, BICK2 of PORT2 and BICK of PORT3. LRCK shows LRCK1 of PORT1, LRCK2 of PORT2 and LRCK of PORT3. SDTI shows SDTI of PORT1 or SDTIO of PORT2 that is used as input port. SDTO shows SDTO of PORT3 or SDTIO of PORT2 that is used as output port.

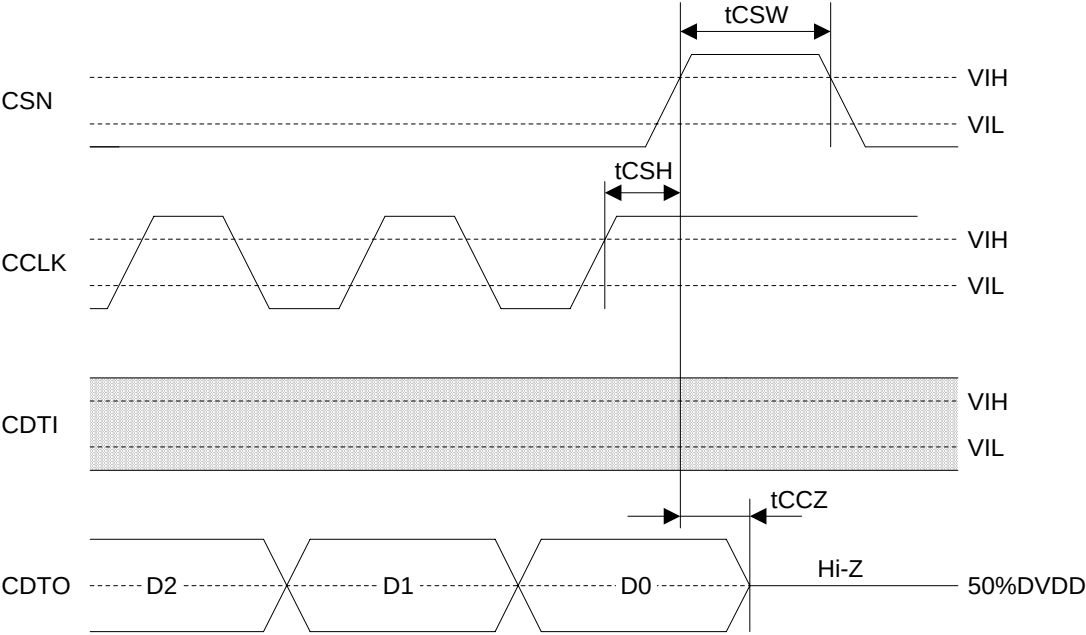




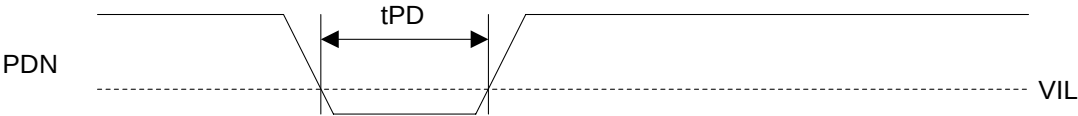
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Output Timing 2



Power Down & Reset Timing

## OPERATION OVERVIEW

### ■ Internal Signal Path

The input source of the SRC can be switched between the outputs of the DIR, PORT1 or PORT2. The input source of the PORT2 and PORT3 can be switched between the outputs of the SRC or BYPASS. When PORT2 is used as an input port, PORT2 cannot be used as an output port. The signal path should be controlled during PWN bit = "0". The Switch Names (ISEL1-0, BYPS and OSEL) in [Figure 1](#) correspond to the register bits that control the switch function. Refer to [Table 1](#).

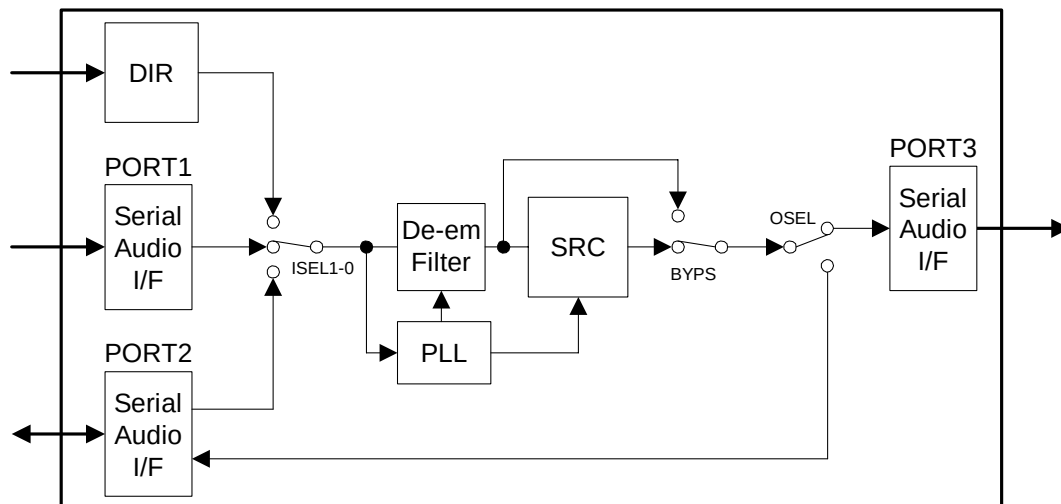


Figure 1. Connection Input Source & Output Source

| Mode | Input PORT  | SRC / Bypass | Output PORT           | Path                |
|------|-------------|--------------|-----------------------|---------------------|
|      | ISEL1-0 bit | BYPS bit     | OSEL bit              |                     |
| 0    | 00: PORT1   | 0: SRC       | 0: PORT3<br>(Note 14) | PORT1 → SRC → PORT3 |
| 1    | 01: PORT2   |              |                       | PORT2 → SRC → PORT3 |
| 2    | 10: DIR     |              |                       | DIR → SRC → PORT3   |
| 3    | 00: PORT1   | 1: Bypass    |                       | PORT1 → PORT3       |
| 4    | 01: PORT2   |              |                       | PORT2 → PORT3       |
| 5    | 10: DIR     |              |                       | DIR → PORT3         |
| 6    | 00: PORT1   | 0: SRC       | 1: PORT2<br>(Note 15) | PORT1 → SRC → PORT2 |
| 7    | 10: DIR     |              |                       | DIR → SRC → PORT2   |
| 8    | 00: PORT1   | 1: Bypass    |                       | PORT1 → PORT2       |
| 9    | 10: DIR     |              |                       | DIR → PORT2         |

Table 1. Path Select

Default is Mode 0. (Path : PORT1 → SRC → PORT3)

After PDN pin = "L" → "H", SDTIO pin of PORT2 is the input pin.

**The DIF1-0 bits of the PORT1 should be set a value except "10" (I<sup>2</sup>S Compatible) when the DIR is selected as an input port.**

Refer to [Table 6](#) and [Table 7](#) for Master/Slave mode setting.



Note 14. In this case, PORT2 is input port. If PORT2 is unused, the digital I/O pins should be processed appropriately as shown in Table 2.

| M/S2 pin | Mode   | Unused pin | Pin I/O | Setting                               |
|----------|--------|------------|---------|---------------------------------------|
| L        | Slave  | MCLK2      | I       | This pin should be connected to DVSS. |
|          |        | BICK2      | I       | This pin should be connected to DVSS. |
|          |        | LRCK2      | I       | This pin should be connected to DVSS. |
|          |        | SDTIO      | I       | This pin should be connected to DVSS. |
| H        | Master | MCLK2      | I       | This pin should be connected to DVSS. |
|          |        | BICK2      | O       | This pin should be open.              |
|          |        | LRCK2      | O       | This pin should be open.              |
|          |        | SDTIO      | I       | This pin should be connected to DVSS. |

Table 2. Pin Setting for PORT2

Note 15. In this case, PORT3 is output port. If PORT3 is unused, the digital I/O pins should be processed appropriately as shown in Table 3.

| M/S3 pin | Mode   | Unused pin | Pin I/O | Setting                               |
|----------|--------|------------|---------|---------------------------------------|
| L        | Slave  | OMCLK      | I       | This pin should be connected to DVSS. |
|          |        | BICK       | I       | This pin should be connected to DVSS. |
|          |        | LRCK       | I       | This pin should be connected to DVSS. |
|          |        | SDTO       | O       | This pin should be open.              |
| H        | Master | OMCLK      | I       | This pin should be connected to DVSS. |
|          |        | BICK       | O       | This pin should be open.              |
|          |        | LRCK       | O       | This pin should be open.              |
|          |        | SDTO       | O       | This pin should be open.              |

Table 3. Pin Setting for PORT3

## ■ System Clock

PORT1 can be operated in slave mode only. PORT2 and PORT3 work in master mode and slave mode. Internal system clock is created by internal PLL using LRCK1, LRCK2 or LRCK of DIR. The MCLK is not needed when PORT2 and PORT3 are in slave mode. Set the MCLK2 pin and OMCLK pin to DVSS. When PORT2 and PORT3 are used in master mode, the MCLK2 pin and OMCLK pin should be supplied MCLK. The M/S2 pin and M/S3 pin control master and slave mode switching. Table 4 and Table 5 show setting of MCLK frequency when PORT2 and PORT3 are master mode. In case of detecting the sampling frequency by MCLK when DIR is used, MCLK (MCLK2 or OMCLK) of selected output port (PORT2 or PORT3) should be input.

| ICKS1 | ICKS0 | MCLK2                                     |                                        |
|-------|-------|-------------------------------------------|----------------------------------------|
|       |       | $32\text{kHz} \leq f_s \leq 48\text{kHz}$ | $48\text{kHz} < f_s \leq 96\text{kHz}$ |
| 0     | 0     | 256fs                                     | 256fs                                  |
| 0     | 1     | 384fs                                     | 384fs                                  |
| 1     | 0     | 512fs                                     | N/A                                    |
| 1     | 1     | 768fs                                     | N/A                                    |

(default)

Table 4. MCLK2 frequency select for Master mode

| OCKS1 | OCKS0 | OMCLK                                     |                                        |
|-------|-------|-------------------------------------------|----------------------------------------|
|       |       | $32\text{kHz} \leq f_s \leq 48\text{kHz}$ | $48\text{kHz} < f_s \leq 96\text{kHz}$ |
| 0     | 0     | 256fs                                     | 256fs                                  |
| 0     | 1     | 384fs                                     | 384fs                                  |
| 1     | 0     | 512fs                                     | N/A                                    |
| 1     | 1     | 768fs                                     | N/A                                    |

(default)

Table 5. OMCLK frequency select for Master mode

## ■ Master Mode and Slave Mode

When PORT2 and PORT3 are used as output port, the M/S2 pin and M/S3 pin select either master or slave mode for each port. “H” is for master mode, and “L” is for slave mode. MCLK should be supplied to the port which is in master mode, and the AK4122A outputs BICK and LRCK. BICK and LRCK should be supplied externally to the port which is in slave mode, and MCLK is not needed from this ports. When PORT2 is used as an input port, the M/S2 pin should be set “H” or “L”.

| M/S2 pin | BYPS bit | Data I/O | Mode           | BICK, LRCK |
|----------|----------|----------|----------------|------------|
| L        | 0        | I/O      | Slave, SRC     | Input      |
| L        | 1        | Input    | Slave, Bypass  |            |
|          |          | Output   | Not Available  |            |
| H        | 0        | I/O      | Master, SRC    | Output     |
| H        | 1        | I/O      | Master, Bypass |            |

Table 6. Master mode/Slave mode for PORT2

| M/S3 pin | BYPS bit | Data I/O | Mode           | BICK, LRCK |
|----------|----------|----------|----------------|------------|
| L        | 0        | Output   | Slave, SRC     | Input      |
| L        | 1        | Output   | Not Available  |            |
| H        | 0        | Output   | Master, SRC    | Output     |
| H        | 1        | Output   | Master, Bypass |            |

Table 7. Master mode/Slave mode for PORT3

## ■ Audio Interface Format

The audio interface should be controlled during PWN bit = “0”. When in BYPASS mode, BICK1, BICK2 and BICK are fixed to 64fs.

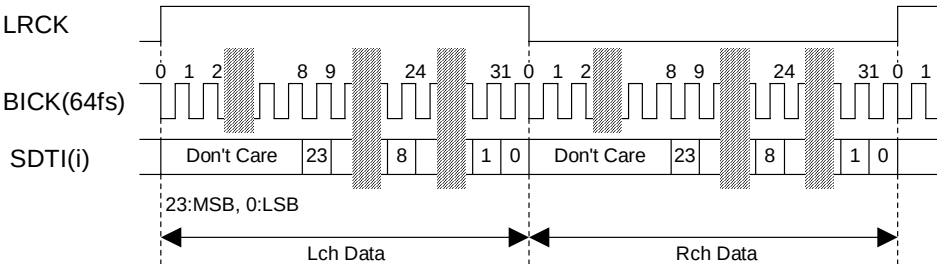
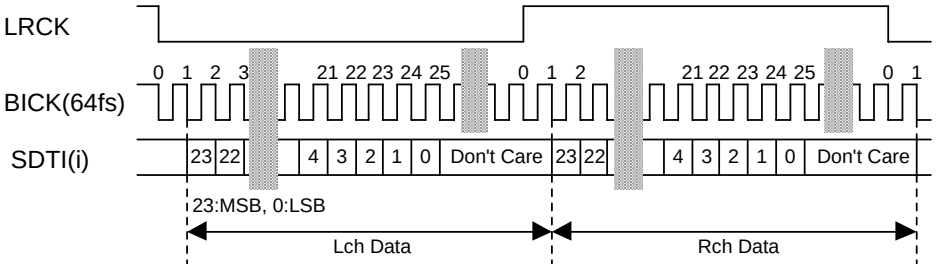
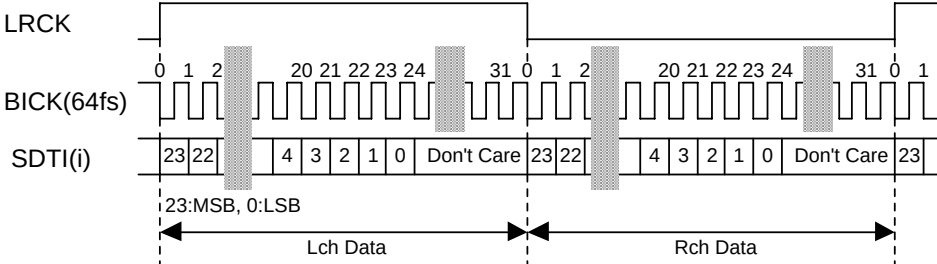
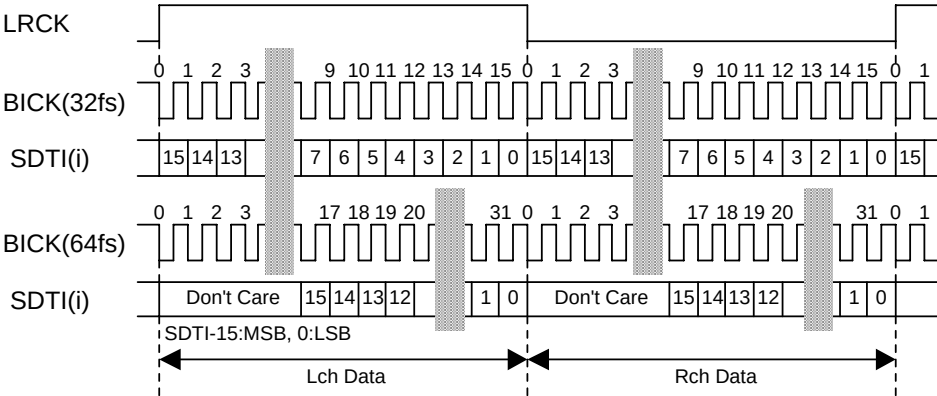
### (1) PORT1

Four types of data formats are available and are selected by setting the DIF1-0 bits. (Table 8) In all modes, the serial data is in MSB first, 2’s compliment format. The SDTI is latched on the rising edge of BICK1. PORT1 corresponds to slave mode only.

| Mode | DIF1 | DIF0 | Input Format                       | LRCK | BICK               |           |
|------|------|------|------------------------------------|------|--------------------|-----------|
| 0    | 0    | 0    | 16bit, LSB justified               | H/L  | $\geq 32\text{fs}$ | (default) |
| 1    | 0    | 1    | 24bit, MSB justified               | H/L  | $\geq 48\text{fs}$ |           |
| 2    | 1    | 0    | 24bit, I <sup>2</sup> S Compatible | L/H  | $\geq 48\text{fs}$ |           |
| 3    | 1    | 1    | 24bit, LSB justified               | H/L  | $\geq 48\text{fs}$ |           |

Table 8. Audio Interface Format for PORT1

**Note: The DIF1-0 bits of the PORT1 must not be set “10” (I<sup>2</sup>S Compatible) when the DIR is selected as an input port.**



## (2) PORT2

Four kinds of data formats are available and are selected by setting IDIF1-0 bits (Table 9). In all modes, the serial data is in MSB first, 2's complement format. If PORT2 is selected as an output port, the SDTIO is clocked out on the falling edge of BICK2, and if PORT2 is selected as an input port, the SDTIO is latched on the rising edge of BICK2. The audio interface supports both master and slave modes. In master mode, BICK2 output is fixed to 64fs and the LRCK2 output fixed to 1fs.

| Mode | IDIF1 | IDIF0 | Output Format                      | Input Format                       | LRCK | BICK        |
|------|-------|-------|------------------------------------|------------------------------------|------|-------------|
| 0    | 0     | 0     | 24bit, MSB justified               | 16bit, LSB justified               | H/L  | $\geq 32fs$ |
| 1    | 0     | 1     | 24bit, MSB justified               | 24bit, MSB justified               | H/L  | $\geq 48fs$ |
| 2    | 1     | 0     | 24bit, I <sup>2</sup> S Compatible | 24bit, I <sup>2</sup> S Compatible | L/H  | $\geq 48fs$ |
| 3    | 1     | 1     | 24bit, MSB justified               | 24bit, LSB justified               | H/L  | $\geq 48fs$ |

Table 9. Audio Interface Format for PORT2

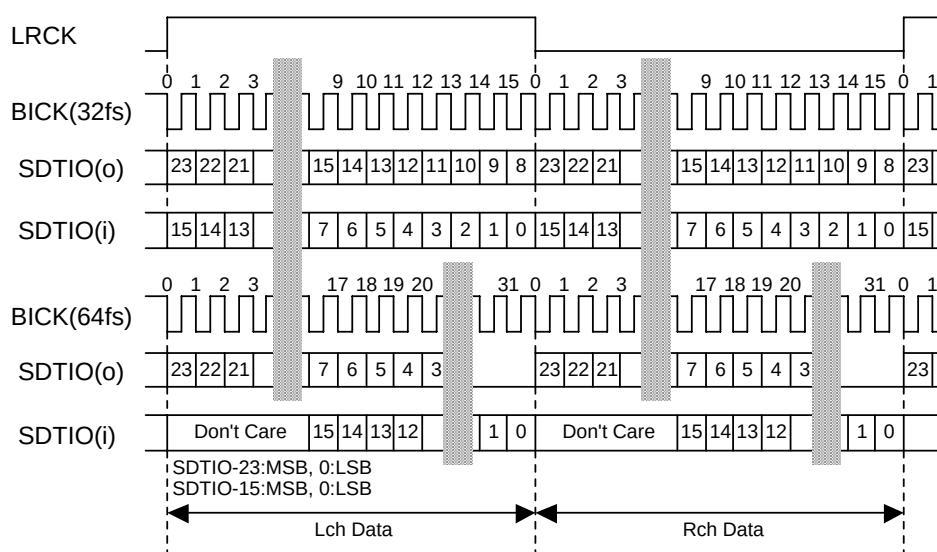


Figure 6. Mode 0 Timing

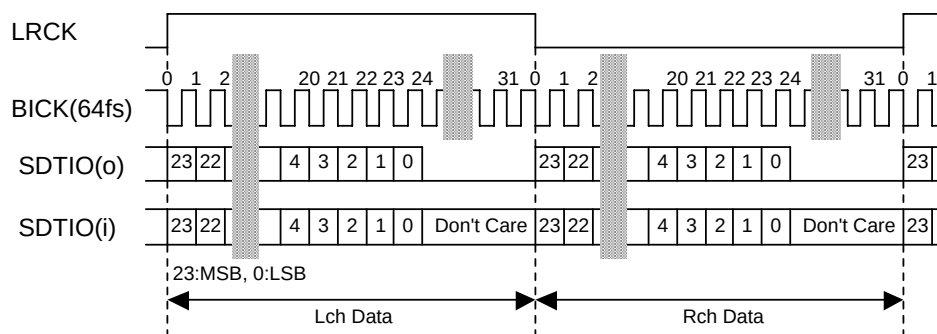


Figure 7. Mode 1 Timing

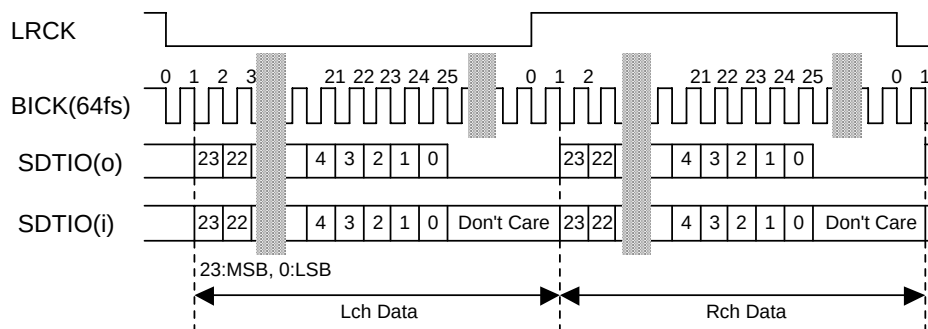


Figure 8. Mode 2 Timing

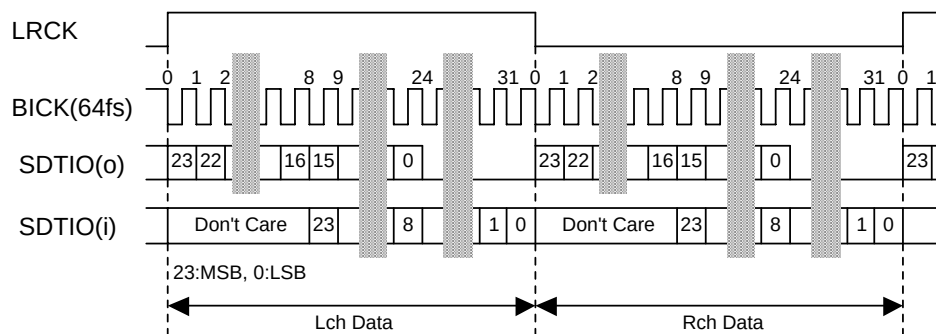


Figure 9. Mode 3 Timing

## (3) PORT3

Two kinds of data formats are available and are selected by setting the ODIF bit (Table 10). In both modes, the serial data is in MSB first, 2's complement format. The SDTO is clocked out on the falling edge of BICK. The audio interface supports both master and slave modes. In master mode, BICK output is fixed to 64fs and LRCK output is fixed to 1fs.

| Mode | ODIF | Output Format                      | LRCK | BICK               | (default) |
|------|------|------------------------------------|------|--------------------|-----------|
| 0    | 0    | 24bit, MSB justified               | H/L  | $\geq 48\text{fs}$ |           |
| 1    | 1    | 24bit, I <sup>2</sup> S Compatible | L/H  | $\geq 48\text{fs}$ |           |

Table 10. Audio Interface Format for PORT3

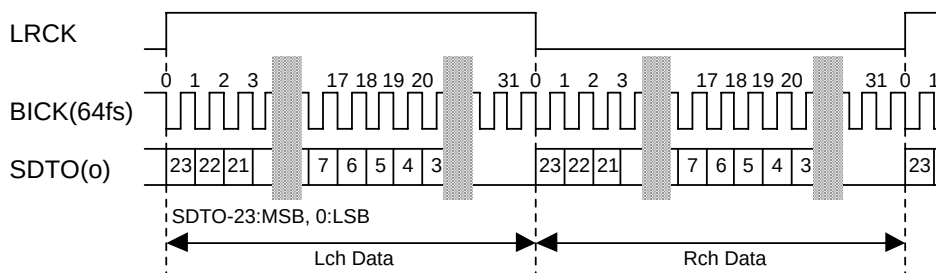


Figure 10. Mode 0 Timing

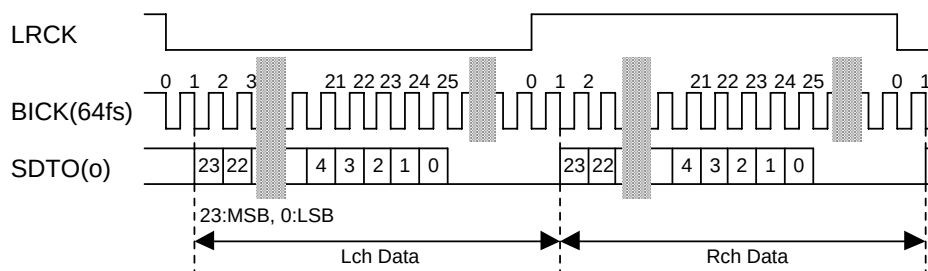


Figure 11. Mode 1 Timing

## ■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the SRC output. Soft mute can be controlled by SMUTE bit or SMUTE pin. The SMUTE bit setting is logically ORed with the SMUTE pin setting. When SMUTE bit goes “1” or SMUTE pin goes “H”, the SRC output data is attenuated by  $-\infty$  within 1024 LRCK cycles. When the SMUTE bit returned “0” and SMUTE pin goes “L” the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled before mute state, the attenuation is discontinued and returned to 0dB in the same cycles. The soft mute is effective for changing the signal source without stopping the signal transmission.

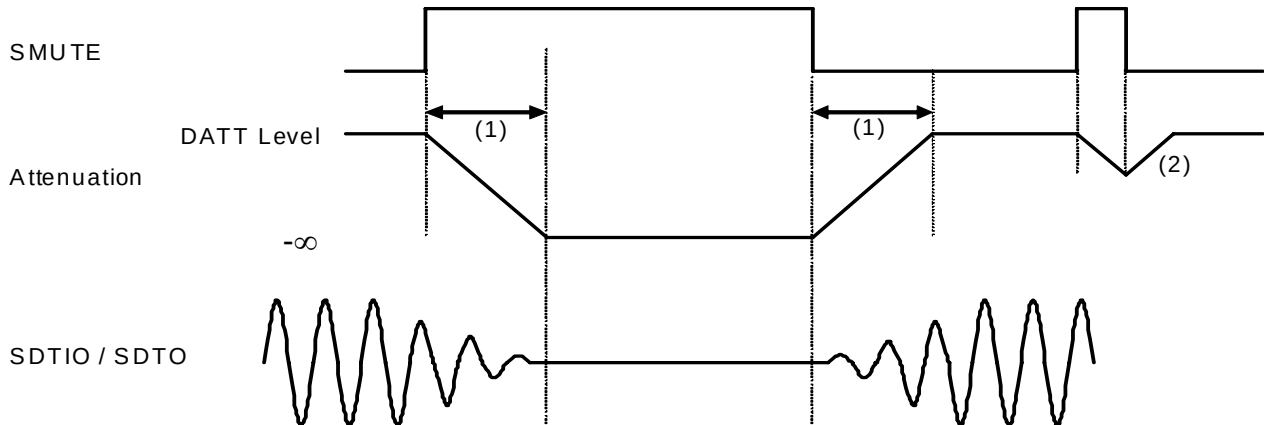


Figure 12. Soft Mute Function

- (1) The output data is attenuated by  $-\infty$  during 1024 LRCK cycles (1024/fs).
- (2) If the soft mute is cancelled before attenuating to  $-\infty$ , the attenuation is discontinued and returned to 0dB in the same clock cycles.

## ■ De-emphasis Filter Control

The AK4122A includes a digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz).

### (1) When input port is DIR

When the input port is DIR and DEAU bit = "1", the de-emphasis filter is enabled automatically by sampling frequency (FS3-0 bit) and pre-emphasis information in the channel status. DEM1-0 bits can control the de-emphasis filter when DEAU bit = "0". When the de-emphasis filter is OFF, the internal de-emphasis filter is bypassed. When PEM bit = "0", the internal de-emphasis filter is always bypassed.

| PEM | FS3      | FS2 | FS1 | FS0 | Mode    |
|-----|----------|-----|-----|-----|---------|
| 1   | 0        | 0   | 0   | 0   | 44.1kHz |
| 1   | 0        | 0   | 1   | 0   | 48kHz   |
| 1   | 0        | 0   | 1   | 1   | 32kHz   |
| 1   | (Others) |     |     |     | OFF     |
| 0   | x        | x   | x   | x   | OFF     |

Table 11. De-emphasis Auto Control (DEAU bit = "1")

| PEM | DEM1 | DEM0 | Mode    |
|-----|------|------|---------|
| 1   | 0    | 0    | 44.1kHz |
| 1   | 0    | 1    | OFF     |
| 1   | 1    | 0    | 48kHz   |
| 1   | 1    | 1    | 32kHz   |

(default)

Table 12. De-emphasis Manual Control (DEAU bit = "0")

### (2) When input port is PORT1 or PORT2

When PORT1 or PORT2 is selected as an input port, DEM1-0 bits can control the de-emphasis filter regardless of the DEAU bit setting. In this case, the de-emphasis filter can not be enabled automatically. When the de-emphasis setting is OFF, the internal de-emphasis filter is bypassed.

| DEM1 | DEM0 | Mode    |
|------|------|---------|
| 0    | 0    | 44.1kHz |
| 0    | 1    | OFF     |
| 1    | 0    | 48kHz   |
| 1    | 1    | 32kHz   |

(default)

Table 13. De-emphasis Manual Control

## ■ System Reset and Power-Down

The AK4122A has a full power-down mode for all circuits that is activated by the PDN pin, and a partial power-down mode activated by the PWN bit. The AK4122A should be reset once at power-up by bringing the PDN pin = "L".

### PDN pin:

All analog and digital circuits are placed in power-down and reset modes by bringing the PDN pin = "L". All the registers are initialized and clocks are stopped. Read/Write operations to the registers are disabled.

### PWN bit (Address 00H; D0):

Unlike the PDN pin operation described above, internal registers and mode settings are not initialized. Read/Write operations to the registers are enabled.

## ■ System Reset

Bringing the PDN pin = “L” sets the AK4122A in power-down mode and initializes digital filters. When the PDN pin = “L”, the SDTO output is “L”. The AK4122A should be reset once by bringing the PDN pin = “L” upon power-up. The SDTO becomes valid in less than 100ms from the rising edge of PDN after a reset release by clock supply. Until the SDTO becomes valid, it outputs “L”. After the rising of PDN pin, the SDTIO pin is an input pin.

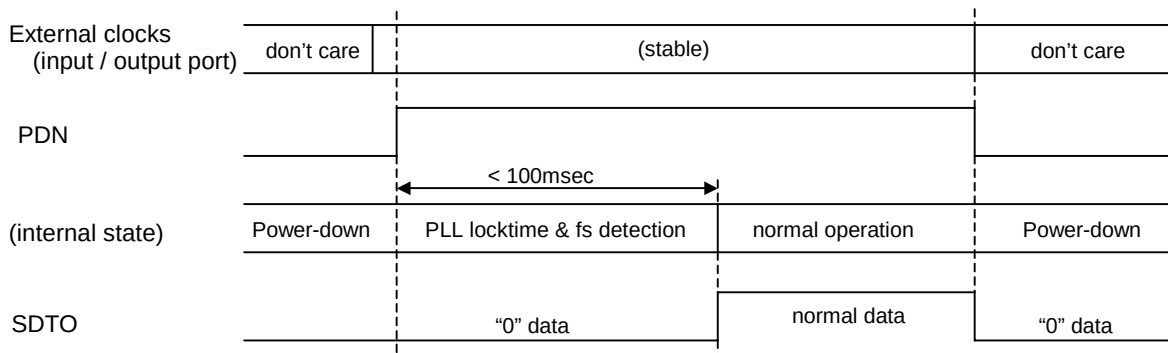


Figure 13. System Reset

## ■ Sequence of Changing Clocks

A clock change sequence is shown in Figure 14. An internal reset is executed when the input or the output clocks are changed. The SDTO data is placed “0” during the reset. Within 100ms, the SDTO outputs normal data after the reset. When the frequency transition occurs gradually without phase change or when the output clock is changed while  $f_{so}/f_{si} > 4$ , the output data may have large distortion for several seconds. A reset should be made by bringing the PDN pin = “L” or PWN bit = “0” to obtain normal data within 100ms when clocks are changed.

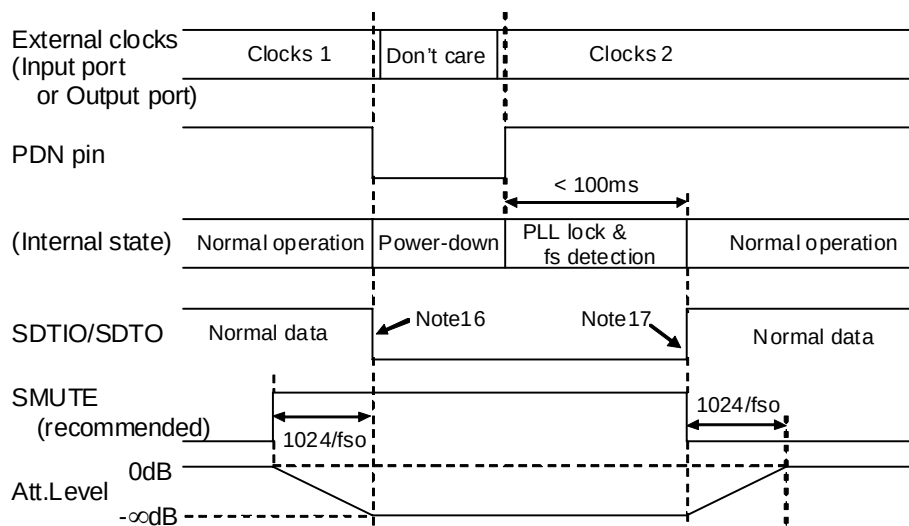


Figure 14. Sequence of Changing Clocks

Note 16. The data on SDTO may cause a clicking noise. To prevent this, set SDTI or SDTIO to “0” from GD before the PDN pin changes to “L”, which will cause the data on SDTO to remain “0”. SMUTE can also remove this clicking noise.

Note 17. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to “0” for  $1024/f_{so} + 100\text{ms}$  or more from the timing when the PDN pin changes to “H” while the SMUTE pin = “H”.

Note 18. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to “0” for  $1024/f_{so} + 100\text{ms}$  or more from the timing when the PDN pin changes to “H” while the SMUTE pin = “H”.



## ■ 96kHz Clock Recovery

An integrated low jitter PLL of the DIR has a wide lock range of 32kHz to 96kHz and its lock time is less than 20ms. The AK4122A has a sampling frequency detect function (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz) that uses either clock comparison against the MCLK2 or OMCLK frequency or the channel status information. The PLL loses synchronization when receiving preambles in incorrect interval.

## ■ Biphase Input

Four inputs (RX1-4) are available for DIR. Each input includes an amplifier for unbalance loads that can accept 200mVpp or greater signal. The IPS1-0 bits select the receiver channel ([Table 14](#)).

| IPS1 | IPS0 | Input Data | (default) |
|------|------|------------|-----------|
| 0    | 0    | RX1        |           |
| 0    | 1    | RX2        |           |
| 1    | 0    | RX3        |           |
| 1    | 1    | RX4        |           |

Table 14. Recovery Data Select

## ■ Biphase Output

The AK4122A can output through data from the digital receiver inputs (RX1-4) to the TX pin. The OPS1-0 bits can select the source of the TX pin output. TX output can be stopped by TXE bit. The AK4122A does not have a TX output buffer (Line Driver), therefore the TX pin cannot drive the 75Ω coaxial cable directly.

| OPS1 | OPS0 | Output Data | (default) |
|------|------|-------------|-----------|
| 0    | 0    | RX1         |           |
| 0    | 1    | RX2         |           |
| 1    | 0    | RX3         |           |
| 1    | 1    | RX4         |           |

Table 15. Output Data Select for TX

## ■ Biphase Signal Input Circuit

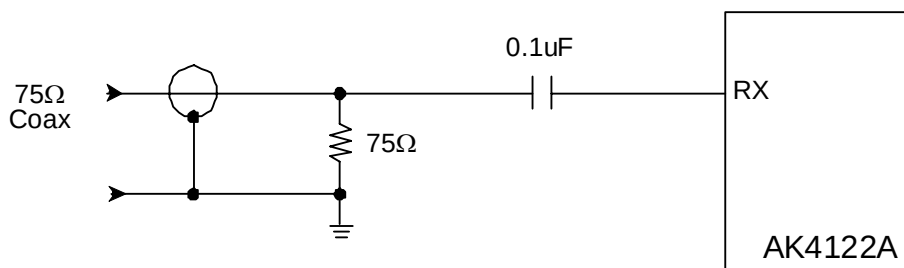


Figure 15. Consumer Input Circuit (Coaxial Input)

Note 19. Coaxial input only : if a coupling level to this input by the next RX input line pattern exceeds 50mV, an malfunction may occur. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

Note 20. Ground of the RCA connector and terminator should be connected to AVSS of the AK4122A with low impedance on PC board.

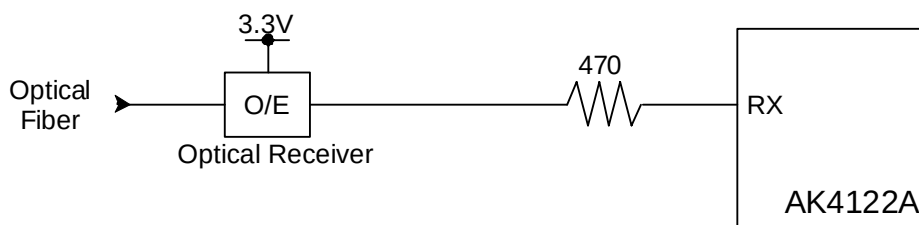


Figure 16. Consumer Input Circuit (Optical Input, Using 3.3V Optical Receiver)

When using coaxial input, the input level of the RX line is small. Care must be taken to reduce, crosstalk among RX input lines by inserting a shield pattern between them.

## ■ Sampling Frequency and Pre-emphasis Detection for DIR

The AK4122A has two methods for detecting sampling frequency for DIR. The sampling frequency is detected by comparing the recovered clock to the MCLK2 or OMCLK frequency, and the detected frequency is reported on FS3-0 bits. XTL1-0 bits, ICKS1-0 bits and OCKS1-0 bits must be set according to the FSO and MCLK frequencies for the detection. (Table 16) When XTL1-0 bits = “11”, the sampling frequency is detected by the channel status sampling frequency information. The detected frequency is reported on FS3-0 bits. The default values of FS3-0 bits are “0001”. In case of detecting the sampling frequency by MCLK when DIR is used, MCLK (MCLK2 or OMCLK) of selected output port (PORT2 or PORT3) should be input.

| FSO     | XTL1 | XTL0 | MCLK2 or OMCLK |               | MCLK Frequency     |
|---------|------|------|----------------|---------------|--------------------|
|         |      |      | ICKS1 / OCKS1  | ICKS0 / OCKS0 |                    |
| 44.1kHz | 0    | 0    | 0              | 0             | 11.2896MHz         |
|         |      |      | 0              | 1             | 16.9344MHz         |
|         |      |      | 1              | 0             | 22.5792MHz         |
|         |      |      | 1              | 1             | 33.8688MHz         |
| 48kHz   | 0    | 1    | 0              | 0             | 12.288MHz          |
|         |      |      | 0              | 1             | 18.432MHz          |
|         |      |      | 1              | 0             | 24.576MHz          |
|         |      |      | 1              | 1             | 36.864MHz          |
| 96kHz   | 1    | 0    | 0              | 0             | 24.576MHz          |
|         |      |      | 0              | 1             | 36.864MHz          |
|         |      |      | 1              | 0             | N/A                |
|         |      |      | 1              | 1             | N/A                |
| -       | 1    | 1    | -              | -             | Use channel status |

(default)

Table 16. Reference MCLK Frequency

| Register Output |     |     |     | fs       | Except XTL1-0 bit = “11”      | XTL1-0 bit = “11”          |                   |                     |
|-----------------|-----|-----|-----|----------|-------------------------------|----------------------------|-------------------|---------------------|
|                 |     |     |     |          | Clock comparison<br>(Note 21) | Consumer Mode<br>(Note 22) | Professional Mode |                     |
| FS3             | FS2 | FS1 | FS0 |          |                               | Byte3<br>Bit3,2,1,0        | Byte0<br>Bit7,6   | Byte4<br>Bit6,5,4,3 |
| 0               | 0   | 0   | 0   | 44.1kHz  | ± 3%                          | 0000                       | 01                | 0000                |
| 0               | 0   | 0   | 1   | Reserved | -                             | 0001                       | (others)          | 0000                |
| 0               | 0   | 1   | 0   | 48kHz    | ± 3%                          | 0010                       | 10                | 0000                |
| 0               | 0   | 1   | 1   | 32kHz    | ± 3%                          | 0011                       | 11                | 0000                |
| 1               | 0   | 0   | 0   | 88.2kHz  | ± 3%                          | (1000)                     | 00                | 1010                |
| 1               | 0   | 1   | 0   | 96kHz    | ± 3%                          | (1010)                     | 00                | 0010                |

Table 17. fs Information

Note 21. Frequencies in a range of ± 3% are identified as shown in the Table 17. Intermediate frequencies between these frequencies shown in Table 17 are identified as nearer value and are shown on FS3-0 bits. FS3-0 bits indicate “1100”, “1110” or “0001” for the frequencies beyond the range of 32~ 96kHz.

Note 22. In consumer mode, Byte3 Bit3-0 are copied to FS3-0.

The pre-emphasis information is detected and reported on the PEM bit. This information is extracted from channel 1 by default (CS12 bit = “0”). It can be switched to channel 2 by changing the CS12 bit in the control register.

| PEM bit | Pre-emphasis | Consumer mode     | Professional mode |
|---------|--------------|-------------------|-------------------|
|         |              | Byte0<br>Bit3,4,5 | Byte0<br>Bit2,3,4 |
| 0       | OFF          | ≠ 0X100           | ≠ 100             |
| 1       | ON           | 0X100             | 100               |

Table 18. PEM Information

## ■ Interrupt Handling for DIR

Following nine events cause that the INT2-0 pins go to “H”.

1. UNLCK: PLL unlock state detection  
UNLCK bit = “1” when the PLL loses lock. The AK4122A loses synchronization when the interval of two preambles is not correct or when those preambles are not correct.
2. PAR: Parity error or biphase coding error detection  
PAR bit = “1” when parity error or biphase coding error is detected. It is updated every sub-frame cycle.
3. AUTO: Non-PCM or DTS-CD Bit Stream detection  
The ORed result of NPCM and DTSCD bits is output to the AUTO bit.
4. V: Validity flag detection  
V bit = “1” when validity flag is detected. It is updated every sub-frame cycle.
5. AUDN: Non-audio detection  
AUDN bit = “1” when the recovered channel status indicates “1”. It is updated every block cycle.
6. STC: Sampling frequency or pre-emphasis information change detection  
STC bit = “1” when FS3-0 or PEM bit is changed. Reading 07H register resets it.
7. CINT: Channel status sync flag  
CINT bit = “1” when received C bits differ from old ones, and stays “1” until this register is read. Updated every block cycle. Reading 07H register resets it.
8. QINT: U bit (Q-subcode) sync flag  
QINT bit = “1” when the Q-subcode differs from old one, and stays “1” until this register is read. Updated every sync code cycle for Q-subcode. Reading 07H register resets it.
9. DAT: DAT Start ID detection  
When the category code shows DAT, this bit becomes “1” if the Start ID of DAT is detected as “1”. Reading 08H register resets it.

INT1-0 pins output an OR’ed signal based on the above nine interrupt events. When these registers are masked, the interrupt event does not affect the operation of the INT1-0 pins (the masks do not affect the registers (UNLCK, PAR, etc.) themselves). Once INT0 pin goes to “H”, it maintains “H” for 1024 cycles (this value can be changed by the EFH1-0 bits) after all events which is not masked by mask bits are cleared. The INT1 pin immediately returns to “L” when those events are cleared.

The INT2 pin outputs “H” by detecting a status change of events 1~5 and ORed results of the events 6~9. It stays “H” until 07H and 08H registers are read. Mask bits are shared with INT0.

UNLCK, PAR, AUTO, V and AUDN bits indicate the interrupt status events above in real time. STC, QINT and CINT bits at address 07H and DAT bit at 08H are changed to “1” by these events. Once STC, QINT or CINT and DAT bit goes to “1”, it stays “1” until the register is read (07H, 08H (DAT bit)).

When the AK4122A loses lock, the channel status bits are initialized. In this initial state, the INT0 and INT2 pins output an OR’ed signal between UNLCK and PAR bits. The INT1 pin outputs an OR’ed signal between AUTO, V and AUDN. INT2-0 pins are “L” when the DIR is not selected.

When DIR is used as input port and the PLL loses lock (unlock state), the output data is muted automatically. When AMUTE bit = “1”, SDTIO and SDTO are muted automatically when the AK4122A detects unlock, Non-Audio or Non-PCM/DTS-CD. After the interrupt events are cleared, mute is cancelled automatically. When AMUTE bit = “0”, SDTIO and SDTO outputs “L” when the PLL loses lock (unlock state), and outputs “H” when other errors (PAR, AUTO and etc.) are occurred.

## (1) UNLCK, PAR, AUTO, V and AUDN bits

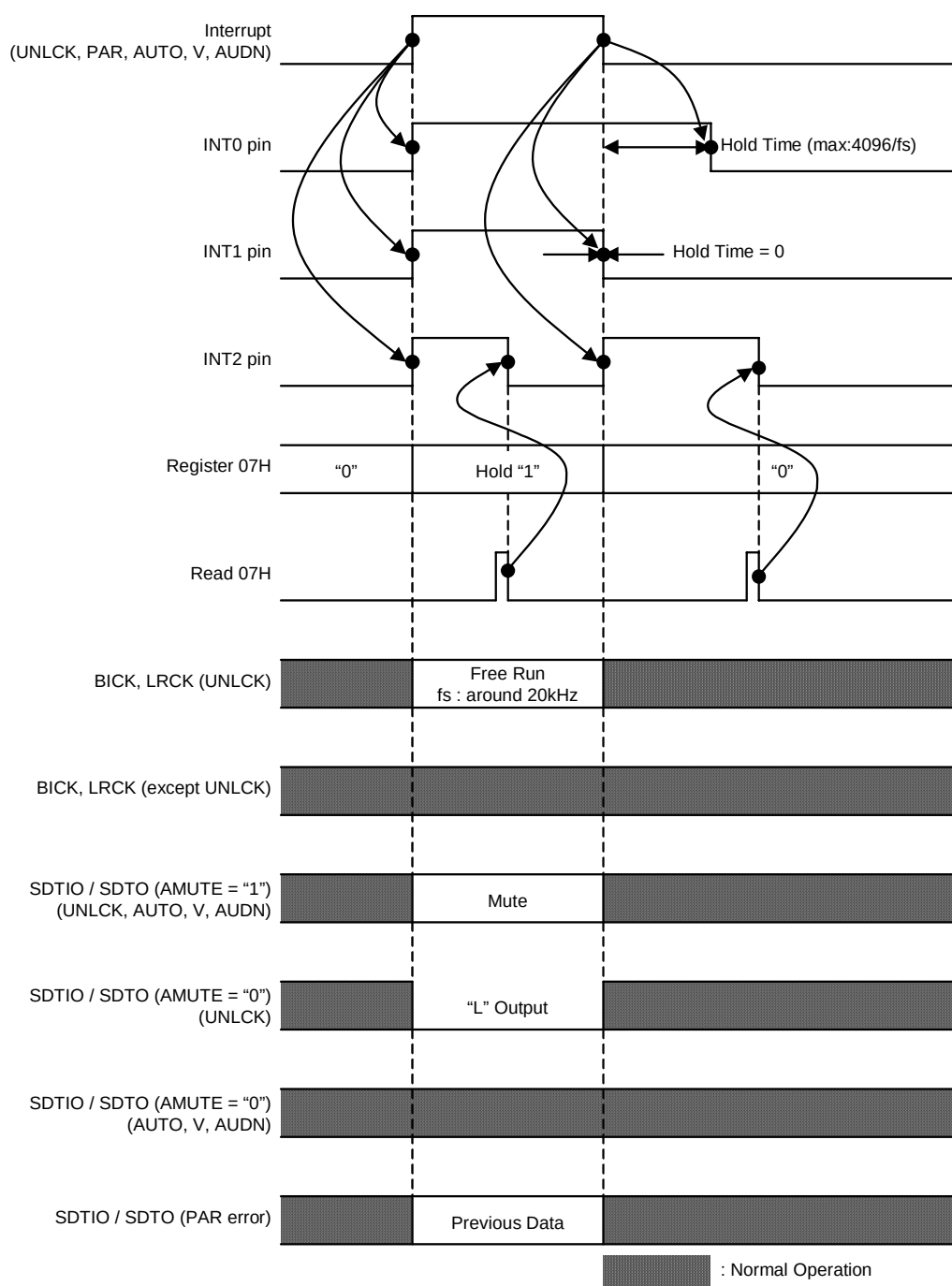


Figure 17. INT2-0 Timing (UNLCK, PAR, AUTO, V, AUDN bits)

## (2) STC, CINT and QINT bits

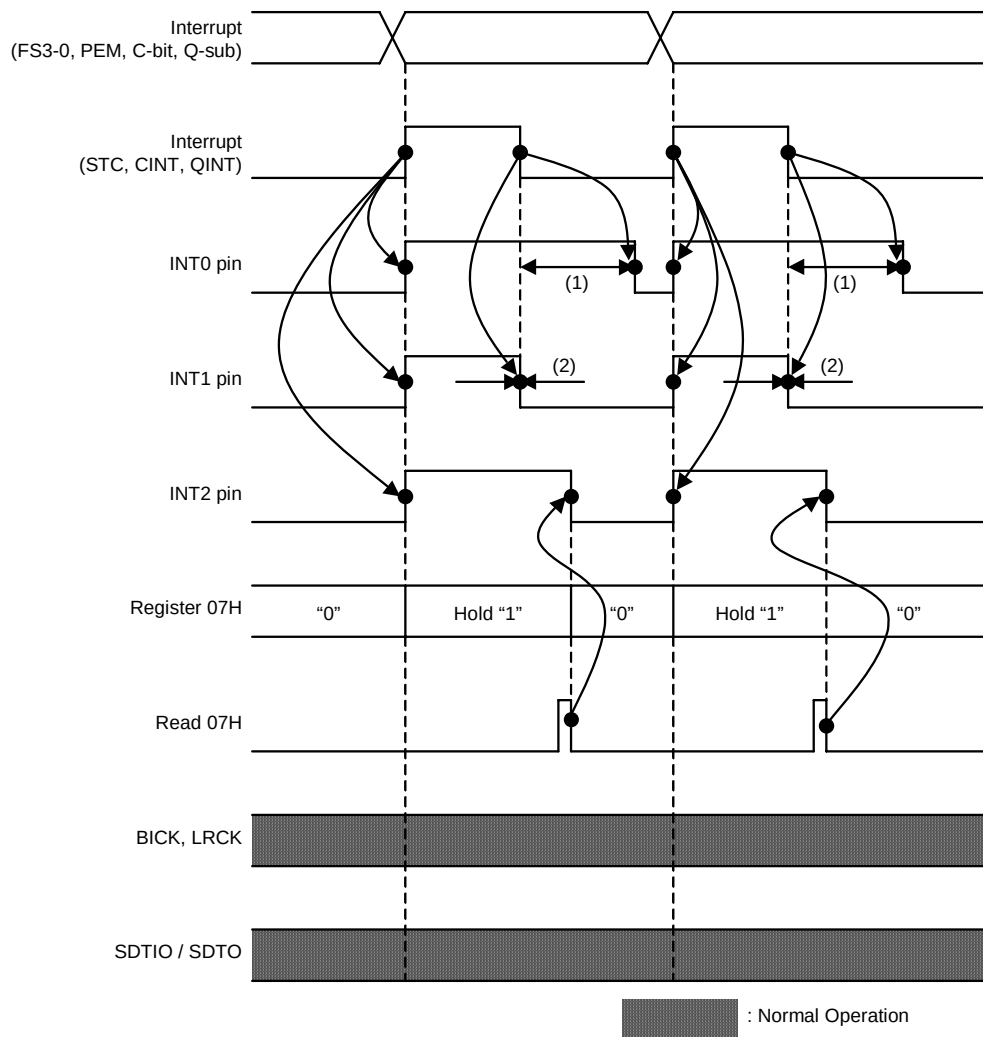


Figure 18. INT2-0 Timing (STC, CINT, QINT bits)

- (1) Hold Time : max. 4096/fs  
 (2) Hold Time = 0

## (3) DAT bit

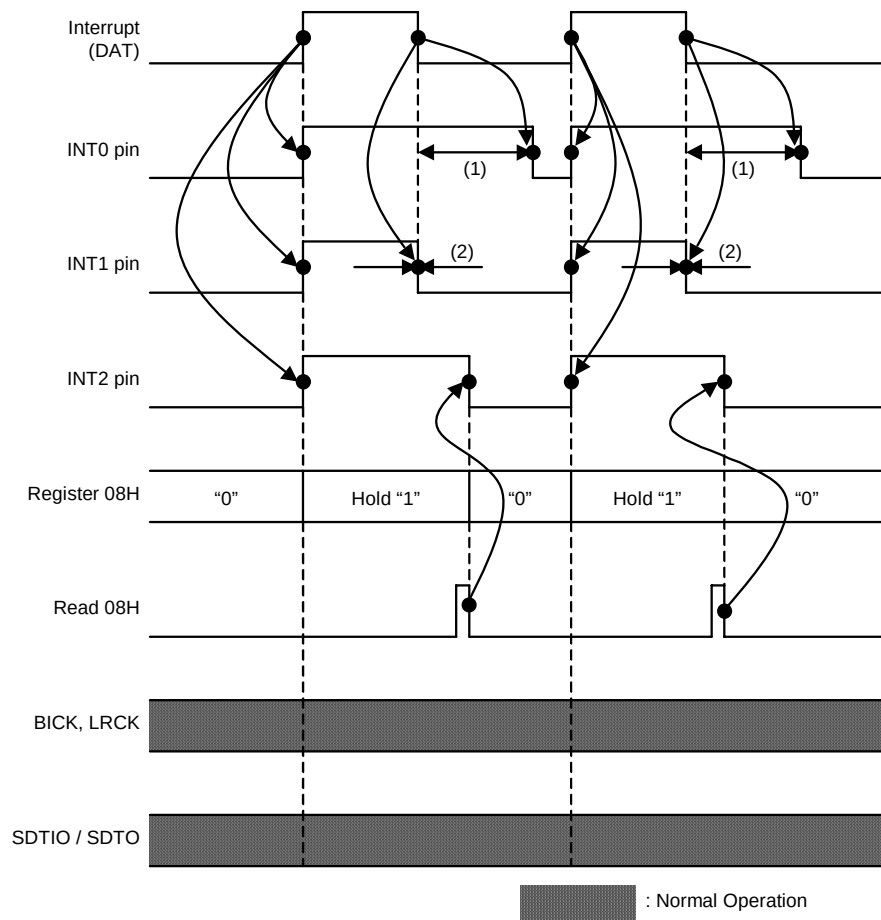


Figure 19. INT2-0 Timing (DAT bit)

(1) Hold Time: max.  $4096/f_s$ 

(2) Hold Time = 0

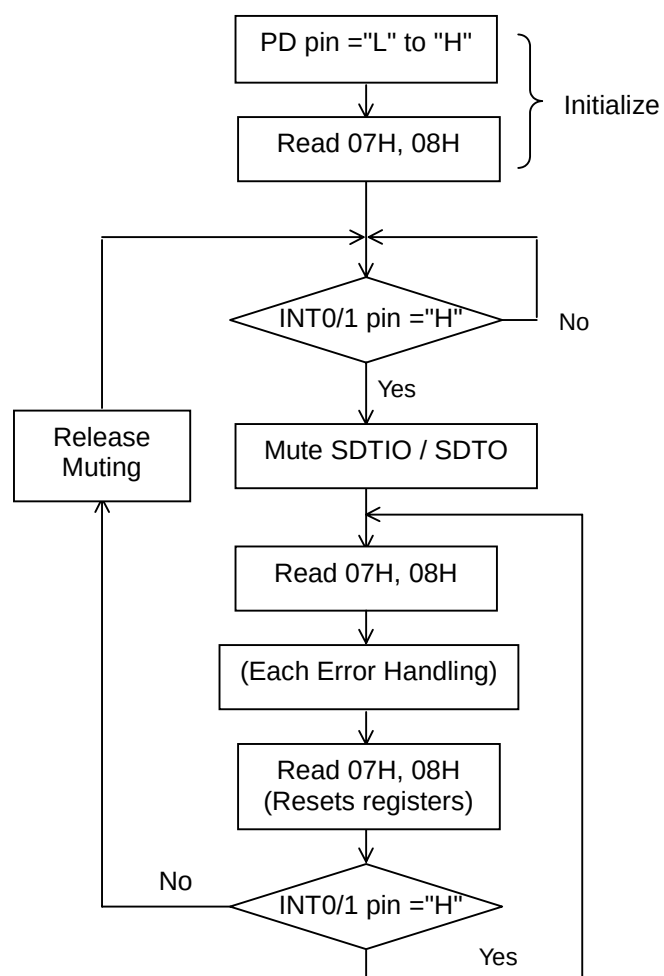


Figure 20. Interrupt Handling Sequence Example 1



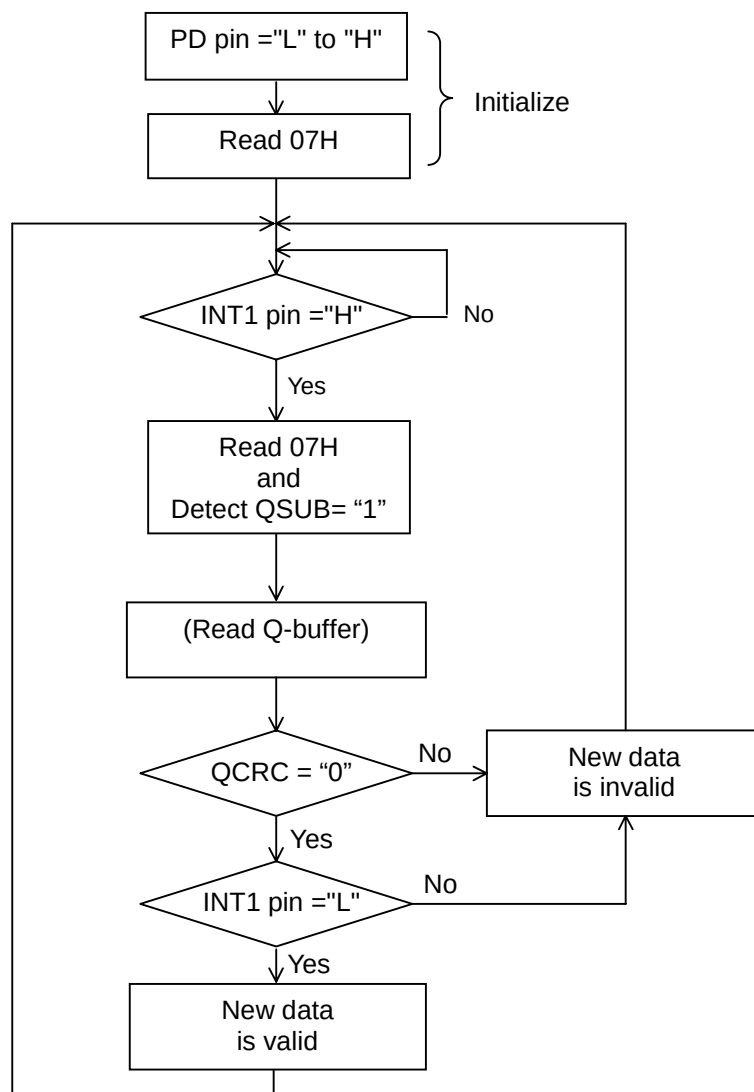


Figure 21. Interrupt Handling Sequence Example 2

## ■ Q-subcode buffers

The DIR of the AK4122A has a Q-subcode buffer for CD applications. The AK4122A takes Q-subcode into registers under the following conditions:

- 1) The sync word (S0, S1) consists of at least 16 “0”s.
- 2) The start bit is “1”.
- 3) Those 7-bits Q-W follow the start bit.
- 4) The distance between two start bits is 8-16 bits.

QINT bit should be valid and “0” while Q-subcode is read from the register.

|     | 1 | 2   | 3   | 4   | 5   | 6   | 7   | 8   | *    |
|-----|---|-----|-----|-----|-----|-----|-----|-----|------|
| S0  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S1  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S2  | 1 | Q2  | R2  | S2  | T2  | U2  | V2  | W2  | 0... |
| S3  | 1 | Q3  | R3  | S3  | T3  | U3  | V3  | W3  | 0... |
| :   | : | :   | :   | :   | :   | :   | :   | :   | :    |
| S97 | 1 | Q97 | R97 | S97 | T97 | U97 | V97 | W97 | 0... |
| S0  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S1  | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0... |
| S2  | 1 | Q2  | R2  | S2  | T2  | U2  | V2  | W2  | 0... |
| S3  | 1 | Q3  | R3  | S3  | T3  | U3  | V3  | W3  | 0... |
| :   | : | :   | :   | :   | :   | :   | :   | :   | :    |

↑  
Q

(\*) number of “0” : min=0; max=8.

Figure 22. Configuration of U-bit(CD)

|                |     |     |     |      |     |     |     |                                                                 |     |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |
|----------------|-----|-----|-----|------|-----|-----|-----|-----------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Q2             | Q3  | Q4  | Q5  | Q6   | Q7  | Q8  | Q9  | Q10                                                             | Q11 | Q12 | Q13 | Q14 | Q15 | Q16 | Q17 | Q18             | Q19 | Q20 | Q21 | Q22 | Q23 | Q24 | Q25 |
| CTRL           |     |     |     | ADRS |     |     |     | TRACK NUMBER                                                    |     |     |     |     |     |     |     | INDEX           |     |     |     |     |     |     |     |
| Q26            | Q27 | Q28 | Q29 | Q30  | Q31 | Q32 | Q33 | Q34                                                             | Q35 | Q36 | Q37 | Q38 | Q39 | Q40 | Q41 | Q42             | Q43 | Q44 | Q45 | Q46 | Q47 | Q48 | Q49 |
| MINUTE         |     |     |     |      |     |     |     | SECOND                                                          |     |     |     |     |     |     |     | FRAME           |     |     |     |     |     |     |     |
| Q50            | Q51 | Q52 | Q53 | Q54  | Q55 | Q56 | Q57 | Q58                                                             | Q59 | Q60 | Q61 | Q62 | Q63 | Q64 | Q65 | Q66             | Q67 | Q68 | Q69 | Q70 | Q71 | Q72 | Q73 |
| ZERO           |     |     |     |      |     |     |     | ABSOLUTE MINUTE                                                 |     |     |     |     |     |     |     | ABSOLUTE SECOND |     |     |     |     |     |     |     |
| Q74            | Q75 | Q76 | Q77 | Q78  | Q79 | Q80 | Q81 | Q82                                                             | Q83 | Q84 | Q85 | Q86 | Q87 | Q88 | Q89 | Q90             | Q91 | Q92 | Q93 | Q94 | Q95 | Q96 | Q97 |
| ABSOLUTE FRAME |     |     |     |      |     |     |     | CRC<br>G(x)=x <sup>16</sup> +x <sup>12</sup> +x <sup>5</sup> +1 |     |     |     |     |     |     |     |                 |     |     |     |     |     |     |     |

Figure 23. Q-subcode

| Addr | Register Name               | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 13H  | Q-subcode Address / Control | Q9  | Q8  | ... | ... | ... | ... | Q3  | Q2  |
| 14H  | Q-subcode Track             | Q17 | Q16 | ... | ... | ... | ... | Q11 | Q10 |
| 15H  | Q-subcode Index             | ... | ... | ... | ... | ... | ... | ... | ... |
| 16H  | Q-subcode Minute            | ... | ... | ... | ... | ... | ... | ... | ... |
| 17H  | Q-subcode Second            | ... | ... | ... | ... | ... | ... | ... | ... |
| 18H  | Q-subcode Frame             | ... | ... | ... | ... | ... | ... | ... | ... |
| 19H  | Q-subcode Zero              | ... | ... | ... | ... | ... | ... | ... | ... |
| 1AH  | Q-subcode ABS Minute        | ... | ... | ... | ... | ... | ... | ... | ... |
| 1BH  | Q-subcode ABS Second        | ... | ... | ... | ... | ... | ... | ... | ... |
| 1CH  | Q-subcode ABS Frame         | Q81 | Q80 | ... | ... | ... | ... | Q75 | Q74 |

Figure 24. Q-subcode register map

## ■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The DIR of the AK4122A has a Non-PCM steam auto-detection function. In the 32-bit mode when Non-PCM preamble based on Dolby “AC-3 Data Stream in IEC60958 Interface” is detected, the NPCM bit goes to “1”. The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the NPCM bit to “1”. Once the NPCM bit is set to “1”, it will remain “1” until 4096 frames pass through the chip without an additional sync pattern being detected (Timing diagram: [Figure 27](#) and [Figure 28](#)). When those preambles are detected, the burst preambles Pc and Pd (Pc: burst information, Pd: length code; Refer to [Table 22](#), [Table 23](#)) that follow those sync codes are stored to registers. The AK4122A also has a DTS-CD bitstream auto-detection function. When AK4122A detects DTS-CD bitstream, the DTSCD bit goes to “1”. If the next sync code does not occur within 4096 frames, the DTSCD bit returns to “0” until either the AK4122A detects the stream again. OR’ed value of the NPCM and DTSCD bits are output to the AUTO bit. The AK4122A detects 14-bit sync word and 16-bit sync word of a DTS-CD bitstream, and these detection can be ON/OFF by DTS14 and DTS16 bits.

## ■ Serial Control Interface

The internal registers may be either written or read by the 4-wire  $\mu$ P interface pins: CSN, CCLK, CDTI and CDTO. The data on this interface consists of Chip address (2bits, C1/0 are fixed to “00”), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge of CCLK, after a high-to-low transition of CSN. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes to high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. The chip address is fixed to “00”. Accessing to the chip address except for “00” is invalid. The PDN pin = “L” resets the registers to their default values. Read/Write operation can be made without MCLK, BICK and LRCK clocks.

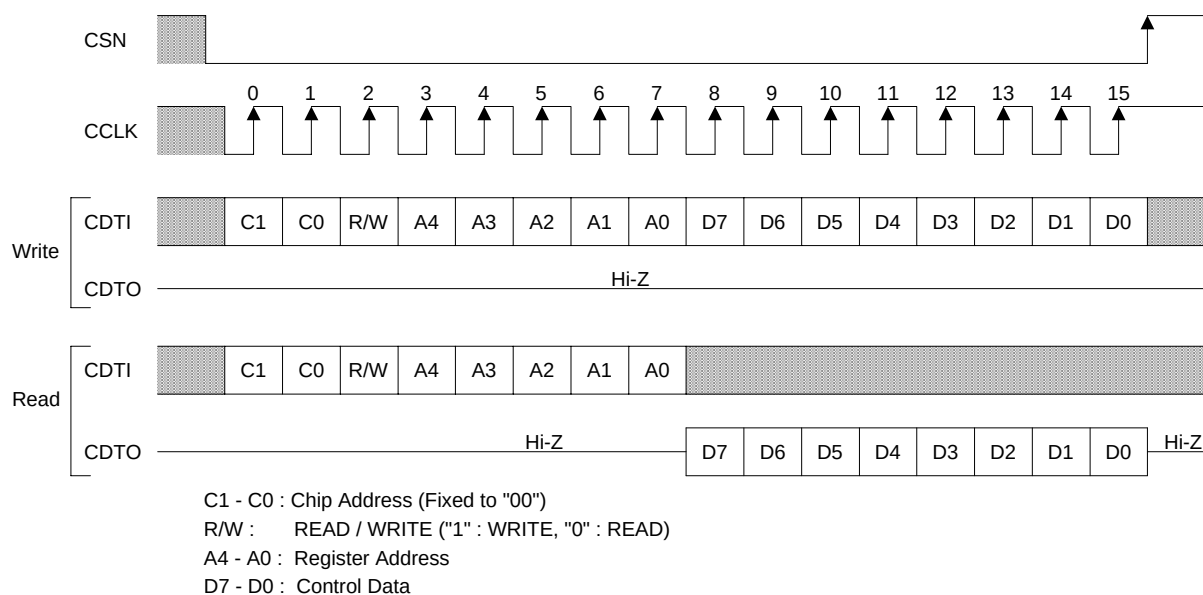


Figure 25. Control I/F Timing

## ■ Register Map

| Addr | Register Name               | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|-----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00H  | PDN & Mode Control          | XTL1  | XTL0  | TXE   | SMUTE | DEAU  | DEM1  | DEM0  | PWN   |
| 01H  | Selector & Clock Control    | BYPS  | OSEL  | ISEL1 | ISEL0 | ICKS1 | ICKS0 | OCKS1 | OCKS0 |
| 02H  | Audio Interface Format      | 0     | 0     | 0     | ODIF  | IDIF1 | IDIF0 | DIF1  | DIF0  |
| 03H  | DIR Control                 | CS12  | AMUTE | EFH1  | EFH0  | IPS1  | IPS0  | OPS1  | OPS0  |
| 04H  | INT0 Mask                   | MULK0 | MPAR0 | MAUT0 | MV0   | MAUD0 | MSTC0 | MCIT0 | MQIT0 |
| 05H  | INT1 Mask                   | MULK1 | MPAR1 | MAUT1 | MV1   | MAUD1 | MSTC1 | MCIT1 | MQIT1 |
| 06H  | DAT Mask & DTS Detect       | 0     | 0     | 0     | 0     | DTS16 | DTS14 | MDAT1 | MDAT0 |
| 07H  | Receiver Status 0           | UNLCK | PAR   | AUTO  | V     | AUDN  | STC   | CINT  | QINT  |
| 08H  | Receiver Status 1           | DAT   | DTSCD | NPCM  | PEM   | FS3   | FS2   | FS1   | FS0   |
| 09H  | Receiver Status 2           | 0     | 0     | 0     | 0     | 0     | 0     | CCRC  | QCRC  |
| 0AH  | RX Channel Status Byte 0    | CR7   | CR6   | CR5   | CR4   | CR3   | CR2   | CR1   | CR0   |
| 0BH  | RX Channel Status Byte 1    | CR15  | CR14  | CR13  | CR12  | CR11  | CR10  | CR9   | CR8   |
| 0CH  | RX Channel Status Byte 2    | CR23  | CR22  | CR21  | CR20  | CR19  | CR18  | CR17  | CR16  |
| 0DH  | RX Channel Status Byte 3    | CR31  | CR30  | CR29  | CR28  | CR27  | CR26  | CR25  | CR24  |
| 0EH  | RX Channel Status Byte 4    | CR39  | CR38  | CR37  | CR36  | CR35  | CR34  | CR33  | CR32  |
| 0FH  | Burst Preamble Pc Byte 0    | PC7   | PC6   | PC5   | PC4   | PC3   | PC2   | PC1   | PC0   |
| 10H  | Burst Preamble Pc Byte 1    | PC15  | PC14  | PC13  | PC12  | PC11  | PC10  | PC9   | PC8   |
| 11H  | Burst Preamble Pd Byte 0    | PD7   | PD6   | PD5   | PD4   | PD3   | PD2   | PD1   | PD0   |
| 12H  | Burst Preamble Pd Byte 1    | PD15  | PD14  | PD13  | PD12  | PD11  | PD10  | PD9   | PD8   |
| 13H  | Q-subcode Address / Control | Q9    | Q8    | Q7    | Q6    | Q5    | Q4    | Q3    | Q2    |
| 14H  | Q-subcode Track             | Q17   | Q16   | Q15   | Q14   | Q13   | Q12   | Q11   | Q10   |
| 15H  | Q-subcode Index             | Q25   | Q24   | Q23   | Q22   | Q21   | Q20   | Q19   | Q18   |
| 16H  | Q-subcode Minute            | Q33   | Q32   | Q31   | Q30   | Q29   | Q28   | Q27   | Q26   |
| 17H  | Q-subcode Second            | Q41   | Q40   | Q39   | Q38   | Q37   | Q36   | Q35   | Q34   |
| 18H  | Q-subcode Frame             | Q49   | Q48   | Q47   | Q46   | Q45   | Q44   | Q43   | Q42   |
| 19H  | Q-subcode Zero              | Q57   | Q56   | Q55   | Q54   | Q53   | Q52   | Q51   | Q50   |
| 1AH  | Q-subcode ABS Minute        | Q65   | Q64   | Q63   | Q62   | Q61   | Q60   | Q59   | Q58   |
| 1BH  | Q-subcode ABS Second        | Q73   | Q72   | Q71   | Q70   | Q69   | Q68   | Q67   | Q66   |
| 1CH  | Q-subcode ABS Frame         | Q81   | Q80   | Q79   | Q78   | Q77   | Q76   | Q75   | Q74   |

When the ODN pin is “L”, the registers are initialized to their default value.

When PORT1 or PORT2 are selected as input port, the status registers (07H ~ 1CH) are initialized.

Note 23. The bits defined as 0 must contain a “0” value.

Note 24. For addresses from 1DH ~ 1FH, data must not be written.

## ■ Register Definitions

| Addr | Register Name      | D7   | D6   | D5  | D4    | D3   | D2   | D1   | D0  |
|------|--------------------|------|------|-----|-------|------|------|------|-----|
| 00H  | PDN & Mode Control | XTL1 | XTL0 | TXE | SMUTE | DEAU | DEM1 | DEM0 | PWN |
|      | R/W                | R/W  | R/W  | R/W | R/W   | R/W  | R/W  | R/W  | R/W |
|      | Default            | 1    | 1    | 1   | 0     | 0    | 0    | 1    | 1   |

PWN: Power Down Control

0: Power down

1: Normal operation (default)

“0” powers down all sections. The contents of all register are not initialized and enabled to write to the registers. The internal registers (00H ~ 06H) are not initialized, however, the status registers (07H ~ 1CH) are initialized. Read/Write operations to the registers are enabled.

DEM1-0: De-emphasis Control ([Table 12](#), [Table 13](#))

Initial values are “01”.

DEAU: De-emphasis Auto Control

0: Disable (default)

1: Enable

When DEAU bit = “1”, the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status.

SMUTE: Soft Mute Control

0: Normal operation (default)

1: SDTIO and SDTO soft mute

When SMUTE bit = “1”, SDTO and SDTIO outputs “L”.

TXE: TX Output enable

0: Disable, TX outputs “L”.

1: Enable (default)

XTL1-0: Reference MCLK Frequency Select ([Table 16](#))

Initial values are “11”.

| Addr | Register Name            | D7   | D6   | D5    | D4    | D3    | D2    | D1    | D0    |
|------|--------------------------|------|------|-------|-------|-------|-------|-------|-------|
| 01H  | Selector & Clock Control | BYPS | OSEL | ISEL1 | ISEL0 | ICKS1 | ICKS0 | OCKS1 | OCKS0 |
|      | R/W                      | R/W  | R/W  | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
|      | Default                  | 0    | 0    | 0     | 0     | 1     | 0     | 1     | 0     |

OCKS1-0: OMCLK Frequency Select for Master mode ([Table 5](#))

Initial values are “10”.

ICKS1-0: MCLK2 Frequency Select for Master mode ([Table 4](#))

Initial values are “10”.

ISEL1-0: Input Port Select

Initial values are “00”.

| ISEL1 | ISEL0 | Input PORT |
|-------|-------|------------|
| 0     | 0     | PORT1      |
| 0     | 1     | PORT2      |
| 1     | 0     | DIR        |
| 1     | 1     | N/A        |

(default)

Table 19. Input PORT Select

OSEL: Output Port Select

Initial values are “0”.

| OSEL | Output PORT |
|------|-------------|
| 0    | PORT3       |
| 1    | PORT2       |

(default)

Table 20. Output PORT Select

BYPS: Select Bypass mode

0: SRC mode (default)

1: Bypass mode

When BYPS bit = “1”, the AK4122A outputs the clocks (BICK, LRCK) and data that is input by input port without SRC.

| Addr | Register Name          | D7 | D6 | D5 | D4   | D3    | D2    | D1   | D0   |
|------|------------------------|----|----|----|------|-------|-------|------|------|
| 02H  | Audio Interface Format | 0  | 0  | 0  | ODIF | IDIF1 | IDIF0 | DIF1 | DIF0 |
|      | R/W                    | RD | RD | RD | R/W  | R/W   | R/W   | R/W  | R/W  |
|      | Default                | 0  | 0  | 0  | 0    | 0     | 1     | 0    | 1    |

DIF1-0: Audio Interface Format for PORT1 ([Table 8](#))  
Initial values are “01”.

IDIF1-0: Audio Interface Format for PORT2 ([Table 9](#))  
Initial values are “01”.

ODIF: Audio Interface Format for PORT3 ([Table 10](#))  
Initial values are “0”.

| Addr | Register Name | D7   | D6    | D5   | D4   | D3   | D2   | D1   | D0   |
|------|---------------|------|-------|------|------|------|------|------|------|
| 03H  | DIR Control   | CS12 | AMUTE | EFH1 | EFH0 | IPS1 | IPS0 | OPS1 | OPS0 |
|      | R/W           | R/W  | R/W   | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
|      | Default       | 0    | 1     | 0    | 1    | 0    | 0    | 0    | 0    |

OPS1-0: Output Through Data Select for TX ([Table 15](#))  
Initial values are “00”.

IPS1-0: Input Recovery Data Select ([Table 14](#))  
Initial values are “00”.

EFH1-0: Interrupt 0 pin Hold Count Select  
Initial values are “01”.  
LRCK of [Table 21](#) is DIR’s LRCK, the hold time scales with 1/fs.

| EFH1 | EFH0 | Hold Count |
|------|------|------------|
| 0    | 0    | 512LRCK    |
| 0    | 1    | 1024LRCK   |
| 1    | 0    | 2048LRCK   |
| 1    | 1    | 4096LRCK   |

(default)

Table 21. Hold count select

AMUTE: Auto Mute Control  
0: Normal operation  
1: Auto Mute (default)  
When AMUTE bit = “1”, SDTIO and SDTO are muted automatically if the AK4122A detects unlock, Non-Audio or Non-PCM/DTS-CD.

CS12: Channel Status select  
0: Channel 1 (default)  
1: Channel 2  
These bit selects the channel status for C-bit, AuDN, PEM, FS3-0, Pc, Pd and CRC bit.

| Addr | Register Name | D7    | D6    | D5    | D4  | D3    | D2    | D1    | D0    |
|------|---------------|-------|-------|-------|-----|-------|-------|-------|-------|
| 04H  | INT0 Mask     | MULK0 | MPAR0 | MAUT0 | MV0 | MAUD0 | MSTC0 | MCIT0 | MQIT0 |
|      | R/W           | R/W   | R/W   | R/W   | R/W | R/W   | R/W   | R/W   | R/W   |
|      | Default       | 0     | 0     | 1     | 1   | 1     | 1     | 1     | 1     |

MQIT0: Mask enable for QINT bit  
 0: Mask disable  
 1: Mask enable (default)

MCIT0: Mask enable for CINT bit  
 0: Mask disable  
 1: Mask enable (default)

MSTC0: Mask enable for STC bit  
 0: Mask disable  
 1: Mask enable (default)

MAUD0: Mask enable for AUDN bit  
 0: Mask disable  
 1: Mask enable (default)

MV0: Mask enable for V bit  
 0: Mask disable  
 1: Mask enable (default)

MAUT0: Mask enable for AUTO bit  
 0: Mask disable  
 1: Mask enable (default)

MPAR0: Mask enable for PAR bit  
 0: Mask disable (default)  
 1: Mask enable

MULK0: Mask enable for UNLCK bit  
 0: Mask disable (default)  
 1: Mask enable

Registers which the corresponding mask bit is set to “0” affects INT0 and INT2 pins operation.



| Addr | Register Name | D7    | D6    | D5    | D4  | D3    | D2    | D1    | D0    |
|------|---------------|-------|-------|-------|-----|-------|-------|-------|-------|
| 05H  | INT1 Mask     | MULK1 | MPAR1 | MAUT1 | MV1 | MAUD1 | MSTC1 | MCIT1 | MQIT1 |
|      | R/W           | R/W   | R/W   | R/W   | R/W | R/W   | R/W   | R/W   | R/W   |
|      | Default       | 1     | 1     | 0     | 0   | 0     | 1     | 1     | 1     |

MQIT1: Mask enable for QINT bit  
 0: Mask disable  
 1: Mask enable (default)

MCIT1: Mask enable for CINT bit  
 0: Mask disable  
 1: Mask enable (default)

MSTC1: Mask enable for STC bit  
 0: Mask disable  
 1: Mask enable (default)

MAUD1: Mask enable for AUDN bit  
 0: Mask disable (default)  
 1: Mask enable

MV1: Mask enable for V bit  
 0: Mask disable (default)  
 1: Mask enable

MAUT1: Mask enable for AUTO bit  
 0: Mask disable (default)  
 1: Mask enable

MPAR1: Mask enable for PAR bit  
 0: Mask disable  
 1: Mask enable (default)

MULK1: Mask enable for UNLCK bit  
 0: Mask disable  
 1: Mask enable (default)

Registers which the corresponding mask bit is set to “0” affects the INT1 pin operation.

| Addr | Register Name         | D7 | D6 | D5 | D4 | D3    | D2    | D1    | D0    |
|------|-----------------------|----|----|----|----|-------|-------|-------|-------|
| 06H  | DAT Mask & DTS Detect | 0  | 0  | 0  | 0  | DTS16 | DTS14 | MDAT1 | MDAT0 |
|      | R/W                   | RD | RD | RD | RD | R/W   | R/W   | R/W   | R/W   |
|      | Default               | 0  | 0  | 0  | 0  | 1     | 1     | 1     | 1     |

MDAT0: Mask enable for DAT bit  
 0: Mask disable  
 1: Mask enable (default)

If this mask bit is set to “0”, DAT bit affects INT0 and INT2 pins operation.

MDAT1: Mask enable for DAT bit  
 0: Mask disable  
 1: Mask enable (default)

If this mask bit is set to “0”, DAT bit affects the INT1 pin operation.

DTS14: DTS-CD 14bit Sync Word Detect  
 0: No detect  
 1: Detect (default)

DTS16: DST-CD 16bit Sync Word Detect  
 0: No detect  
 1: Detect (default)

| Addr | Register Name     | D7    | D6  | D5   | D4 | D3   | D2  | D1   | D0   |
|------|-------------------|-------|-----|------|----|------|-----|------|------|
| 07H  | Receiver Status 0 | UNLCK | PAR | AUTO | V  | AUDN | STC | CINT | QINT |
|      | R/W               | RD    | RD  | RD   | RD | RD   | RD  | RD   | RD   |
|      | Default           | 0     | 0   | 0    | 0  | 0    | 0   | 0    | 0    |

QINT: Q-subcode Buffer Interrupt

0: No change

1: Changed

This bit goes to “1” when Q-subcode stored in register addresses 13H to 1CH is updated.

CINT: Channel Status Buffer Interrupt

0: No change

1: Changed

This bit goes to “1” when C-bit stored in register addresses 0AH to 0EH changes.

STC: Sampling Frequency or Pre-emphasis Information Change Detection

0: No detect

1: Detect

This bit goes to “1” when either the FS3-0 or PEM bit changes.

AUDN: Audio Bit Output

0: Audio

1: Non audio

This bit is made by encoding channel status bits.

V: Validity Bit

0: Valid

1: Invalid

AUTO: Non-PCM or DTS-CD Bit Steam Auto Detection

0: No detect

1: Detect

This bit outputs an OR’ed result of NPCM and DTSCD bits.

PAR: Parity Error or Bi-phase Error Status

0: No error

1: Error

This bit goes to “1” if a parity error or biphase error is detected in the sub-frame.

UNLCK: PLL Lock Status

0: Lock

1: Unlock

QINT, CINT and STC bits are initialized when 07H is read.

| Addr | Register Name     | D7  | D6    | D5   | D4  | D3  | D2  | D1  | D0  |
|------|-------------------|-----|-------|------|-----|-----|-----|-----|-----|
| 08H  | Receiver Status 1 | DAT | DTSCD | NPCM | PEM | FS3 | FS2 | FS1 | FS0 |
|      | R/W               | RD  | RD    | RD   | RD  | RD  | RD  | RD  | RD  |
|      | Default           | 0   | 0     | 0    | 0   | 0   | 0   | 0   | 1   |

FS3-0: Sampling Frequency Detection ([Table 17](#))

PEM: Pre-emphasis Detect ([Table 18](#))

0: OFF

1: ON

This bit is made by decoding the channel status bits.

NPCM: Non-PCM Bit Stream Auto Detection

0: No detect

1: Detect

DTSCD: DTS-CD Bit Stream Auto Detect

0: No detect

1: Detect

DAT: DAT Start ID Detect

0: No detect

1: Detect

When the category code shows DAT, this bit becomes “1” if the Start ID of DAT is detected as “1”.

Reading 08H register resets this bit to “0”.

DAT bit is initialized when 08H is read.

| Addr | Register Name     | D7 | D6 | D5 | D4 | D3 | D2 | D1   | D0   |
|------|-------------------|----|----|----|----|----|----|------|------|
| 09H  | Receiver Status 2 | 0  | 0  | 0  | 0  | 0  | 0  | CCRC | QCRC |
|      | R/W               | RD | RD | RD | RD | RD | RD | RD   | RD   |
|      | Default           | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0    |

QCRC: Cyclic Redundancy Check for Q-subcode

0: No error

1: Error

CCRC: Cyclic Redundancy Check for Channel Status

0: No error

1: Error

This bit is enabled only in professional mode and only for the channel selected by the CS12 bit.

| Addr    | Register Name            | D7              | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|--------------------------|-----------------|------|------|------|------|------|------|------|
| 0AH     | RX Channel Status Byte 0 | CR7             | CR6  | CR5  | CR4  | CR3  | CR2  | CR1  | CR0  |
| 0BH     | RX Channel Status Byte 1 | CR15            | CR14 | CR13 | CR12 | CR11 | CR10 | CR9  | CR8  |
| 0CH     | RX Channel Status Byte 2 | CR23            | CR22 | CR21 | CR20 | CR19 | CR18 | CR17 | CR16 |
| 0DH     | RX Channel Status Byte 3 | CR31            | CR30 | CR29 | CR28 | CR27 | CR26 | CR25 | CR24 |
| 0EH     | RX Channel Status Byte 4 | CR39            | CR38 | CR37 | CR36 | CR35 | CR34 | CR33 | CR32 |
| R/W     |                          | RD              |      |      |      |      |      |      |      |
| Default |                          | Not initialized |      |      |      |      |      |      |      |

CR39-0: Receiver Channel Status Byte 4-0

All 40 bits are updated at the same time every block (192 frames) cycle.

| Addr    | Register Name            | D7              | D6   | D5   | D4   | D3   | D2   | D1  | D0  |
|---------|--------------------------|-----------------|------|------|------|------|------|-----|-----|
| 0FH     | Burst Preamble Pc Byte 0 | PC7             | PC6  | PC5  | PC4  | PC3  | PC2  | PC1 | PC0 |
| 10H     | Burst Preamble Pc Byte 1 | PC15            | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| 11H     | Burst Preamble Pd Byte 0 | PD7             | PD6  | PD5  | PD4  | PD3  | PD2  | PD1 | PD0 |
| 12H     | Burst Preamble Pd Byte 1 | PD15            | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| R/W     |                          | RD              |      |      |      |      |      |     |     |
| Default |                          | Not initialized |      |      |      |      |      |     |     |

PC15-0: Burst Preamble Pc Byte 0 and 1

PD15-0: Burst Preamble Pd Byte 0 and 1

| Addr    | Register Name               | D7              | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|---------|-----------------------------|-----------------|-----|-----|-----|-----|-----|-----|-----|
| 13H     | Q-subcode Address / Control | Q9              | Q8  | Q7  | Q6  | Q5  | Q4  | Q3  | Q2  |
| 14H     | Q-subcode Track             | Q17             | Q16 | Q15 | Q14 | Q13 | Q12 | Q11 | Q10 |
| 15H     | Q-subcode Index             | Q25             | Q24 | Q23 | Q22 | Q21 | Q20 | Q19 | Q18 |
| 16H     | Q-subcode Minute            | Q33             | Q32 | Q31 | Q30 | Q29 | Q28 | Q27 | Q26 |
| 17H     | Q-subcode Second            | Q41             | Q40 | Q39 | Q38 | Q37 | Q36 | Q35 | Q34 |
| 18H     | Q-subcode Frame             | Q49             | Q48 | Q47 | Q46 | Q45 | Q44 | Q43 | Q42 |
| 19H     | Q-subcode Zero              | Q57             | Q56 | Q55 | Q54 | Q53 | Q52 | Q51 | Q50 |
| 1AH     | Q-subcode ABS Minute        | Q65             | Q64 | Q63 | Q62 | Q61 | Q60 | Q59 | Q58 |
| 1BH     | Q-subcode ABS Second        | Q73             | Q72 | Q71 | Q70 | Q69 | Q68 | Q67 | Q66 |
| 1CH     | Q-subcode ABS Frame         | Q81             | Q80 | Q79 | Q78 | Q77 | Q76 | Q75 | Q74 |
| R/W     |                             | RD              |     |     |     |     |     |     |     |
| Default |                             | Not initialized |     |     |     |     |     |     |     |

Q81-2: Q-subcode

All 80 bits are updated at the same time every sync code cycle for Q-subcode.

■ Burst Preambles in Non-PCM Bitstreams

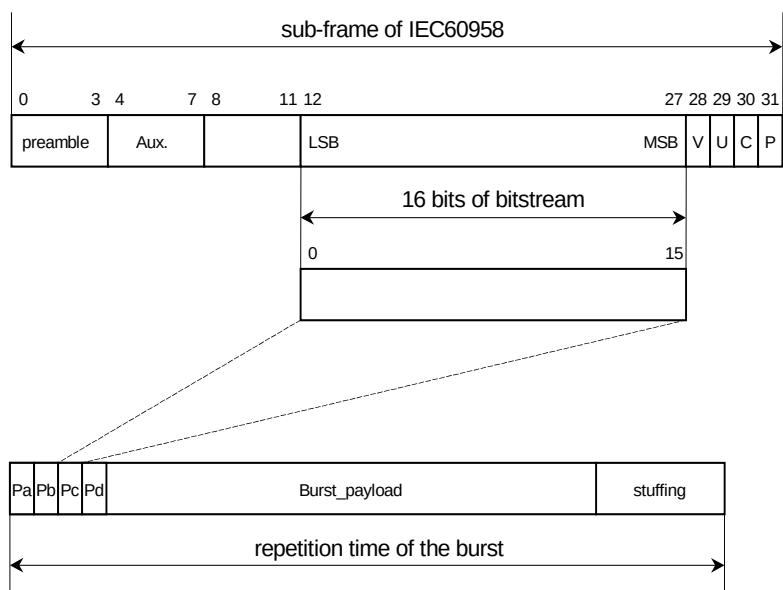


Figure 26. Data Structure of IEC60958

| Preamble word | Length of field | Contents    | Value           |
|---------------|-----------------|-------------|-----------------|
| Pa            | 16 bits         | sync word 1 | 0xF872          |
| Pb            | 16 bits         | sync word 2 | 0x4E1F          |
| Pc            | 16 bits         | Burst info  | see Table 23    |
| Pd            | 16 bits         | Length code | numbers of bits |

Table 22. Burst Preamble Word

| Bits of Pc | Value | Contents                                                        | Repetition time of burst<br>in IEC60958 frames |
|------------|-------|-----------------------------------------------------------------|------------------------------------------------|
| 0-4        | 0     | data type<br>NULL data                                          | ≤ 4096                                         |
|            | 1     | Dolby AC-3 data                                                 | 1536                                           |
|            | 2     | reserved                                                        |                                                |
|            | 3     | PAUSE                                                           |                                                |
|            | 4     | MPEG-1 Layer1 data                                              | 384                                            |
|            | 5     | MPEG-1 Layer2 or 3 data or MPEG-2 without extension             | 1152                                           |
|            | 6     | MPEG-2 data with extension                                      | 1152                                           |
|            | 7     | MPEG-2 AAC ADTS                                                 | 1024                                           |
|            | 8     | MPEG-2, Layer1 Low sample rate                                  | 384                                            |
|            | 9     | MPEG-2, Layer2 or 3 Low sample rate                             | 1152                                           |
|            | 10    | reserved                                                        |                                                |
|            | 11    | DTS type I                                                      | 512                                            |
|            | 12    | DTS type II                                                     | 1024                                           |
|            | 13    | DTS type III                                                    | 2048                                           |
|            | 14    | ATRAC                                                           | 512                                            |
|            | 15    | ATRAC2/3                                                        | 1024                                           |
|            | 16-31 | reserved                                                        |                                                |
| 5, 6       | 0     | reserved, shall be set to “0”                                   |                                                |
| 7          | 0     | error-flag indicating a valid burst_payload                     |                                                |
|            | 1     | error-flag indicating that the burst_payload may contain errors |                                                |
| 8-12       |       | data type dependent info                                        |                                                |
| 13-15      | 0     | bit stream number, must be set to “0”                           |                                                |

Table 23. Field of Burst Information Pc

■ Non-PCM Bitstream Timing

(1) When Non-PCM preamble does not arrive within 4096 frames

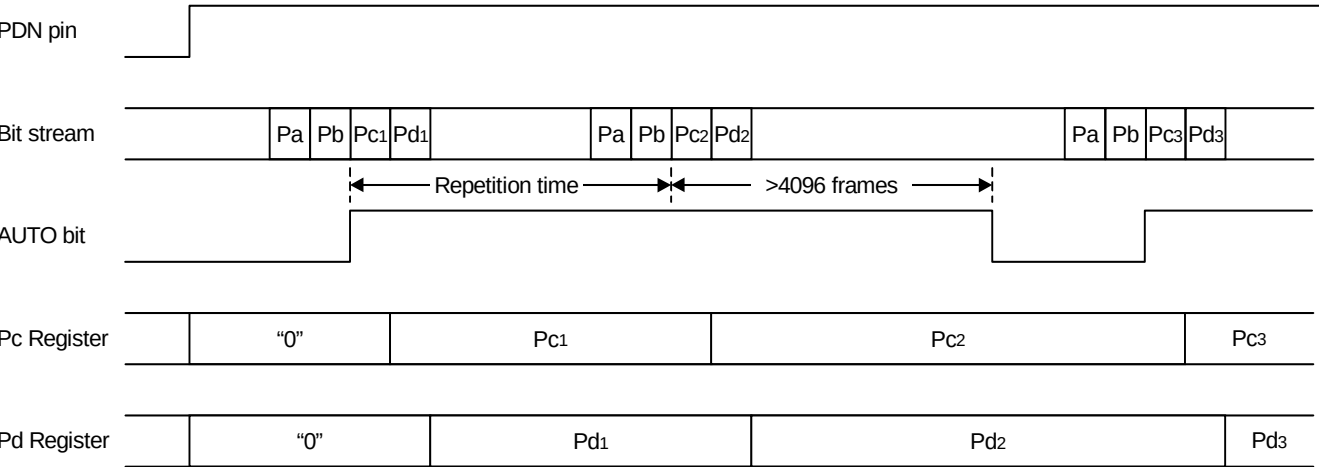


Figure 27. Timing example 1

(2) When Non-PCM bitstream stops (when MULK0 bit = "0")

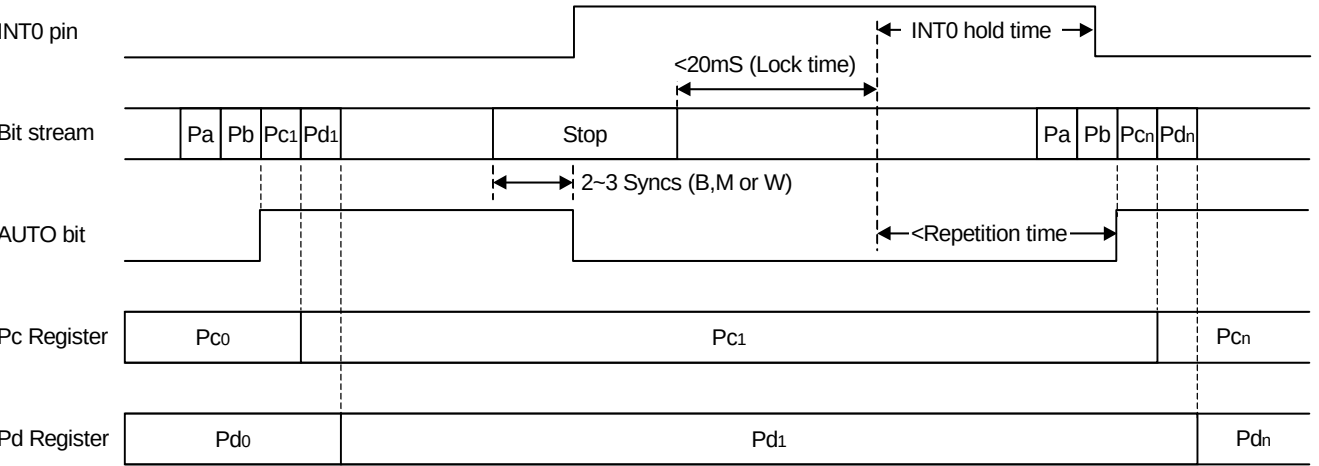


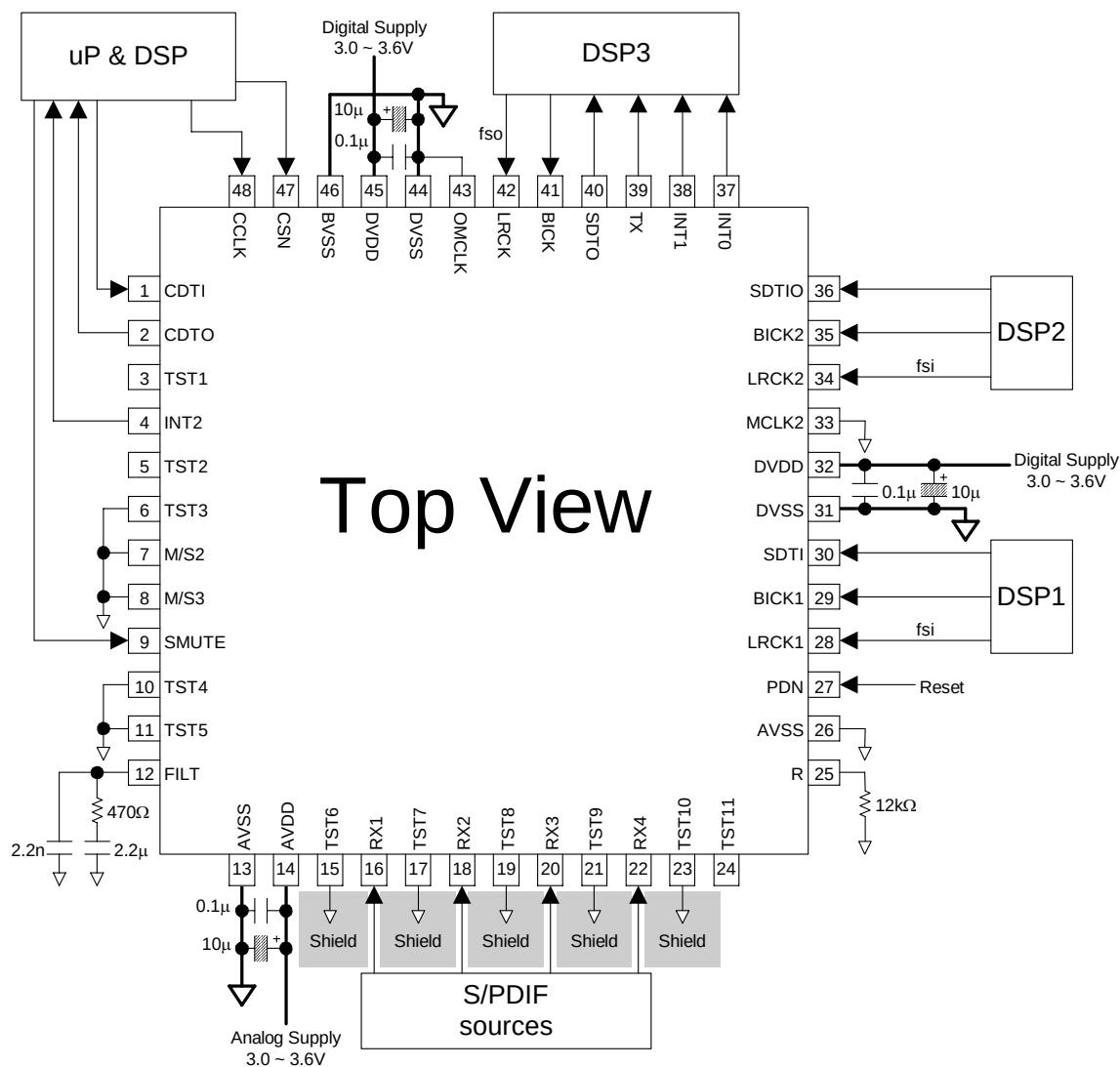
Figure 28. Timing example 2



## SYSTEM DESIGN

Figure 29 shows the typical system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- PORT2, PORT3 : Slave Mode



Note:

- AVSS, BVSS and DVSS of the AK4122A should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.

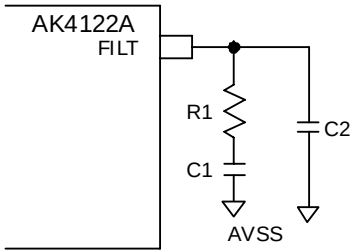
Figure 29. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4122A requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS of the AK4122A must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4122A as possible, with the small value ceramic capacitor being the nearest.

2. PLL Loop-Filter

The C1 (2.2μF) and R1 (470Ω) should be connected in series and attached between the FILT pin and AVSS in parallel with C2 (2.2nF). Noises onto the FILT pin should be avoided.

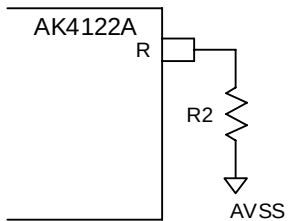


| Parameter | Recommended value | Accuracy    |
|-----------|-------------------|-------------|
| R1        | 470Ω              | -5% ~ +5%   |
| C1        | 2.2μF             | -50% ~ +50% |
| C2        | 2.2nF             | -50% ~ +50% |

Note: The accuracy includes temperature dependence.

Figure 30. Loop Filter for SRC

The R2 (12kΩ) should be connected in series between R pin and AVSS. Please be careful the noise onto the R pin.



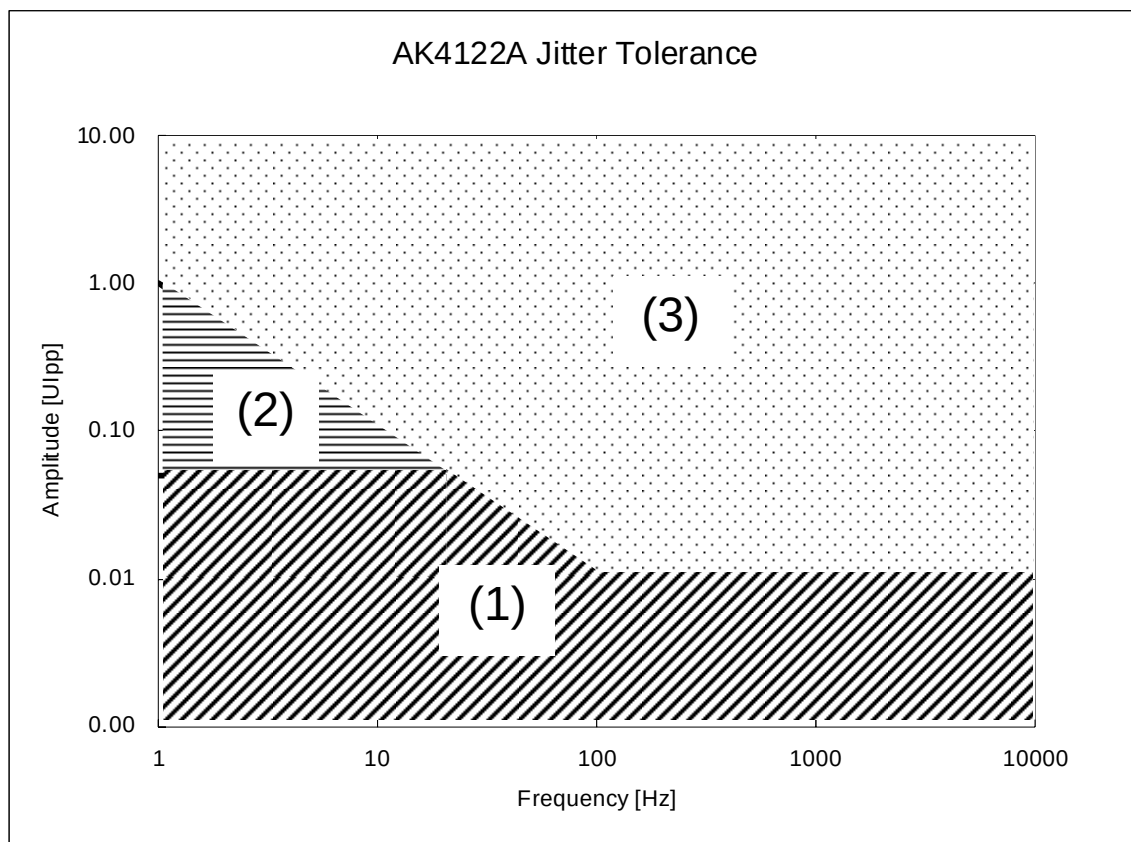
| Parameter | Recommended value | Accuracy  |
|-----------|-------------------|-----------|
| R2        | 12kΩ              | -5% ~ +5% |

Note: The accuracy includes temperature dependence.

Figure 31. Loop Filter for DIR

### 3. Jitter Tolerance

Figure 32 shows the jitter tolerance to ILRCK. The jitter frequency and the jitter amplitude shown in Figure 32 define the jitter quantity. When the jitter amplitude is 0.01U<sub>ipp</sub> or less, the AK4122A operate normally regardless of the jitter frequency.



- (1) Normal operation
- (2) There is a possibility that the distortion degrades. (It may degrade up to about -50dB.)
- (3) There is a possibility that the output data is lost.

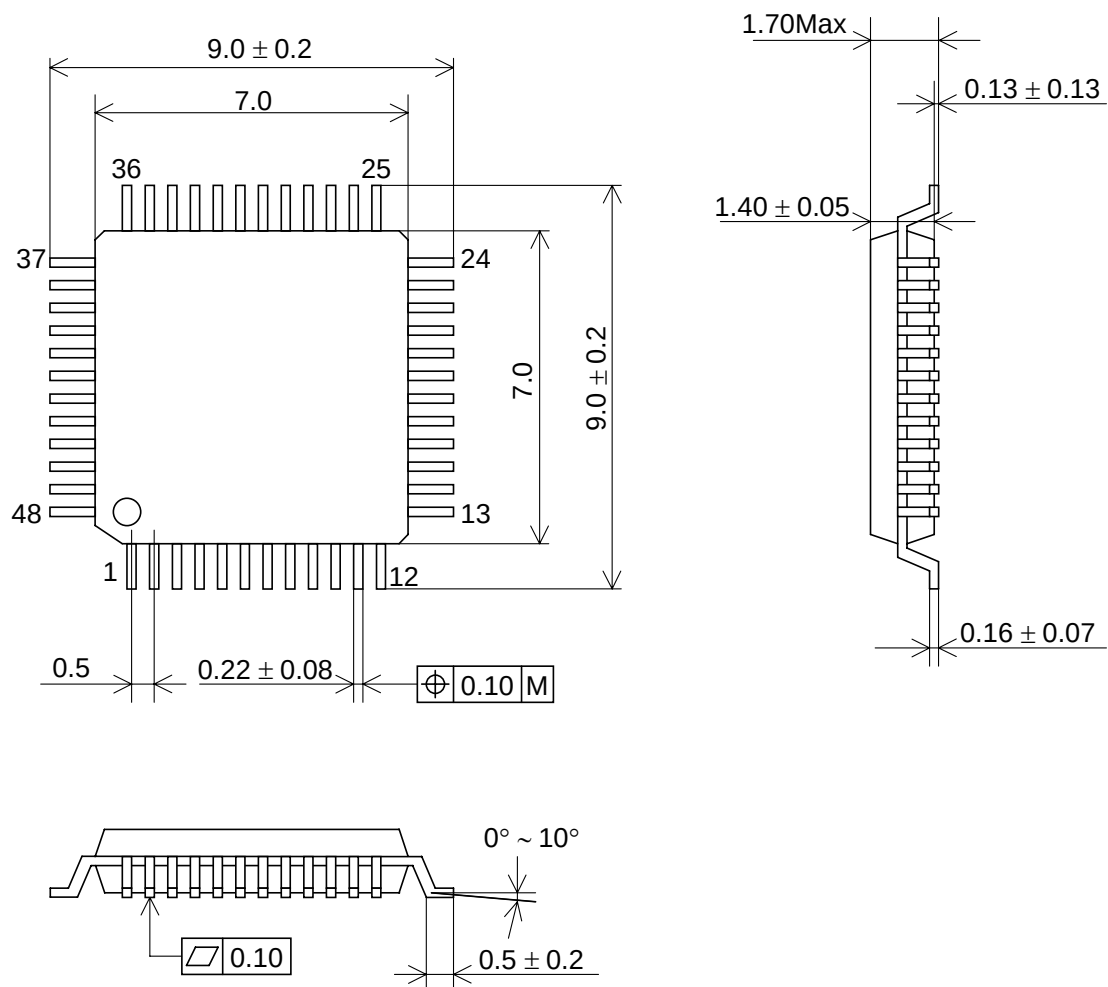
Note:

- The jitter amplitude is for ILRCK and 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is  $1/48\text{kHz} = 20.8\mu\text{s}$ .

Figure 32. Jitter Tolerance

## PACKAGE

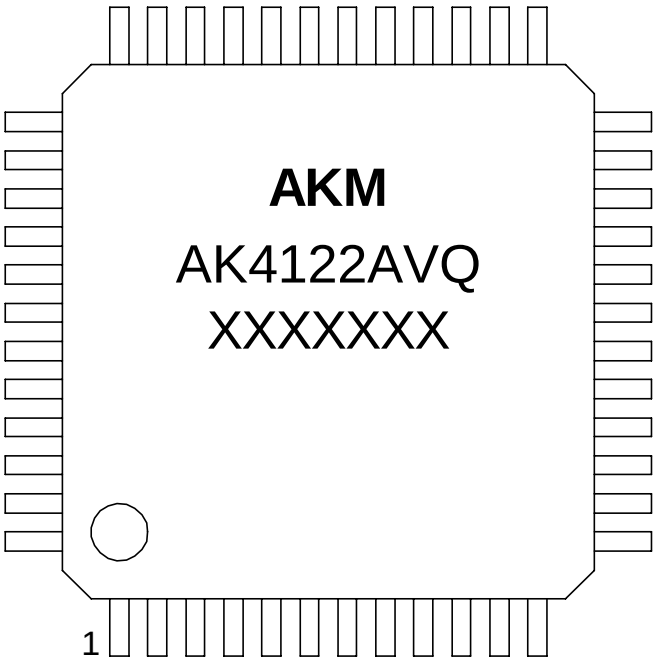
## 48pin LQFP(Unit: mm)



### Material & Lead finish

|                               |                        |
|-------------------------------|------------------------|
| Package molding compound:     | Epoxy                  |
| Lead frame material:          | Cu                     |
| Lead frame surface treatment: | Solder (Pb free) plate |

MARKING



XXXXXXXX: Date code identifier

REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason               | Page | Contents                                                        |
|-----------------|----------|----------------------|------|-----------------------------------------------------------------|
| 09/05/19        | 00       | First Edition        |      |                                                                 |
| 10/05/17        | 01       | Description Addition | 24   | ■ Sequence of changing clocks<br>Description is added in notes. |

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