

**AK4104****192kHz 24-Bit 3.3V DIT****GENERAL DESCRIPTION**

The AK4104 is a digital audio interface transmitter (DIT) which supports data rate up to 192kHz sample rate operation. The AK4104 encodes and transmits audio data according to the AES3, IEC60958, S/PDIF & EIAJ CP1201 interface standards. The AK4104 accepts audio and digital data, which is then encoded. The audio serial port supports four formats.

FEATURES

- ☐ **Sampling Rate up to 192kHz**
- ☐ **Support AES3, IEC60958, S/PDIF & EIAJ CP1201 Consumer Formats**
- ☐ **Generates Parity Bits**
- ☐ **1-channel Transmission Output**
- ☐ **42-bit Channel Status Buffer**
- ☐ **Supports Multiple Clock Frequencies: 128/192/256/384/512/768/1024/1536fs**
- ☐ **Supports Left/Right justified and I²S Audio Formats**
- ☐ **Easy to use 4 wire/3 wire Serial Host Interface**
- ☐ **CMOS Input Level**
- ☐ **Power Supply: 2.7 to 3.6V**
- ☐ **Small Package: 16pin TSSOP**
- ☐ **Temperature Range of -20 to 85 °C**

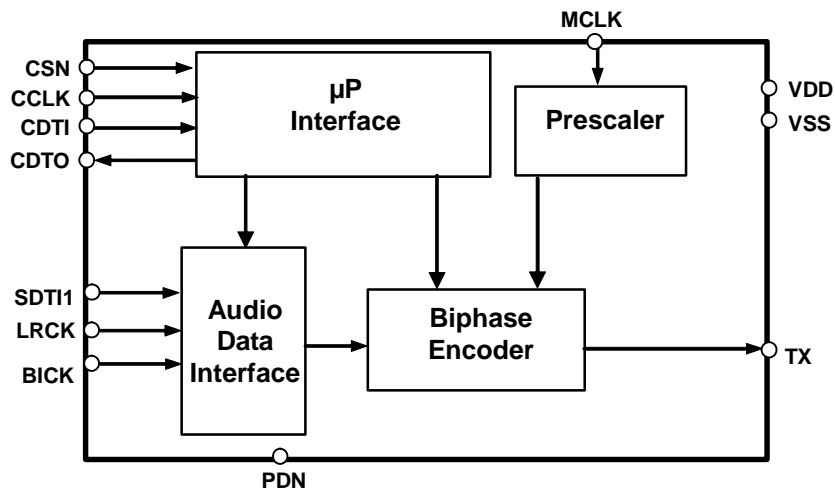


Figure 1. AK4104 Block Diagram (Mode= "0")

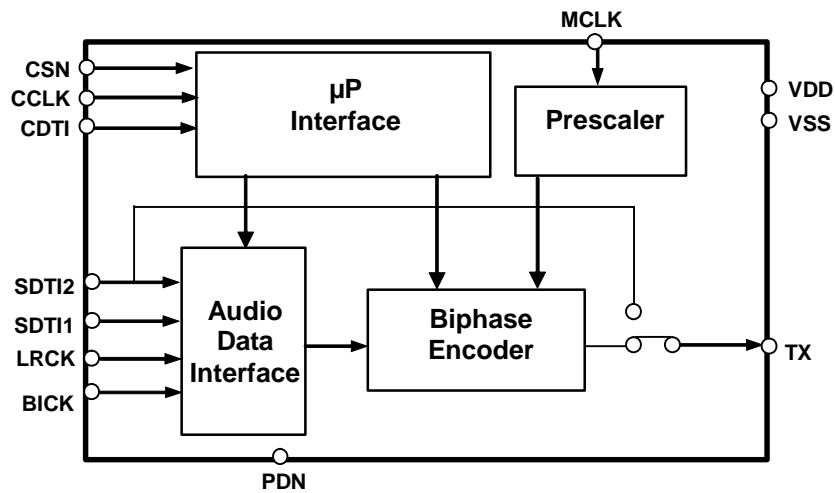
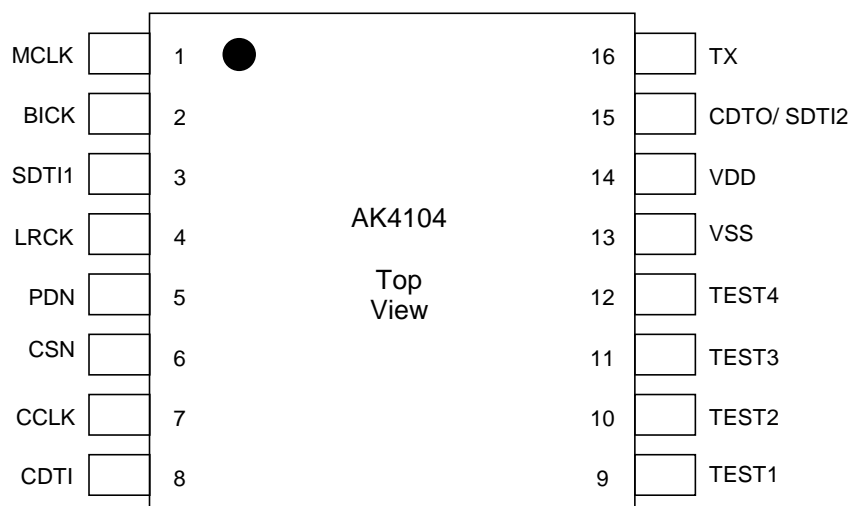


Figure 2. AK4104 Block Diagram (Mode= "1")

■ Ordering GuideAK4104ET
AKD4104-20 ~ +85°C
Evaluation Board for AK4104

16pin TSSOP (0.65mm pitch)

■ Pin Layout

| PIN/FUNCTION | | | |
|--------------|----------|-----|--|
| No. | Pin Name | I/O | Function |
| 1 | MCLK | I | Master Clock Input Pin |
| 2 | BICK | I | Audio Serial Data Clock Pin |
| 3 | SDTI1 | I | Audio Serial Data Input 1 Pin |
| 4 | LRCK | I | Input Channel Clock Pin |
| 5 | PDN | I | Power Down and Reset Pin “L”: Power down and Reset, “H”: Power up |
| 6 | CSN | I | Chip Select Pin |
| 7 | CCLK | I | Control Data Clock Pin |
| 8 | CDTI | I | Control Data Input Pin |
| 9 | TEST1 | I | TEST Pin This pin should be connected to VDD. |
| 10 | TEST2 | O | TEST Pin This pin should be OPEN. |
| 11 | TEST3 | O | TEST Pin This pin should be OPEN. |
| 12 | TEST4 | O | TEST Pin This pin should be OPEN. |
| 13 | VSS | - | Ground Pin |
| 14 | VDD | - | Power Supply Pin, 2.7 ~ 3.6V |
| 15 | CDTO | O | Control Data Output Pin, The output is “Hi-Z” when PDN pin = “L”. |
| | SDTI2 | I | Audio Serial Data Input 2 Pin |
| 16 | TX | O | Transmit Channel Output Pin, The output is “L” when PDN pin = “L” or RSTN bit = “0” or PW bit = “0” or MCLK stops. |

Note: All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS(VSS=0V; [Note 1](#))

| Parameter | Symbol | min | max | Units |
|--|--------|------|---------|-------|
| Power Supply | VDD | -0.3 | 4.6 | V |
| Input Current, Any Pin Except Supplies | IIN | - | ±10 | mA |
| Digital Input Voltage (Note 2) | VIND | -0.3 | VDD+0.3 | V |
| Ambient Temperature (Powered applied) | Ta | -20 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 1. All voltages with respect to ground.

Note 2. MCLK, BICK, SDTI1, LRCK, PDN, CSN, CCLK, CDTI, SDTI2

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS(VSS=0V; [Note 1](#))

| Parameter | Symbol | min | typ | max | Units |
|--------------|--------|-----|-----|-----|-------|
| Power Supply | VDD | 2.7 | 3.3 | 3.6 | V |

Note 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

DC CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|--------|---------|-----|--------|-------|
| Power Supply Current (Note 3) | | | | | |
| Normal Operation (PDN pin = "H", fs=44.1kHz) (Note 3) | | | 0.9 | 1.8 | mA |
| Full power-down mode (PDN pin = "L") (Note 4) | | | 10 | 50 | μA |
| High-Level Input Voltage | VIH | 70%VDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%VDD | V |
| High-Level Output Voltage (Iout=-80μA) | VOH1 | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80μA) | VOL1 | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

Note 3. TX pin: open . Power supply current (IDD@3.3V) is 1.0mA(typ)@fs=48kHz, 1.4mA(typ)@fs=96kHz and 2.6mA(typ)@fs=192kHz. IDD is 10μA(typ) if PDN= "L" and all other input pins are held to VSS(@3.3V).

(TX pin: 20pF, Power supply current (IDD@3.3V) is 3.3mA(typ)@fs=192kHz.)

Note 4. All digital input pins are fixed to VDD or VSS.

TX CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|---------|-----|-----|-------|
| High-Level Output Voltage (Iout=-400μA) | VOH2 | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=400μA) | VOL2 | - | - | 0.4 | V |
| Load Capacitance | CL | - | - | 50 | pF |

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD=2.7 ~ 3.6V, CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|--------------------------------------|--------|-------|-----|--------|-------|
| Master Clock Frequency | | | | | |
| Frequency | fCLK | 2.048 | | 36.864 | MHz |
| Duty Cycle | dCLK | 40 | | 60 | % |
| LRCK Frequency | | | | | |
| Frequency | fs | 8 | | 192 | kHz |
| Duty Cycle | dCLK | 45 | | 55 | % |
| Audio Interface Timing | | | | | |
| BICK Period | tBCK | 81 | | | ns |
| BICK Pulse Width Low | tBCKL | 30 | | | ns |
| Pulse Width High | tBCKH | 30 | | | ns |
| BICK “↑” to LRCK Edge (Note 5) | tBLR | 20 | | | ns |
| LRCK Edge to BICK “↑” (Note 5) | tLRB | 20 | | | ns |
| SDTI Hold Time | tSDH | 20 | | | ns |
| SDTI Setup Time | tSDS | 20 | | | ns |
| Control Interface Timing | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 40 | | | ns |
| CDTI Hold Time | tCDH | 40 | | | ns |
| CSN “H” Time | tCSW | 150 | | | ns |
| CSN “↓” to CCLK “↑” | tCSS | 150 | | | ns |
| CCLK “↑” to CSN “↑” | tCSH | 50 | | | ns |
| CDTO Delay | tDCD | | | 45 | ns |
| CSN “↑” to CDTO Hi-Z | tCCZ | | | 70 | ns |
| Power-Down & Reset Timing | | | | | |
| PDN Pulse Width (Note 6) | tPD | 150 | | | ns |

Note 5. BICK rising edge must not occur at the same time as LRCK edge.

Note 6. The AK4104 can be reset by bringing PDN pin = “L”.

■ Timing Diagram

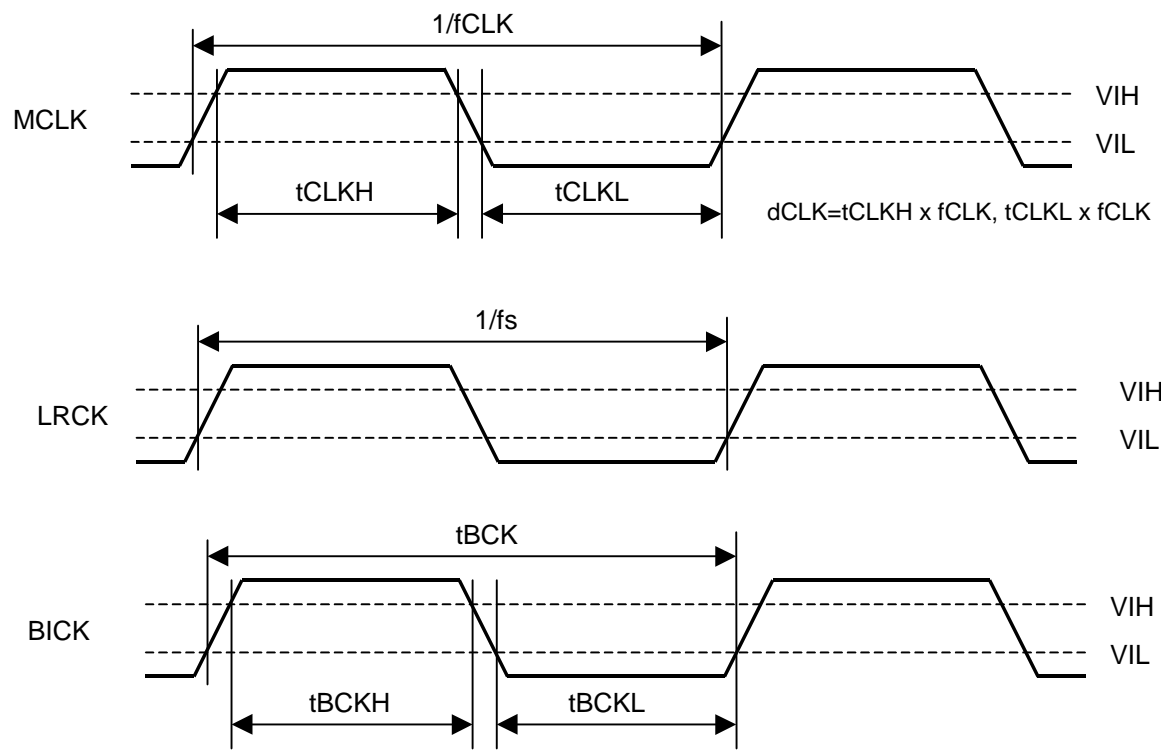


Figure 3. Clock Timing

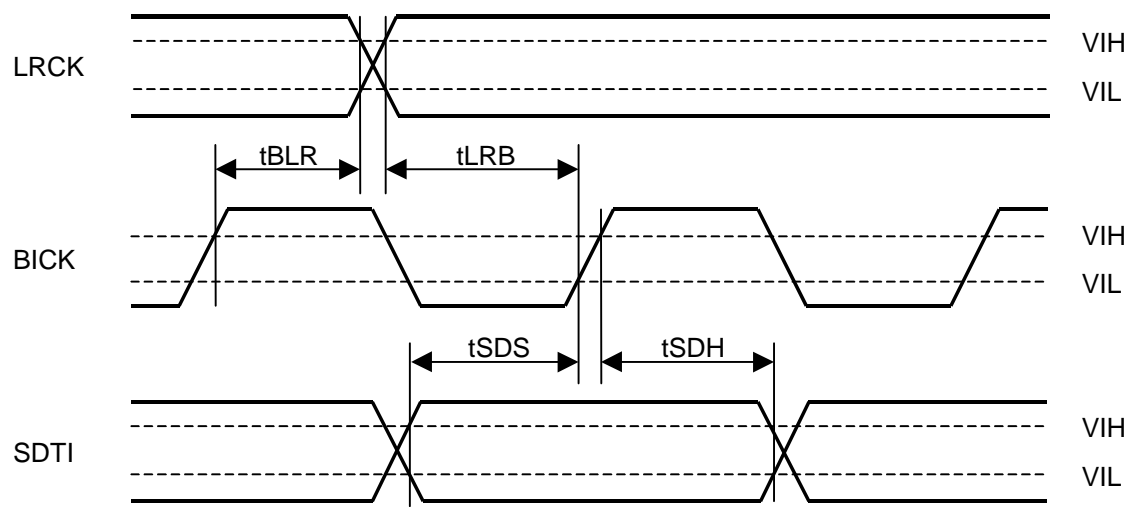


Figure 4. Serial Interface Timing

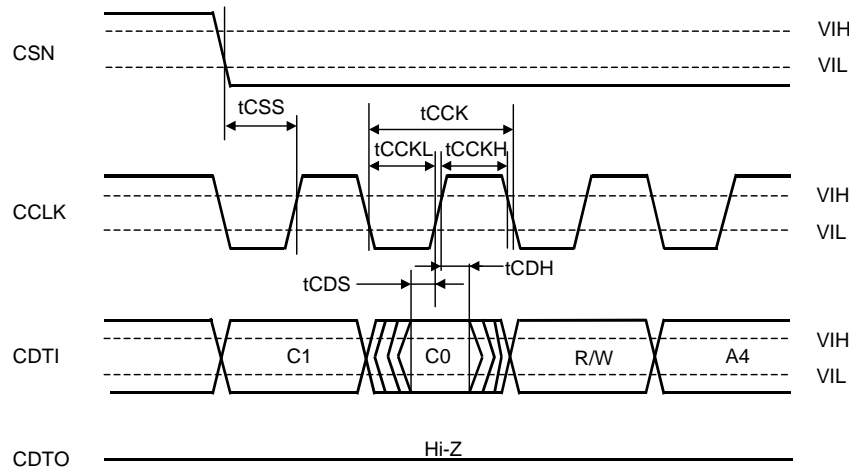


Figure 5. WRITE/READ Command Input Timing in 3-wire/4-wire serial mode

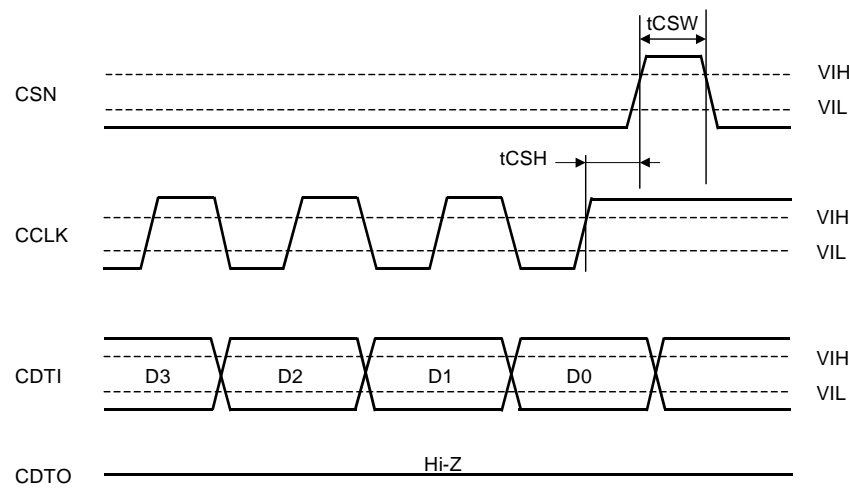


Figure 6. WRITE Data Input Timing in 3-wire/4-wire serial mode

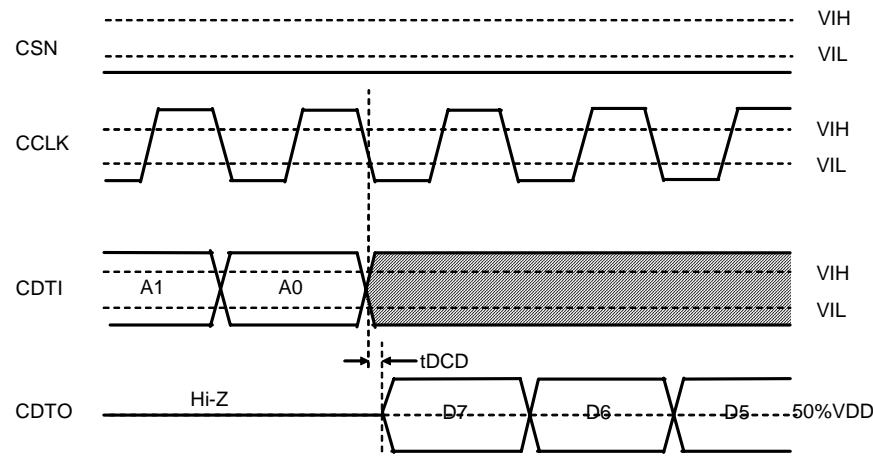


Figure 7. READ Data Output Timing 1 in 4-wire serial mode

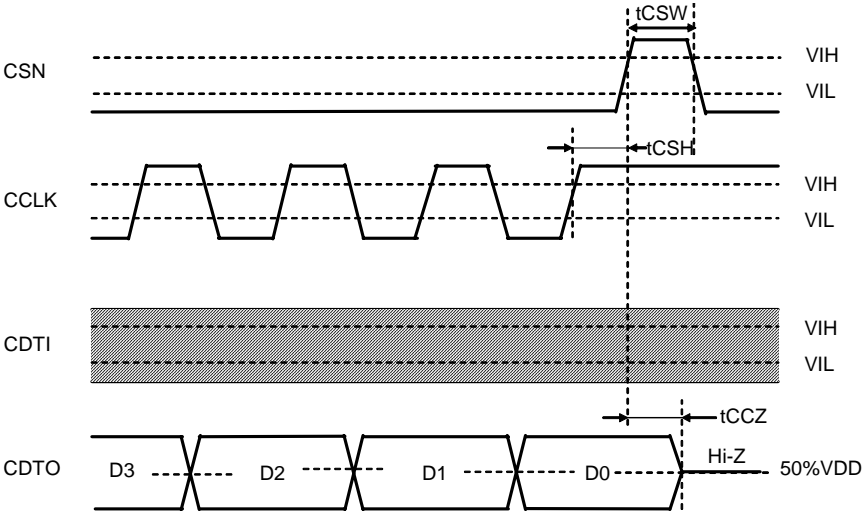


Figure 8. READ Data Output Timing 2 in 4-wire serial mode

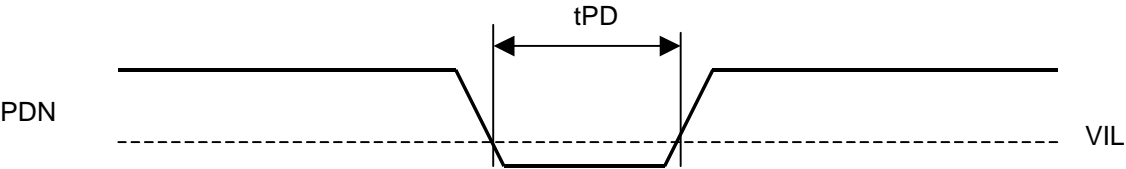


Figure 9. Power-Down & Reset Timing

OPERATION OVERVIEW**■ Reset and Initialization**

The AK4104 should be reset once by bringing PDN = “L” upon power-up. It takes 8 bit clock cycles for the AK4104 to initialize after PDN pin goes “H”.

■ MCLK and LRCK Relationship

For correct synchronization, MCLK and LRCK should be derived from the same clock signal either directly (as through a frequency divider) or indirectly (for example, as through a DSP). The phase relationship between MCLK and LRCK should be kept after power-up. The MCLK frequencies shown in [Table 1](#) are supported. The internal clock frequency is set depending on the external MCLK frequency automatically.

| MCLK | Fs |
|--------|------------|
| 128fs | 16k-192kHz |
| 192fs | 16k-192kHz |
| 256fs | 8k-128kHz |
| 384fs | 8k-96kHz |
| 512fs | 8k-48kHz |
| 768fs | 8k-48kHz |
| 1024fs | 8k-32kHz |
| 1536fs | 8k-24kHz |

Table 1. MCLK Frequency

■ Audio Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF1-0 bits as shown in [Table 2](#) can select four serial data modes. In all modes the serial data is MSB-first, 2's complement format and is latched on the rising edge of BICK. Mode 3 can be used for 16bit I²S Compatible format by zeroing the unused LSBs at BICK \geq 48fs or BICK = 32fs.

| Mode | DIF1 | DIF0 | SDTI Format | BICK | Figure |
|------|------|------|---------------------------------------|----------------------------|---------------------------|
| 0 | 0 | 0 | 16bit, LSB justified | $\geq 32\text{fs}$ | Figure 10 |
| 1 | 0 | 1 | 24bit, LSB justified | $\geq 48\text{fs}$ | Figure 11 |
| 2 | 1 | 0 | 24bit, MSB justified | $\geq 48\text{fs}$ | Figure 12 |
| 3 | 1 | 1 | 16/24bit, I ² S Compatible | $\geq 48\text{fs}$ or 32fs | Figure 13 |

Table 2. Audio Interface Format

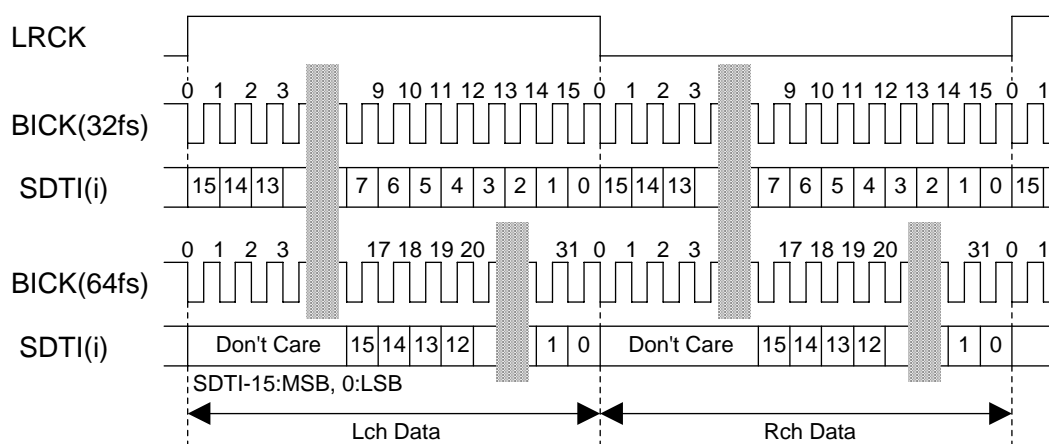


Figure 10. Mode 0 Timing

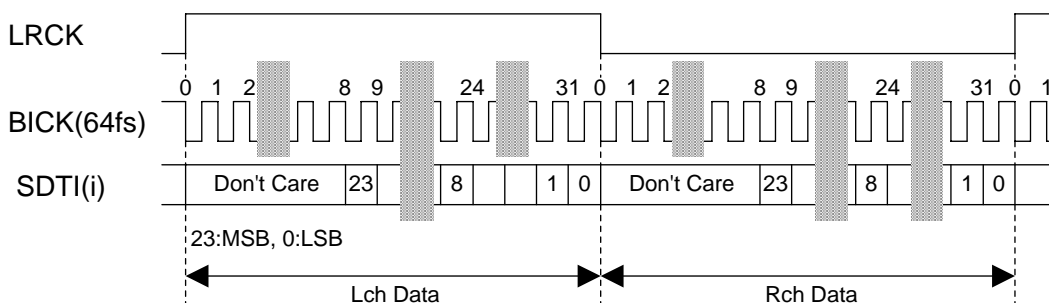


Figure 11. Mode 1 Timing

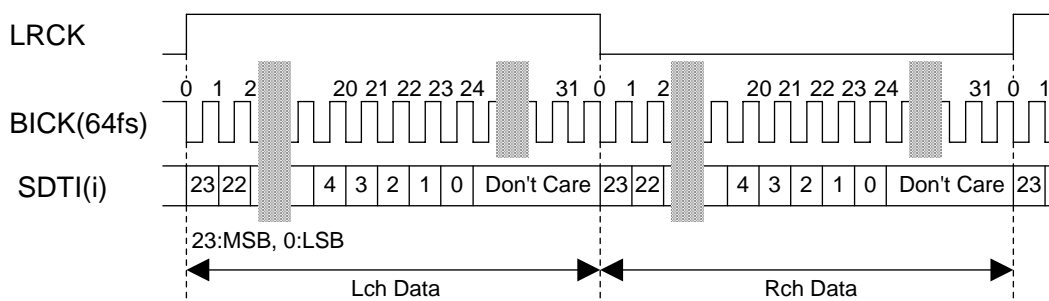


Figure 12. Mode 2 Timing

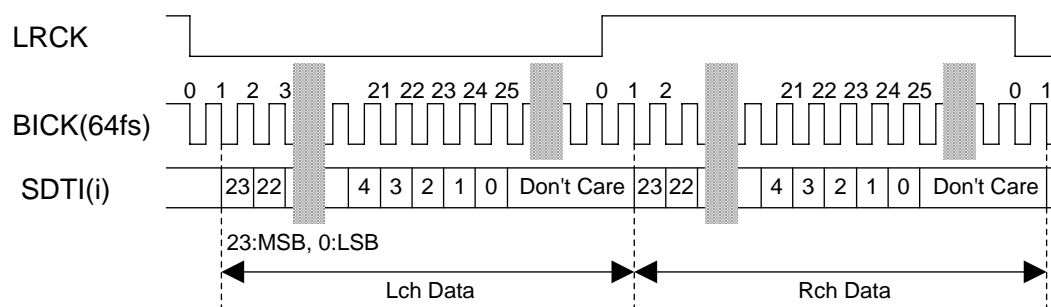


Figure 13. Mode 3 Timing

■ DIT input select

The AK4104 can select 4-wire μ P I/F mode (MODE bit = "0") or 3-wire μ P I/F mode (MODE bit = "1"). In 3-wire μ P I/F mode, the AK4104 can select the input data of DIT from SDTI1 or SDTI2 data.

| MODE | SEL1 | SEL0 | μ P I/F | DIT input |
|------|------|------|-------------|------------------|
| 0 | x | x | 4-wire | SDTI1 |
| 1 | 0 | 0 | 3-wire | SDTI1 |
| 1 | 0 | 1 | 3-wire | SDTI2 |
| 1 | 1 | 0 | 3-wire | SDTI2:DIT Bypass |
| 1 | 1 | 1 | Reserved | |

(x: Don't care)

Table 3. DIT Input

■ Data Transmission Format

The Data transmitted on the TX outputs is formatted in blocks as shown in Figure 14. Each block consists of 192 frames. A frame of data contains two sub-frames. A sub-frame consists of 32 bits of information. Each received data bit is coded using a bi-phase mark encoding as a two binary state symbol. The preambles violate bi-phase encoding so they may be differentiated from data. In bi-phase encoding, the first state of input symbol is always the inverse of the last state of the previous data symbol. For a logic 0, the second state of the symbol is the same as the first state. For a logic 1, the second state is opposite of the first. Figure 15 illustrates a sample stream of 8 data bits encoded in 16 symbol states.

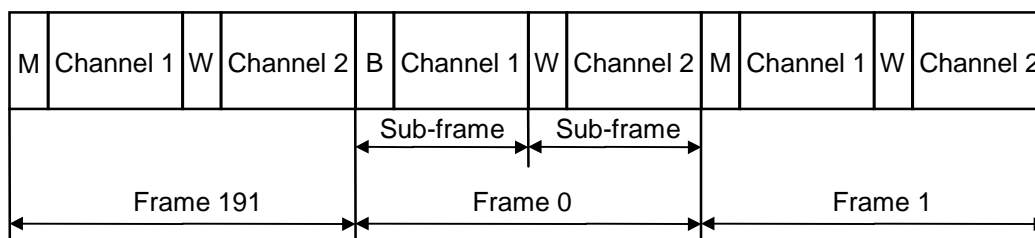


Figure 14. Block format

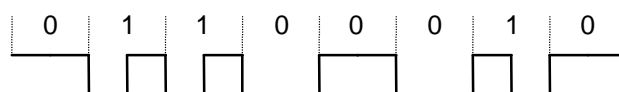


Figure 15. A biphas-encoded bit stream

The sub-frame is defined in Figure 16 below. Bits 0-3 of the sub-frame represent a preamble for synchronization. There are three preambles. The block preamble, B, is contained in the first sub-frame of Frame 0. The channel 1 preamble, M, is contained in the first sub-frame of all other frames. The channel 2 preamble, W, is contained in all of the second sub-frames.

Table 4 below defines the symbol encoding for each of the preambles. Bits 4-27 of the sub-frame contain the 24 bit audio sample in 2's complement format with bit 27 as the most significant bit. For 16 bit mode, Bits 4-11 are all 0. Bit 28 is the validity flag. It is "H" if the audio sample is unreliable. Bit 29 is a user data bit. Frame 0 contains the first bit of a 192 bit user data word. Frame 191 contains the last bit of the user data word. Bit 30 is a channel status bit. Again frame 0 contains the first bit of the 192 bit word with the last bit in frame 191. Bit 31 is an even parity bit for bits 4-31 of the sub-frame.

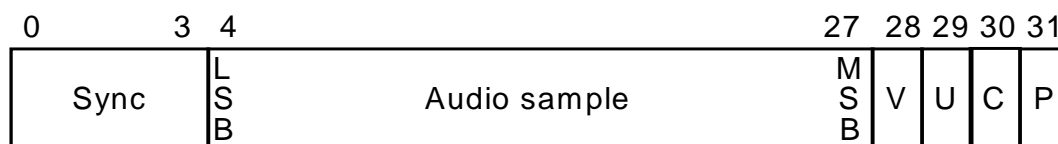


Figure 16. Sub-frame format

The block of data contains consecutive frames transmitted at a state-bit rate of 64 times the sample frequency, f_s . For stereophonic audio, the left or A channel data is in channel 1 while the right or B data is in channel 2. For monophonic audio, channel 1 contains the audio data.

| Preamble | Preceding state = 0 | Preceding state = 1 |
|----------|---------------------|---------------------|
| B | 11101000 | 00010111 |
| M | 11100010 | 00011101 |
| W | 11100100 | 00011011 |

Table 4. Sub-frame preamble encoding

Channel Status bit

In the consumer mode (bit0 = "0"), bits20-23(audio channel) must be controlled by the CT20 bit. When the CT20 bit is "1", the AK4104 corresponds to "stereo mode", bits20-23 are set to "1000"(left channel) in sub-frame 1, and is set to "0100"(right channel) in sub-frame 2. When the CT20 bit is "0", bits20-23 is set to "0000" in both sub-frame 1 and sub-frame 2.

■ μ P Control Interface

The AK4104 can select 4-wire μ P I/F mode (MODE bit = "0") or 3-wire μ P I/F mode (MODE bit = "1").

1.4-wire Serial mode (MODE bit = "0", default)

The internal registers may be either written or read by the 4-wire μ P interface pins: CSN, CCLK, CDTI and CDTO. The data on this interface consists of Chip address (2bits, C1/0; fixed to "11"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. CSN should be set to "H" once after the 16th CCLK. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN pin = "L" resets the registers to their default values.

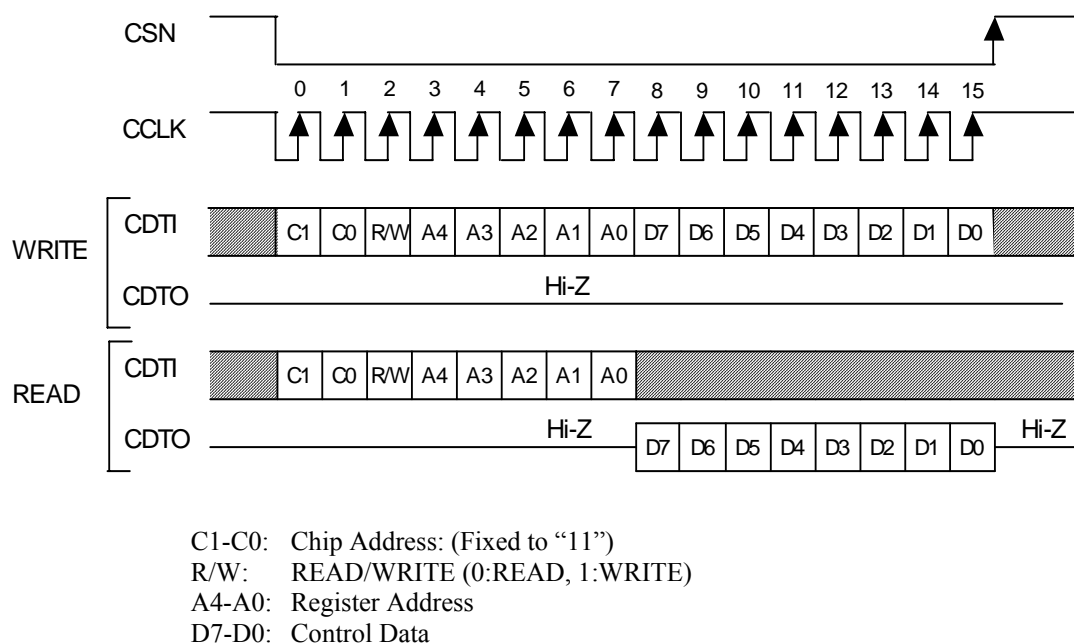


Figure 17. 4-wire μ P I/F Timing

*When the AK4104 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.

2.3-wire μ P I/F mode (MODE bit = "1")

Internal registers may be written by 3-wire μ P interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "11"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4104 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by 16th CCLK after a high to low transition of CSN. CSN should be set to "H" once after the 16th CCLK. The clock speed of CCLK is 5MHz (max).

PDN pin = "L" resets the registers to their default values. The internal timing circuit is reset by RSTN bit, but the registers are not initialized.

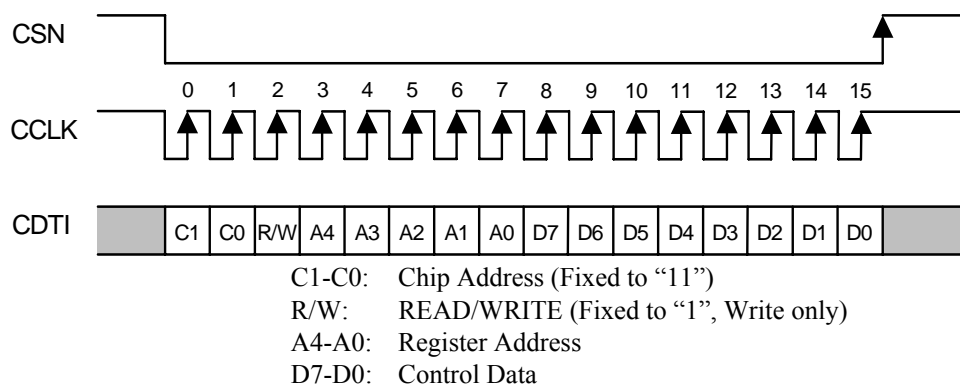


Figure 18. 3-wire μ P I/F Timing

*The AK4104 does not support the read command and chip address. C1/0 and R/W are fixed to "011"

*When the AK4104 is in the power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|------|------|------|------|------|------|------|------|
| 00H | Control 1 | 1 | 0 | 0 | 0 | DIF1 | DIF0 | PW | RSTN |
| 01H | Reserved | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 02H | Control 2 | 0 | 0 | 0 | 0 | 0 | MODE | SEL1 | SEL0 |
| 03H | TX | 1 | 0 | 0 | 0 | 0 | 0 | V | TXE |
| 04H | Channel Status Byte0 | CS7 | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| 05H | Channel Status Byte1 | CS15 | CS14 | CS13 | CS12 | CS11 | CS10 | CS9 | CS8 |
| 06H | Channel Status Byte2 | CS23 | CS22 | CS21 | CS20 | CS19 | CS18 | CS17 | CS16 |
| 07H | Channel Status Byte3 | CS31 | CS30 | CS29 | CS28 | CS27 | CS26 | CS25 | CS24 |
| 08H | Channel Status Byte4 | CS39 | CS38 | CS37 | CS36 | CS35 | CS34 | CS33 | CS32 |
| 09H | Channel Status Byte5 | 0 | 0 | 0 | 0 | 0 | 0 | CS41 | CS40 |

Notes:

For addresses from 0AH to 1FH, data must not be written.

When PDN pin goes “L”, the registers are initialized to their default values.

When RSTN bit goes “0”, the only internal timing is reset and the registers are not initialized to their default values. All data can be written to the register even if PW or RSTN bit is “0”.

The “0” register should be written “0”, the “1” register should be written “1” data.

■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|---------------|-----|----|----|----|------|------|----|------|
| 00H | Control 1 | 1 | 0 | 0 | 0 | DIF1 | DIF0 | PW | RSTN |
| R/W | | R/W | | | | | | | |
| Default | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

RSTN: Internal timing reset control

0: Reset. All registers are not initialized.

1: Normal Operation

PW: Power down control

0: Power down. All registers are not initialized.

1: Normal Operation

DIF1-0: Audio data interface formats ([Table 2](#))

Initial: “11”, Mode 3

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|---------------|-----|----|----|----|----|------|------|------|
| 02H | Control 3 | 0 | 0 | 0 | 0 | 0 | MODE | SEL1 | SEL0 |
| | R/W | R/W | | | | | | | |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MODE: Mode Control

0: 4 wire mode

1: 3 wire mode

SEL1-0: DIT input

00: SDTI1 input

01: SDTI2 input

10: SDTI2 input (DIT Bypass)

11: Reserved

(NOTE) SEL1-0 bits can not use in 4 wire mode (MODE="0").

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|---------------|-----|----|----|----|----|----|----|-----|
| 03H | TX | 1 | 0 | 0 | 0 | 0 | 0 | V | TXE |
| | R/W | R/W | | | | | | | |
| | Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

V: Validity Flag

0: Valid

1: Invalid

TXE: TX output

0: "L"

1: normal operation

| | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|----------------------|------|------|------|------|------|------|------|------|
| 04H | Channel Status Byte0 | CS7 | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | CS0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 05H | Channel Status Byte1 | CS15 | CS14 | CS13 | CS12 | CS11 | CS10 | CS9 | CS8 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06H | Channel Status Byte2 | CS23 | CS22 | CS21 | CS20 | CS19 | CS18 | CS17 | CS16 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07H | Channel Status Byte3 | CS31 | CS30 | CS29 | CS28 | CS27 | CS26 | CS25 | CS24 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08H | Channel Status Byte4 | CS39 | CS38 | CS37 | CS36 | CS35 | CS34 | CS33 | CS32 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09H | Channel Status Byte5 | 0 | 0 | 0 | 0 | 0 | 0 | CS41 | CS40 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CS7-0: Transmitter Channel Status Byte 0

Default: "00000100"

CS39-8: Transmitter Channel Status Byte 4-1

Default: "00000000"

CS41-CS40: Transmitter Channel Status Byte 5

Default: "00000000", D7-D2 bits should be written "1".

SYSTEM DESIGN

Figure 19 and Figure 20 show the system connection diagram. The evaluation board AKD4104 demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

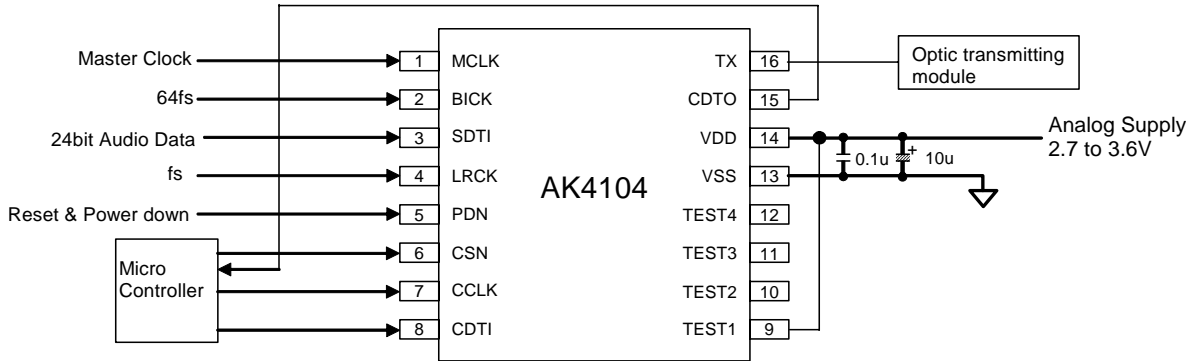


Figure 19. Typical Connection Diagram (Mode= "0", 4 wire mode)

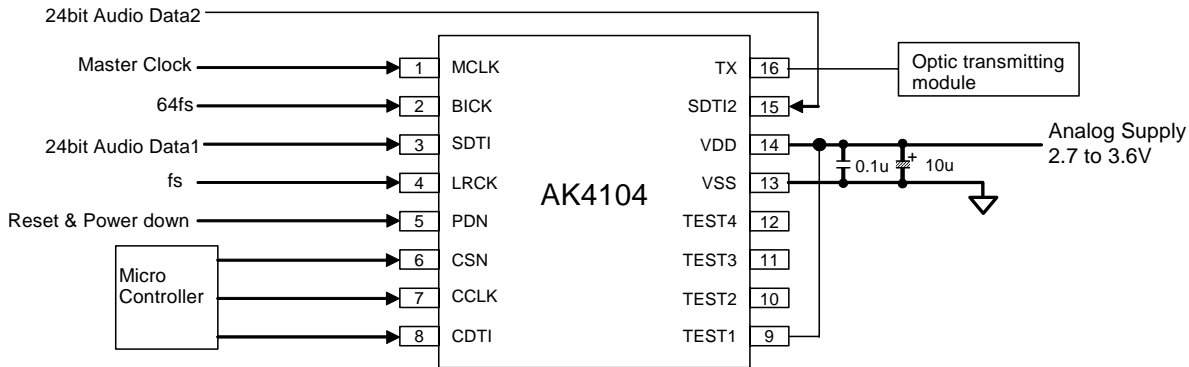
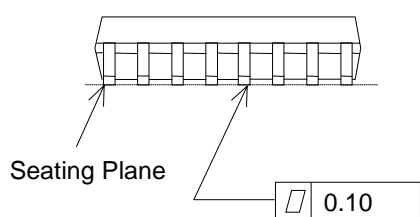
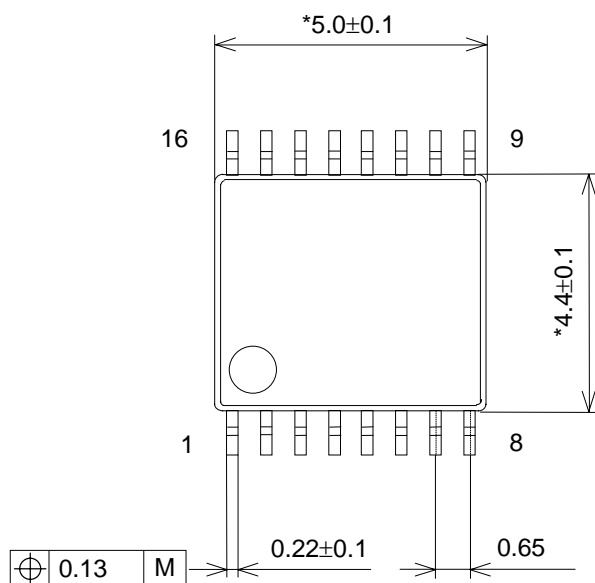


Figure 20. Typical Connection Diagram (Mode= "1", 3 wire mode)

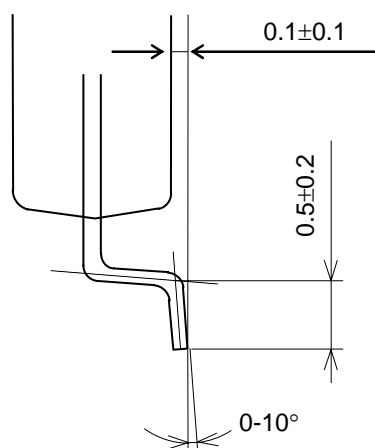
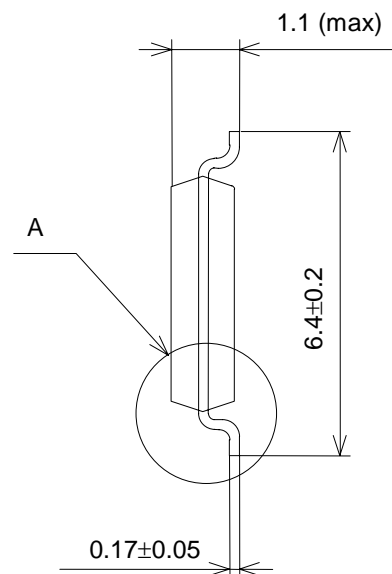
| |
|----------------|
| PACKAGE |
|----------------|

16pin TSSOP (Unit: mm)



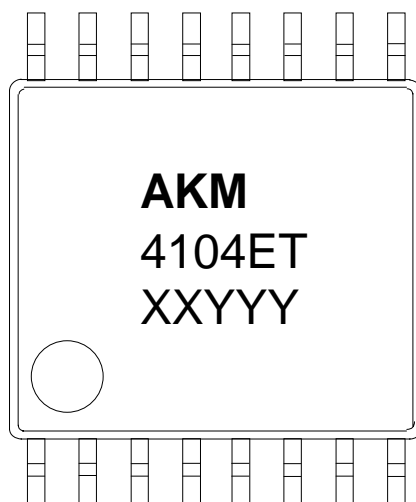
NOTE: Dimension "*" does not include mold flash.

Detail A



■ Package & Lead frame material

| | |
|-------------------------------|------------------------|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

MARKING

- 1) Pin #1 indication
- 2) Date Code : XXYYY (5 digits)
XX: Lot#
YYY: Date Code
- 3) Marketing Code : 4104ET
- 4) Asahi Kasei Logo

REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|----------------------|------|---|
| 07/07/09 | 00 | First Edition | | |
| 10/09/28 | 01 | Specification Change | 19 | PACKAGE The package dimension was changed. |

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