



**FEATURES**

- Ultra Low Dropout - 0.2V(typical) at 1A Output Current
- Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit and Thermal Shutdown Protection
- Power-OK Output with a Delay Time
- ESOP-8 and DFN 2x2 Pb-Free Packages.

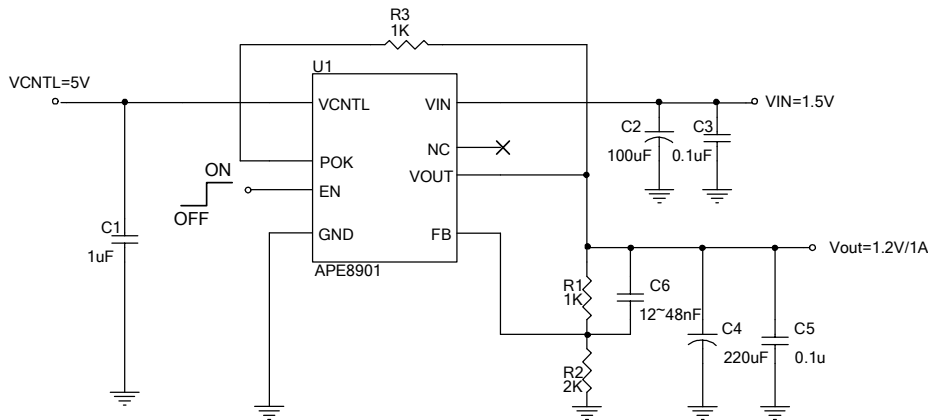
**DESCRIPTION**

The APE8901 is a 1A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8901 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The APE8901 can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

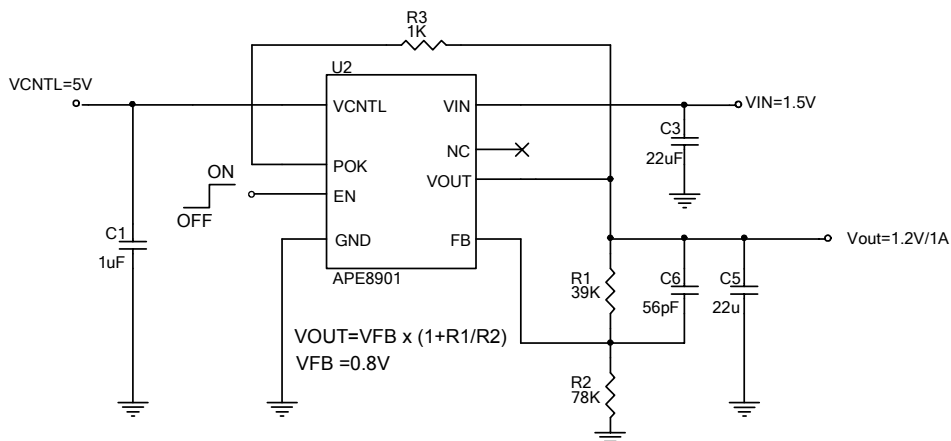
The APE8901 is available in ESOP-8 and DFN 2x2 packages. That features small size as SOP-8 with an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

**TYPICAL APPLICATION CIRCUIT**

**1. Using an Output Capacitor with  $ESR \geq 20m\Omega$**



**2. Using an MLCC as the Output Capacitor**





**ABSOLUTE MAXIMUM RATINGS** (at  $T_A=25^{\circ}\text{C}$ )

VCNTL Supply Voltage ( $V_{\text{CNTL}}$ )	-----	-0.3V to 7V
VIN Supply Voltage ( $V_{\text{IN}}$ )	-----	-0.3V to 6V
EN & FB Pin Voltage ( $V_{\text{I/O}}$ )	-----	-0.3V to $V_{\text{CNTL}}+0.3\text{V}$
Power Voltage ( $V_{\text{POK}}$ )	-----	-0.3V to 7V
Power Dissipation ( $P_D$ )		
	ESOP-8 -----	3W
	DFN 2x2 -----	0.8W
Storage Temperature Range ( $T_{\text{ST}}$ )	-----	-65°C To 150°C
Junction Temperature Range ( $T_J$ )	-----	-40°C To 125°C
Operating Temperature Range ( $T_{\text{OP}}$ )	-----	-40°C To 85°C
Thermal Resistance Junction to Ambient ( $R_{\text{thja}}$ )		
	ESOP-8 -----	40°C/W
	DFN 2x2 -----	125°C/W
Thermal Resistance Junction to Case ( $R_{\text{thjc}}$ )		
	ESOP-8 -----	15°C/W
	DFN 2x2 -----	20°C/W

Note.  $R_{\text{thja}}$  is measured with the PCB copper area (need connect to Expose-Pad) of approximately 1.5 irf<sup>2</sup> (Multi-layer) by ESOP-8 and DFN-8L packages.

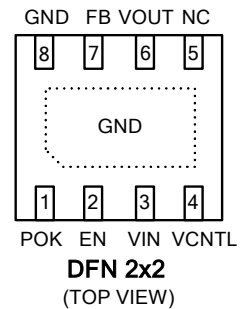
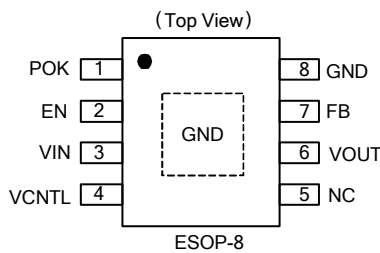
**RECOMMENDED OPERATING CONDITIONS**

$V_{\text{CNTL}}$ Supply Voltage ( $V_{\text{CNTL}}$ )	-----	3V to 6V
VIN Supply Voltage ( $V_{\text{IN}}$ )	-----	1V to 5.5V
Output Voltage ( $V_{\text{OUT}}$ )	-----( $V_{\text{CNTL}}-V_{\text{OUT}} > 1.9\text{V}$ )-----	0.8V to 2.8V
Output Current ( $I_{\text{OUT}}$ )	-----	0 to 1A

**ORDERING / PACKAGE INFORMATION**

**APE8901X**

Package Type  
MP : ESOP-8  
GN2 : DFN 2x2





**ELECTRICAL SPECIFICATIONS**

( $V_{CNTL} = 5V$ ,  $V_{IN} = 1.5V$ ,  $V_{OUT} = 1.2V$ ,  $T_A = 25^\circ C$  unless otherwise specified)

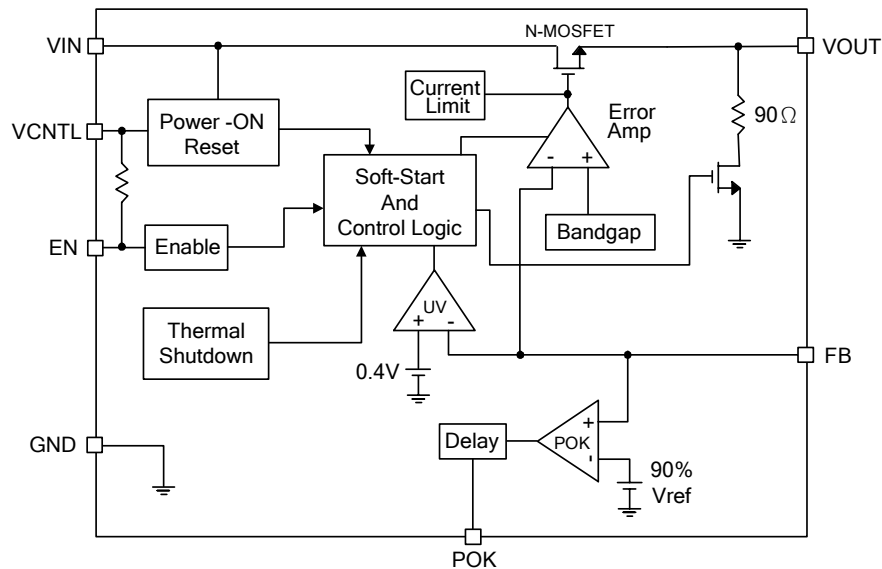
Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VCNTL POR Threshold	$V_{CNTL}$		2.5	2.7	2.9	V
VCNTL POR Hysteresis	$V_{CNTL(hys)}$		-	0.4	-	V
VIN POR Threshold	$V_{IN}$		0.8	0.9	1	V
VIN POR Hysteresis	$V_{IN(hys)}$		-	0.5	-	V
VCNTL Nominal Supply Current	$I_{CNTL}$	EN= $V_{CNTL}$	0.4	1	2	mA
VCNTL Shutdown Current	$I_{SD}$	EN= 0V	-	10	30	uA
Feedback Voltage	$V_{FB}$	$V_{CNTL} = 3 \sim 6.0V$	0.784	0.8	0.816	V
Load Regulation		$I_{OUT} = 0A \sim 1A$	-	0.06	0.25	%
Dropout Voltage	$V_{DROP}$	$V_{OUT} < 2.0V, I_{OUT} = 1A$	-	200	250	mV
		$2.0V < V_{OUT} < 2.8V, I_{OUT} = 1A$	-	250	300	
VOU Pull Low Resistance		EN=0V	-	90	120	$\Omega$
Soft Start Time	$T_{SS}$		-	2	-	ms
EN Pin Logic High Threshold Voltage	$V_{ENH}$	Enable	1.2	-	-	V
	$V_{ENL}$	Disable	-	-	0.4	
EN Hysteresis			-	50	-	mV
EN Pin Pull-Up Current	$I_{EN}$	EN=GND	-	10	-	uA
Current Limit	$I_{LIM}$	$V_{CNTL} = 3 \sim 6.0V, T_J = -40 \sim 125^\circ C$	1.2	-	-	A
Ripple Rejection	$\frac{V_{IN}}{V_{CNTL}}$	PSRR F=120Hz, $I_{OUT} = 100mA$	-	70	-	dB
			-	65	-	
Under-Voltage Threshold		VFB Falling	-	0.4	-	V
POK Threshold Voltage for Power OK	$V_{POK}$	VFB Rising	89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK	$V_{PNOK}$	VFB Falling	78%	81%	84%	VFB
POK Low Voltage		POK sinks 5mA	-	0.25	0.4	V
POK Delay Time	$T_{DELAY}$		0.8	2	10	mS
Thermal Shutdown Temp	TSD		-	150	-	$^\circ C$
Thermal Shutdown Hysteresis			-	40	-	$^\circ C$

**PIN DESCRIPTIONS**

PIN SYMBOL	PIN DESCRIPTION
<b>FB</b>	Feedback Pin
<b>EN</b>	Internal Pull High. EN=High or Floating → Enable EN=Low → Shutdown Mode
<b>VIN</b>	Input voltage.
<b>POK</b>	Power OK Output Pin
<b>VCNTL</b>	CNTL Pin Input Voltage
<b>NC</b>	No connect
<b>VOUT</b>	Output Voltage
<b>GND</b>	GND Pin.



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

**FB**

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left( 1 + \frac{R1}{R2} \right) \quad (V)$$

Where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100kΩ.

**VIN**

Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

**VCNTL**

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

**POK**

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

**EN**

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, this pin is internal pulled up to VCNTL voltage, enabling the regulator.



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## **PIN DESCRIPTION**

### **VOUT**

Output of the regulator. Please connect Pin 6 using wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

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## **FUNCTION DESCRIPTION**

### **Power-On-Reset**

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

### **Internal Soft-Start**

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2ms.

### **Output Voltage Regulation**

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

### **Current-Limit**

The APE8901 monitors the current via the output NMOS and limits the maximum current to prevent load and APE8901 from damages during overload or short circuit conditions.

### **Under-Voltage Protection (UVP)**

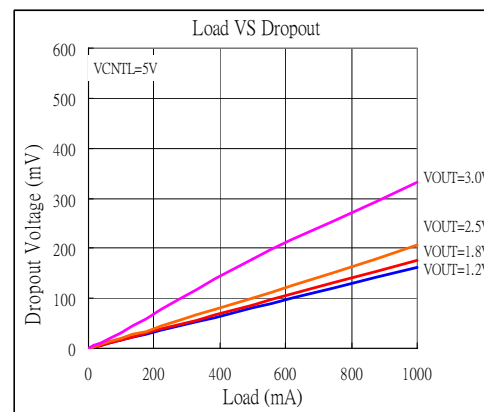
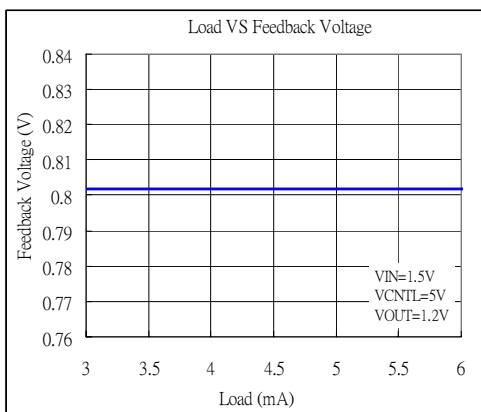
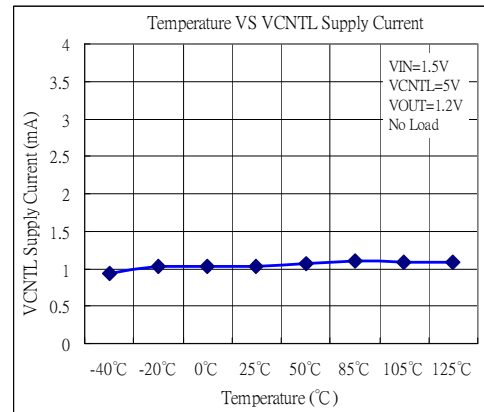
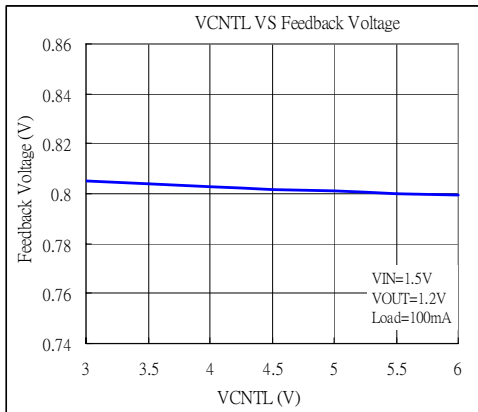
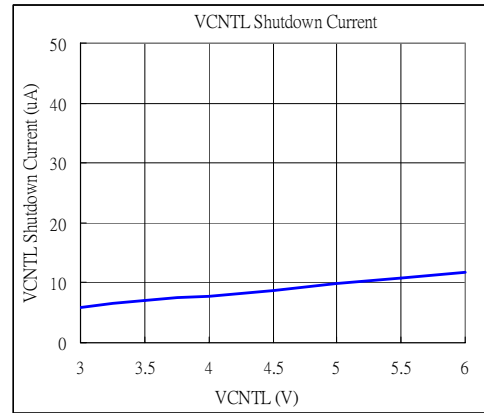
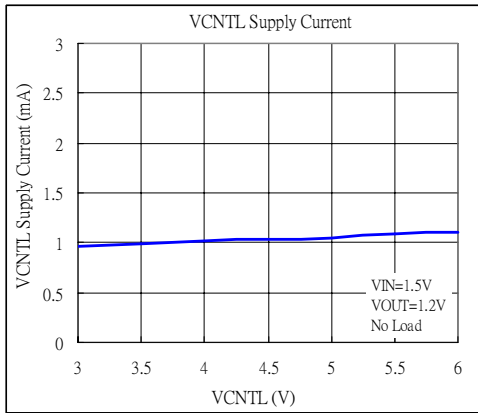
The APE8901 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APE8901 starts a new soft-start to regulate output.

### **Thermal Shutdown**

A thermal shutdown circuit limits the junction temperature of APE8901. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed

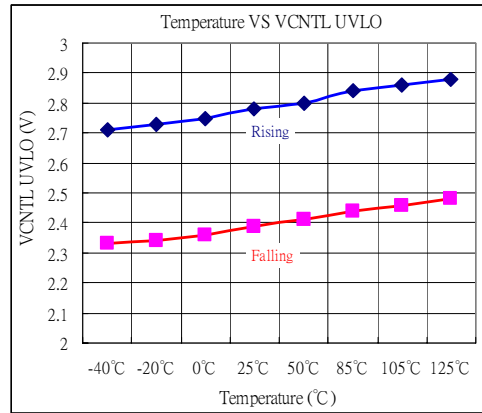
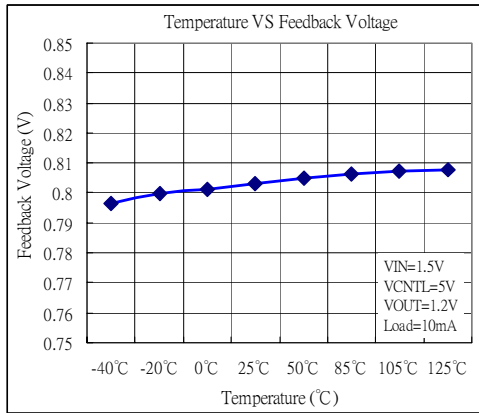


TYPICAL PERFORMANCE CHARACTERISTICS

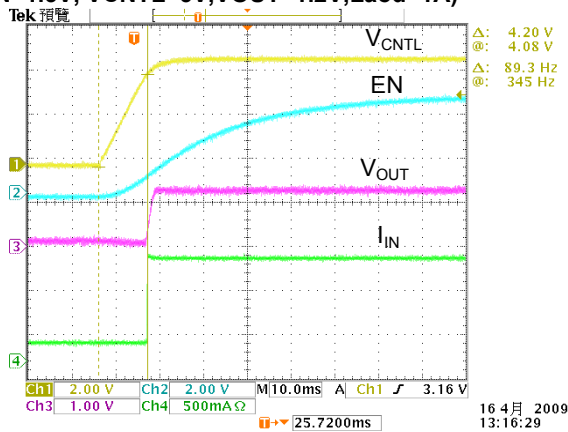




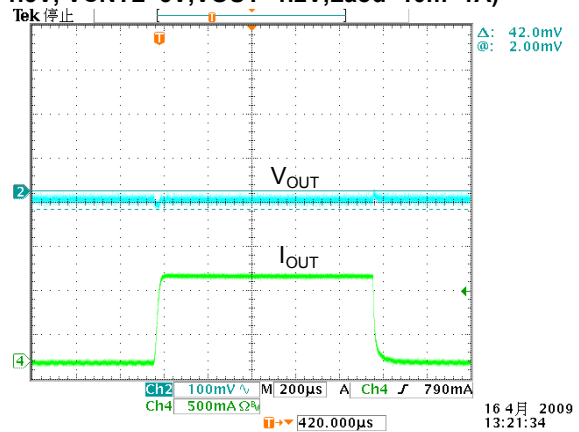
TYPICAL PERFORMANCE CHARACTERISTICS



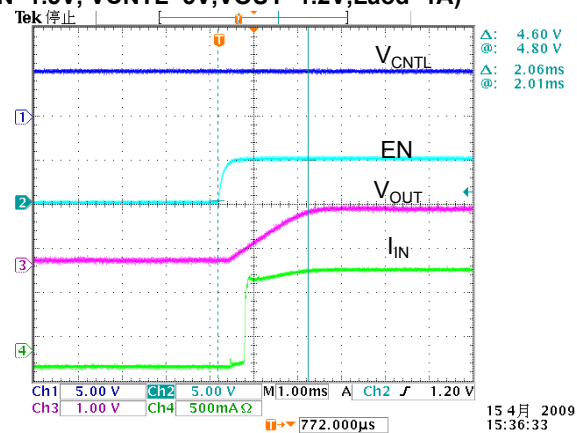
Power -ON  
(VIN=1.5V, VCNTL=5V, VOUT=1.2V, Laod=1A)



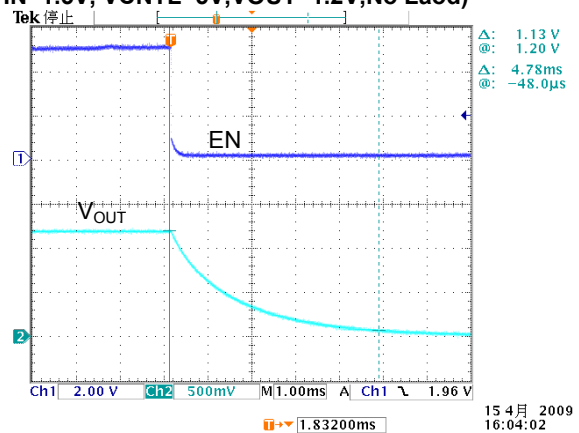
Load Transient  
(VIN=1.5V, VCNTL=5V, VOUT=1.2V, Laod=10m~1A)



Enable -ON  
(VIN=1.5V, VCNTL=5V, VOUT=1.2V, Laod=1A)



Enable -OFF  
(VIN=1.5V, VCNTL=5V, VOUT=1.2V, No Laod)





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**MARKING INFORMATION**

ESOP-8

