3A/23V High Efficiency Synchronous Rectified Step-Down DC/DC Converter

FEATURES

- Input Voltage Supply Range from 4.5V to 23V
- High Efficiency up to 90%
- Adjustable Output Voltage from 0.8V to 12V
- 3A Continuous Output Current
- 1MHz Constant Frequency Operation
- Current Mode Operation
- Programmable Soft-start
- Over-temperature Protection
- Over-current Protection
- Input Under Voltage Lockout
- 15 μA Shutdown Current
- ESOP-8 Package
- RoHS Compliant

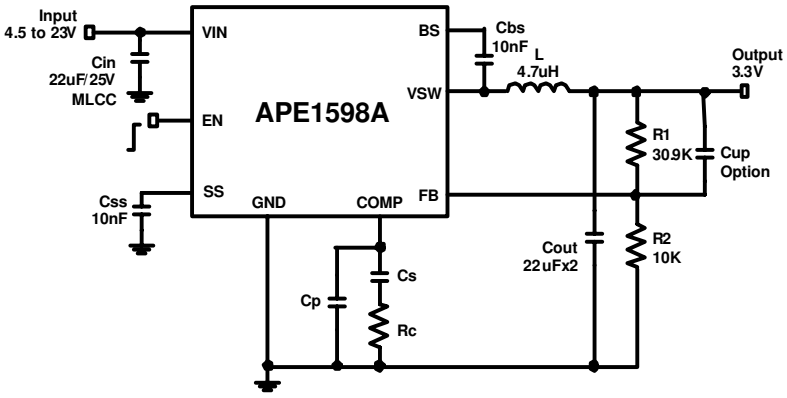
DESCRIPTION

The APE1598A is a high efficiency synchronous step-down DC/DC converter series with 3A continuous output current supplied. Included on the substrate with the features listed is a high performance trans-conductance error amplifier that provides tight voltage regulation and accuracy under transient conditions. A built-in under voltage lockout circuit is provided to prevent start-up until the input voltage reaches to 4.5V. In addition, it features over-current protection and thermal shutdown. The APE1598A is available in ESOP-8 package.

APPLICATION

- Data comm. xDSL CPE Graphics Cards
- Set-Top-Box, DVD
- Servers/Networking
- DSP and FPGA Power Supply
- Telecomm Equipments
- DC-DC Regulator Modules
- LCD Monitor and LCD TV

TYPICAL APPLICATION

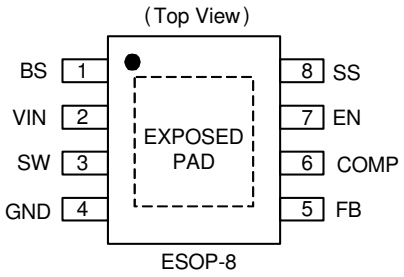


PACKAGE ORDERING INFORMATION

APE1598A X

Package Type

MP : ESOP-8



ABSOLUTE MAXIMUM RATINGS (at T_A=25℃)

Input Supply Voltage(V_{IN})	GND - 0.3V to +24V
SW PIN Voltage(V_{SW})	- 1V (-5V for 10nS) toVIN+0.3V
EN PIN Voltage(V_{EN})	- 0.3 to VIN+0.3V
Other Pins Voltage	- 0.3V to +6V
Boost Voltage	Vsw+6V
Power Dissipation(P_D)@T_A=25°C	1.96W
Storage Temperature Range(T_{ST})	-65℃ To 150℃
Junction Temperature Range(T_j)	-40℃ To 150℃
Lead Temperature (Soldering 10s)	260°C
Thermal Resistance from Junction to Case(Rth_{JC})	13℃/W
Thermal Resistance from Junction to Ambient(Rth_{JA})	51℃/W

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage(V_{IN})	4.5V to +23V
Operating Temperature	-30℃ To 85℃

Note 1: Stresses beyond above listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
Note 2: Guaranteed by design, not production tested.
Note3: For the measuring condition of Rth_{ja}, it is under the natural convection at T_A = 25°C and on a four-layer test board with highly effective thermal conductivity following the JEDEC 51-7 thermal measurement standard. As for the case position of Rth_{jc}, it is on the exposed pad of the package.

ELECTRICAL SPECIFICATIONS

(Recommended Operating Conditions, Unless Otherwise Noted; V_{IN} = 12V; T_A = 25 °C)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}		4.5	-	23	V
Shutdown Supply Current	I_{SD}	VEN = 0V	-	15	-	uA
Regulated Feedback Voltage		4.5V≦VIN≦23V	-	0.8	-	V
Error Amplifier Transconductance		$\triangle I_{COMP}$ = ±10uA	-	700	-	uA/V

ELECTRICAL SPECIFICATIONS

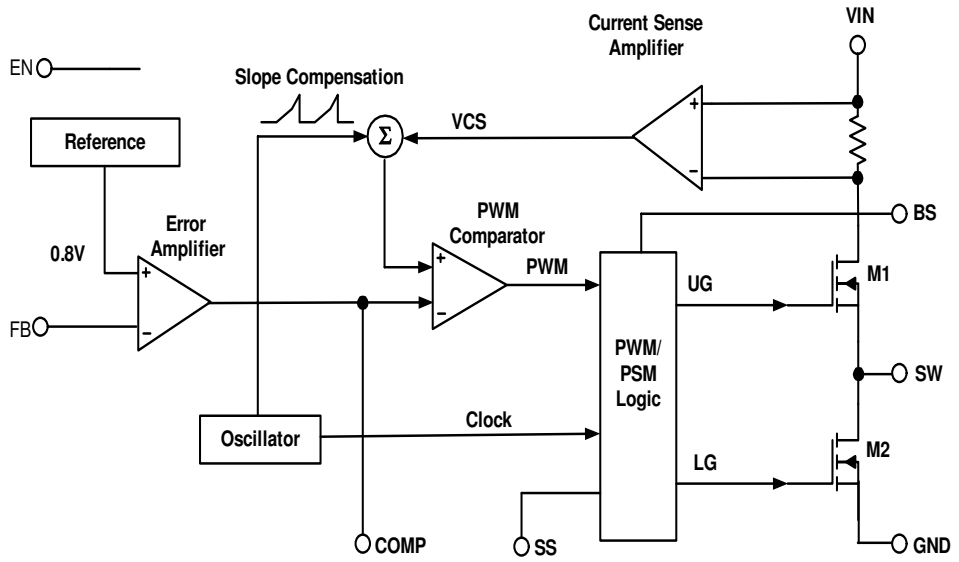
Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Sense to COMP Transconductance			-	2.2	-	A/V
Current Limit			-	4.5	-	A
SW Leakage Current		V_{EN} = 0V, V_{SW} = 0V	-	-	10	uA
High Side On Resistance			-	0.1	-	Ω
Low Side On Resistance			-	0.1	-	Ω
Oscillation Frequency			-	1	-	MHz
Short Circuit Oscillation Frequency		V_{FB}=0V	-	250	-	kHz
Maximum Duty Cycle		V_{FB}=0.7V	-	80	-	%
Minimum On Time			-	100	-	ns
Under Voltage Lockout Threshold		V_{IN} Rising	3.7	4	4.1	V
Under Voltage Lockout Threshold Hysteresis			-	400	-	mV
Thermal Shutdown Threshold			-	155	-	°C
EN High Level			-	2.35	-	V
EN Low Level			-	1.2	-	V
EN Input Current		V_{EN} = 0V	0.8	1	1.2	uA
Soft Start		C_{ss}=0.1uF	-	18	-	ms

Note: Fully production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
BS	It is required to connect SW and BS by a capacitor, which is able to boost the gate drive to the internal NMOS above VIN to fully turn it ON.
FB	This is the input to an error amplifier, which drives the PWM controller. It is necessary to connect this pin to the actual output of power supply to set the DC output voltage.
EN	This input provides an electrical ON/OFF control of the power supply. If the EN pin is open, it will be pulled to high by the internal circuit.
GND	This is the reference of the ground connection for all components in the power supply.
SW	This is the output of a power MOSFET switch.
V_{IN}	The input voltage for the power supply is connected to this pin.
SS	This pin is connected to an external capacitor to control soft-start timing. Connect a capacitor from SS to GND to set the soft-start period. A 0.1uF capacitor sets the soft-start period to 18ms.
COMP	This pin is to compensate the regulation control loop by connecting a series of RC network from COMP pin to GND pin.

BLOCK DIAGRAM



FUNCTION PIN DESCRIPTION

The APE1598A is a current mode PWM synchronous step-down converter with a constant switching frequency. It regulates the input voltage from 4.5V to 23V and a low output voltage of 0.8V.The supplied load current is up to 3A.

Pulse Skip Mode

The APE1598A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. A zero-cross sensing circuit monitors the low side N-MOSFET current for zero crossing. When the inductor current crossing zero is detected, the regulator enters the skip mode.

Oscillator Frequency

Slope compensated current mode PWM control provides not only stable switching and cycle-by-cycle current limit for superior load and line response but also protection of the internal main switch and synchronous rectifier. The APE1598A switches at a constant frequency (1MHz) and regulates the output voltage. The PWM comparator modulates the power transferred to the load by changing the inductor's peak current based on the feedback error voltage during each cycle. The main switch is turned on for a certain period to ramp the inductor's current at each rising edge of the internal oscillator under normal operation whereas off when the inductor's peak current is above the error voltage. After the main switch is turned off, the low side MOS will be turned on immediately and stay on until the next cycle starts.

Short Circuit Protection

The APE1598A provides short circuit protection. When the output is shorted to ground, the oscillator's frequency is reduced to prevent the inductor's current from increasing beyond the NMOS current limit. The NMOS current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.8V.

Maximum Load current

The APE1598A can operate down to 4.5V input voltage; however the maximum load current decreases at lower input due to large IR voltage drop on the main switch and low side switch. The slope compensation signal reduces the inductor's peak current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Enable

The EN pin provides electrical on/off control of the regulator. Once the voltage of the EN pin exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the voltage of the EN pin is pulled below the threshold, the regulator will stop switching and the internal slow start reset. If the EN pin is open, it will be pulled to high by the internal circuit.

Under Voltage Lockout

The APE1598A incorporates an under voltage lockout circuit to keep the device disabled when VIN is below the UVLO start threshold. During power-up, the internal circuit is held inactive until VIN exceeds the UVLO start threshold voltage. Once this threshold voltage is reached, device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteretic in the UVLO comparator is 400mV.

Soft-start

The built-in soft-start function is provided by APE1598A to reduce the input inrush current after power-on. If the SS pin is activated, it will provide about 150uS to make the duty transferred from small to specific duty during the power-on period. Thus this function can lower the current stress on input power, MOSFET, and freewheeling diode. The soft start time can be programmed by connecting this pin with a capacitor, which is defined as the following. A 0.1uF capacitor sets the soft-start period to 18ms.

$$Tss = \frac{Css \times Vref}{Iss}$$

Boost Capacitor

The BS pin and SW pin can be connected by a 10nF low ESR ceramic capacitor, providing the gate drive voltage for the high side MOSFET.

Thermal Shutdown

The APE1598A protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold, the voltage reference will be grounded and high side MOSFET turned off.

Compensation

The system stability is controlled through COMP pin. It will present a general design procedure to ensure a stable and operational circuit. The design in this data sheet is optimized for particular requirements. Some components may need to be changed to ensure stability if there are different requirements. First of all, the power components and their corresponding effects need to be determined. Following are the compensation components, which are to produce stability.

The compensation steps for the converter are listed below:

(1). Choose an appropriate inductor and output capacitance based on the allowed output voltage ripple and load transient.

(2). Placing FC as high as possible can respond quickly to the load transient. Considering the output capacitor's tolerances and temperature effects, typically place FC approximately 1/10 of FS for the multi-layer ceramic output capacitor (X5R, X7R). However, if the type of the output capacitor is the aluminum electrolytic or that largely variable with the temperature, place FC approximately 1/20 of F_S.

(3). Set the compensation RC to zero to cancel the R_{LOAD} C_{OUT} pole.

$$R_C = \frac{2\pi \times F_C \times C_{OUT} \times V_{OUT}}{G_M \times G_{CS} \times V_{REF}}$$

$$C_C = \frac{C_{OUT} \times R_{LOAD}}{R_C}$$

G_M : error amp transconductance
G_{CS} : current sense transconductance

(4). Determine CP if required. If Z_{ESR} (zero occurs by output capacitor ESR) is less than F_C, it should be cancelled with a pole set by capacitor C_P connected between C_C to GND.

$$C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$$

APPLICATION INFORMATION

Input Capacitor Selection

It is necessary for the input capacitor to sustain the ripple current produced during the period of "on" state of the upper MOSFET, so a low ESR is required to minimize the loss. The RMS value of this ripple can be obtained by the following:

$$I_{IN}RMS = I_{OUT}\sqrt{D\times(1-D)}$$

Where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. The loss of the input capacitor can be calculated by the following equation:

$$P_{CIN} = ESR_{CIN}\times I_{IN}RMS^{2}$$

Where P_{CIN} is the power loss of the input capacitor and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitor, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge-protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor selection is to meet the requirements of the output voltage ripple and affects the load transient response. The higher inductance can reduce the inductor's ripple current and induce the lower output ripple voltage. The ripple voltage and current can be approximately calculated approximated by the following equations:

$$\Delta I = \frac{V_{in}-V_{out}}{F_S\times L}\bullet\frac{V_{out}}{Vin}$$

$$\Delta V_{out} = \Delta I\times ESR$$

Although the increase of the inductance reduces the ripple current and voltage, it contributes to the decrease of the response time for the regulator to load transient as well. Increasing the switching frequency (Fs) for a given inductor also can reduce the ripple current and voltage but it will increase the switching loss of the power MOS.

The way to set a proper inductor value is to have the ripple current ($\triangle$ I) be approximately 10%~50% of the maximum output current. Once the value has been determined, select an inductor capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) is reasonable tolerance able to be met by most manufacturers. For some types of inductors, especially those with core made of ferrite, the ripple current will increase abruptly when it saturates, resulting in a larger output ripple voltage.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. The high capacitor value and low ESR will reduce the output ripple and the load transient drop. These requirements can be met by a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number Of Capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR
(assigned by the designer)
$\triangle I_{OUT}$ = load transient.
ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR_{MAX} = maximum allowable ESR.
High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. For the decoupling requirements, please consult the capacitor manufacturers for confirmation.

Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in the following AP Circuit. The output voltage (V_{OUT}) can be calculated according to the voltage of the FB pin (V_{FB}) and ratio of the feedback resistors by the following equation, where (V_{FB}) is 0.8V:

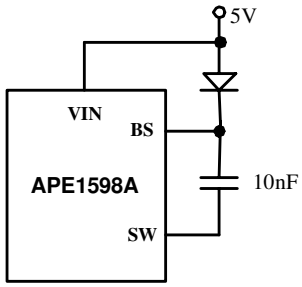
$$V_{FB} = V_{out} \times \frac{R_2}{(R_1 + R_2)}$$

Thus the output voltage is:

$$V_{out} = 0.8 \times \frac{(R_1 + R_2)}{R_2}$$

External Bootstrap Diode

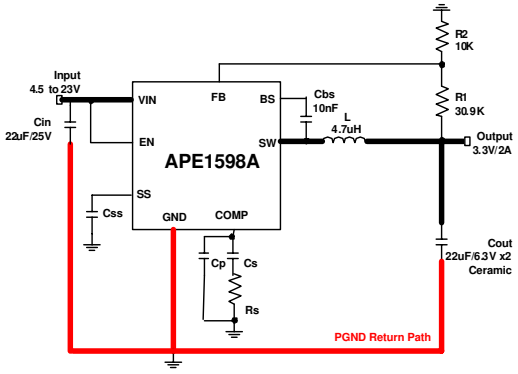
It is strongly recommended that an external bootstrap diode be added when there is a 5V fixed input for the system or the power supply generates a 5V output in order to improve the efficiency of the APE1598A regulator. The boost diode can be the one with lost cost such as IN4148 or BAT54.



This diode is also recommended for high duty cycle operation when Duty Cycle>65% (Example: V_{IN}=5V & V_{OUT}=3.3V; Duty Cycle=66%) and high output voltage (V_{OUT}>12V) applications.

Layout Consideration

For proper operation of the converter, some layout rules should be followed. It is necessary to understand which pin of APE1598A is sensitive and which is insensitive. Please refer the following for the location where noise comes from on the circuit and where the clear ground is for the small signal ground.



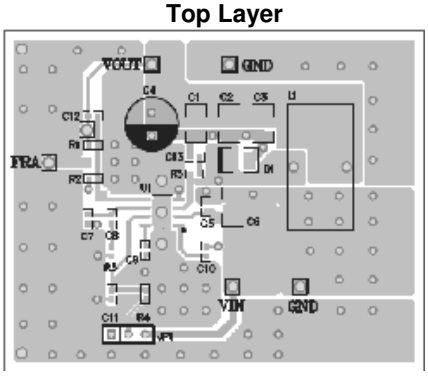
1.) First, put the input capacitor (CIN) as close as possible to the VIN pin.
2.) Secondly, place the Cs, Rs, Cp, Css and R2 as close as APE1598A and connect these analog grounds (Clear AGND) to APE1598A's GND pin. It is recommended to use a dot short for these AGND pins or connect the GND pin via contact.

3.) The large current loop shown in bold lines in the above figure circuit should be routed as short and wide as possible and the switch node is a high dv/dt. It easily couples noise to other traces by the capacitive path. Therefore the sensitive signals like FB, COMP and AGND should be routed away with this noise source.

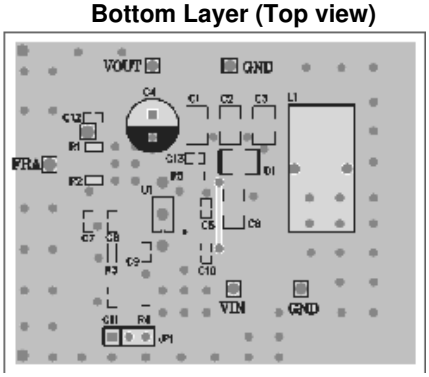
4.) The feedback network resistors (R1 & R2) should be routed away from the inductor and switch node to minimize noise and EMI issue. And the R1 resistor should be sensed the output capacitor or device loading, not the inductor's output node.

PCB Layout Guide

Top Layer

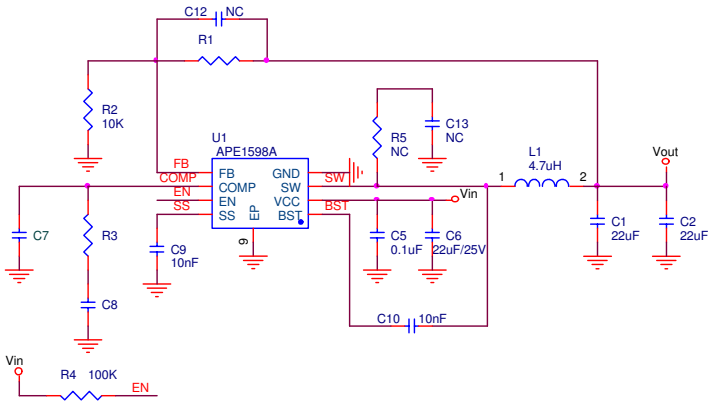


Bottom Layer (Top view)



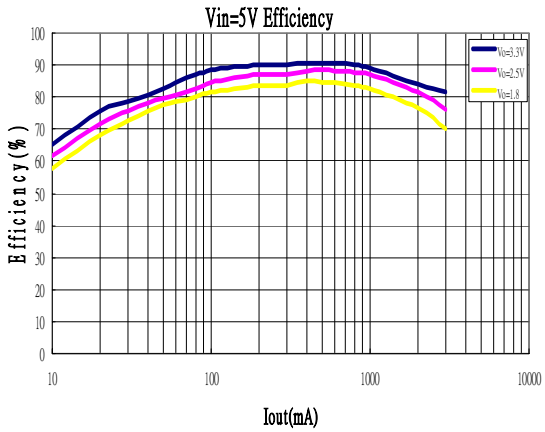
APE1598A EVB Schematic

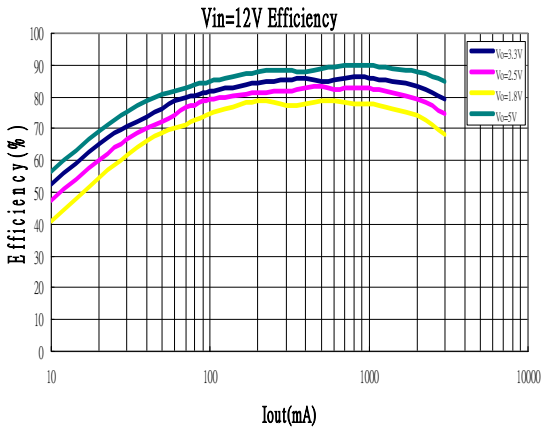
Application



Qty	Ref	Value		Description	Package
2	C1, C2,	22µF		Ceramic Capacitor X5R 16V	1206
1	C6	22uF		Ceramic Capacitor X5R 25V	1206
1	C5	0.1µF		Ceramic Capacitor	0603
1	L1	4.7uH		Inductor, Rated Current 4.5A WE-part number: 744 779 7470---4.7uH	SMD
1	R4	100KΩ		Resistor, ±1%	0603
1	R1	Vout=5V	52.3KΩ	Resistor, ±1%	0603
		Vout=3.3V	31.6KΩ		
		Vout=2.5V	21.5KΩ		
		Vout=1.8V	12.7KΩ		
1	R2	10KΩ			
1	R3	Vout=5V	36KΩ	Resistor, ±1%	0603
		Vout=3.3V	30KΩ		
		Vout=2.5V	24.9KΩ		
		Vout=1.8V	22KΩ		
3	C9, C10, C11	10nF		Ceramic Capacitor	0603
1	C7	Vout=5V	10pF	C7 value is adjustable for the ESR of Cout.	0603
		Vout=3.3V	10pF		
		Vout=2.5V	10pF		
		Vout=1.8V	10pF		
1	C8	Vout=5V	2.2nF	Ceramic Capacitor	0603
		Vout=3.3V	2.2nF		
		Vout=2.5V	2.2nF		
		Vout=1.8V	2.2nF		
1	U1	APE1598AMP		Step-Down DC/DC Converter	ESOP-8

TYPICAL PERFORMANCE CHARACTERISTICS





MARKING INFORMATION

ESOP-8