2MHz, 2A Synchronous Step Down Converter

FEATURES

- Two 60mΩ (typical) MOSFETs for High Efficiency at 2A Loads
- 200kHz to 2MHz Switching Frequency
- 0.803V ± 1% Voltage Reference
- Synchronizes to External Clock from 300kHz to 2MHz
- Adjustable Slow Start/Sequencing
- UV and OV Power Good Output
- Low Operating and Shutdown Quiescent Current
- Cycle by Cycle Current Limit, Thermal and Frequency Fold Back Protection
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- DSPs, FPGAs, ASIC, and Microprocessors
- I/O Supplies
- System Power Supplies

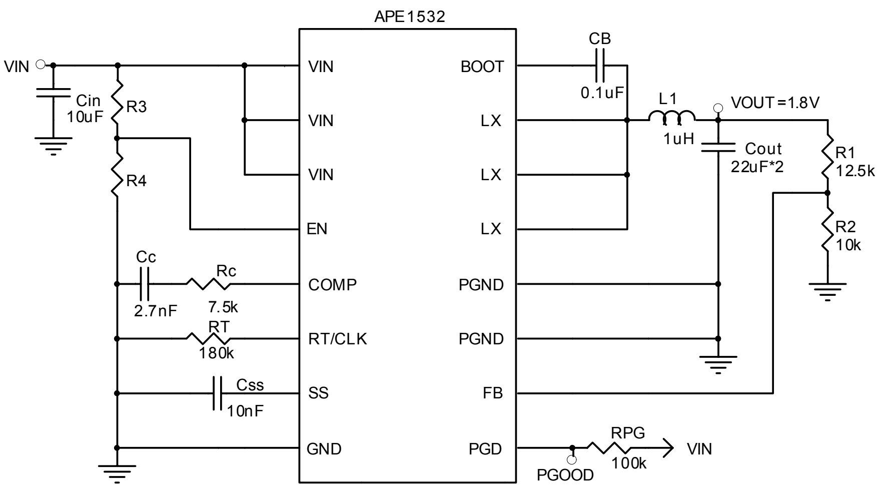
DESCRIPTION

The APE1532 is a synchronous step down converter designed with integrated MOSFETs. The current mode PWM DC/DC converter decreases external component counts and up to 2MHz switching frequency also reduces the inductor size.

The APE1532 integrates 60mΩ MOSFET and 400μA operation current to maximize the efficiency. The 1% high accurate of reference voltage over temperature provides well load regulation.

The soft start time is adjustable by an external capacitor at SS pin. The UVLO threshold is set at 2.6V internally, and can be increase by a programmable resistor at the EN pin. The APE1532 also features the frequency fold back and thermal shutdown to protect the device against the over-current fault condition.

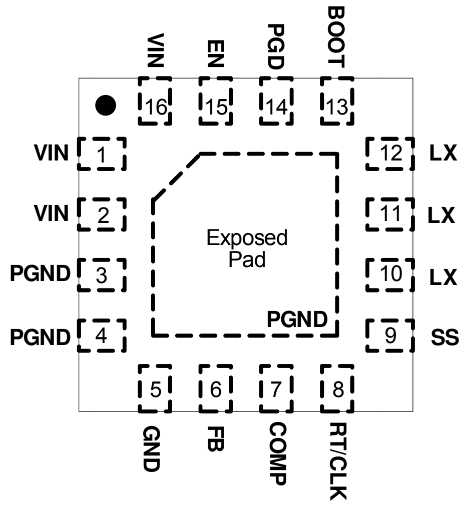
TYPICAL APPLICATION



ORDERING / PACKAGE INFORMATION

APE1532X

Package Type
VN3 : QFN 3x3-16L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN	-0.3V to 6V
EN	-0.3V to 6V
LX	-0.3V to 6V
BOOT	LX+6V
RT/CLK	-0.3V to 6V
FB, SS	-0.3V to 6V
PGD	-0.3V to 6V
PGD Sink Current	10mA
GND, PGND	-0.3V to 0.3V
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
QFN 3x3-16L	60°C/W

RECOMMENDED OPERATING CONDITIONS

VIN	2.95V to 6V
EN	-0.3V to 6V
LX	-0.3V to 6V
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(VIN=2.95 to 6V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Input						
Operation Voltage Range	V_{IN}		2.95		6	V
Under Voltage Lockout Threshold	UVLO	Rising		2.6	2.8	V
		hysteresis		200		mV
Quiescent Current	I_Q	V_{IN}=5V, V_{FB}=0.9V, RT=400kΩ		400		μA
Shutdown Current	I_{SD}	EN=0V, 0.95V≦VIN≦6V		3		μA
EN Threshold	V_{EN}	Rising		1.25		V
		Falling		1.18		V
EN Input Current	I_{EN}	V_{EN} + 50mV		-3.2		μA
		V_{EN} - 50mV		-0.65		μA
Reference Voltage	V_{FB}	VIN=2.95 to 6V	0.795	0.803	0.811	V
Controller						
High Side Switch Resistance (Note1)	R_{DRVH}	BOOT-LX=5V		60		mΩ
		BOOT-LX=2.95V		74		mΩ
Low Side Switch Resistance (Note1)	R_{DRVL}	V_{IN}=5V		60		mΩ
		V_{IN}=2.95V		74		mΩ
Switching Current Limit	I_{LM}		4			A
LX Rise/Fall Time (Note1)		V_{IN}=5V		1.5		V/ns
BOOT Charge Resistance		V_{IN}=5V		16		Ω
Error Amplifier						
COMP Leakage Current				7		nA
EA Transconductance (Note1)	gm	I_{COMP} = ± 2μA, V_{COMP}=1V		225		μA/V
COMP Sink/Source Current		V_{COMP}=1V, 0.1V overdrive		±20		μA
Current Sense to COMP Transconductance (Note1)	gm_{CS}			13		A/V

ELECTRICAL SPECIFICATIONS (Continued)

(T_A =25°C, unless otherwise specified)

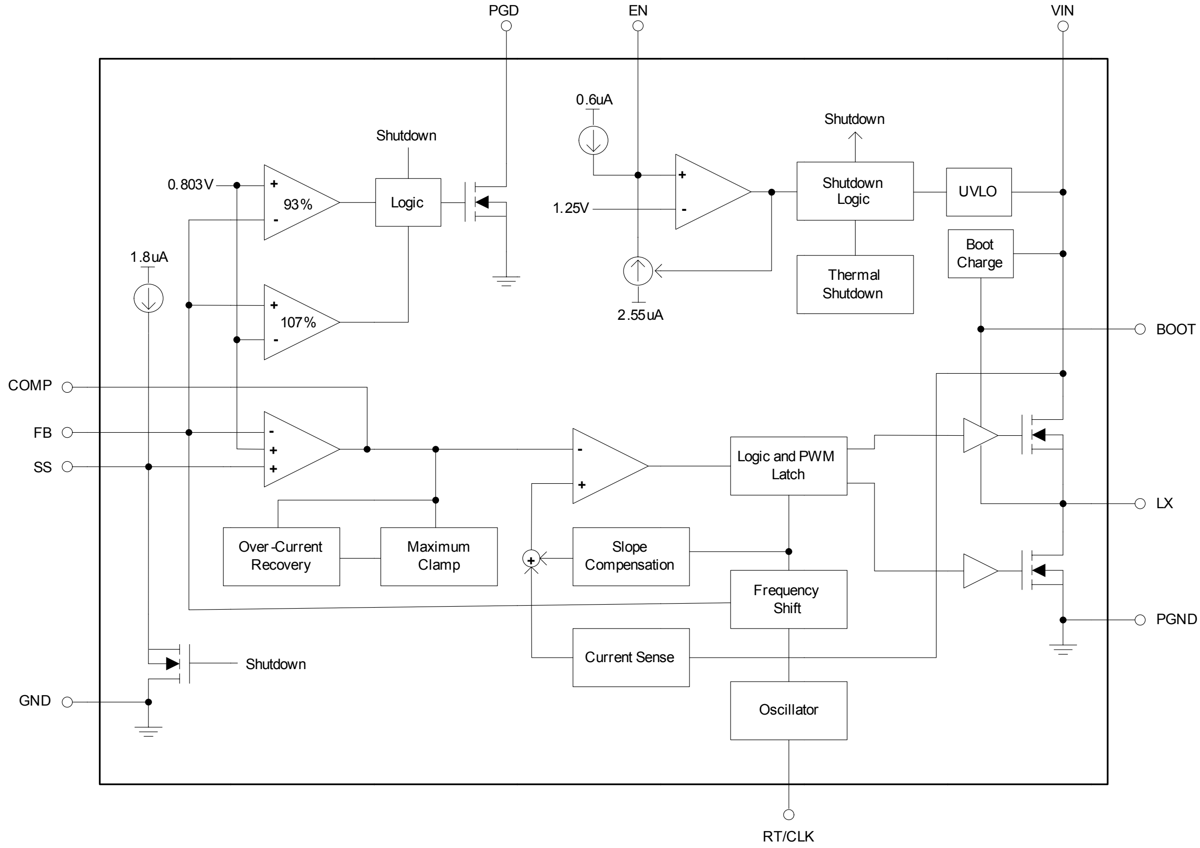
PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Resistor Timing and External Clock (RT/CLK)						
Switching Frequency Range		RT mode	200		2000	kHz
		CLK mode	300		2000	kHz
Switching Frequency	fsw	RT=400kΩ	400	500	600	kHz
Minimum CLK ON Time	T_{CLK_MIN}			75		ns
RT/CLK Voltage	$V_{RT/CLK}$	RT=400kΩ		0.5		V
RT/CLK Threshold		High	2.2			V
		Low			0.4	V
Delay Time (Note1)	t_D	RT/CLK falling to LX rising edge, fsw=500kHz, with RT resistor		150		ns
Soft Start (SS)						
SS Charge Current	I_{SS}	Vss=0.4V		1.8		μA
SS Discharge Current	I_{SS-D}	UVLO, EN, Tthermal fault, V_{IN}=5V, Vss=0.5V		20		mA
		Over-current, V_{FB}=0V		20		μA
Power Good (PGD)						
FB Threshold (Good)	V_{FB-R1}	Rising		93		$\%V_{FB}$
	V_{FB-F1}	Falling		105		$\%V_{FB}$
FB Threshold (Fault)	V_{FB-R2}	Rising		91		$\%V_{FB}$
	V_{FB-F2}	Falling		107		$\%V_{FB}$
PGD Leakage Current	I_{PGD}	$V_{FB}=V_{REF}$, V_{PGD}=5.5V		0.1		μA
PGD On Resistance (Note1)	R_{PGD}			10		Ω
PGD Output Low		I_{PGD}=3.5mA		0.3		V
Minimum VIN for Valid PGD Output		V_{PGD}<0.5V at 100μA		1.2		V
Thermal Shutdown						
Thermal Shutdown Threshold (Note1)	T_{SD}			150		°C
		Hysteresis		20		°C

Note1: Guarantee by design, not production tested.

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2, 16	VIN	Input supply voltage from 2.95V to 6V.
3, 4	PGND	Power ground.
5	GND	Analog ground.
6	FB	Output feedback pin.
7	COMP	Compensation pin. Connect frequency compensation components at this pin.
8	RT/CLK	Resistor timing or external clock input pin.
9	SS	Soft-start pin. Connect an external capacitor to adjust the output rise time.
10, 11, 12	LX	Switching node.
13	BOOT	Supply input for internal high-side N-MOSFET gate drive (boot terminal). Connect a bootstrap capacitor from this pin to LX node.
14	PGD	Power good output pin. PGD is an open-drain output. Pull up to VIN rail with a pull-up resistor.
15	EN	Enable pin, internal pull-up current source.
17	Exposed pad	Connect to power ground directly.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

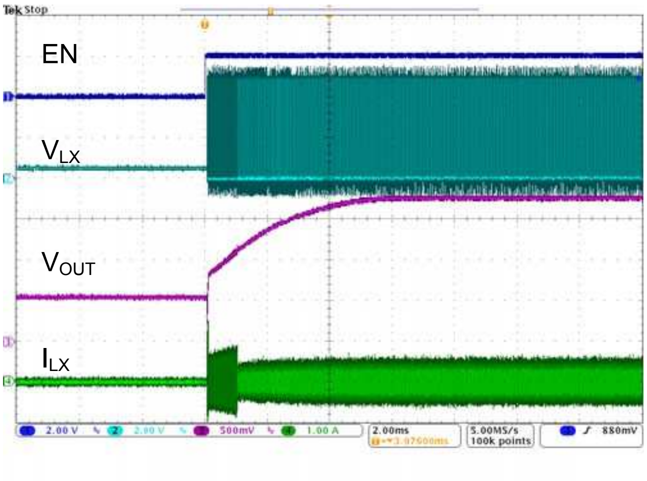


Fig.1 Enable, 5Vi to 1.8Vo/0A

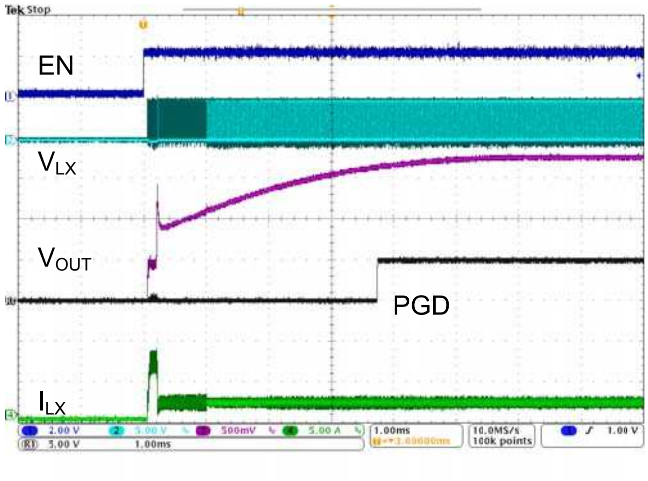


Fig.2 Enable, 5Vi to 1.8Vo/2A

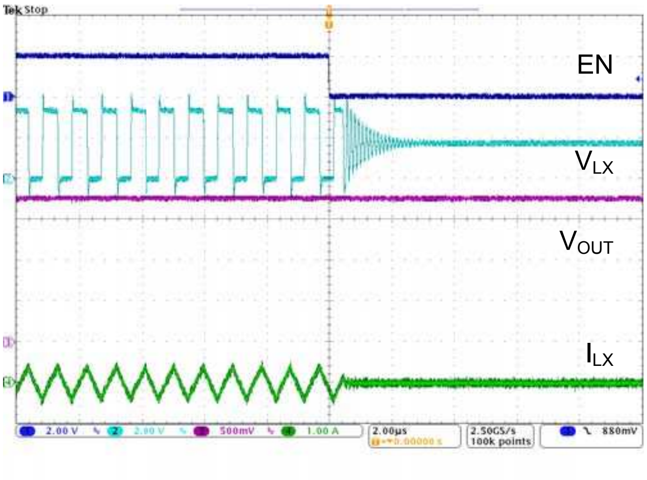


Fig.3 Disable, 5Vi to 1.8Vo/0A

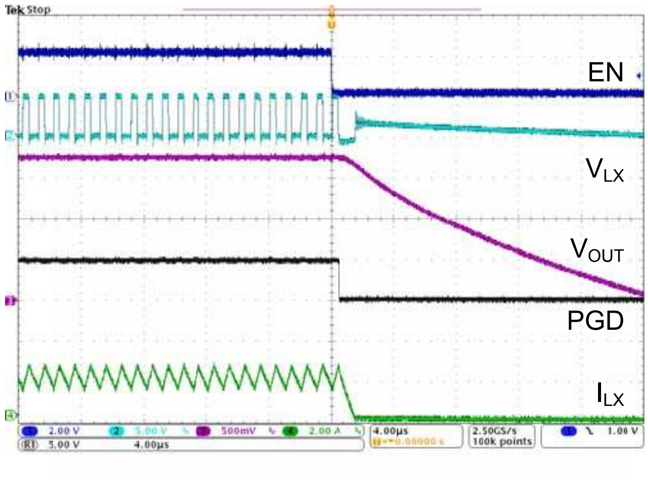


Fig.4 Disable, 5Vi to 1.8Vo/2A

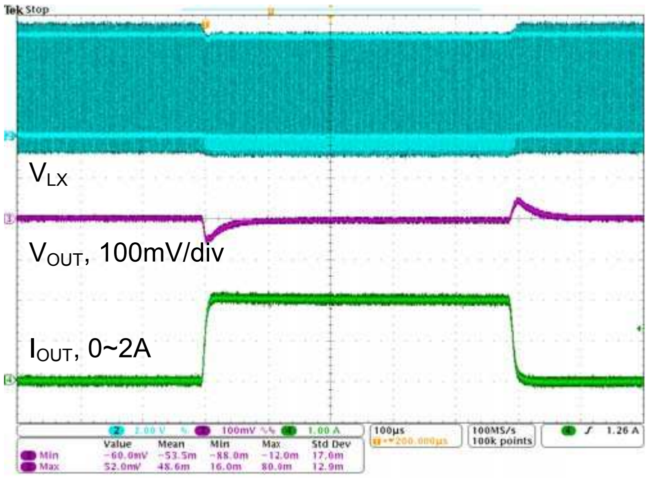


Fig.5 Load Transient, Vin=5V, Vo=1.8V

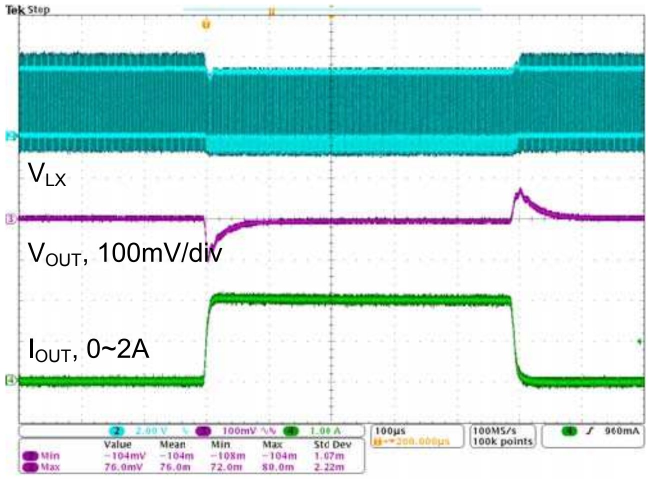


Fig.6 Load Transient, Vin=3.3V, Vo=1.8V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

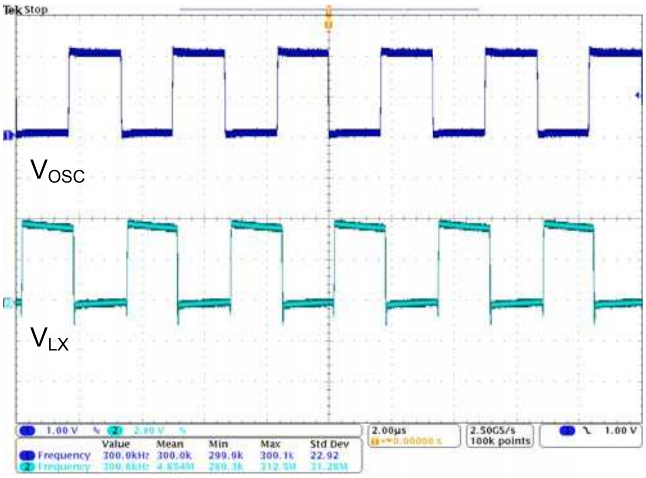


Fig.7 External PWM at RT pin, fosc=300kHz

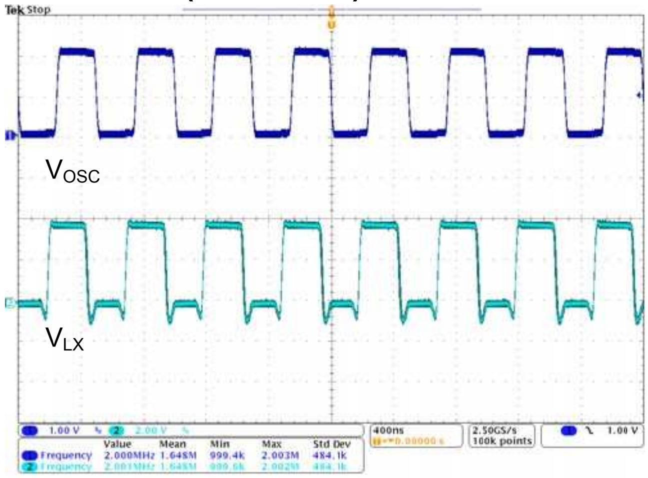


Fig.8 External PWM at RT pin, fosc=2MHz

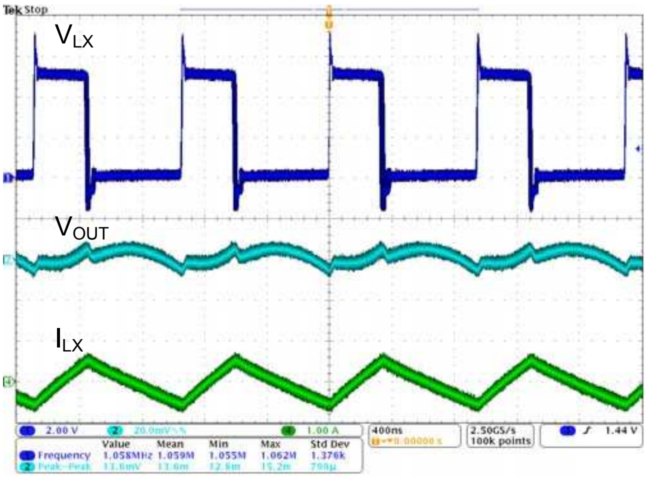


Fig.9 Output Ripple, Vin=5V, Vo=1.8V, Io=0A

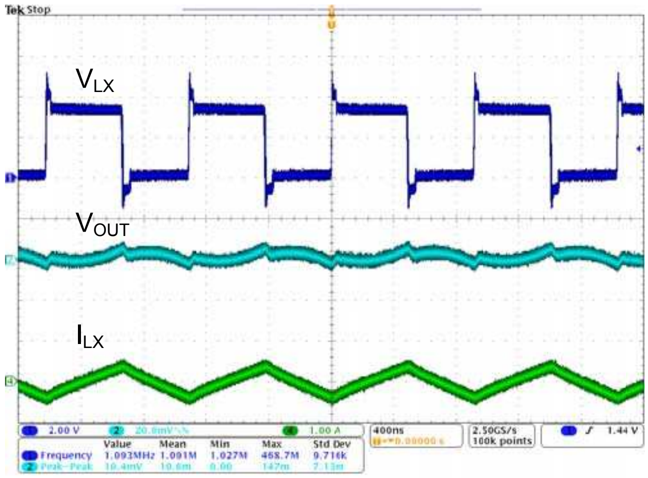


Fig.10 Output Ripple, Vin=3.3V, Vo=1.8V, Io=0A

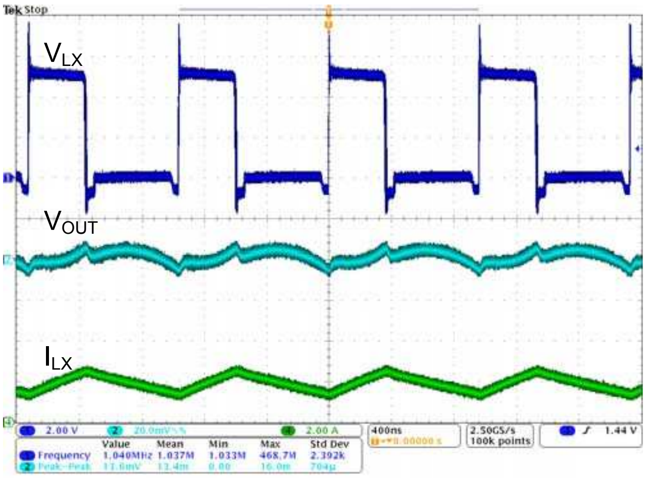


Fig.11 Output Ripple, Vin=5V, Vo=1.8V, Io=2A

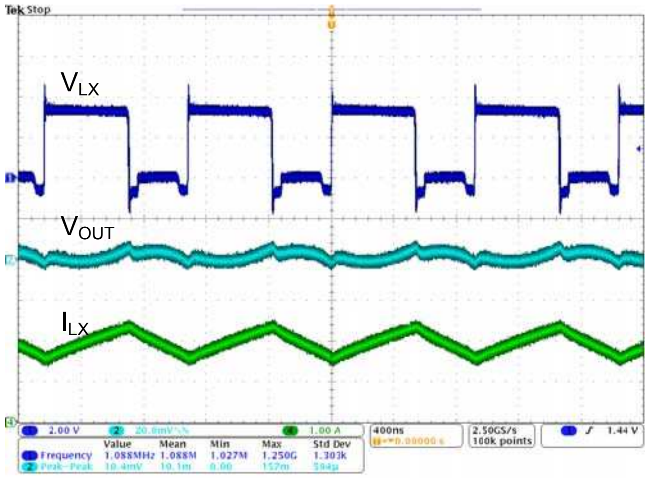


Fig.12 Output Ripple, Vin=3.3V, Vo=1.8V, Io=2A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

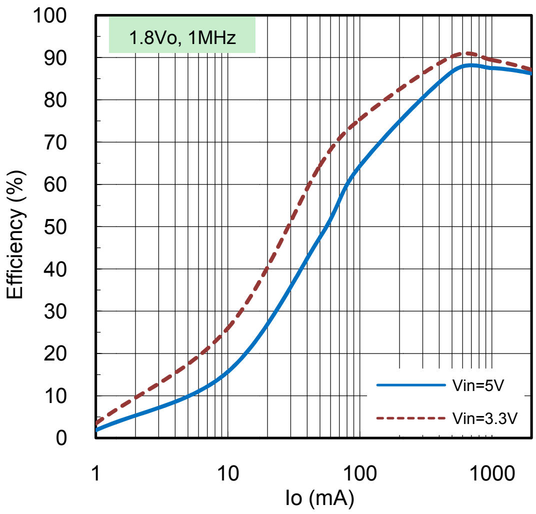


Fig.13 Efficiency for Vo=1.8V

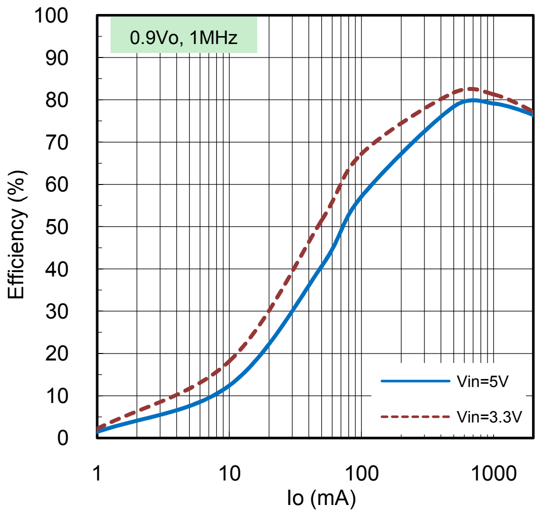


Fig.14 Efficiency for Vo=0.9V

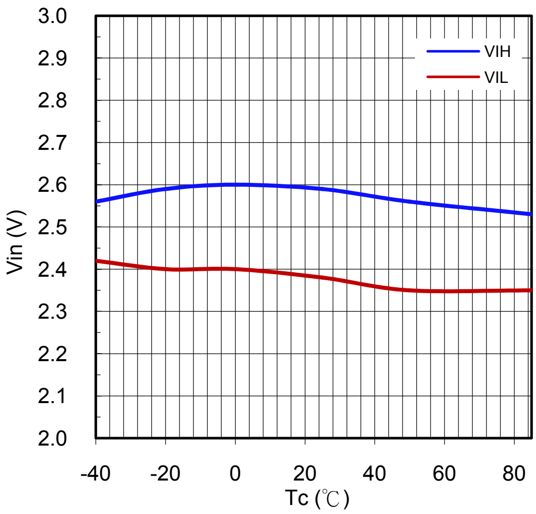


Fig.15 UVLO Threshold vs. Temperature

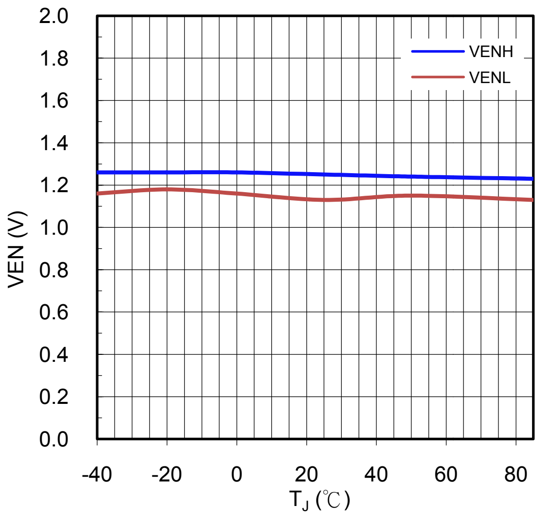


Fig.16 EN Threshold vs. Temperature

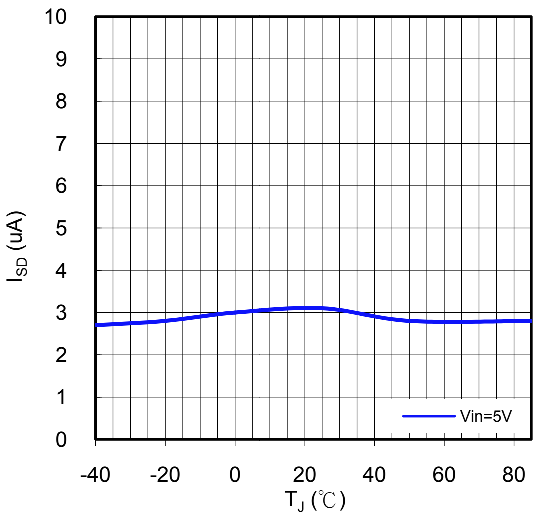


Fig.17 Shutdown Current vs. Temperature

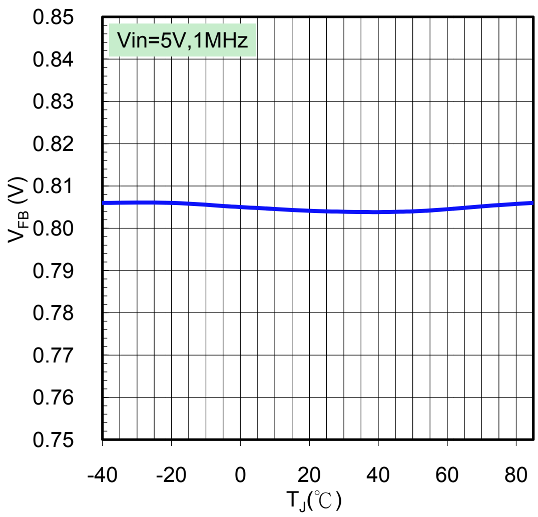


Fig.18 Feedback Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

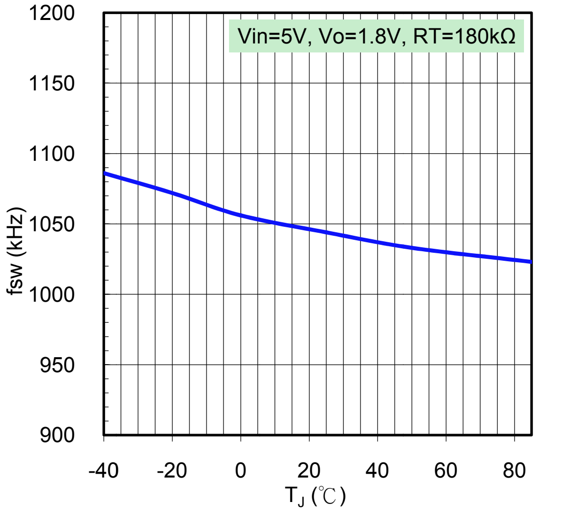


Fig.19 Switching Frequency vs. Temperature

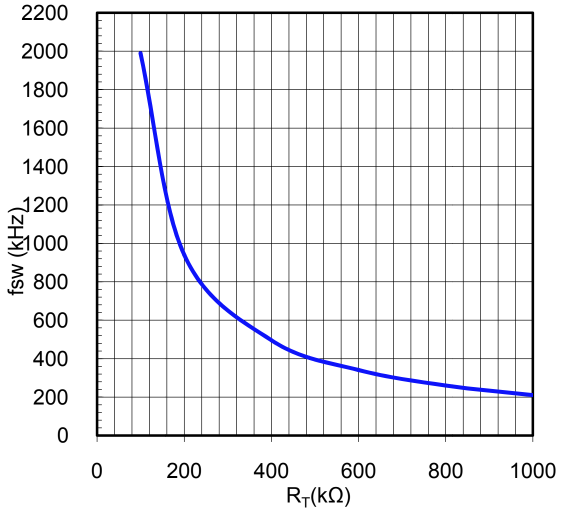


Fig.20 Switching Frequency vs. RT resistor

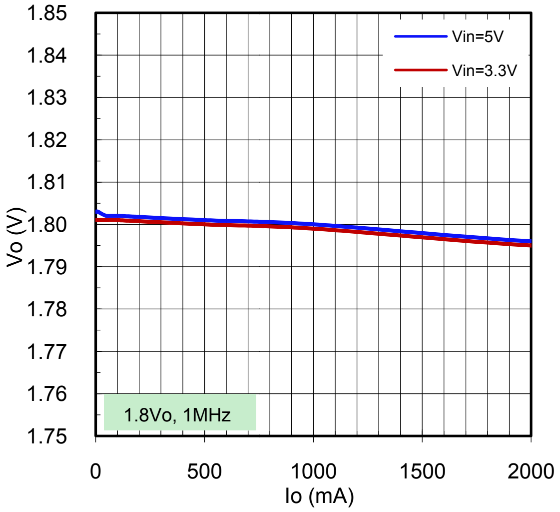


Fig.21 Load Regulation

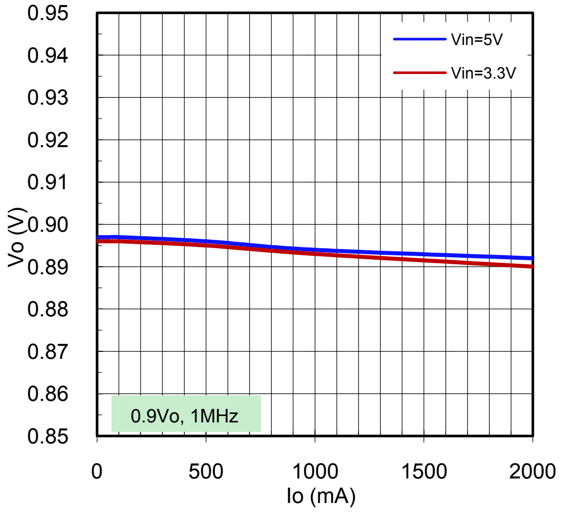


Fig.22 Load Regulation

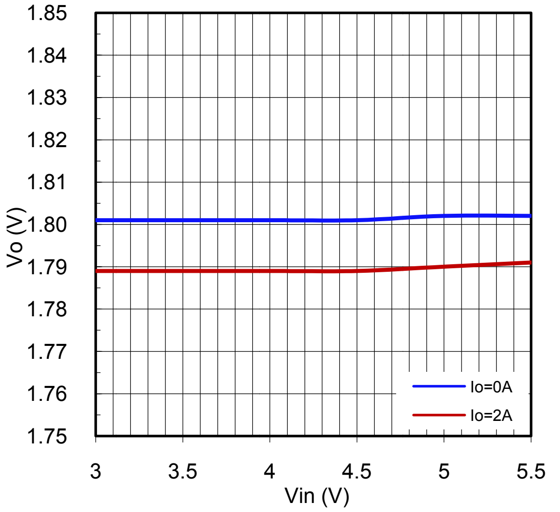


Fig.23 Line Regulation

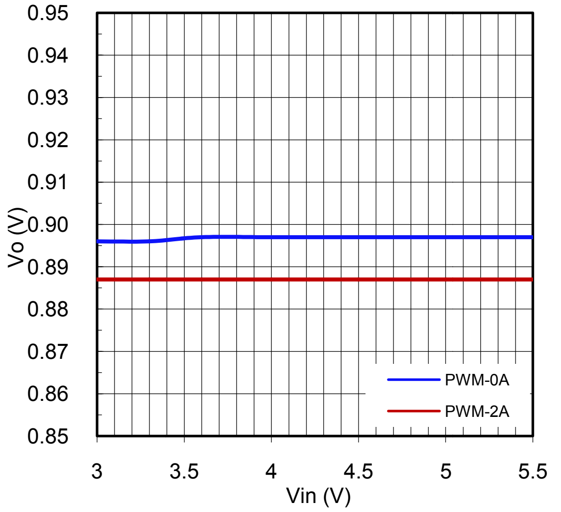


Fig.24 Line Regulation

APPLICATION INFORMATION

Forced PWM Control

The APE1532 is designed in low noise, adjustable fixed frequency, and current mode PWM control. The constant switching frequency has two benefits: first, the frequency can be selected to avoid noise-sensitive regions; second, the inductor ripple-current remains relatively constant which resulting in simplify external compensation design and reduce output capacitance.

Under-Voltage Lockout

The APE1532 has VIN under-voltage lockout protection (UVLO). This is a non-latched protection. When the VIN voltage is lower than 2.6V, the APE1532 is off. If higher UVLO is needed, use EN pin as TYPICAL APPLICATION circuit to adjust the UVLO threshold by using two external resistors, R3 and R4. When the EN pin floats, the internal 0.6μA current source provides the APE1532 default operation. If the EN voltage exceeds 1.25V, an additional 2.55μA hysteresis current is added. If the EN voltage is below 1.18V, the hysteresis current is removed.

$$R3 = \frac{0.944 \times V_{UVLO-H} - V_{UVLO-L}}{2.58 \times 10^{-6}}$$

$$R4 = \frac{1.18 \times R3}{V_{UVLO-L} - 1.18 + R3 \times 3.15 \times 10^{-6}}$$

The UVLO has two thresholds, V_{UVLO-H} for power up when the input voltage is rising and V_{UVLO-L} for power down when the input voltage is falling.

Soft Start

The APE1532 has an internal 1.8μA current source which charges external capacitor to implement a soft start time. When the EN pin voltage rises above the enable threshold, the converter enters its start-up sequence. The soft start time can be calculated by:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.803(V)}{1.8(\mu A)}$$

Power Good Output

The APE1532 provides a power good (PGD) output, which is an open-drain output requiring a pull-up resistor. Typically connect to +5V voltage source or less through a resistor between the values of 1kΩ and 100kΩ. The PGD comparator continuously monitors the FB voltage. In shutdown and soft start period, PGD is actively low. If the FB voltage rises above 93% or falls below 105% of the internal reference voltage, the PGD is high. If the FB voltage falls below 91% or rises above 107% of the internal reference voltage, the PGD becomes low immediately which enters the fault condition.

Output Voltage Setting

The output voltage is adjusted with a resistor divider from the output to the FB pin. It can be calculated as:

$$V_{OUT} = 0.803V \times (\frac{R1}{R2} + 1)$$

APPLICATION INFORMATION (Continued)

Switch frequency

The switching frequency is adjustable from 200kHz to 2MHz by a preset resistor connected to the RT/CLK pin. This pin is fixed at 0.5V when using an external resistor to ground to determine the switching frequency. The external resistor, RT, is given as:

$$RT(k\Omega) = \frac{311890}{f_{SW}(kHz)^{1.0793}}$$

The high switching frequency allows lower value inductor and smaller output capacitor. However, the highest switching frequency causes more switching loss. A moderate switching frequency of 1MHz is selected to achieve both a small solution size and a high efficiency operation. So that, RT is calculated to be 180kΩ.

Synchronize

The RT/CLK pin is also used to synchronize the converter to an external clock. Connect a square wave with a 75ns on time at least to the RT/CLK pin to determine the synchronization frequency ranging from 300kHz to 2MHz. The amplitude of square wave must converse lower than 0.6V and higher than 1.6V. The internal amplifier is disabled if the RT/CLK pin is pulled above the 1.6V threshold and the pin becomes a synchronization input. The rising edge of the LX is synchronized to the falling edge of external clock.

Frequency Compensation

The APE1532 has the transconductance amplifier with Type II compensation control loop. Figure25 shows the small signal equivalent model for the APE1532 control loop which can check frequency response and dynamic load response. The APE1532 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations when duty cycle increases.

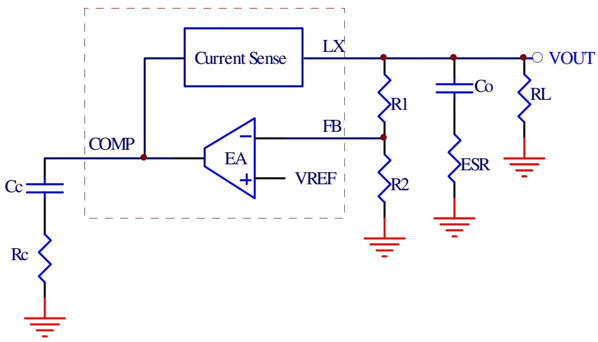


Fig.25 Simple small signal model

In Figure25, the error amplifier is a transconductance amplifier with a gm of 225μA/V. The current sense transconductance with a gm of 13A/V is the proportion of the variation in switch current and the variation in COMP pin voltage. The small signal transfer function is dominated by a DC gain and developed by a pole at f_P and a zero at f_Z.

APPLICATION INFORMATION (Continued)

$$GAIN = gm_{CS} \times R_L$$

$$f_p = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

$$f_C = \sqrt{f_P \times f_Z}$$

Proper compensation of the system is allowed for a calculable bandwidth. The targeted compensation network is to provide the closed loop transfer function with 0dB crossover frequency (fc, below one-tenth of fsw typically) and sufficient phase margin (greater than 45°). As the load current decreases, the gain increases and the pole frequency lowers to keep the same 0dB crossover frequency for the varied load conditions.

The compensation network Rc, Cc can take as following:

$$R_C = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{V_{REF} \times gm_{EA} \times gm_{CS}}$$

Choose the compensation resistor (Rc) to set the desired crossover frequency.

$$C_C = \frac{R_L \times C_{OUT}}{R_C}$$

Choose the compensation capacitor (Cc) to achieve the desired phase margin.

Inductor Selection

The inductor value determines the ripple current and the ripple voltage of the converter. This inductor choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The inductor selection is based on the ripple current which is typically set between 1/10 to 3/10 of the maximum load current. The switching frequency and ripple current determine the inductor which can be calculated as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW} \times V_{IN}}$$

The ripple current can be given by: $\Delta I_L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{L \times f_{SW} \times V_{IN}}$

Output Capacitor Selection

The output capacitor needs to be selected based on three considerations, the output ripple, load transient, and the modulator pole. Below equation shows the minimum output capacitance necessary to perform this.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

The low ESR ceramic capacitor is recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = ESR / \Delta I_L$$

MARKING INFORMATION

QFN 3x3-16L