Main Power Supply Controllers for Notebook Computers

FEATURES

- Wide Input Range: 6.5V to 28V
- Output Range: 2V to 5.5V
- Integrate 100mA 5V/3.3V LDO with Switches
- Built-in 2V Reference Output (1% Accuracy)
- 4500ppm/°C R_{DS-ON} Current Sense Compensation
- With/Without Ultrasonic Mode Selectable and Forced-PWM Operation
- Low-Side R_{DS-ON} Current Sense
- Positive and Negative Current limit
- Integrated OV/UV and Thermal Shutdown Protections
- Integrated Boost Diode
- Power Good (PGOOD) Signal
- 1.6ms Soft Start and Output Discharge Function (Soft-stop)

APPLICATIONS

- Notebook and Sub-Notebook Computers
- I/O Supplies
- System Power Supplies

DESCRIPTION

The APE3520/A is a cost effective, dual-synchronous buck controller targeted for notebook system power supply solutions. It provides 5V and 3.3V LDOs and requires few external components. The 270kHz CLK output (APE3520) can be used to drive an external charge pump which is generating gate drive voltage for the load switches without reducing the main converter's efficiency.

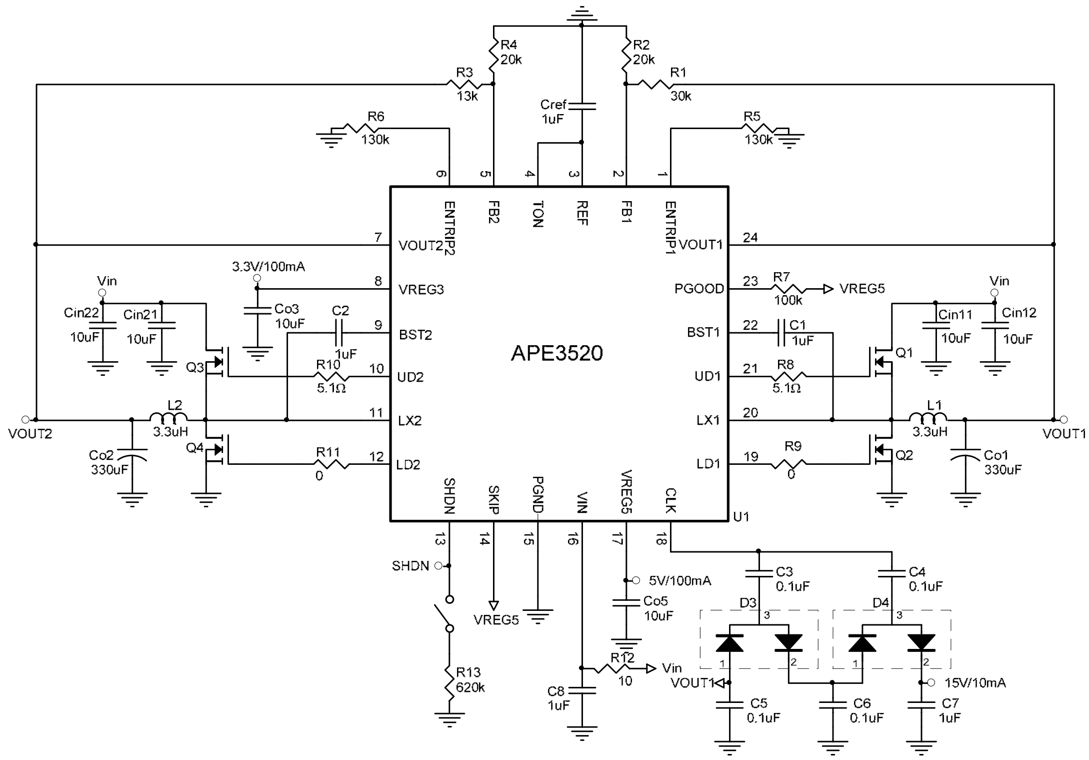
A constant on-time PWM control scheme operates without sense resistor and provides 100ns response to load transients while maintaining a relatively constant switching.

The ultrasonic mode enables low acoustic noise at much higher efficiency than forced-PWM operation.

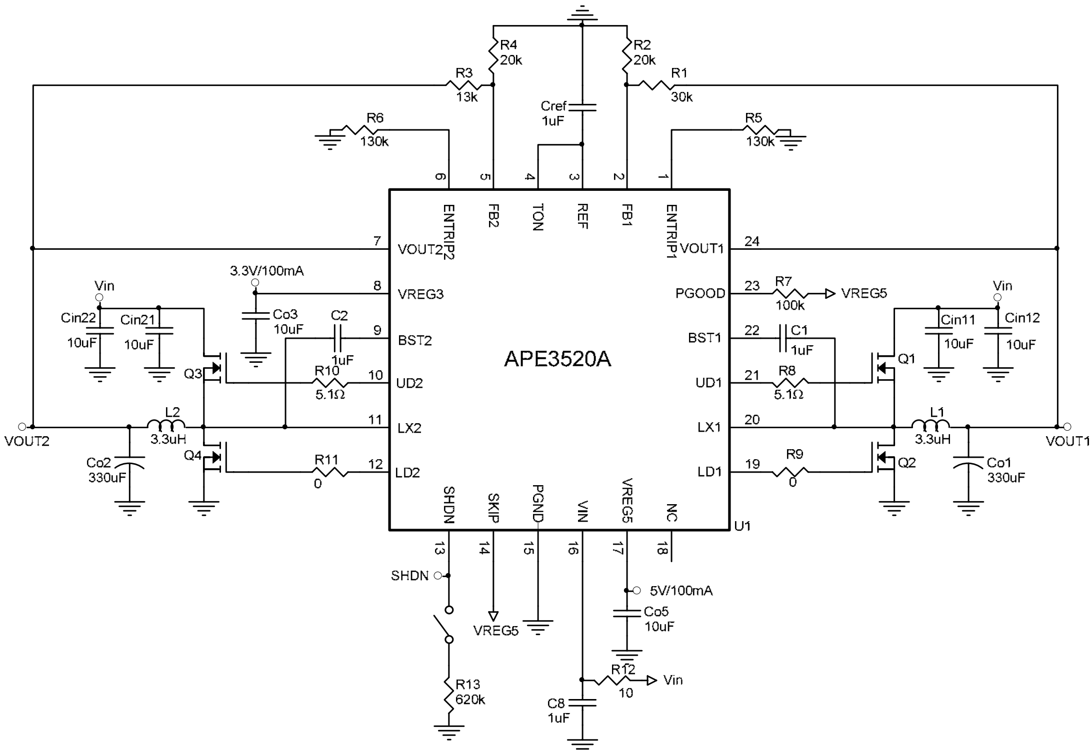
The APE3520/A includes power-up sequencing, the power-good output, internal soft-start and internal soft-stop output that prevents negative voltages on shutdown.

The APE3520/A is available in a 24-pin QFN package and is specified from -40°C to 85°C ambient temperature range.

TYPICAL APPLICATION



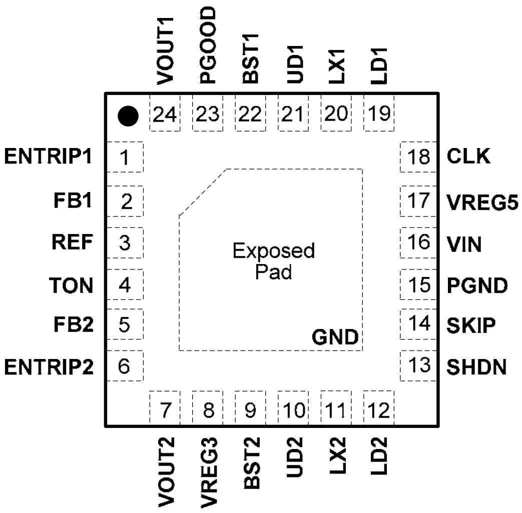
TYPICAL APPLICATION (Continued)



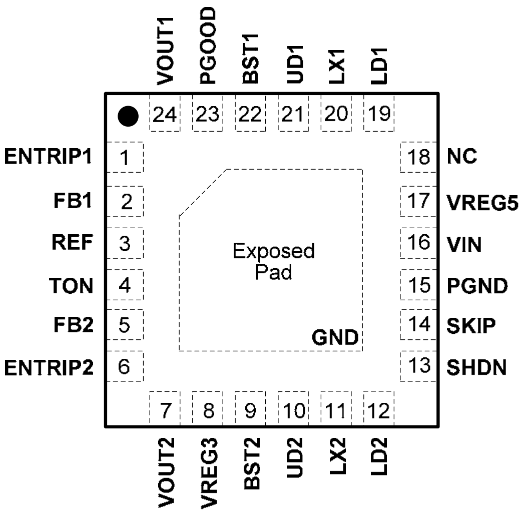
ORDERING / PACKAGE INFORMATION

APE3520XX
- Package Type
  VN4: QFN 4x4-24L
- CLK Function
  Blank: with CLK
  A: without CLK

APE3520 Top View
QFN 4x4-24L



APE3520A Top View
QFN 4x4-24L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

BST1, BST2	-0.3V to 31V
BST1 to LX1, BST2 to LX2	-0.3V to 6V
UD1 to LX1, UD2 to LX2	-0.3V to 6V
LX1, LX2	-0.3V to 25V
LD1, LD2	-0.3V to 6V
VIN	-0.3V to 31V
SHDN, ENTRIP1, ENTRIP2, TON, SKIP	-0.3V to 6V
FB1, FB2, VOUT1, VOUT2	-0.3V to 6V
PGOOD, CLK, VREG3, VREG5, REF	-0.3V to 6V
PGND, GND	-0.3V to 0.3V
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
QFN-24 (4mmx4mm)	37°C/W

RECOMMENDED OPERATING CONDITIONS

VIN	6.5V to 28V
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(V_{IN}=12V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Input						
Quiescent Power Consumption	P_T	VOUT1=5V,VOUT2=3.3V,SHDN=1.2V, ENTRIPx=5V,FB1=FB2=2.05V, TON=SKIP=REF P_T=P_{VIN}+P_{VREG5}		4	8	mW
VIN Standby Current	I_{INSTB}	SHDN=1.2V,ENTRIPx=0V		200	250	μA
VIN Shutdown Current	I_{INSD}	SHDN=ENTRIPx=0V		10	25	μA
Output						
VREG5 Output Voltage	V_{REG5}	VOUT1=0V,I_{VREG5} < 100mA	4.8	5	5.2	V
		VOUT1=0V,I_{VREG5} < 100mA, 6.5V < VIN < 28V	4.75	5	5.25	V
		VOUT1=0V,I_{VREG5} < 50mA, 6.5V < VIN < 28V	4.75	5	5.25	V
VREG5 Output Current	I_{VREG5}	VOUT1=0V,VREG5=4.5V	100	175	250	mA
VREG5 Switchover Threshold to VOUT1	V_{TH5VSW}	Raising	4.55	4.7	4.85	V
		Hysteresis	0.21	0.31	0.36	V
VREG5 Switchover Equivalent Resistance	R_{SW5V}	VOUT1=5V, I_{VREG5}=100mA		1	3	Ω
VREG3 Output Voltage	V_{REG3}	VOUT2=0V, I_{VREG3} < 100mA	3.2	3.33	3.46	V
		VOUT2=0 V, I_{VREG3} < 100mA, 6.5V < VIN < 28V	3.13	3.33	3.5	V
		VOUT2=0 V, I_{VREG3} < 50mA, 6.5V < VIN < 28V	3.13	3.33	3.5	V
VREG3 Output Current	I_{VREG3}	VOUT2=0V, VREG3=3V	100	175	250	mA
VREG3 Switchover Threshold to VOUT2	V_{TH3VSW}	Raising	3.05	3.15	3.25	V
		Hysteresis	0.15	0.25	0.3	V
VREG3 Switchover Equivalent Resistance	R_{SW3V}	VOUT2=3.3V, I_{VREG3}=100mA		1.5	4	Ω
VOUTx Discharge Current	I_{DIS}	ENTRIPx=0V, VOUTx=0.5V	10	60		mA

ELECTRICAL SPECIFICATIONS (Continued)

(V_{IN}=12V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
VREG5 UVLO Threshold	$V_{UVVREG5}$	Wake up (Note1)		4.2		V
		Hysteresis (Note1)		0.43		V
VREG3 UVLO Threshold	$V_{UVVREG3}$	Shutdown (Note1)		2.5		V
Reference Voltage						
REF Output Voltage	V_{REF}	I_{REF} = 0A	1.98	2.00	2.02	V
		-5uA < I_{REF} < 100uA	1.97	2.00	2.03	V
Internal Reference Voltage	V_{IREF}	I_{REF} = 0A, beginning of ON state	1.97	2.00	2.03	V
FBx Voltage	V_{FB}	I_{REF}= 0A, auto-skip mode	1.98	2.01	2.04	V
		I_{REF}= 0A, ultrasonic mode (Note1)		2.035		V
		I_{REF}= 0A, forced-PWM mode (Note1)		2		V
FBx Input Current	I_{FB}	V_{FBx}=2V	-1		+1	μA
Driver						
UD Resistance	R_{UD}	Source, $V_{BSTx-UDx}$=0.1V		4	8	Ω
		Sink, $V_{UDx-LXx}$=0.1V		1.5	4	Ω
LD Resistance	R_{LD}	Source, $V_{VREG5-LDx}$=0.1V		4	8	Ω
		Sink, V_{LDx}=0.1V		1.5	6	Ω
Dead Time	T_D	UDx-low(UDx=1V) to LDx-high(LDx=1V)		10		ns
		LDx-low(LDx=1V) to UDx-high(UDx=1V)		30		ns
Boot Strap Switch						
Forward Voltage	V_{FBST}	$V_{VREG5-VBSTx}$, I_F=10mA	0.6	0.7	0.8	V
Clock Output						
High Level Voltage	V_{CLKH}	I_{VCLK}= -10mA, VOUT1=5V	4.84	4.92		V
Low Level Voltage	V_{CLKL}	I_{VCLK}= 10mA, VOUT1=5V		0.06	0.12	V
Clock Frequency	f_{CLK}	APE3520	175	270	325	kHz
Soft Start						
Internal Soft Start Time	T_{SS}		1.1	1.6	2.1	ms

ELECTRICAL SPECIFICATIONS (Continued)

(V_{IN}=12V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Duty and Frequency Control						
CH1 On Time	T_{ON11}	VOUT1=5V,200kHz setting		2080		ns
	T_{ON12}	VOUT1=5V,245kHz setting		1700		ns
	T_{ON13}	VOUT1=5V,300kHz setting		1390		ns
	T_{ON14}	VOUT1=5V,365kHz setting		1140		ns
CH2 On Time	T_{ON21}	VOUT2=3.3V,250kHz setting		1100		ns
	T_{ON22}	VOUT2=3.3V,305kHz setting		900		ns
	T_{ON23}	VOUT2=3.3V,375kHz setting		730		ns
	T_{ON24}	VOUT2=3.3V,460kHz setting		600		ns
Minimum On Time	$T_{ON(min)}$			80		ns
Minimum Off Time	$T_{OFF(min)}$			300		ns
Logic Threshold and Setting Conditions						
SHDN Setting Voltage	V_{SHDN}	Shutdown			0.4	V
		Enable, VCLK = off	0.8		1.6	V
		Enable, VCLK = on	2.4			V
SHDN Input Current	I_{SHDN}	SHDN=0V	1.2	2	2.8	μA
ENTRIPx Threshold	V_{EN}	Shutdown	350	400	450	mV
		Hysteresis	10	30	60	mV
TON Setting Voltage	V_{TON}	200kHz / 250kHz			1.5	V
		245kHz / 305kHz	1.9		2.1	V
		300kHz / 375kHz	2.7		3.6	V
		365kHz / 460kHz	4.7			V
SKIP Setting Voltage	V_{SKIP}	Forced-PWM mode			1.5	V
		Auto-skip mode	1.9		2.1	V
		Ultrasonic mode	2.7			V

ELECTRICAL SPECIFICATIONS (Continued)

(V_{IN}=12V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Sense						
ENTRIPx Source Current	I_{ENTRIP}	$V_{ENTRIPx}$ = 920 mV	9.4	10	10.6	uA
ENTRIPx Current Temperature Coefficient	$TC_{IENTRIP}$			4500		ppm/ °C
OCP Comparator Offset	Vos_{OCP}			0		mV
Maximum OCL Setting	$V_{OCL(max)}$	VENTRIPx=5V		205		mV
Zero Cross Detection Comparator Offset	Vos_{ZC}	$V_{GND-LXx}$ voltage		0		mV
Current Limit Threshold	V_{ENTRIP}	$V_{ENTRIPx-GND}$ voltage (Note1)	0.515		2	V
Power Good Function						
PGOOD Threshold	V_{THPG}	PG low threshold (PGOOD goes high)	92.5	95	97.5	%
		PG high threshold (PGOOD goes low)	102.5	105	107.5	%
		PG hysteresis	2.5	5	7.5	%
PGOOD Sink Current	I_{PG}	PGOOD=0.5V	5	12		mA
PGOOD Delay	T_{PGDEL}	Delay for PGOOD in	350	510	670	us
Under-Voltage and Over-Voltage Protection						
FBx OVP Trip Threshold	V_{OVP}	OVP detect	110	115	120	%
FBx OVP Propagation Delay	T_{OVPDEL}	(Note1)		2		us
FBx UVP Trip Threshold	V_{UVP}	UVP detect	55	60	65	%
		Hysteresis		10		%
FBx UVP Delay	T_{UVPDEL}		20	32	40	us
UVP Enable Delay	T_{UVPEN}	From Enable to UVP work	1.4	2	2.6	ms
Thermal Shutdown						
Thermal Shutdown Threshold (Note1)	T_{SD}	(Note1)		150		°C
		Hysteresis		10		°C

Note1: Guaranteed by design, not production tested.

PIN DESCRIPTIONS

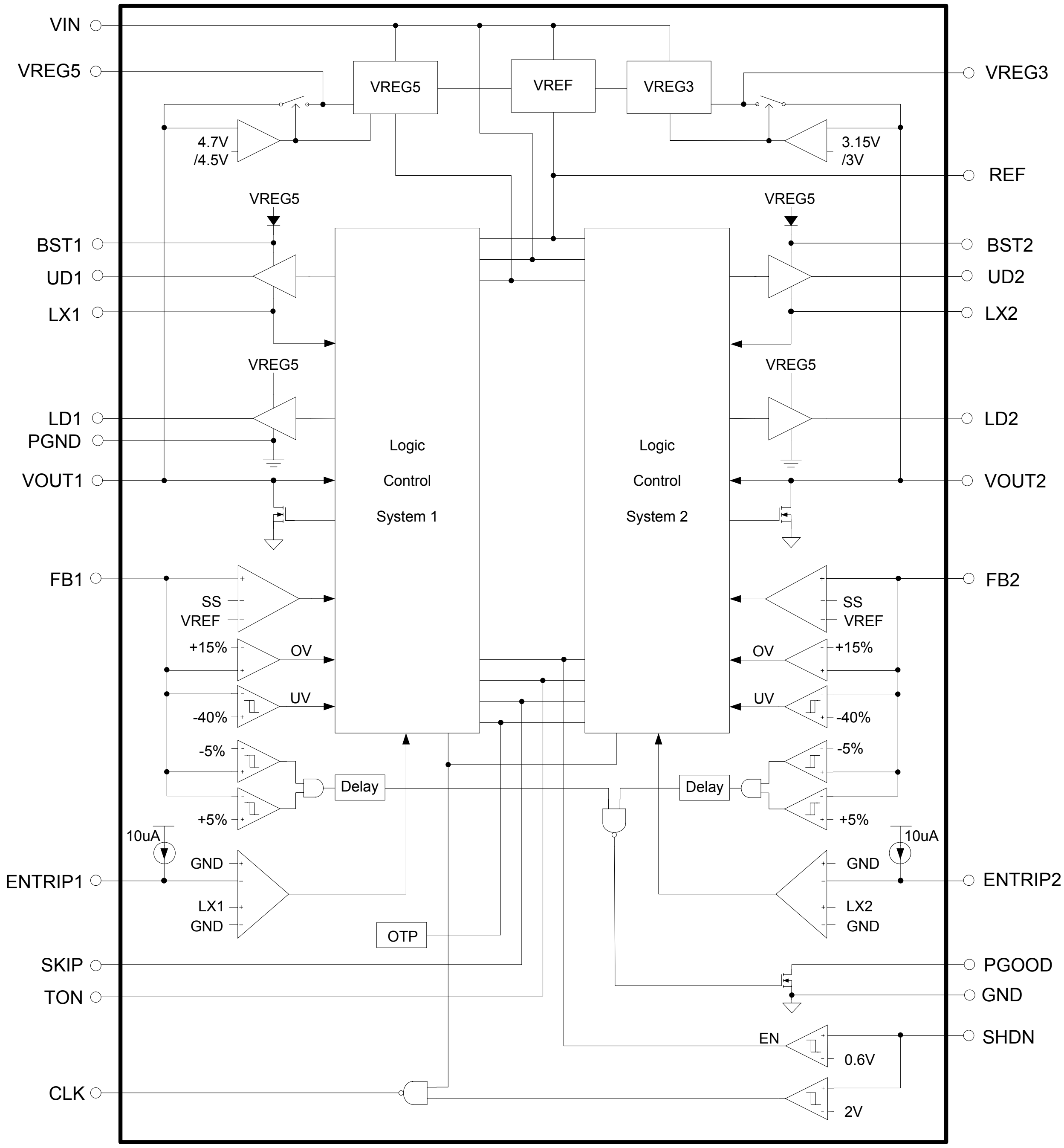
PIN No.	PIN SYMBOL	PIN DESCRIPTION
1	**ENTRIP1**	Channel 1 enable and current limit threshold setting pins. Connect resistor from this pin to GND to set R_{DS-ON} sense threshold. Short to ground to shutdown the channel.
2	**FB1**	SMPS voltage feedback input
3	**REF**	2V reference voltage output.
4	**TON**	On-time selection pin 365 kHz/460 kHz setting : connect to VREG5 300 kHz/375 kHz setting : connect to VREG3 245 kHz/305 kHz setting : connect to REF 200 kHz/250 kHz setting : connect to GND
5	**FB2**	SMPS voltage feedback input
6	**ENTRIP2**	Channel 2 enable and current limit threshold setting pins. Connect resistor from this pin to GND to set R_{DS-ON} sense threshold. Short to ground to shutdown the channel.
7	**VOUT2**	Output connection to SMPS. This terminal works as fixed voltage input and output discharge input. OUT2 also works as 3.3V switch over return power input.
8	**VREG3**	3.3V LDO output.
9	**BST2**	Supply input for high side N-MOS gate driver (Boost terminal). Connect capacitor from this pin to LX2.
10	**UD2**	High side N-MOS gate driver output. Drive voltage corresponds to BST2 to LX2 voltage.
11	**LX2**	Switch node connections for high-side driver.
12	**LD2**	Low side N-MOS gate driver output.
13	**SHDN**	SMPS Enable pin Float: LDOs on, and ready to turn on CLK and switcher channels. 620kΩ to GND : enable both LDOs, VCLK off and ready to turn on switcher channels. Power consumption is almost the same as the case of CLK = ON. GND : disable all circuit.

PIN DESCRIPTIONS (Continued)

PIN No.	PIN SYMBOL	PIN DESCRIPTION
14	SKIP	Operation mode selection pin Ultrasonic: Connect to VREG3 or VREG5. Auto-skip: Connect to REF. Forced-PWM: Connect to GND.
15	PGND	Power Ground.
16	VIN	High voltage power supply input for 5V/3.3V LDO.
17	VREG5	5V LDO output.
18	CLK / NC	CLK: APE3520, 270kHz clock output for 15V charge pump. NC: APE3520A
19	LD1	Low-side N-channel MOSFET driver output.
20	LX1	Switch node connections for high-side driver.
21	UD1	High side N-MOS gate driver output. Drive voltage corresponds to BST1 to LX1 voltage.
22	BST1	Supply input for high side N-MOS gate driver (Boost terminal). Connect capacitor from this pin to LX1.
23	PGOOD	Power Good window comparator output for channel 1 and 2. (Logic AND) PGOOD is an open-drain output. Connect a pull up resister to 5V.
24	VOUT1	Output connection to SMPS. This terminal works as fixed voltage input and output discharge input. OUT1 also works as 5V switch over return power input.
Exposed Pad	GND	Analog pad. The exposed pad must be soldered to a large PCB and connect to GND.

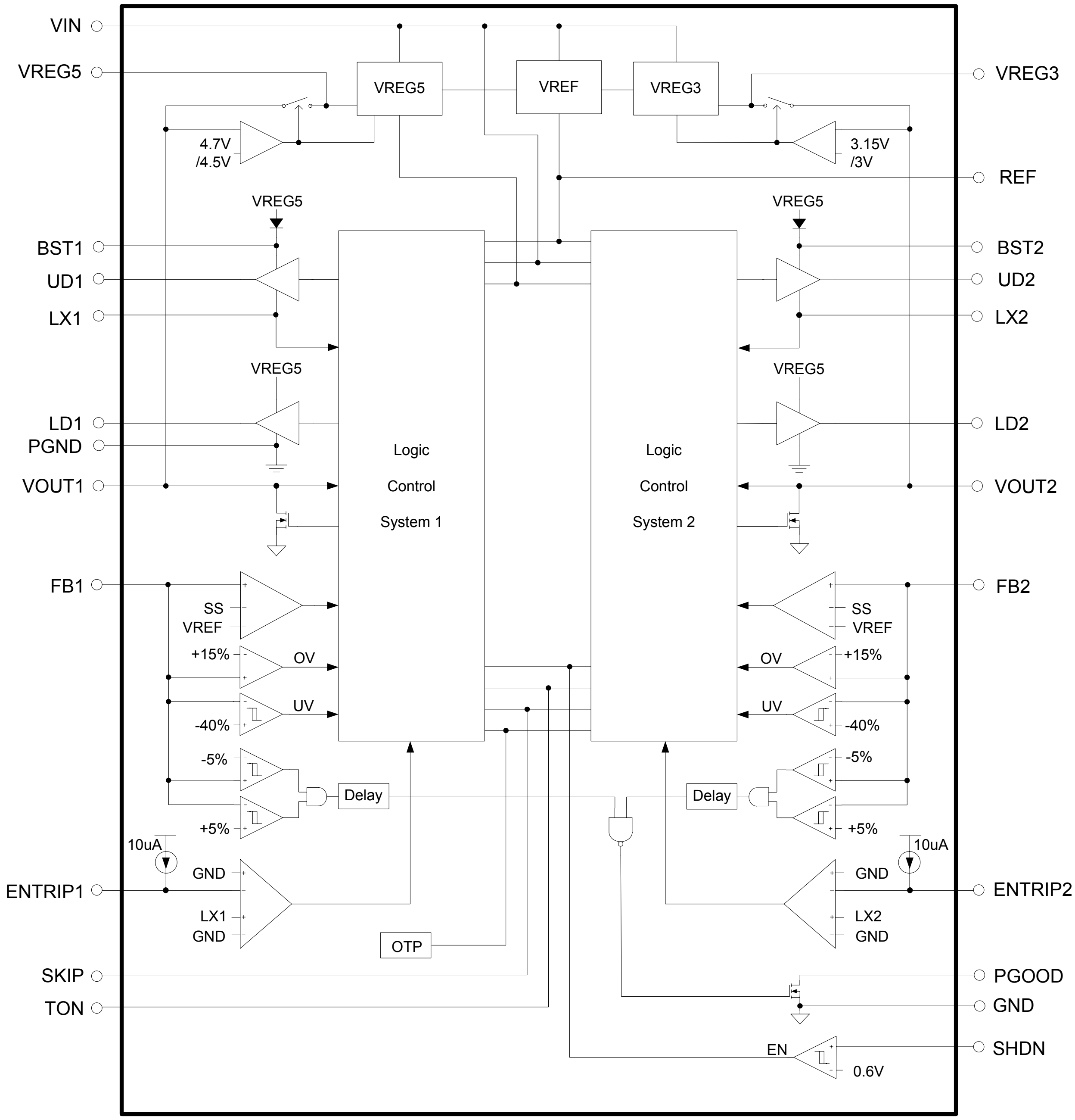
BLOCK DIAGRAM

APE3520



BLOCK DIAGRAM (Continued)

APE3520A



TYPICAL PERFORMANCE CHARACTERISTICS

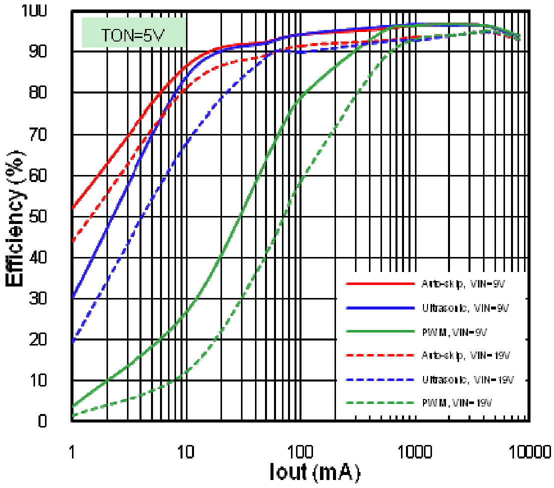


Fig1 Efficiency for VOUT1

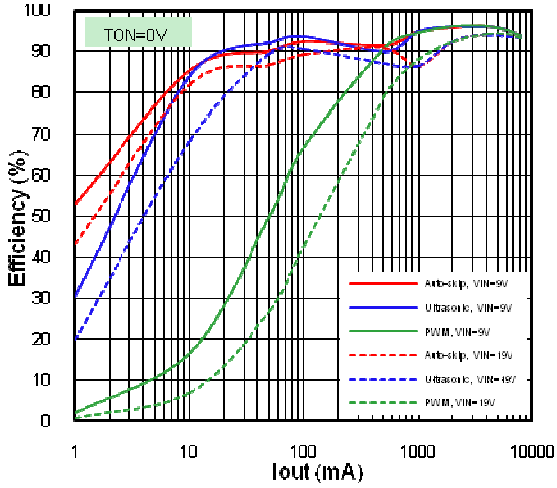


Fig2 Efficiency for VOUT1

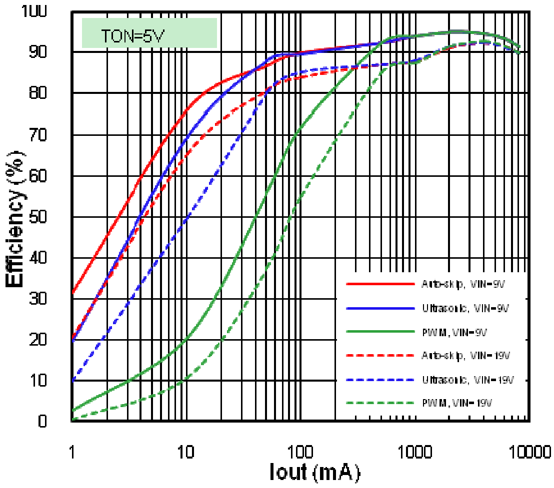


Fig3 Efficiency for VOUT2

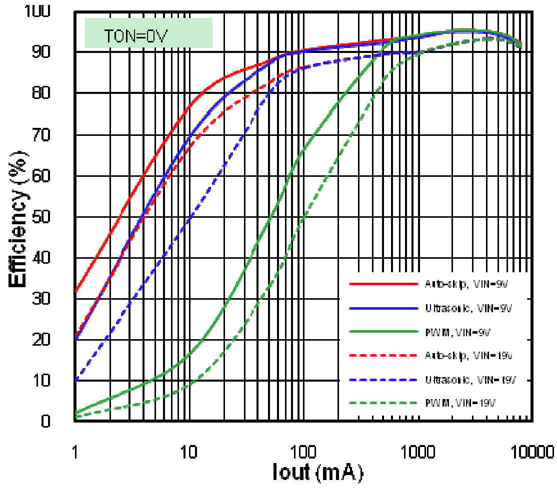


Fig4 Efficiency for VOUT2

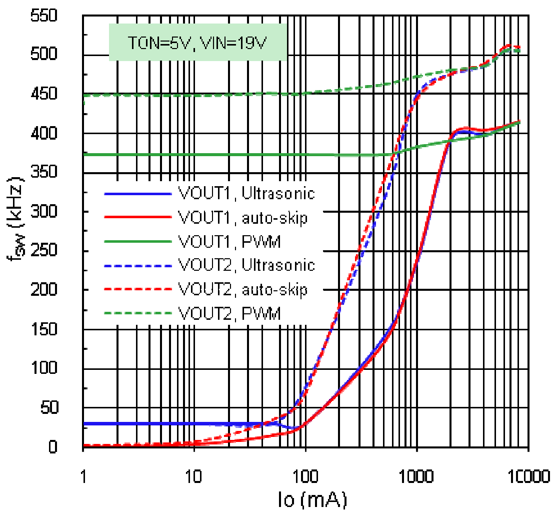


Fig5 Frequency vs. Output Current

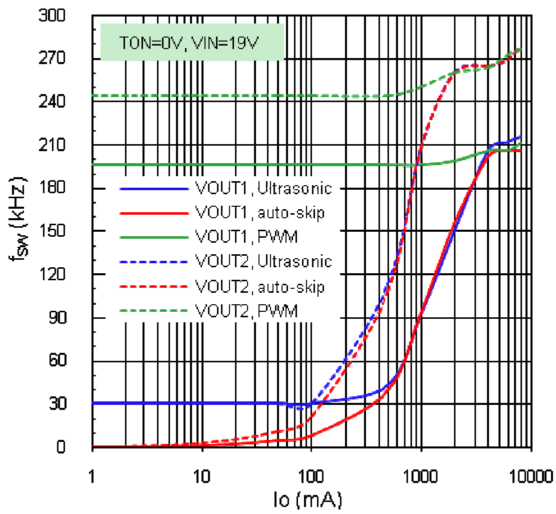


Fig6 Frequency vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

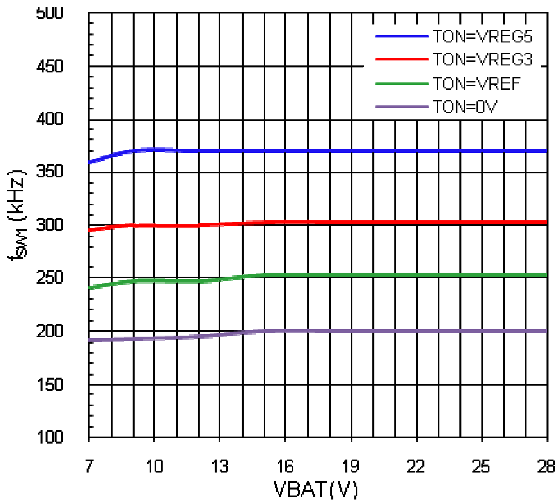


Fig7 Frequency vs. Input Voltage

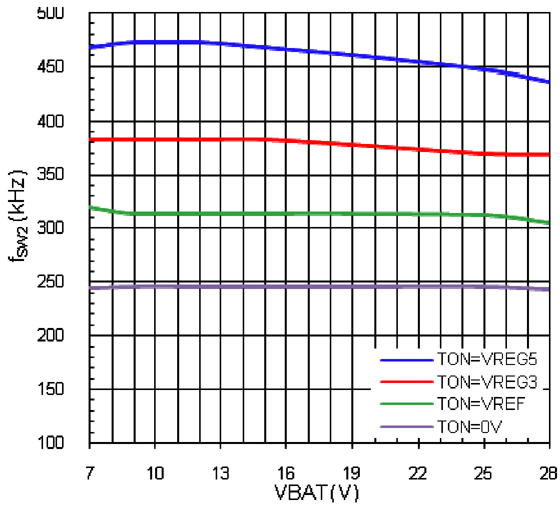


Fig8 Frequency vs. Input Voltage

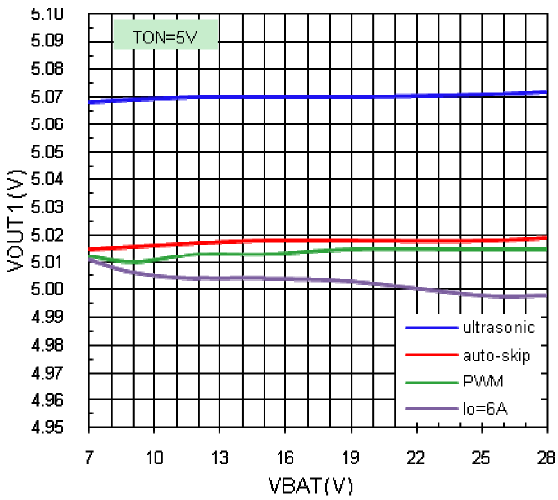


Fig9 VOUT1 Line Regulation

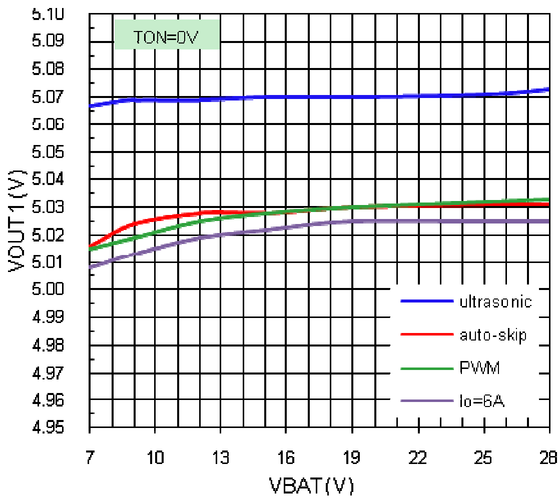


Fig10 VOUT1 Line Regulation

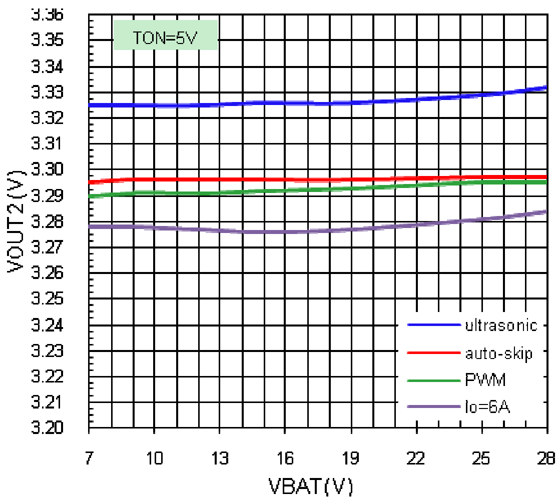


Fig11 VOUT2 Line Regulation

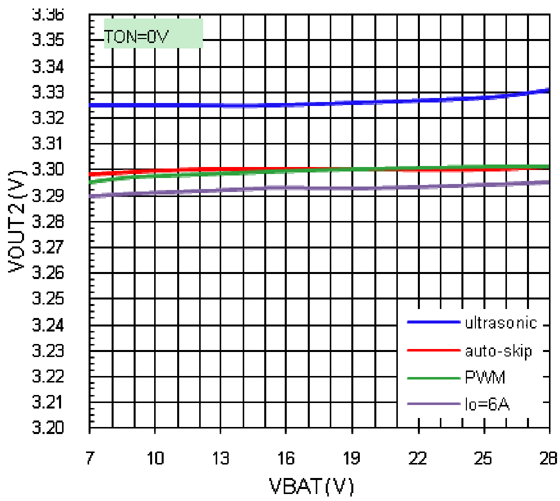


Fig12 VOUT2 Line Regulation

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

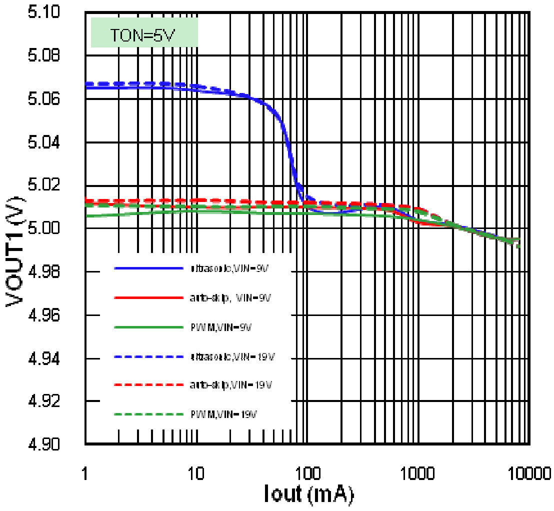


Fig13 VOUT1 Load Regulation

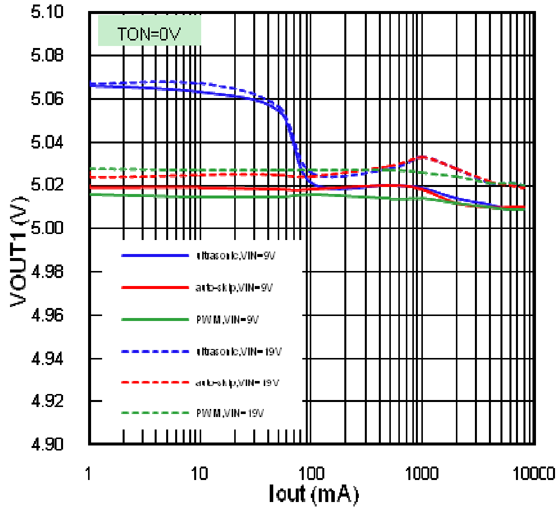


Fig14 VOUT1 Load Regulation

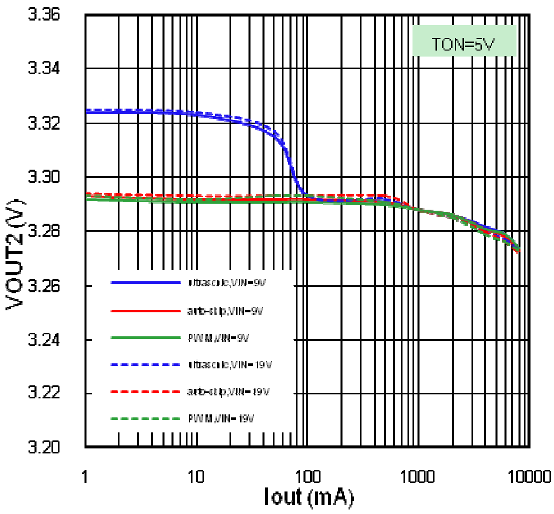


Fig15 VOUT2 Load Regulation

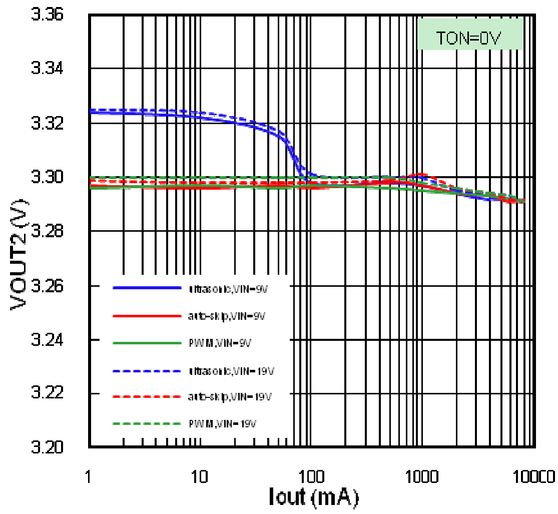


Fig16 VOUT2 Load Regulation

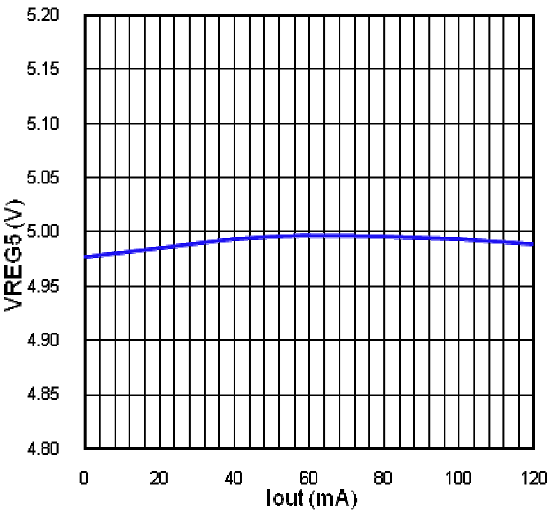


Fig17 VREG5 Load Regulation

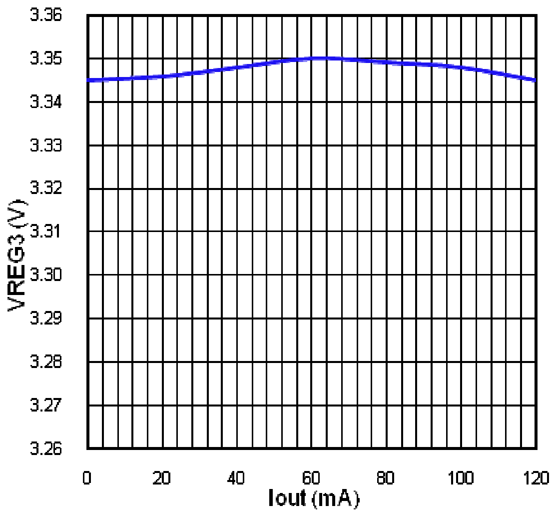


Fig18 VREG3 Load Regulation

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

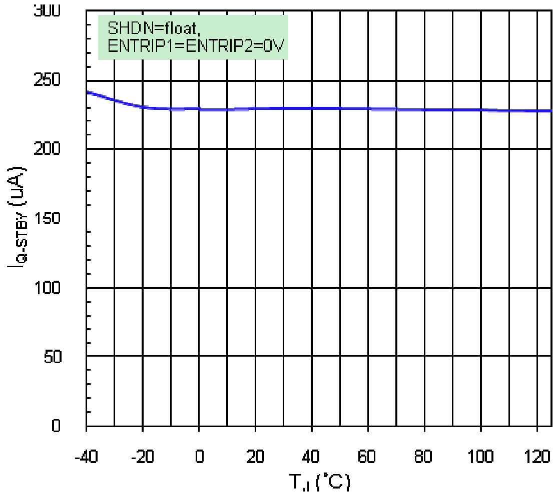


Fig19 VIN Standby Current vs. Temperature

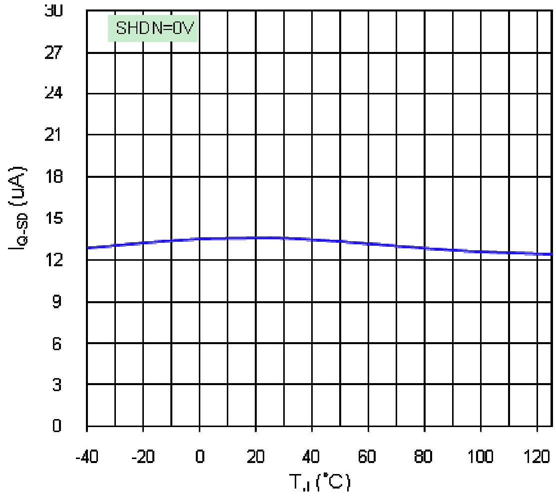


Fig20 VIN Shutdown Current vs. Temperature

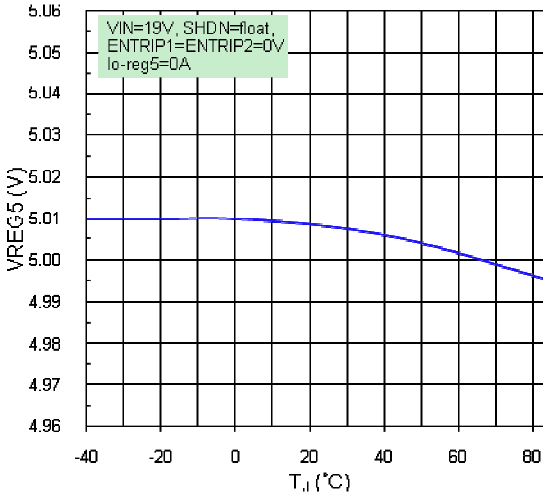


Fig21 VREG5 vs. Temperature

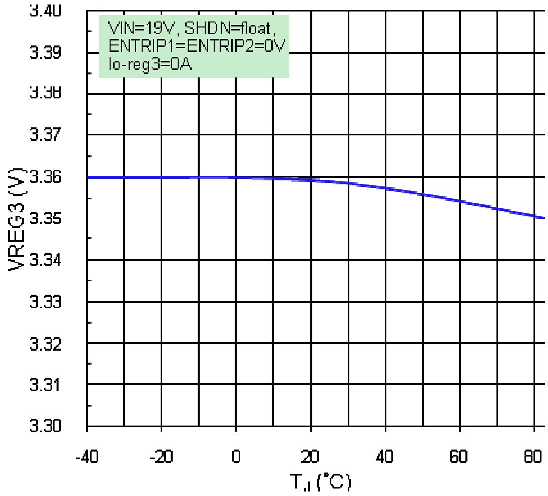


Fig22 VREG3 vs. Temperature

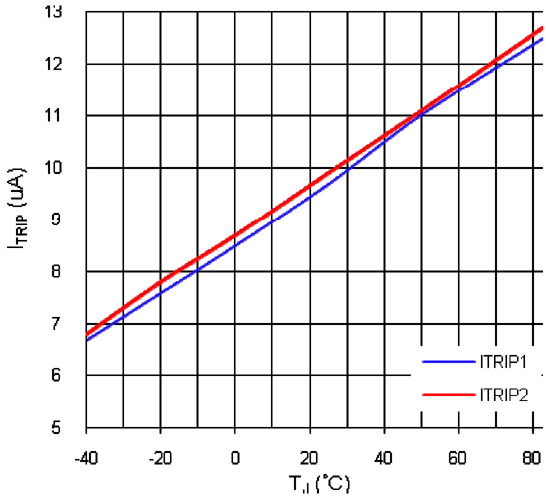


Fig23 Sense Current vs. Temperature

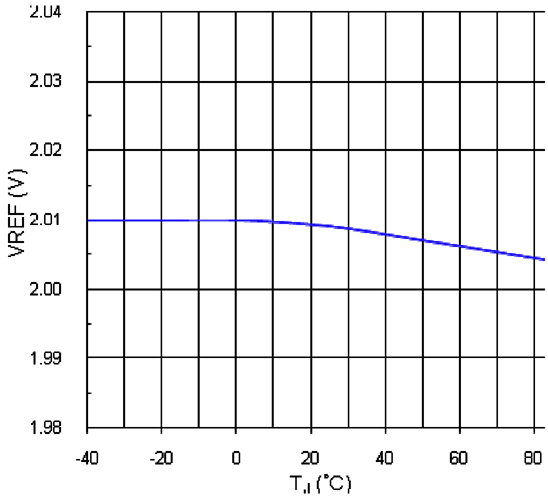


Fig24 Reference Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

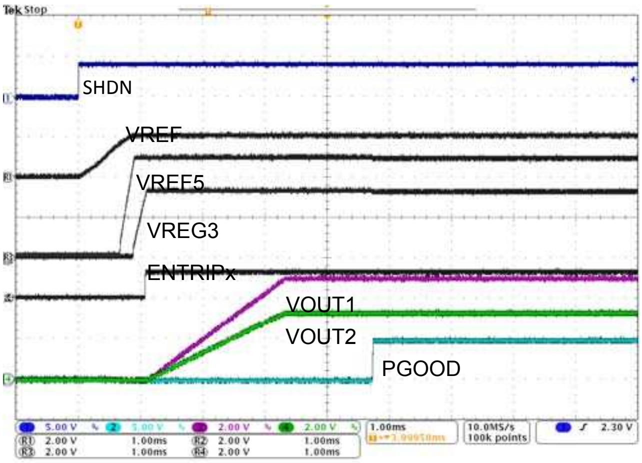


Fig25 SHDN On-state

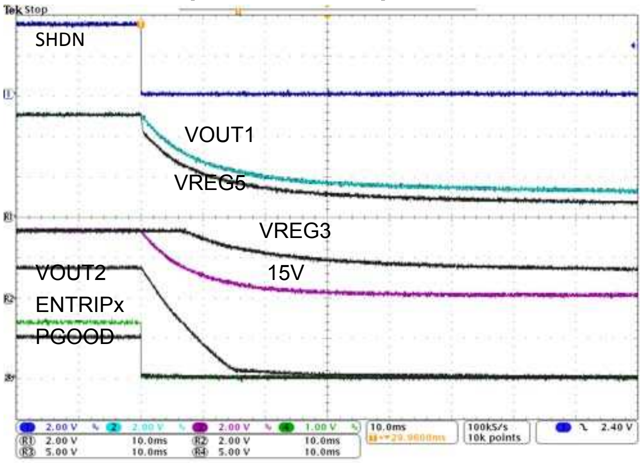


Fig26 SHDN Off-state

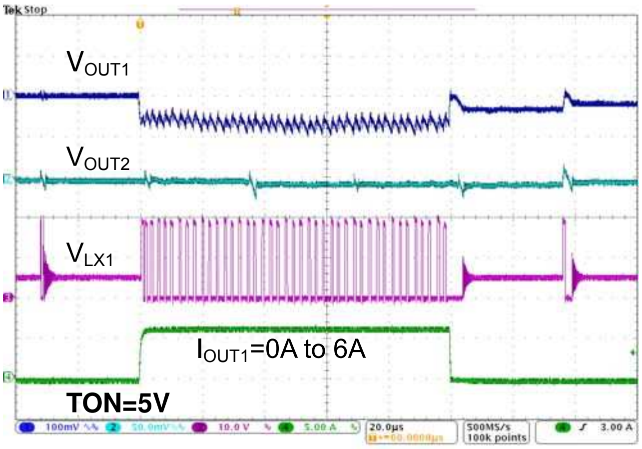


Fig27 OUT1 Load Transient, Ultrasonic Mode

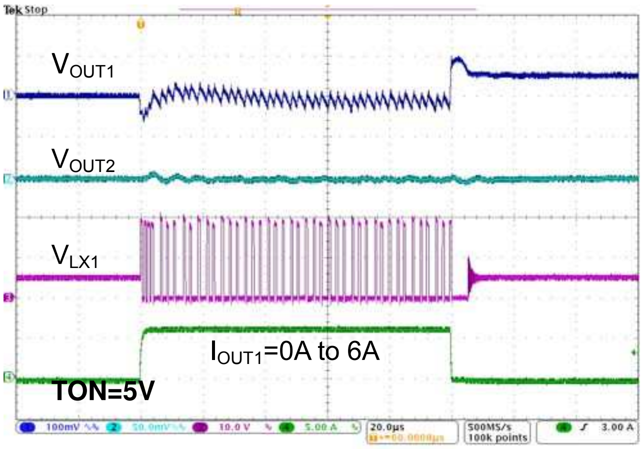


Fig28 OUT1 Load Transient, Auto-skip Mode

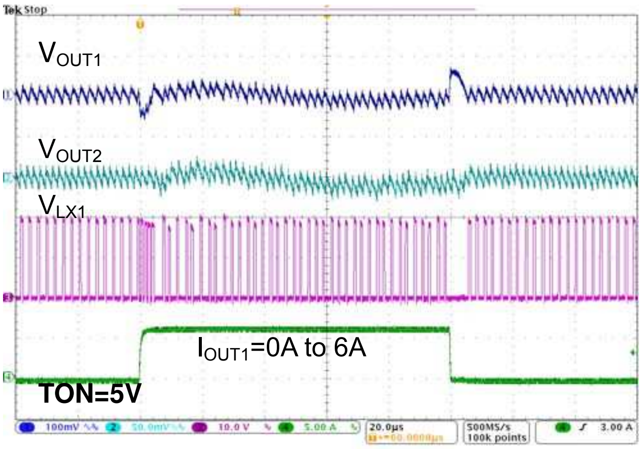


Fig29 OUT1 Load Transient, Forced-PWM Mode

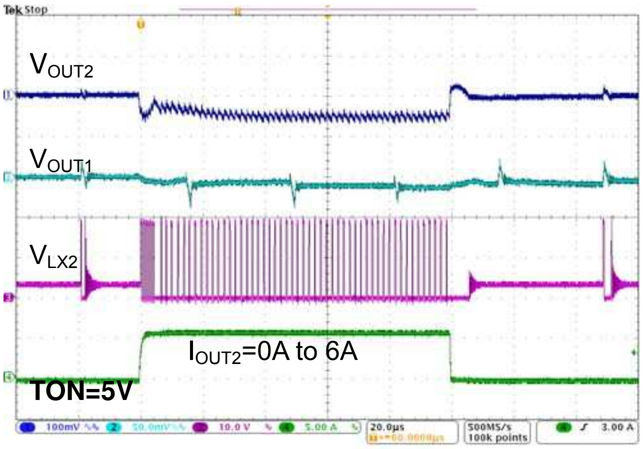


Fig30 OUT2 Load Transient, Ultrasonic Mode

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

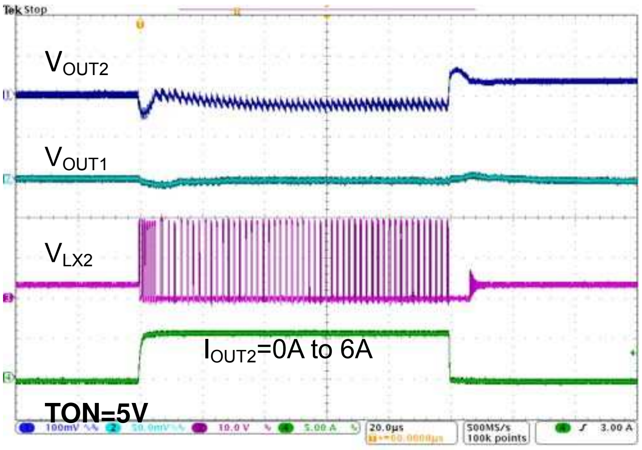


Fig31 OUT2 Load Transient, Auto-skip Mode

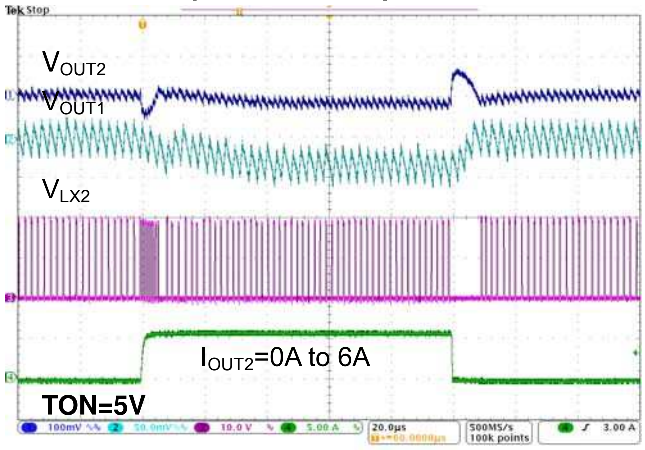


Fig32 OUT2 Load Transient, Forced-PWM Mode

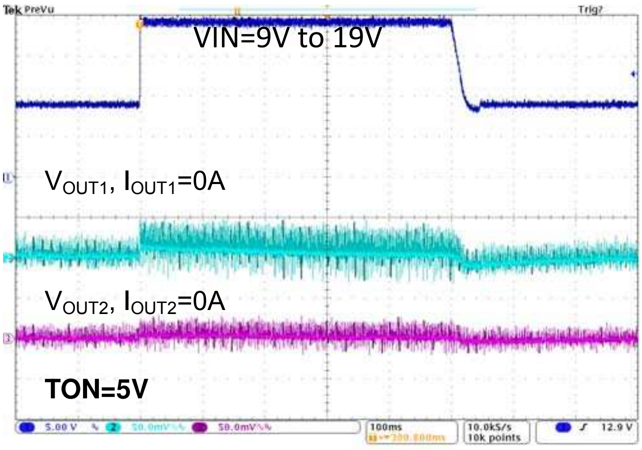


Fig33 Line Transient, Ultrasonic Mode

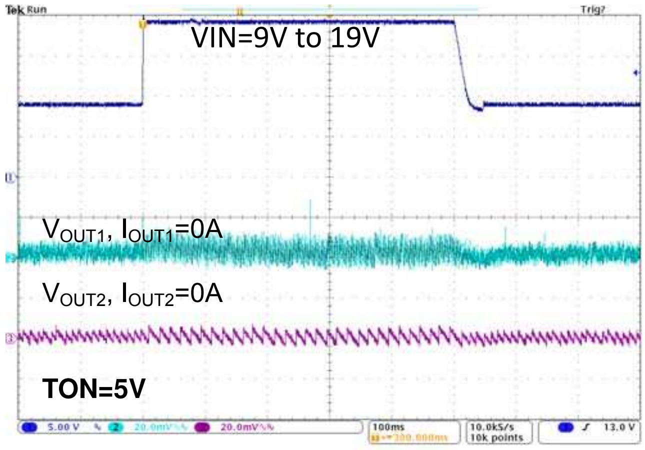


Fig34 Line Transient, Auto-skip Mode

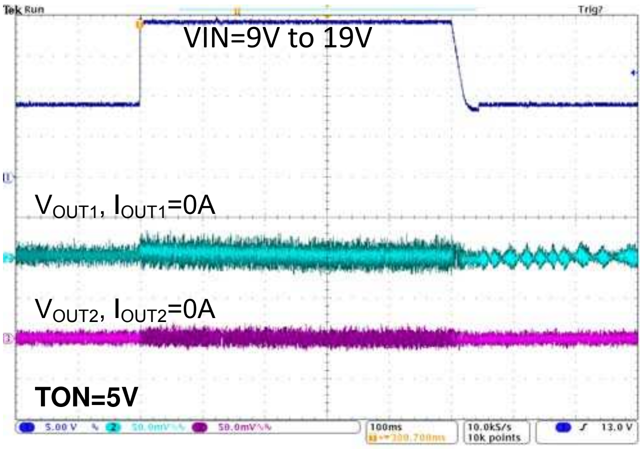


Fig35 Line Transient, Forced-PWM Mode

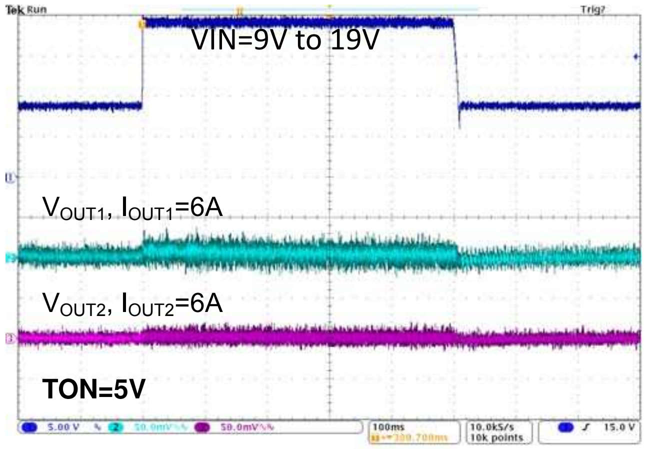


Fig36 Line Transient, IOUT1= IOUT2=6A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

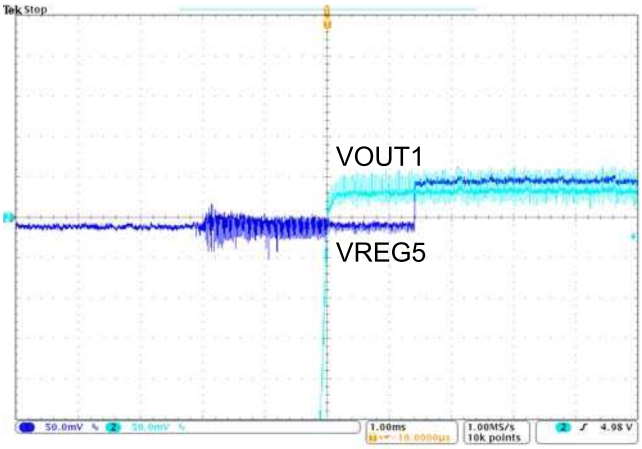


Fig37 VREG5 switchover to VOUT1

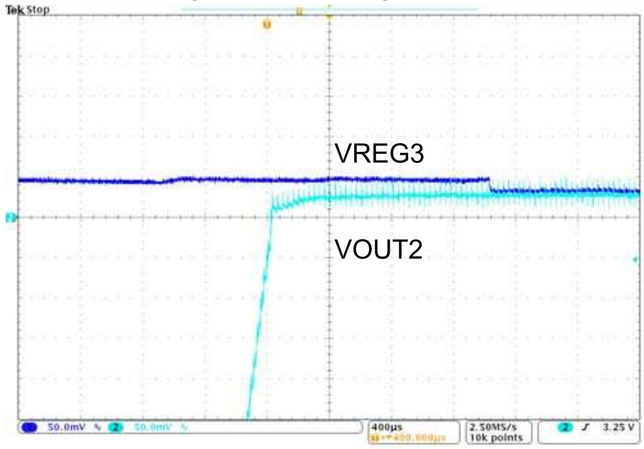


Fig38 VREG3 switchover to VOUT2

DETAIL DESCRIPTION

The APE3520/A synchronous buck controller is designed for power supplies for notebook PC applications. The APE3520/A control scheme is a constant-on-time, pseudo-fixed frequency, PWM controller and specifically designed for leading fast load transient while maintaining a relative constant switching frequency and operating over a wide range of input voltage. This architecture depends on the ESR of output capacitor; the output ripple voltage across the ESR provides the PWM ramp signal, eliminating the need for compensation circuit. The high-side switch on-time is determined by an internal one-shot which pulse width is inversely proportional to input voltage and proportional to output voltage. Another one-shot sets a minimum off-time (300ns typ.). The on-time one-shot is triggered if the error comparator is low.

On-Time One-Shot (T_{ON})

The core of pseudo fixed frequency PWM is the one-shot that sets the on-time of high-side switch for the controller. This low jitter, adjustable one-shot includes circuitry that varies the on-time in response to VIN and output voltage. The on-time is disproportional to the input voltage, and proportional to the output voltage, so that the duty ratio is kept as VOUT/VIN theoretically.

Switch frequency / Mode selection

The switching frequency is selection from four preset values by the TON setting as shown in Table 1. The APE3520/A operates with forced-PWM, auto-skip or ultrasonic mode by the SKIP setting to provide multi-function as Table 2.

TON Setting	**Switching Frequency (kHz)**	
	VOUT1	VOUT2
5V (VREG5)	365kHz	460kHz
3V (VREG3)	300kHz	375kHz
2V (VREF)	245kHz	305kHz
0V (GND)	200kHz	250kHz

Table1 Frequency Selection

SKIP Setting	**Operation Mode**
3V/5V (VREG3/VREG5)	Ultrasonic Mode
2V (VREF)	Auto-Skip Mode
0V (GND)	Forced-PWM Mode

Table2 Mode Selection

DETAIL DESCRIPTION (Continued)

Ultrasonic Mode

In ultrasonic mode, the switching frequency keeps 30kHz to avoid the audible frequencies at light load condition. The control circuit monitors both MOSFET and force into the 'ON' state if both of MOSFETs are off for more than 33us. The output is toward overcharge results from the h-side MOSFET is turned on even the output voltage is higher than the target value. So that, the output voltage is 1% higher than auto-skip mode operation.

Auto-Skip Mode

In auto-skip mode, the internal Zero-Cross comparator looks for inductor current. When the zero current is detected, the controller enters auto-skip mode and turns low-side MOSFET off on each cycle. If the inductor current does not cross zero, the controller immediately exits auto-skip mode. At light load condition, the APE3520/A operates in power save mode and reduces the switching frequency automatically to maintain high efficiency. This decreased frequency is performed smoothly and without increasing output ripple. The boundary between continuous and discontinuous inductor-current conduction mode, $I_{OUT(LB)}$, can be calculated by:

$$I_{OUT(LB)} = \frac{1}{2 \times L \times f_{sw}} \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Forced-PWM Mode

The low-noise, forced PWM mode disables the zero-crossing comparator, which controls the low-side switch on-time. The constant switching frequency has two benefits: first, the frequency can be selected to avoid noise-sensitive regions; second, the inductor ripple-current remains relatively constant which resulting in easy to design and predictable output voltage ripple.

Soft Start

The APE3520/A has an internal, 1.6ms, soft start with overcurrent limit. When the ENTRIPx pin rises above the enable threshold, the switch controller enters its start-up sequence. Soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge currents.

Soft Stop

The APE3520/A discharges output by an internal MOSFET connected between VOUTx and GND while ENTRIPx is low or any fault shutdown condition. The discharge time is depended on the output capacitance and the discharge resistance.

DETAIL DESCRIPTION (Continued)

Enable

SHDN pin controls VREF, VREG3 and VREG5 regulators. ENTRIPx pin controls VOUT1 and VOUT2. Connect SHDN node to GND to disable the device and minimize the shutdown current. Pulling SHDN node high will turn the three regulators on; two switch power supplies are into standby mode and wait ENTRIPx to enable. The enable state refers to table3.

SHDN	ENTRIP1	ENTRIP2	VREG5	VREG3	VOUT1	VOUT2	VCLK
620k to GND	low	low	on	on	off	off	off
620k to GND	low	high	on	on	off	on	off
620k to GND	high	low	on	on	on	off	off
620k to GND	high	high	on	on	on	on	off
Float	low	low	on	on	off	off	off
Float	low	high	on	on	off	on	off
Float	high	low	on	on	on	off	on
Float	high	high	on	on	on	on	on

Table3 Enable State

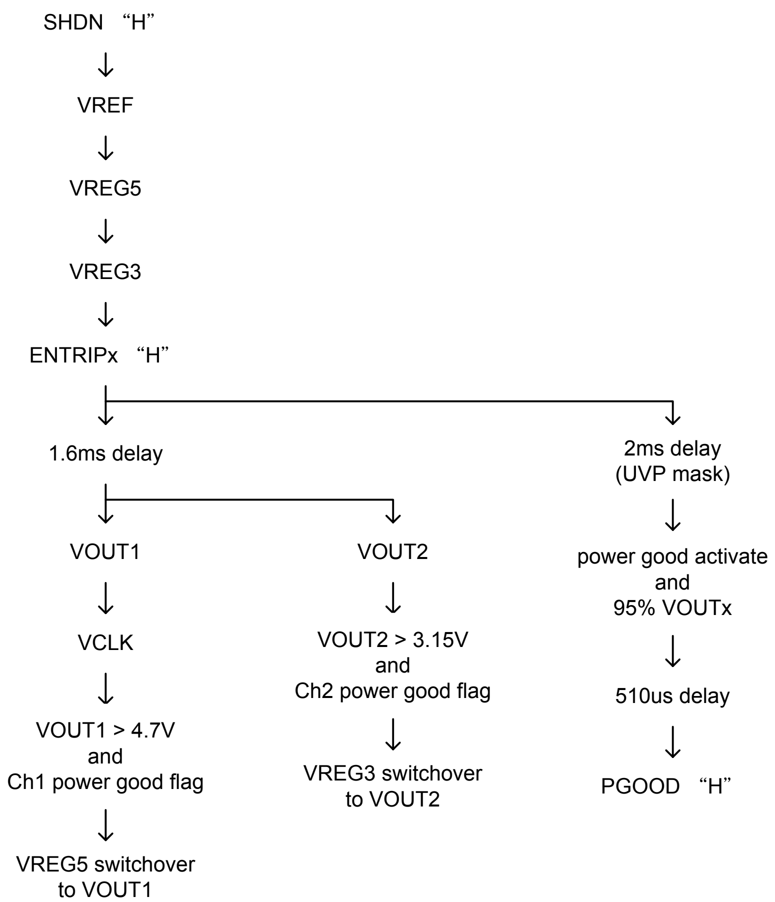


Fig39 Enable Timing

DETAIL DESCRIPTION (Continued)

Linear Regulator (VREG5/VREG3)

The APE3520/A builds two linear regulators internally which are 5V (VREG5) and 3.3V (VREG3). Both of them have 100mA current ability. Place a 10uF ceramic capacitor close to the VREG5 and VREG3 pins to stabilize the regulators. If VREG3 is not loaded, a 1uF ceramic capacitor is acceptable.

Regulator Switchover

If VOUT1 voltage is higher than 4.7V and internal power good flag of ch1 is generated, the internal 5V regulator is turn off and the VREG5 output is connected to VOUT1 by internal MOSFET.

If VOUT2 voltage is higher than 3.15V and internal power good flag of ch2 is generated, the internal 3.3V regulator is turn off and the VREG3 output is connected to VOUT2 by internal MOSFET.

When VREG5 and VREG3 switch to VOUT1 and VOUT2, the current ability of them will limit by the R_{ON} of the internal MOSFET, 3Ω and 4Ω, receptively.

Power Good Output

The APE3520/A provides a power good (PGOOD) output, which is an open-drain output requiring a pull-up resistor. Typically connect to VREG5 through a 100kΩ resistor. The PGOOD comparator continuously monitors the output for both over-voltage and under-voltage conditions. In shutdown and soft-start period, PGOOD is actively low. The power good function is triggered after 2ms delay time when ENTRIPx goes high and both switcher outputs are within 95% of the targets, PGOOD will indicates high after 510us delay. If the output voltage is without 90% or 110% of the target threshold, the PGOOD becomes low immediately. Note that the PGOOD window detector is independent of the output over-voltage and under-voltage protection thresholds, but held low after an UVP or OVP.

Under-Voltage Lockout Protection (UVLO)

The APE3520/A has VREG5 and VREG3 under-voltage lockout protection (UVLO). This is a non-latched protection. When the VREG5 or VREG3 voltage is lower than the UVLO threshold, both switcher outputs are also shut off.

Under Voltage Protection (UVP)

If VFBx falls lower than 60% of nominal value, the UDx and LDx are pulled low to turn off the MOSFETs after 32us. The APE3520/A latches off until the SHDN or ENTRIPx input is re-started. The UVP function is disabled during soft start period.

Over Voltage Protection (OVP)

If VFBx exceeds 115% of nominal value or VOUTx become high than 5.75V, over-voltage protection is triggered. The LDx latches high and the low side MOSFET is turned on and high side MOSFET is turned off. This action discharges the output capacitor rapidly. DLx stays high and the output latches off until the SHDN or ENTRIPx input is re-started.

DETAIL DESCRIPTION (Continued)

Current Limit Protection

The current-limit circuit of APE3520/A senses the $R_{DS\text{-}ON}$ of low-side MOSFET, monitors valley inductor current. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. The current limit threshold is adjusted with an external resistor at ENTRIPx pin. V_{ENTRIP} is set the current limit valley level, which is the following equation:

$$V_{ENTRIP}(mV) = R_{ENTRIP}(k\Omega) \times I_{ENTRIP} = R_{ENTRIP}(k\Omega) \times 10uA$$

Note that V_{ENTRIP} is internally limited ranging is from 0.515V to 2V.

The valley current limit threshold can be given as:

$$I_{OC(Valley)} = \frac{R_{ENTRIP}(k\Omega) \times I_{ENTRIP}(uA)}{8 \times R_{DS-ON}(m\Omega)} = \frac{V_{ENTRIP}(mV)}{8 \times R_{DS-ON}(m\Omega)}$$

Therefore, the load current at over-current threshold, Iocp, can be calculated as follows:

$$I_{OCP} = I_{OC(Valley)} + \frac{\Delta I_L}{2} = \frac{V_{ENTRIP}}{8 \times R_{DS-ON}} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}$$

The output voltage tends to fall down cause of an over current condition. Finally, it crosses the UVP threshold and shuts down the controller. The APE3520/A also supports temperature compensated for $R_{DS\text{-}ON}$ sensing. I_{ENTRIP} has 4500ppm/°C temperature coefficient to compensate the temperature dependency of the $R_{DS\text{-}ON}$ to keep almost identical current limit threshold in operation temperature range.

There is also a negative current limit in the forced continuous conduction mode that prevents excessive reverse inductor currents when VOUTx is sinking current. The negative current limit detect threshold is approximate to the negative polarity of positive current limit threshold.

Switch Output Voltage Setting

The two switch output can be adjusted to a voltage range from 2V to 5.5V. The output voltage can be calculated as:

$$V_{OUT1} = 2V \times (\frac{R1}{R2} + 1); \quad V_{OUT2} = 2V \times (\frac{R3}{R4} + 1)$$

Charge Pump

When SHDN is high than 2.4V, the CLK terminal generates 270kHz clock signal which can be used for charge pump circuit. VCLK is powered by VOUT1. If CLK is not used, one can let CLK pin open or SHDN pin connect to GND through a resistor to disable CLK.

APPLICATION INFORMATION

Inductor Selection

The inductor value determines the ripple current and the ripple voltage of the converter. This inductor choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The inductor selection is based on the ripple current which is typically set between 1/4 to 1/2 of the maximum load current. The switching frequency and ripple current determine the inductor which can be calculated as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN}}$$

The ripple current can be given by:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}}$$

Output Capacitor Selection

The output capacitor must have high enough ESR to satisfy the ripple requirements for loop stability. The important parameters of capacitor are the ESR, the capacitance value, the RMS ripple current rating, and the voltage rating. For the output capacitor of APE3520/A, ESR is the most important parameter. Determine ESR to meet the required ripple voltage as follow:

$$ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L}$$

A minimum ESR is required to generate the required ripple voltage for regulation. Due to the pseudo fixed frequency PWM mode not contain an error amplifier in the loop; a sufficient feedback signal needs to be provided from output ripple. The VFB required 20mV ripple signal at least. That will generate output ripple

ΔV_{OUT} = (VOUT/2) × 20mV

The capacitor is usually selected by ESR and voltage rating rather than by capacitance value. The conductive polymer capacitors are recommended to proper high capacitance and low ESR.

Stability Consideration

The constant on-time, pseudo fixed frequency PWM scheme has natural frequency jitter. An mV order of noise on the feedback signal affects the frequency jitter from a few to ten percent of switching frequency. Double pulse and feedback loop unstable results in unstable operation. Double pulse occurs because the insufficient ripple on the FBx, or the FBx and VOUTx ripple waveforms are very noisy and trigger the feedback comparator. If the ripple voltage of FBx is too small, the FBx waveform will be interfered with switching noise. The noise causes the FBx comparator to trigger too quickly after the 300ns minimum off -time. Double pulse will result in higher output ripple voltage but in most cases is harmless.

APPLICATION INFORMATION (Continued)

Design Procedure

First of all, specify the external component, input voltage range, output voltage tolerance, load current, and the desired switching frequency. There are two values of load current to consider: continuous and peak load current. Continuous load current is concerned with thermal stresses of MOSFETs. Peak load current determines the components stresses and design of threshold of the current limit. The following guidelines will help calculate the external components of the APE3520/A as Typical Application Circuit.

1. Select inductor. Before determine the inductance, the ripple current, ΔI_L, must be defined first, typically set between 1/4 to 1/2 of the maximum load current. The ripple current can be defined as:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}}$$

The inductor value can be calculated as follows:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{\Delta I_L \times f_{SW} \times V_{IN(max)}}$$

The inductor current must be rated for maximum peak current.

$$I_{L(PEAK)} = I_{OC(Valley)} + \Delta I_L = \frac{V_{ENTRIP}}{R_{DS-ON}} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}}$$

2. Select R1, R2, R3 and R4. The recommended value for R2 and R4 are between 10kΩ and 20kΩ.

$$R1 = R2 \times \left(\frac{V_{OUT1} - 2}{2}\right); \quad R3 = R4 \times \left(\frac{V_{OUT2} - 2}{2}\right)$$

3. Choose output capacitor. The output capacitance is based on transient ability.

$$C_{OUT(min)} = \frac{L \times (I_{out(max)} + 0.5\Delta I_L)^2}{\Delta V_{OUT}^{\ 2}}$$

Determine ESR to meet the required ripple voltage, above 20mV. $ESR(m\Omega) = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{20mV \times V_{OUT}}{\Delta I_L \times 2V}$

4. Decide current limit threshold. Determine the current limit threshold when minimum VIN and maximum load current conditions. The $R_{ENTRIPx}$ determines by

$$R_{ENTRIPx}(\Omega) = \frac{R_{DS-ON}}{10uA} \times \left(I_{OCP} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}\right)$$

APPLICATION INFORMATION (Continued)

Layout Considerations

The switching power stages require more attention in PCB layout. Keep the high current paths short. Separate the ground terminals. Four-layer board is recommended. Use two middle layers as ground planes, with interconnections between top and bottom layers as needed. Below lists help start layout work.

1. Minimize the resistance by keeping the power component group together with short and wide trace (60mil at least).
2. Connect the drivers of UDx and LDx close to the gate of high-side and low-side MOSFET with short trace as possible to reduce stray inductance.
3. Keep sensitive analog node (FBx, ENTRIPx, VOUTx, REF, TON and SKIP) away from high-speed switching loop to avoid noise coupling.
4. Place feedback resistors near FBx and GND pin with short wire and should be far away to the noise source, such as switching loop. Use ground plane to shield feedback trace from power components.
5. The current limit setting resistor, $R_{ENTRIPx}$, should connect to ENTRIPx and GND pin directly.
6. Place the bypass capacitor of VIN, REF, VREG5, and VREG3 close to the pin.
7. Group the analog ground connection of the VREF bypass capacitors, VFBx, and ENTRIPx. Connect the analog ground plane directly to GND pin of the IC.
8. Group the power ground connection of the VIN capacitor, VOUT capacitor, the low-side MOSFETs, charge pump circuit, VREG5 and VREG3 as close as possible. Connect this power ground plane directly to PGND pin of the IC.
9. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.
10. Use plane connection between GND (analog ground) and PGND (power ground) near the IC.

MARKING INFORMATION

QFN 4x4-24L