

AP9973GM

Pb Free Plating Product

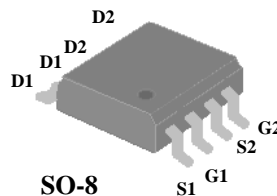


**Advanced Power
Electronics Corp.**

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

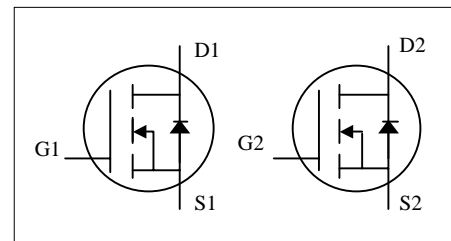
- ▼ Low Gate Charge
- ▼ Single Drive Requirement
- ▼ Surface Mount Package
- ▼ RoHS Compliant



BV_{DSS}	60V
$R_{DS(ON)}$	80m Ω
I_D	3.9A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, lower on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current ³ , $V_{GS} @ 10V$	3.9	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current ³ , $V_{GS} @ 10V$	2.5	A
I_{DM}	Pulsed Drain Current ^{1,2}	20	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ C/W$



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Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1\text{mA}$	-	0.06	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=3.9A$	-	-	80	$m\Omega$
		$V_{GS}=4.5V, I_D=2A$	-	-	100	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=3.9A$	-	3.5	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=48V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=3.9A$	-	8	13	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=48V$	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=30V$	-	8	-	ns
t_r	Rise Time	$I_D=1A$	-	4	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	20	-	ns
t_f	Fall Time	$R_D=30\Omega$	-	6	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	700	1120	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	80	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	50	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=3.9A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_S=3.9A, V_{GS}=0V,$	-	28	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	35	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in^2 copper pad of FR4 board; $135^\circ\text{C}/W$ when mounted on min. copper pad.

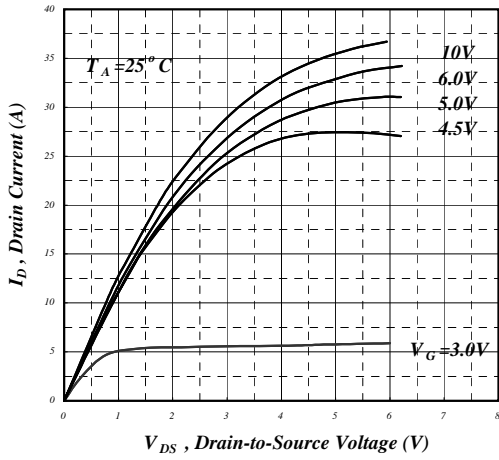


Fig 1. Typical Output Characteristics

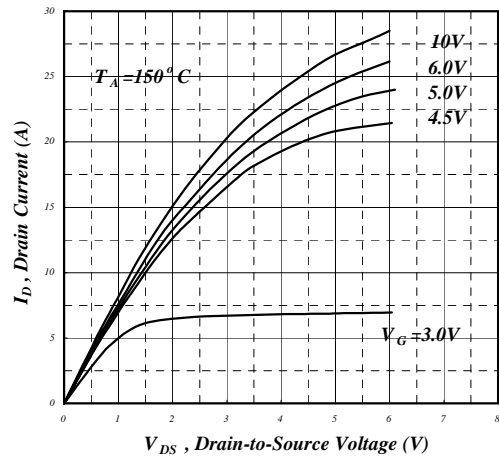


Fig 2. Typical Output Characteristics

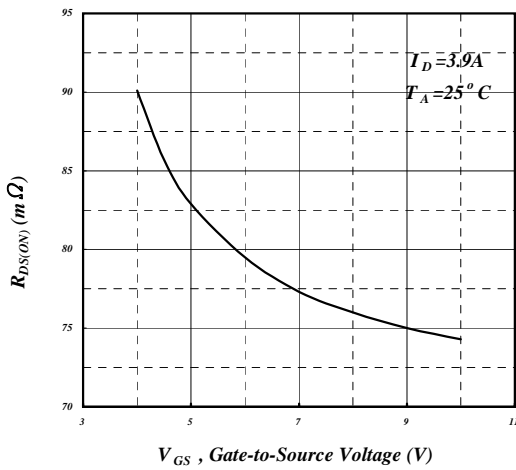


Fig 3. On-Resistance v.s. Gate Voltage

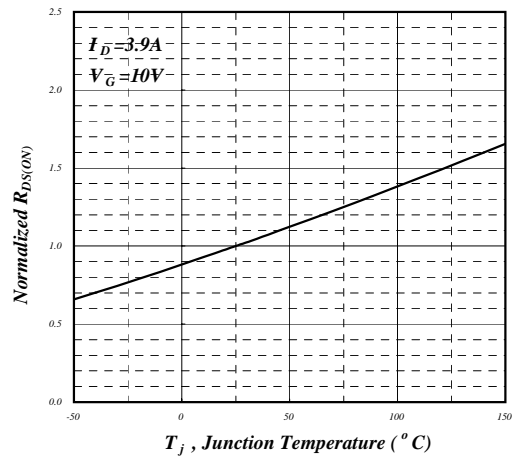


Fig 4. Normalized On-Resistance v.s. Junction Temperature

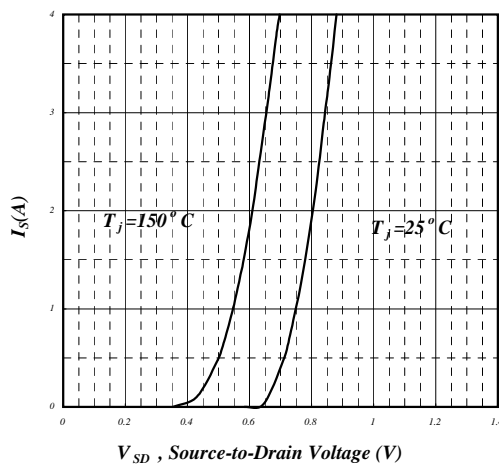


Fig 5. Forward Characteristic of Reverse Diode

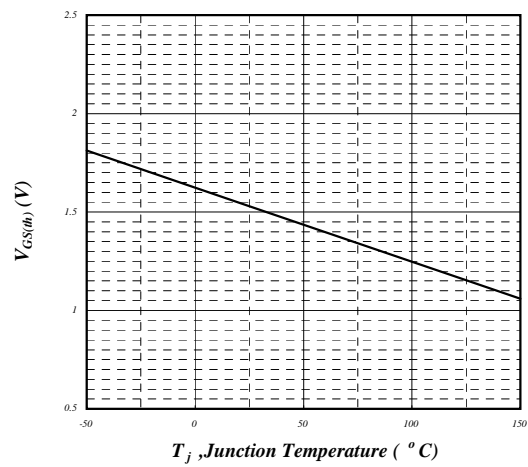


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

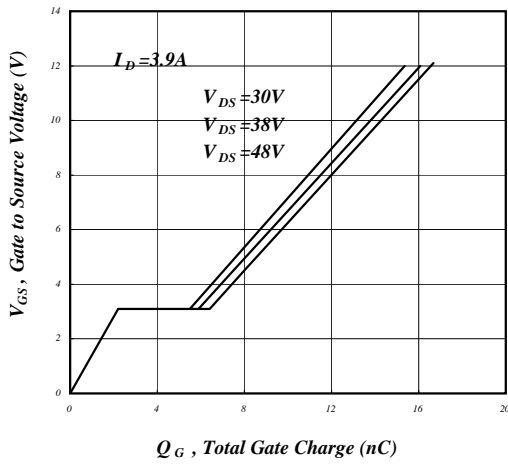


Fig 7. Gate Charge Characteristics

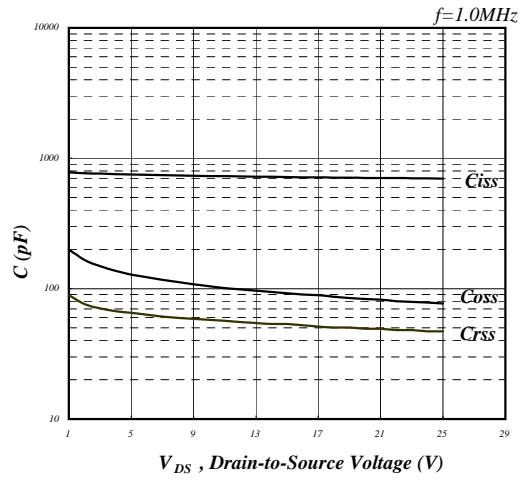


Fig 8. Typical Capacitance Characteristics

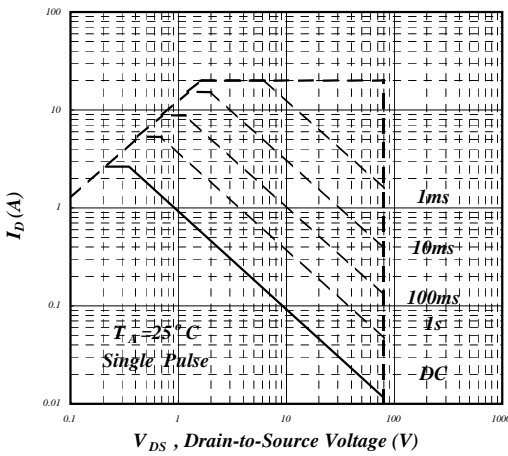


Fig 9. Maximum Safe Operating Area

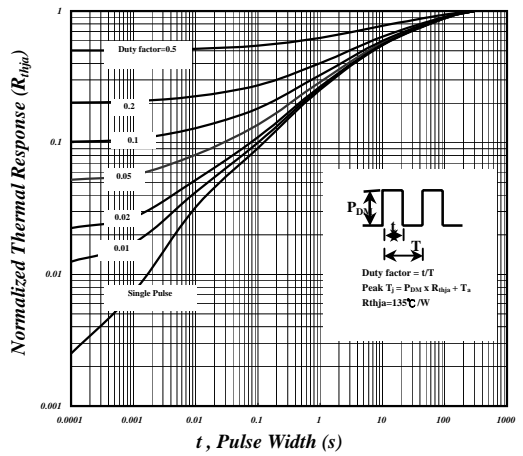


Fig 10. Effective Transient Thermal Impedance

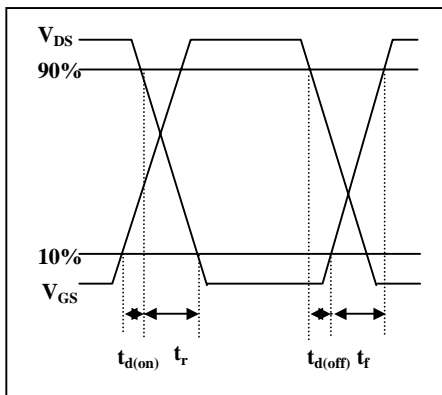


Fig 11. Switching Time Waveform

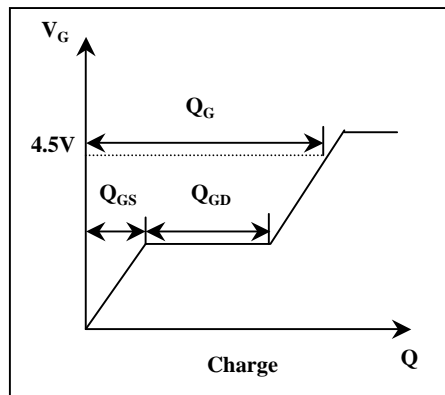


Fig 12. Gate Charge Waveform