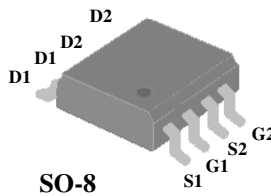




- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Performance
- ▼ RoHS Compliant

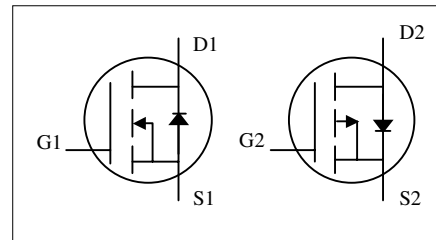


N-CH	BV_{DSS}	60V
	$R_{DS(ON)}$	36m Ω
	I_D	6A
P-CH	BV_{DSS}	-60V
	$R_{DS(ON)}$	72m Ω
	I_D	-4.2A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	6	-4.2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	4.7	-3.3	A
I_{DM}	Pulsed Drain Current ¹	30	-30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	62.5	$^\circ C/W$



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N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.04	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	-	-	36	mΩ
		V _{GS} =4.5V, I _D =3A	-	-	42	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	-	8	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =60V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =48V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =5A	-	18	29	nC
Q _{gs}	Gate-Source Charge	V _{DS} =48V	-	5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	10	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =30V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	32	-	ns
t _f	Fall Time	R _D =30Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1670	2670	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	160	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	117	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =1.7A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =5A, V _{GS} =0V	-	34	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	48	-	nC



P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-60	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.04	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-4A	-	-	72	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	88	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-4A	-	6	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-60V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-48V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-4A	-	21	34	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-48V	-	5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	9	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-30V	-	12	-	ns
t _r	Rise Time	I _D =-1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =-10V	-	82	-	ns
t _f	Fall Time	R _D =30Ω	-	36	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1780	2850	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	157	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-1.7A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =-4A, V _{GS} =0V	-	43	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	87	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board ; 135°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.
 USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.
 APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED
 HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.
 APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE
 RELIABILITY, FUNCTION OR DESIGN.



AP4575GM-HF

N-Channel

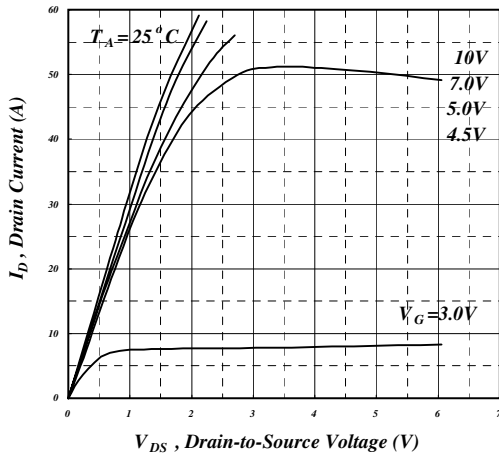


Fig 1. Typical Output Characteristics

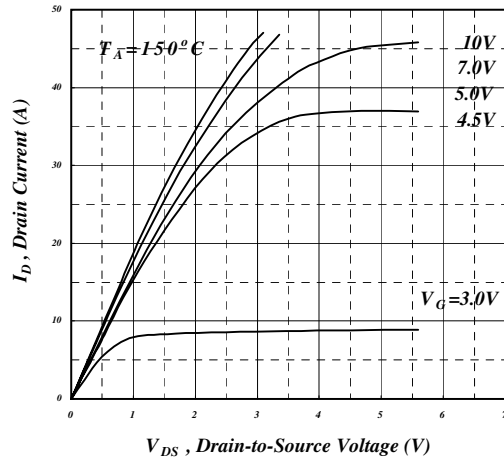


Fig 2. Typical Output Characteristics

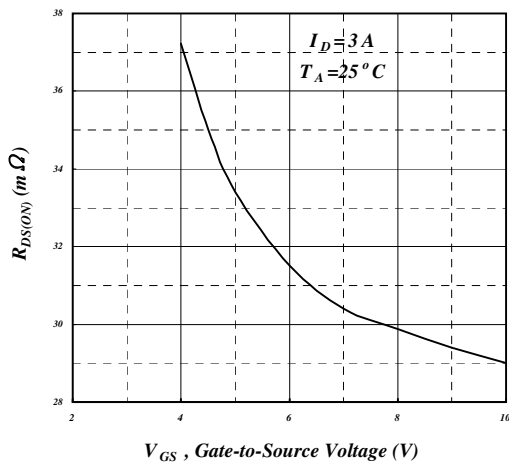


Fig 3. On-Resistance v.s. Gate Voltage

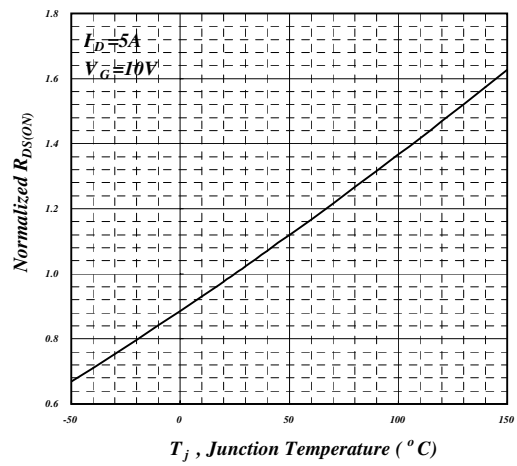


Fig 4. Normalized On-Resistance v.s. Junction Temperature

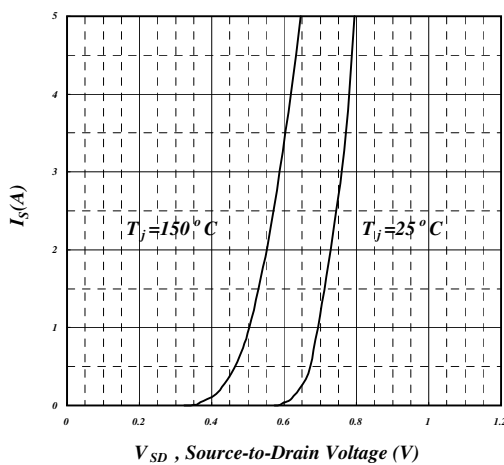


Fig 5. Forward Characteristic of Reverse Diode

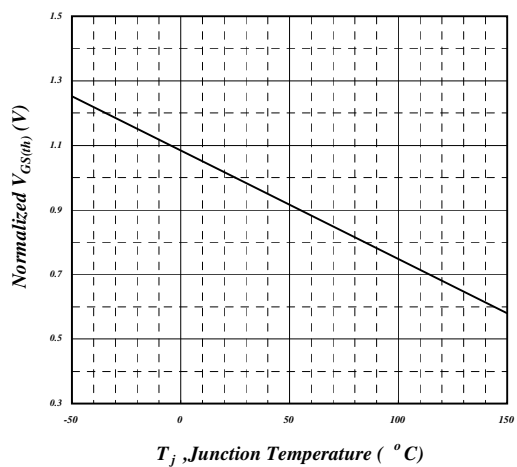


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

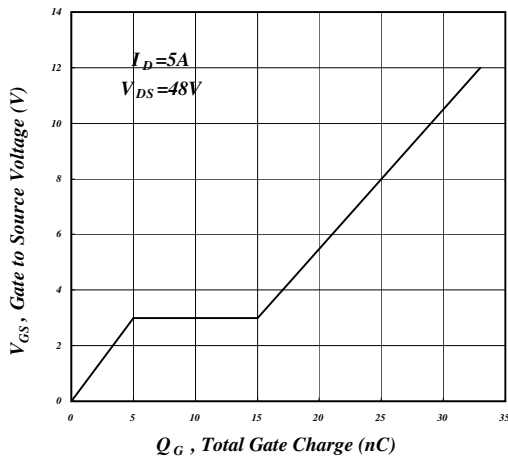


Fig 7. Gate Charge Characteristics

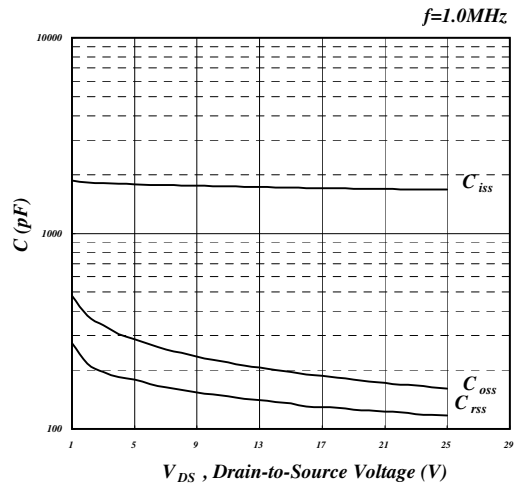


Fig 8. Typical Capacitance Characteristics

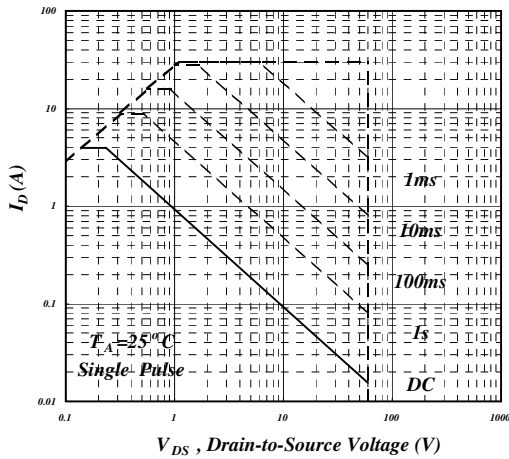


Fig 9. Maximum Safe Operating Area

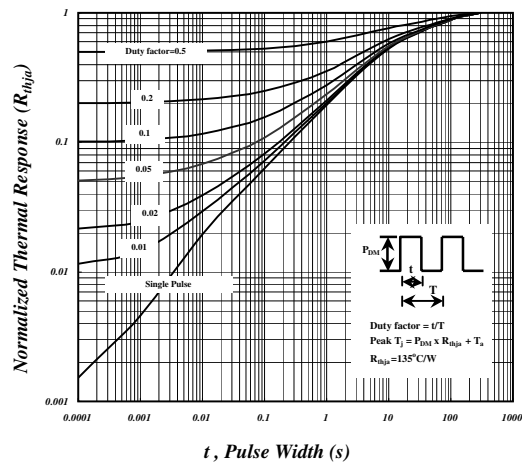


Fig 10. Effective Transient Thermal Impedance

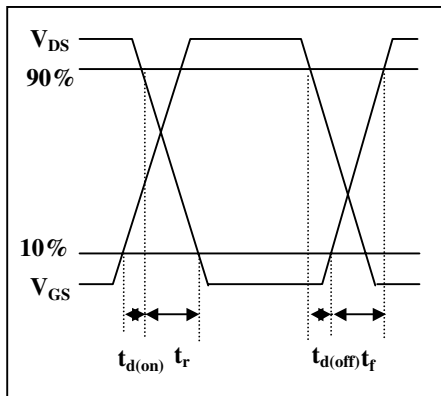


Fig 11. Switching Time Waveform

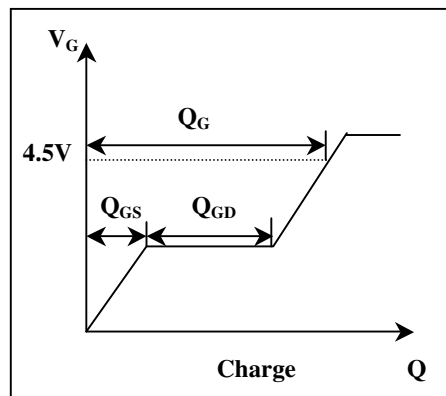


Fig 12. Gate Charge Waveform



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P-Channel

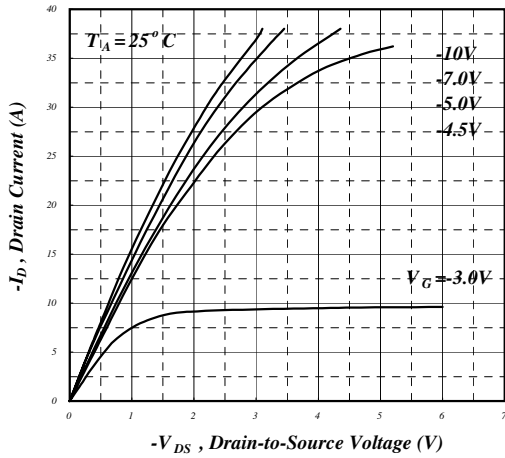


Fig 1. Typical Output Characteristics

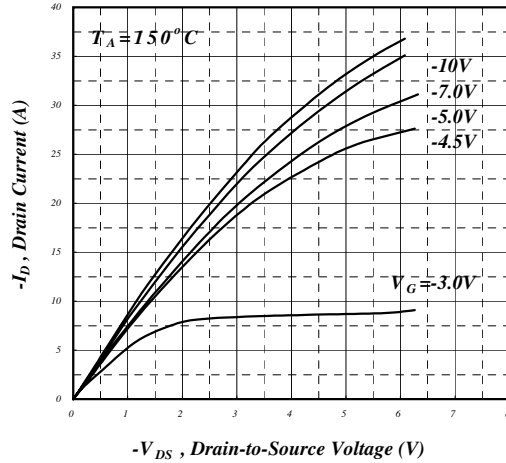


Fig 2. Typical Output Characteristics

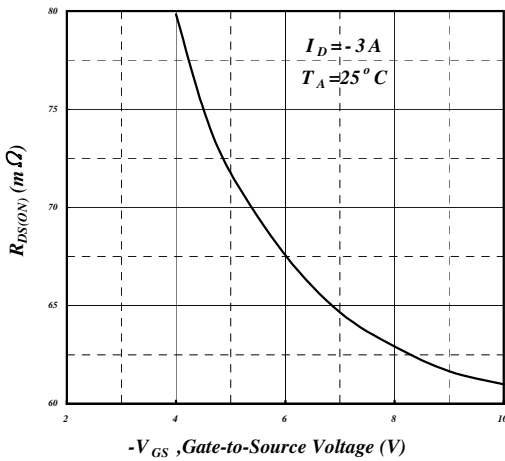


Fig 3. On-Resistance v.s. Gate Voltage

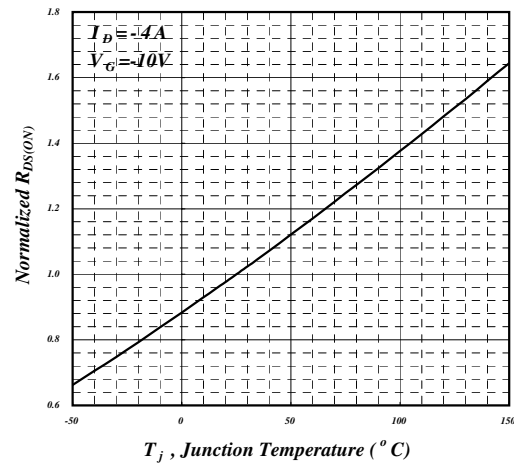


Fig 4. Normalized On-Resistance v.s. Junction Temperature

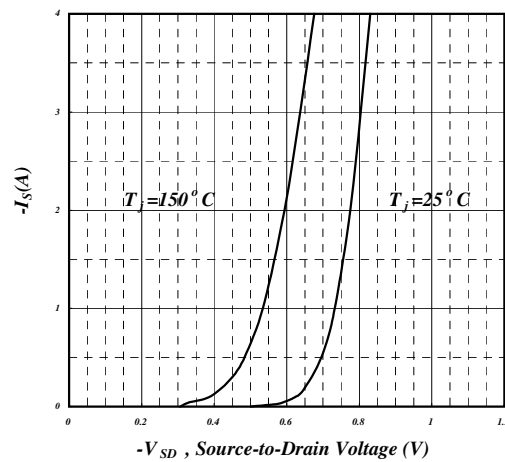


Fig 5. Forward Characteristic of Reverse Diode

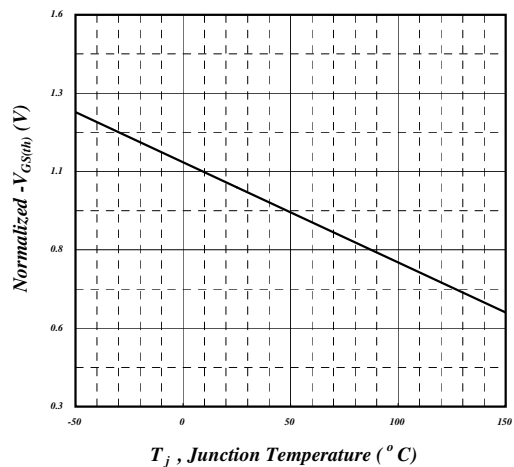


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

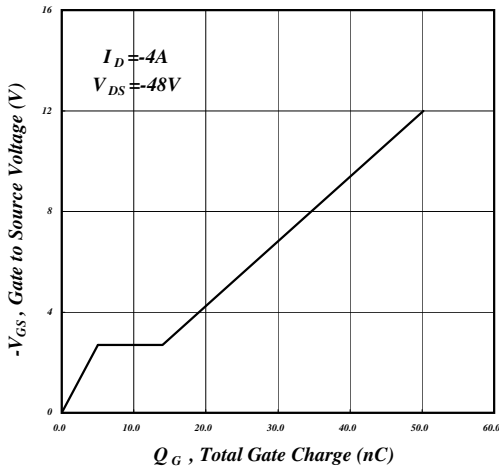


Fig 7. Gate Charge Characteristics

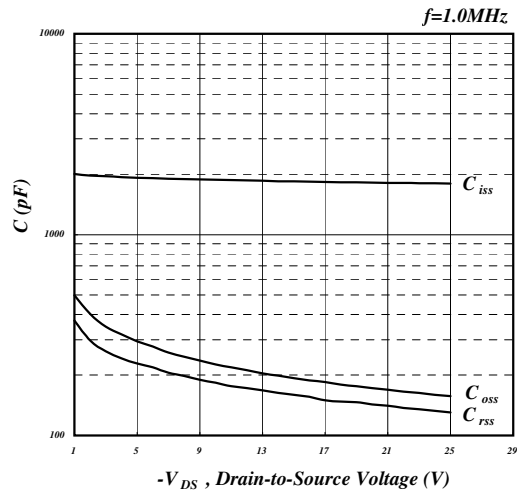


Fig 8. Typical Capacitance Characteristics

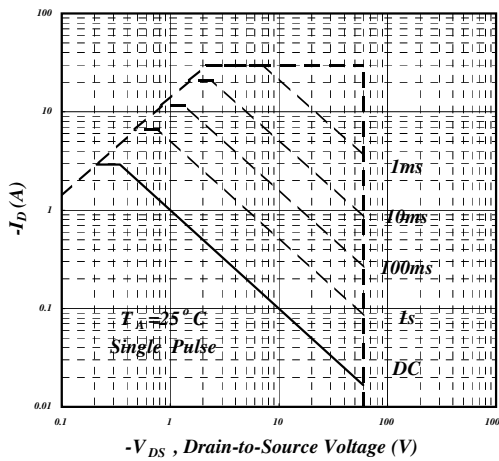


Fig 9. Maximum Safe Operating Area

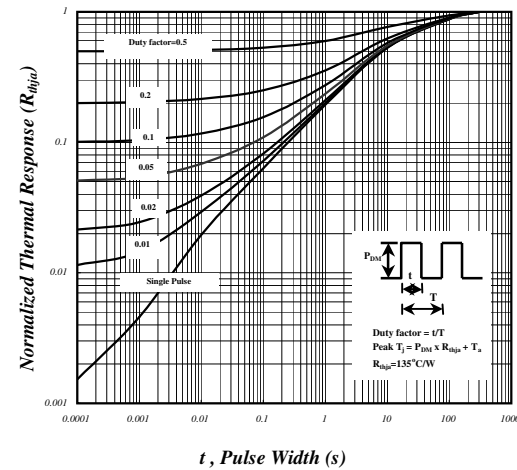


Fig 10. Effective Transient Thermal Impedance

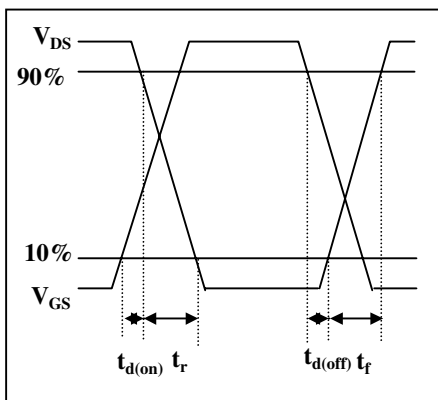


Fig 11. Switching Time Waveform

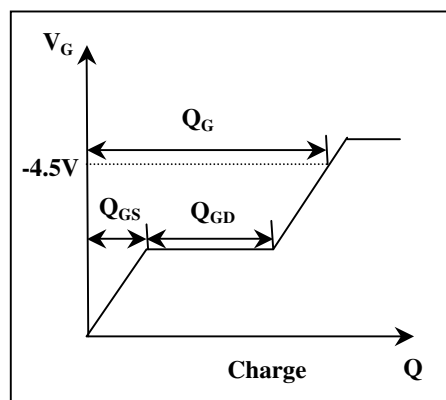
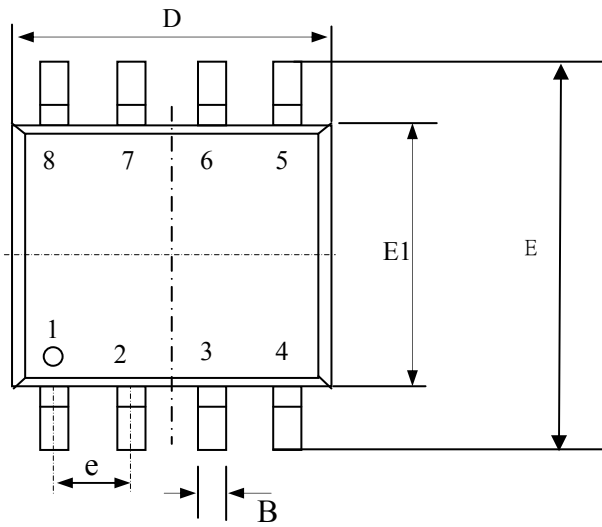


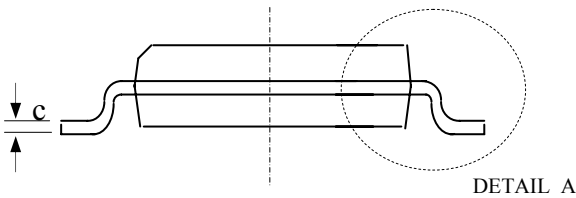
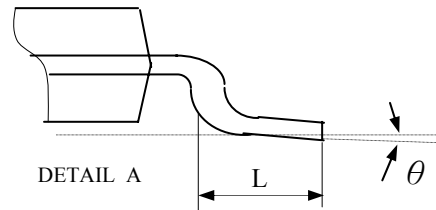
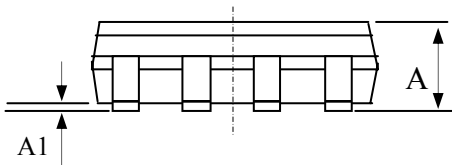
Fig 12. Gate Charge Waveform



Package Outline : SO-8

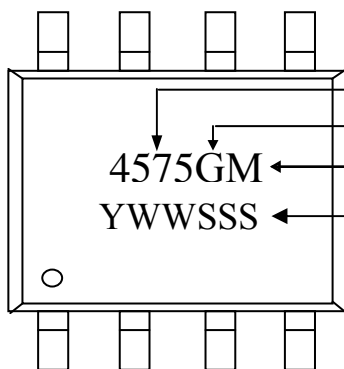


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
c	0.19	0.22	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.15	6.50
L	0.38	0.71	1.27
θ	0.00	4.00	8.00
e	1.27 TYP		



1. All Dimension Are In Millimeters.
2. Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : SO-8



Part Number

Package Code

Date Code (YWWSSS)

meet Rohs requirement
for low voltage MOSFET only

Y : Last Digit Of The Year

WW : Week

SSS : Sequence

If last "S" is numerical letter : Rohs product

If last "S" is English letter : HF & Rohs