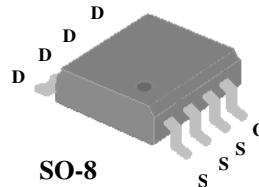




- ▼ Simple Drive Requirement
- ▼ Good Recovery Time
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

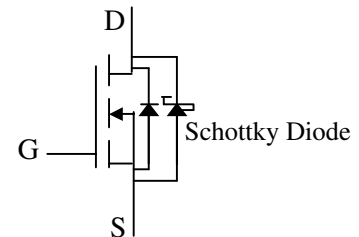


BV_{DSS}	30V
$R_{DS(ON)}$	9m Ω
I_D	13A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	13	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	10.6	A
I_{DM}	Pulsed Drain Current ¹	50	A
V_{KA}	Schottky Reverse Voltage	30	V
$I_F@T_A=25^\circ C$	Continous Forward Current	1	A
I_{FM}	Pulsed Diode Forward Current	25	A
$P_D@T_A=25^\circ C$	Max Power Dissipation (MOSFET)	2.5	W
	Max Power Dissipation (Schottky)	2.0	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³ (MOSFET)	50	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³ (Schottky)	60	$^\circ C/W$



AP4813GSM-HF

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =12A	-	-	9	mΩ
		V _{GS} =4.5V, I _D =8A	-	-	15	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =8A	-	20	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V	-	-	100	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =24V, V _{GS} =0V	-	-	1	mA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =8A	-	11.5	18	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	2.5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	7	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =15V	-	9	-	ns
t _r	Rise Time	I _D =1A	-	7	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	23	-	ns
t _f	Fall Time	R _D =15Ω	-	8	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	730	1170	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	205	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	150	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.5	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Diode+Schottky Forward On Voltage ²	I _S =1.0A, V _{GS} =0V	-	0.48	0.5	V
t _{rr}	Body Diode+Schottky Reverse Recovery Time	I _S =8A, V _{GS} =0V,	-	20	-	ns
Q _{rr}	Body Diode+Schottky Reverse Recovery Charge	di/dt=100A/μs	-	9	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10 sec.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

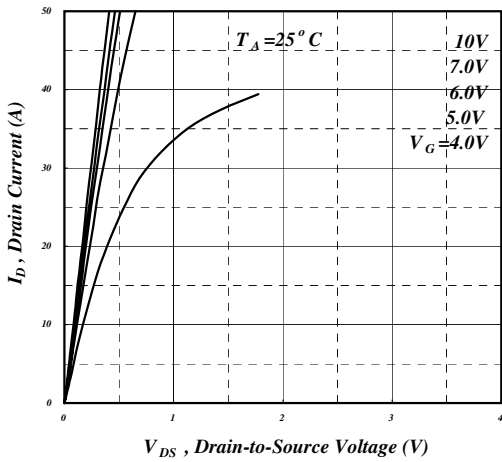


Fig 1. Typical Output Characteristics

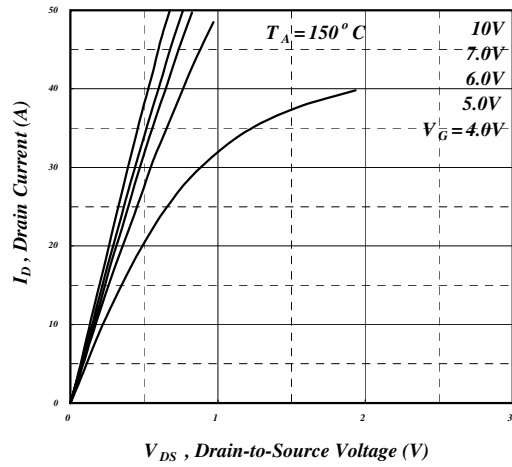


Fig 2. Typical Output Characteristics

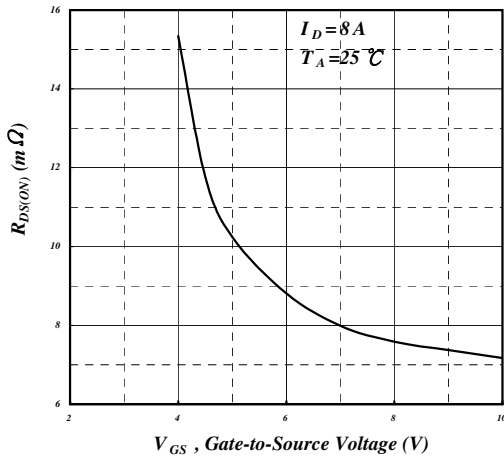


Fig 3. On-Resistance v.s. Gate Voltage

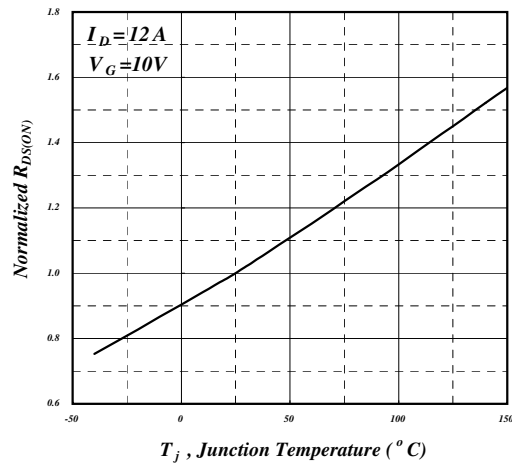


Fig 4. Normalized On-Resistance v.s. Junction Temperature

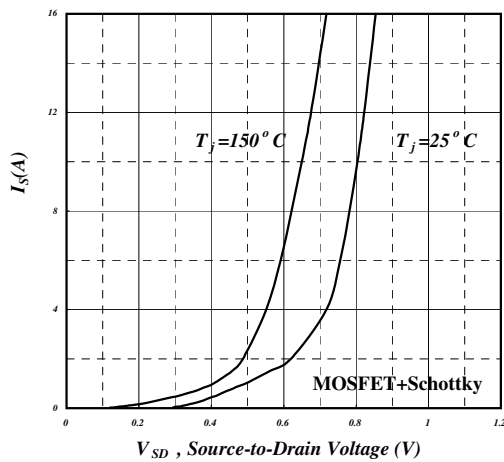


Fig 5. Forward Characteristic of Reverse Diode

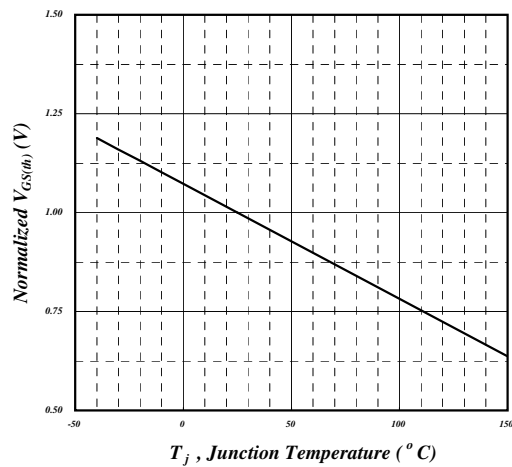


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

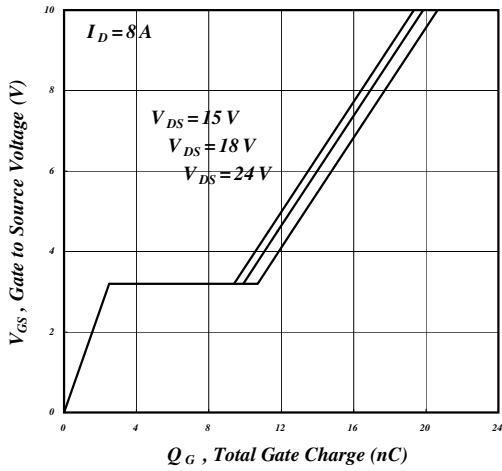


Fig 7. Gate Charge Characteristics

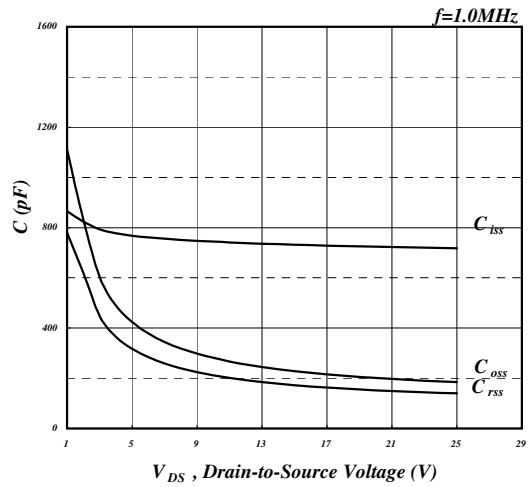


Fig 8. Typical Capacitance Characteristics

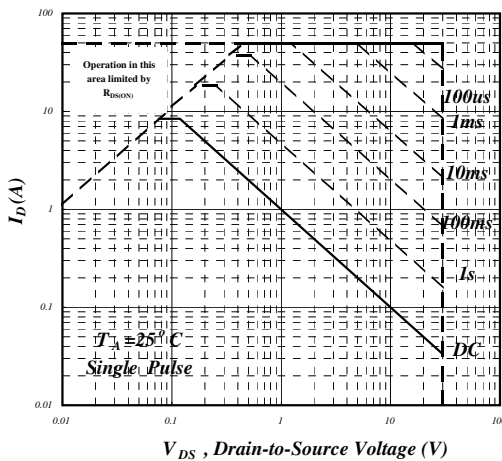


Fig 9. Maximum Safe Operating Area

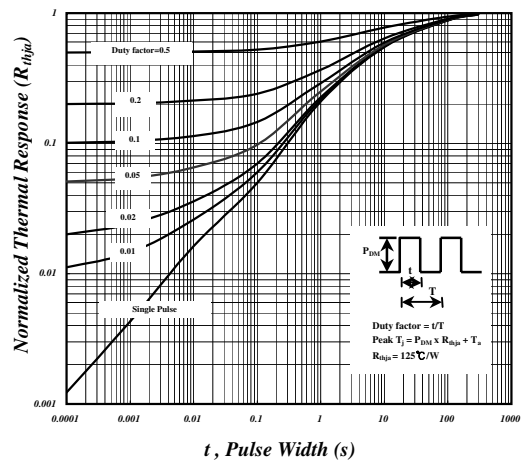


Fig 10. Effective Transient Thermal Impedance

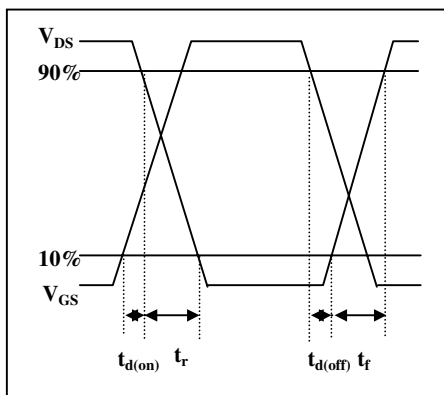


Fig 11. Switching Time Waveform

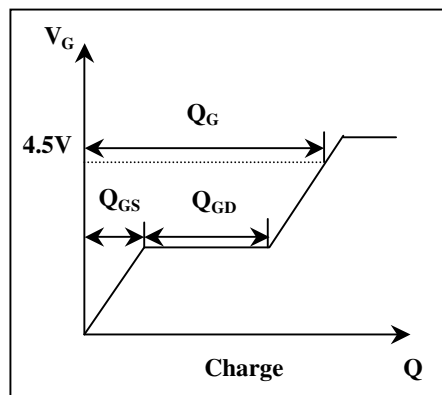


Fig 12. Gate Charge Waveform