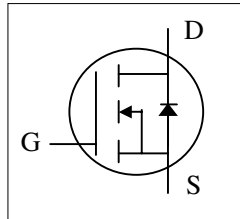




- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic

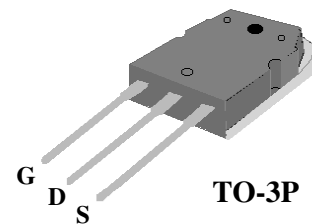


BV_{DSS}	75V
$R_{DS(ON)}$	11m Ω
I_D	90A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-3P package is widely preferred for commercial-industrial surface mount applications and suited for higher voltage applications such as SMPS.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^4$	90	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	70	A
I_{DM}	Pulsed Drain Current ¹	360	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	250	W
	Linear Derating Factor	2	W/ $^\circ\text{C}$
E_{AS}	Single Pulse Avalanche Energy ³	450	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	40	$^\circ\text{C}/\text{W}$



AP75N07GW

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	75	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.08	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =40A	-	-	11	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =40A	-	120	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =75V, V _{GS} =0V	-	-	10	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =60V, V _{GS} =0V	-	-	250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =40A	-	83	130	nC
Q _{gs}	Gate-Source Charge	V _{DS} =60V	-	10	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	51	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DD} =40V	-	15	-	ns
t _r	Rise Time	I _D =30A	-	73	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =10Ω, V _{GS} =10V	-	340	-	ns
t _f	Fall Time	R _D =1.33Ω	-	200	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	4270	6830	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	690	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	320	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.8	2.7	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =40A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time	I _S =40A, V _{GS} =0V	-	90	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	235	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , I_{AS}=30A.
- 4.Package limitation current is 90A .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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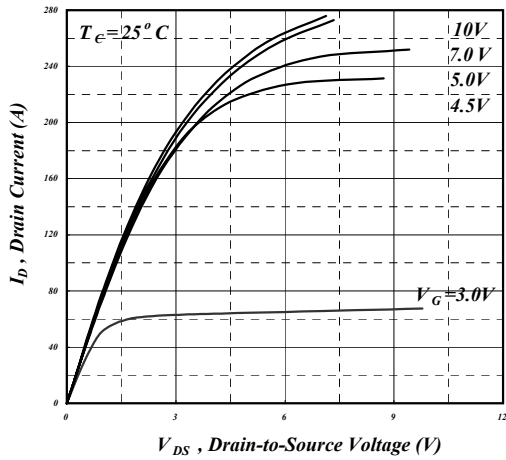


Fig 1. Typical Output Characteristics

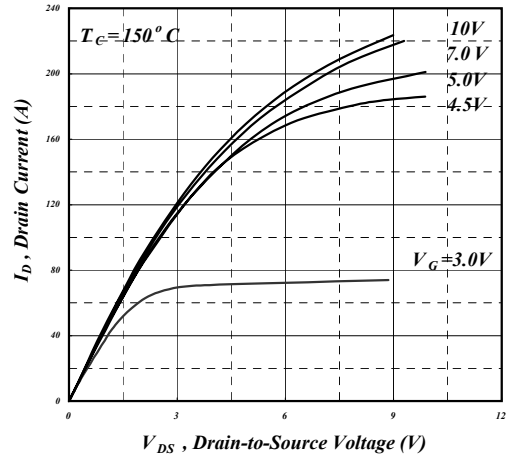


Fig 2. Typical Output Characteristics

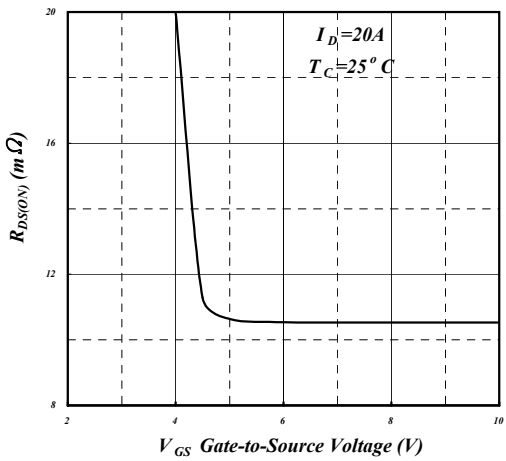


Fig 3. On-Resistance v.s. Gate Voltage

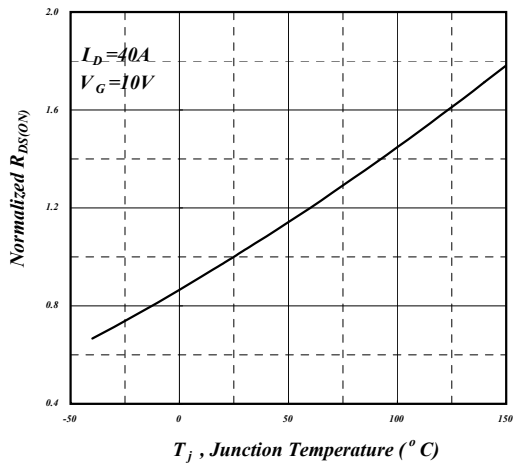


Fig 4. Normalized On-Resistance v.s. Junction Temperature

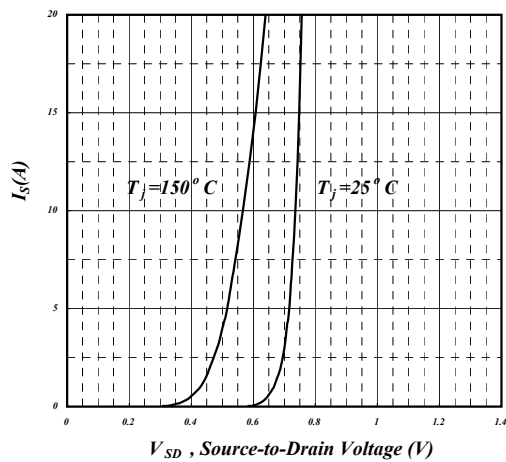


Fig 5. Forward Characteristic of Reverse Diode

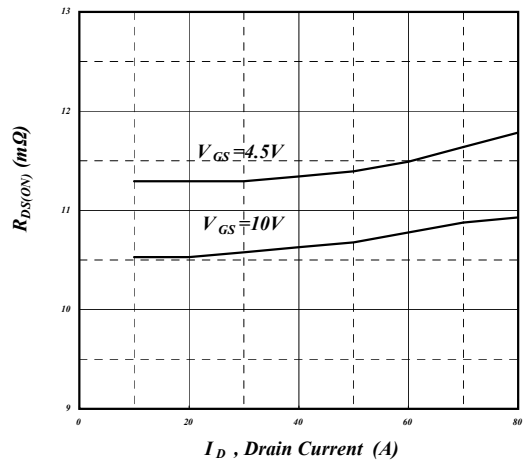


Fig 6. On-Resistance vs. Drain Current

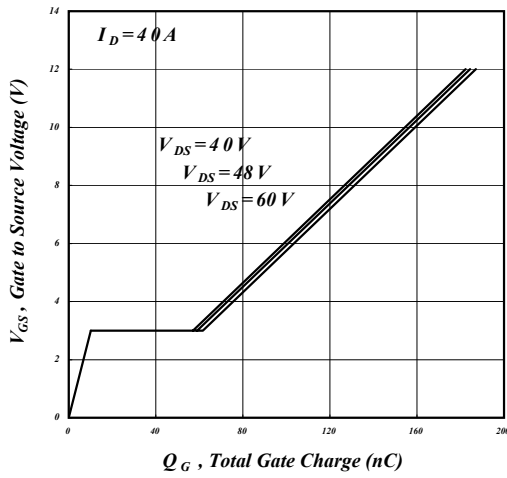


Fig 7. Gate Charge Characteristics

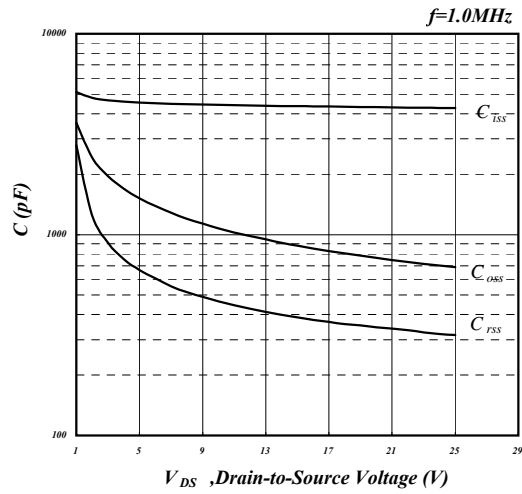


Fig 8. Typical Capacitance Characteristics

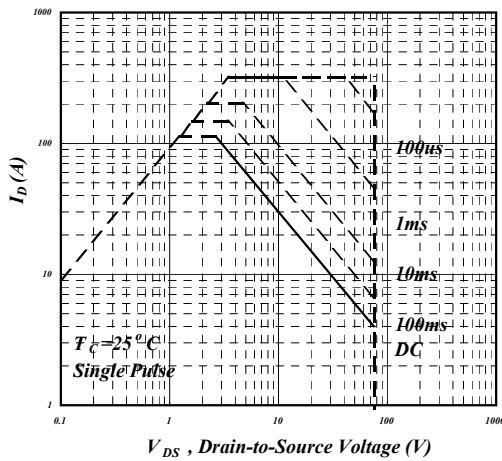


Fig 9. Maximum Safe Operating Area

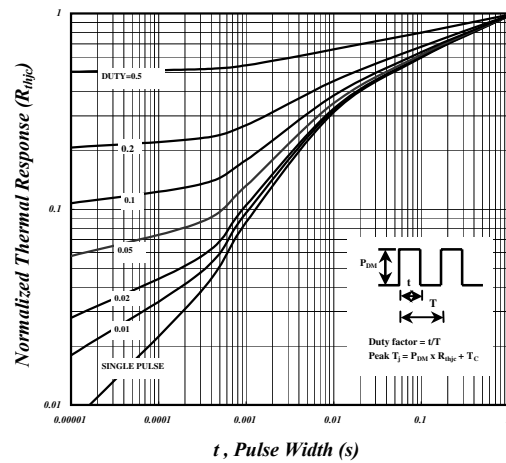


Fig 10. Effective Transient Thermal Impedance

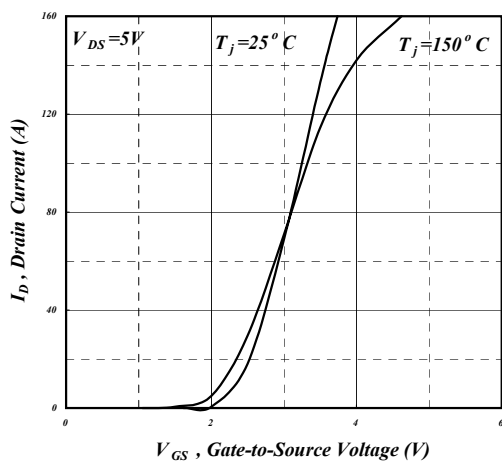


Fig 11. Transfer Characteristics

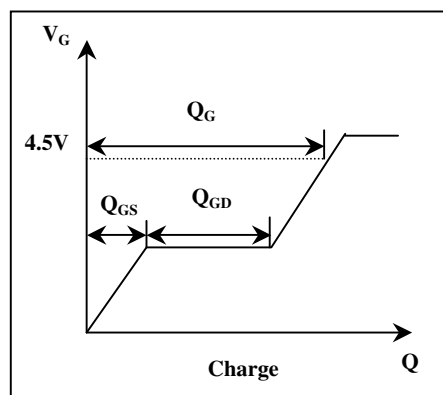


Fig 12. Gate Charge Waveform