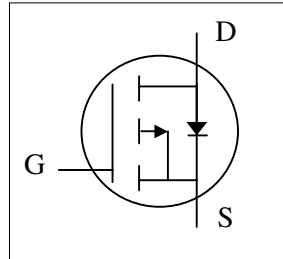




- ▼ Lower Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

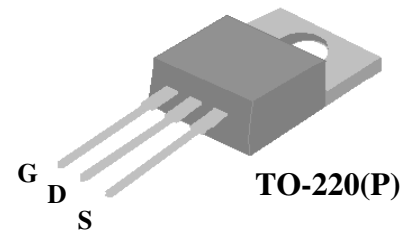


$BV_{DSS}$	-140V
$R_{DS(ON)}$	180m $\Omega$
$I_D$	-15A

### Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is widely preferred for commercial-industrial power through hole applications. The low thermal resistance and low package cost contribute to the world wide popular package.



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-140	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	-15	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V	-9.7	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	-60	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	89.2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.4	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ C/W$



# AP15P15GP-HF

## Electrical Characteristics@T<sub>j</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-140	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A	-	-	180	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-	-3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-12A	-	12	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-120V, V <sub>GS</sub> =0V	-	-	-25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =-12A	-	55	90	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-80V	-	8	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =-10V	-	16.5	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =-50V	-	11	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =-12A	-	26	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω	-	67	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =-10V	-	60	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	2850	4560	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =-25V	-	150	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	6.6	13	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =-12A, V <sub>GS</sub> =0V	-	-	-1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =-12A, V <sub>GS</sub> =0V,	-	75	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=-100A/μs	-	250	-	nC

### Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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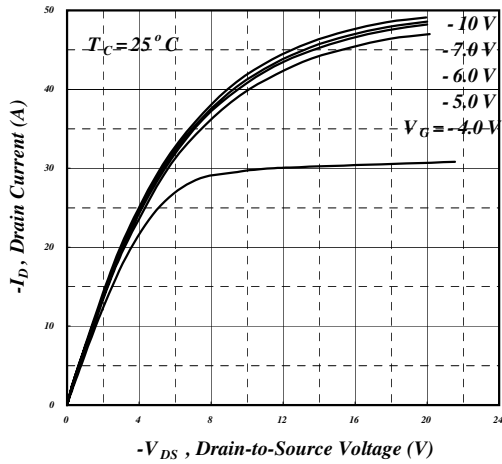


Fig 1. Typical Output Characteristics

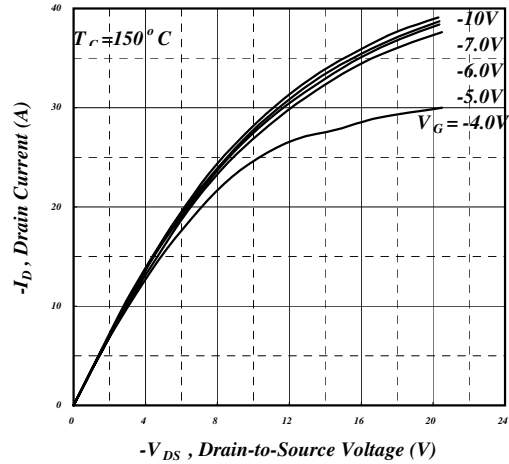


Fig 2. Typical Output Characteristics

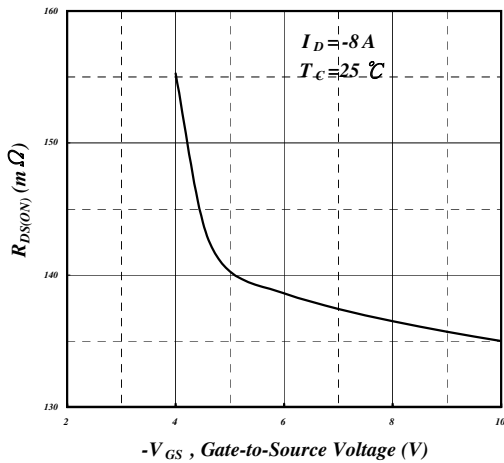


Fig 3. On-Resistance v.s. Gate Voltage

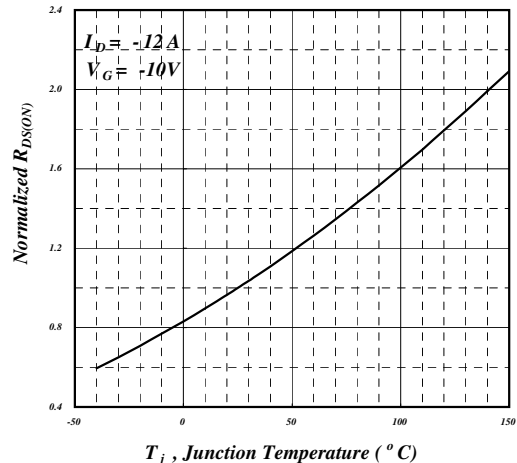


Fig 4. Normalized On-Resistance v.s. Junction Temperature

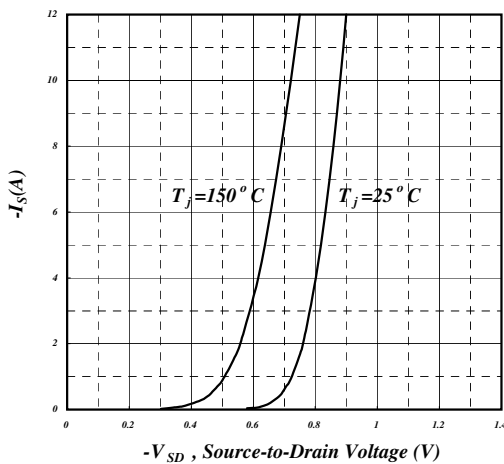


Fig 5. Forward Characteristic of Reverse Diode

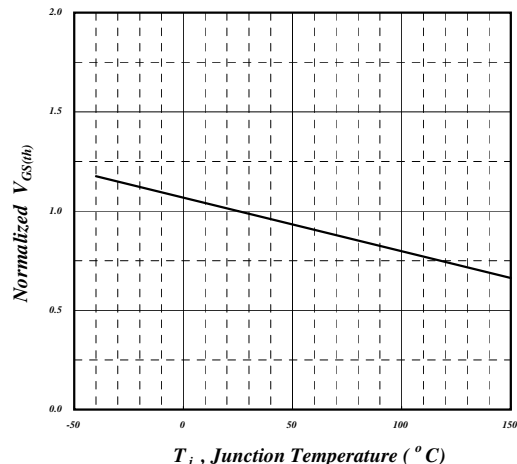


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

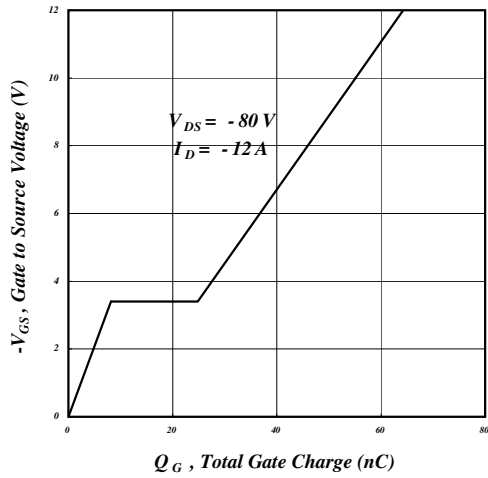


Fig 7. Gate Charge Characteristics

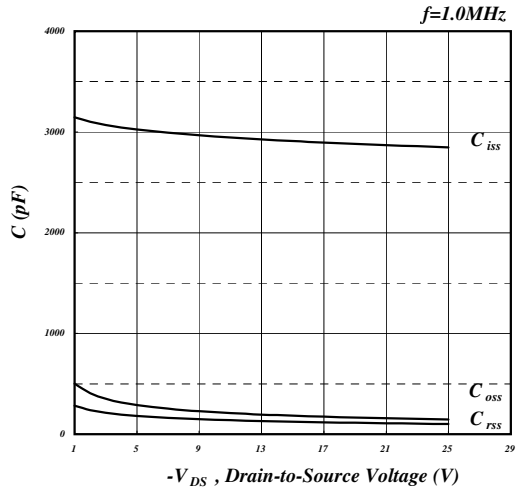


Fig 8. Typical Capacitance Characteristics

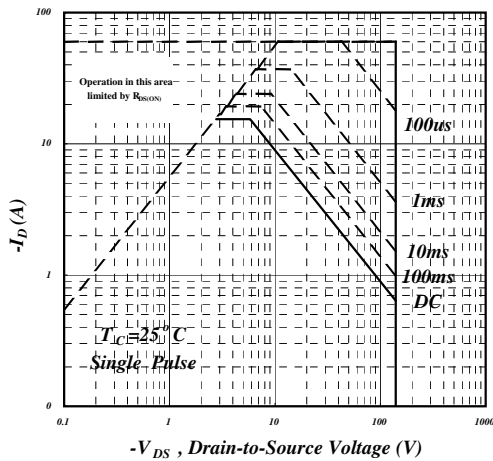


Fig 9. Maximum Safe Operating Area

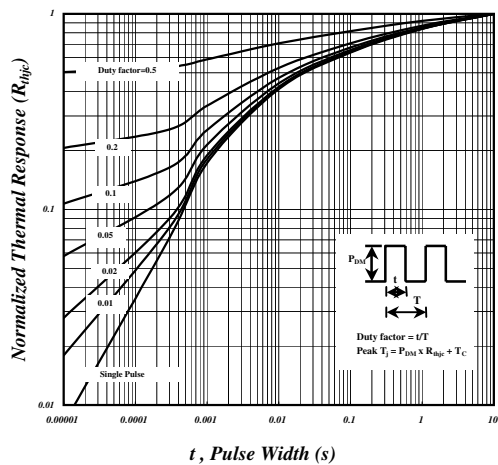


Fig 10. Effective Transient Thermal Impedance

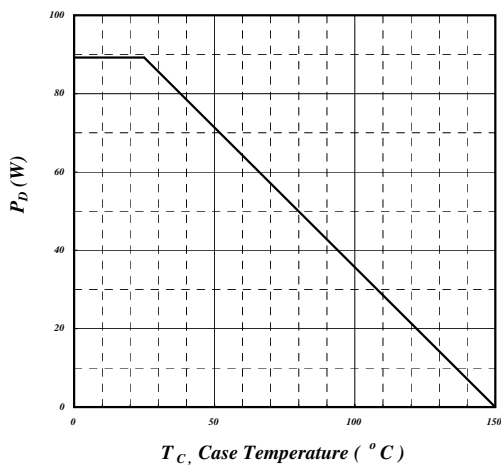


Fig 11. Typical Power Dissipation

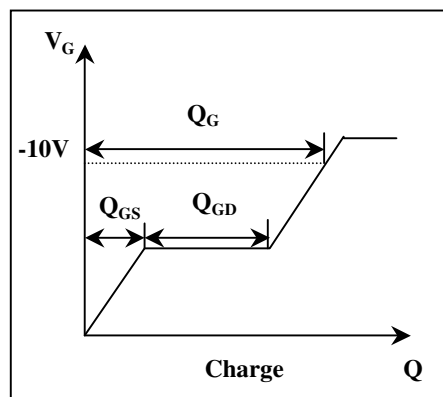


Fig 12. Gate Charge Waveform