



2.5A SINK/SOURCE BUS TERMINATION REGULATOR

FEATURES

- Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications
- Sink and Source up to 2.5Amp
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Built-in Soft-start Function
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in DFN 3x3-8L Packages
- V_{IN} and V_{CNTL} Under Voltage Protection
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATION

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

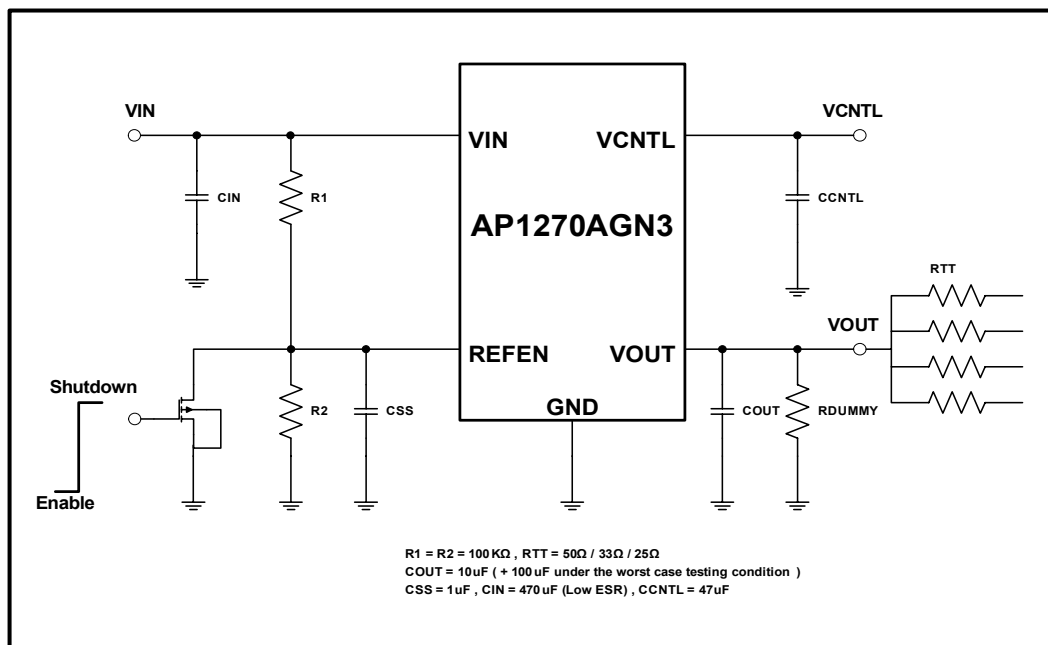
DESCRIPTION

The AP1270AGN3 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2.5A while regulating an output voltage to within 26mV. The output termination voltage can be tightly regulated to track $1/2V_{DDQ}$ by two external voltage divider resistors or the desired output voltage can be pro-programmed by externally forcing the REFEN pin voltage.

The AP1270AGN3 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection. Built-in softstart function avoids a misoperation by inrush current.

The AP1270AGN3 are available in the DFN 3x3-8L surface mount packages.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS^(Note1)

Input Voltage (V_{IN})	6V
CNTL Pin Voltage (V_{CNTL})	6V
Power Dissipation (P_D)	Internally Limited
Storage Temperature Range (T_{ST})	-65 to +150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Case (R_{thjc})	28°C/W

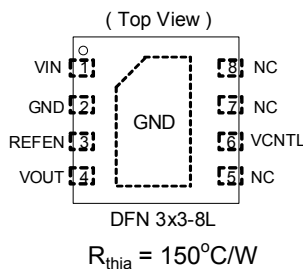
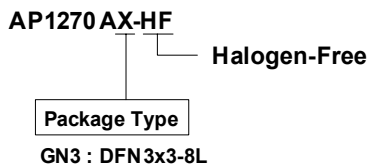
Note1 : Exceeding the absolute maximum rating may damage the device.

OPERATING RATING^(Note2)

Input Voltage (V_{IN})	2.5V to 1.2V \pm 3%
CNTL Pin Voltage (V_{CNTL})	5.5V or 3.3V \pm 5%
Junction Temperature Range (T_J)	-40 to +125°C
Ambient Temperature Range (T_A)	-40 to +85°C

Note2 : The device is not guaranteed to function outside its operating conditions.

ORDERING / PACKAGE INFORMATION



ELECTRICAL SPECIFICATIONS

($V_{IN}=1.8\text{V}$, $V_{CNTL}=3.3\text{V}$, $V_{REFEN}=0.9\text{V}$, $C_{OUT}=10\mu\text{F}$ (Ceramic), $T_A=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operation Current	I_{CNTL}	$I_{OUT} = 0\text{A}$	-	1	2.5	mA
Standby Current	I_{STBY}	$V_{REFEN} = 0\text{V}$ (Shutdown)	-	2	5	μA
VIN Shutdown Current	I_{VIN}	$V_{REFEN} = 0\text{V}$ (Shutdown)	-	-	5	μA
UVP Function						
VCNTL UVP Rising Threshold	V_{COP}	V_{CNTL} Rising	2.4	2.55	2.7	V
VCNTL UVP Hysteresis	V_{CHYS}		-	0.35	-	V
VIN UVP Rising Threshold	V_{IOP}	V_{IOP} Rising	0.8	0.95	1.1	V
VIN UVP Hysteresis	V_{IHYS}		-	0.15	-	V
Output (DDR / DDRII / DDRIII)						
Output Voltage	V_{OUT}	$V_{REF}=0.9\text{V}$	-	0.9	-	V
		$V_{REF}=0.75\text{V}$	-	0.75	-	
		$V_{REF}=0.675\text{V}$	-	0.675	-	
Output Offset Voltage ^(Note3)	ΔV_{OS}	$I_{OUT} = 10\text{mA}$	-13	-	13	mV
		$I_{OUT} = -10\text{mA}$	-13	-	13	
Load Regulation ^(Note4)	ΔV_{Load}	$I_{OUT}=10\text{mA} \sim 2.5\text{A}$	-13	-	13	mV
		$I_{OUT}=-10\text{mA} \sim -2.5\text{A}$	-13	-	13	



ELECTRICAL SPECIFICATIONS (Cont.)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Protection						
Current Limit	I_{LIM}	Sourcing Current ($V_{IN}=1.8V$, $T_J=25^{\circ}C$)	2.6	3.2	4	A
		Sinking Current ($V_{IN}=1.8V$, $T_J=25^{\circ}C$)	2.6	3.2	4	
		Sourcing Current ($V_{IN}=1.5V$, $T_J=25^{\circ}C$)	2.6	3	3.8	
		Sinking Current ($V_{IN}=1.5V$, $T_J=25^{\circ}C$)	2.6	3	3.8	
Thermal Shutdown Temperature	T_{SD}	$3.3V \leq V_{CNTL} \leq 5V$	-	150	-	$^{\circ}C$
Thermal Shutdown Hysteresis	ΔT_{SD}	$3.3V \leq V_{CNTL} \leq 5V$	-	20	-	
ENABLE and Soft-Start						
REFEN Threshold	V_{EN}		0.15	-	0.4	V
Soft-Start Interval	T_{SS}	$\Delta V_{OUT}=1V$	-	0.8	-	ms

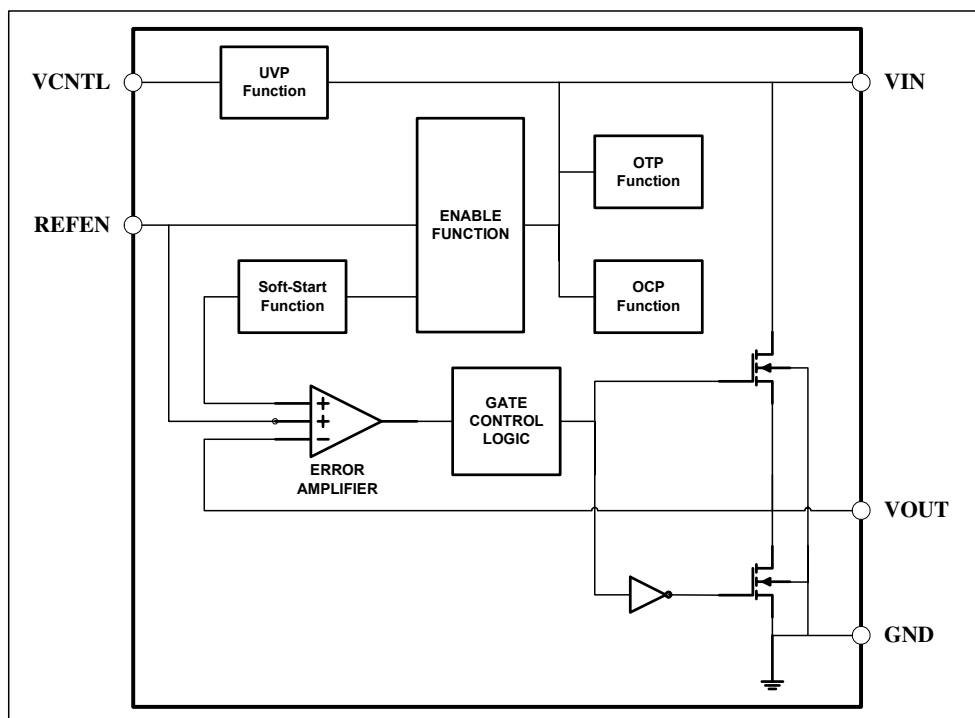
Note3. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN} .

Note4. Regulation is measured at constant junction temperature by using a 1ms(on) / 9ms(off) current pulse. Devices are tested for load regulation in the load range from 10mA to 2.5A peak for source and -10mA to -2.5A peak for sink capability.

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VIN	Power Input Voltage.
GND	Ground Pin
VOUT	Output Voltage
VCNTL	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable

BLOCK DIAGRAM





APPLICATION INFORMATION

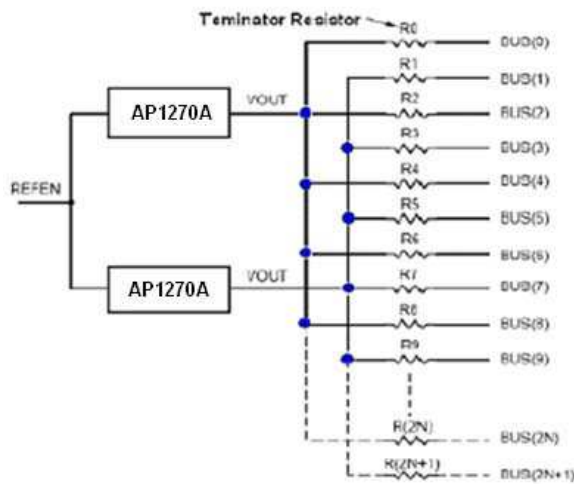
Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AP1270AGN3. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AP1270AGN3 and the preceding power converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.15V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Consideration

AP1270AGN3 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{th_{ja}}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the $R_{th_{ja}}$ is the junction to ambient thermal resistance. The junction to ambient thermal resistance ($R_{th_{ja}}$ is layout dependent) for DFN 3x3-8L is 150°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula:

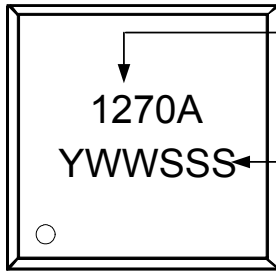
$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / 150^\circ\text{C/W} = 0.66\text{W}$$

The thermal resistance $R_{th_{ja}}$ of DFN 3x3-8L is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of DFN 3x3-8L package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow



MARKING INFORMATION

DFN 3x3-8L



Part Number

Date Code (YWWS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence