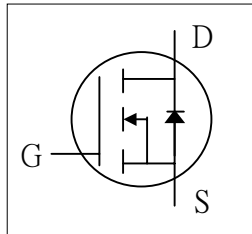




- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

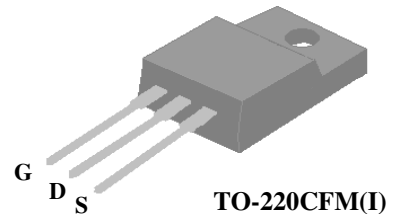


BV_{DSS}	700V
$R_{DS(ON)}$	0.85 Ω
I_D	8.3A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220CFM isolation package is widely preferred for all commercial-industrial through hole applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	700	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.3	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.2	A
I_{DM}	Pulsed Drain Current ¹	40	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	42	W
	Linear Derating Factor	0.34	W/ $^\circ C$
$P_D@T_A=25^\circ C$	Total Power Dissipation	1.92	W
E_{AS}	Single Pulse Avalanche Energy ²	32	mJ
I_{AR}	Avalanche Current	8	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ C/W$



Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	700	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.6	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ³	V _{GS} =10V, I _D =4A	-	-	0.85	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =50V, I _D =4.5A	-	4.5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =600V, V _{GS} =0V	-	-	10	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =480V, V _{GS} =0V	-	-	500	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ³	I _D =9A	-	44	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	11	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	12	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =300V	-	19	-	ns
t _r	Rise Time	I _D =9A	-	21	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =10Ω, V _{GS} =10V	-	56	-	ns
t _f	Fall Time	R _D =34Ω	-	24	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2660	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	170	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	10	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =1.5V	-	-	8.3	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	40	A
V _{SD}	Forward On Voltage ³	T _j =25°C , I _S =9A, V _{GS} =0V	-	-	1.5	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , I_{AS}=8A.
- 3.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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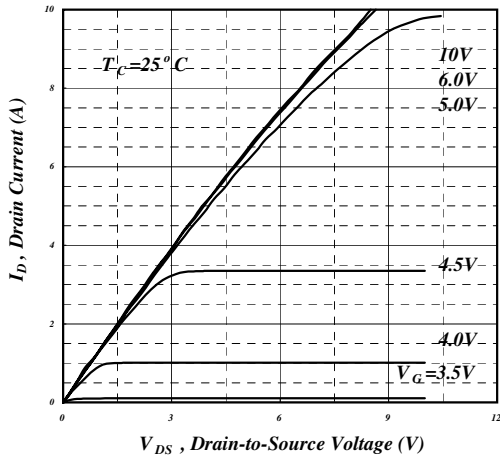


Fig 1. Typical Output Characteristics

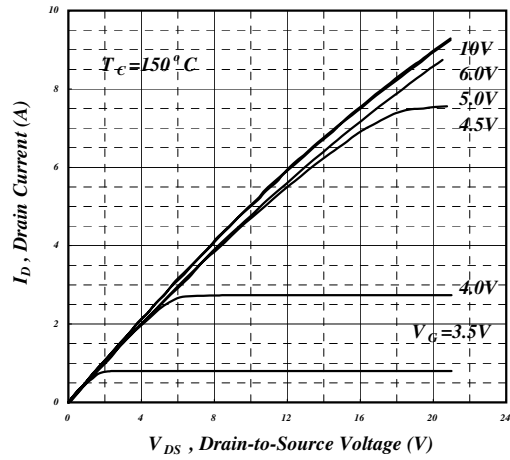


Fig 2. Typical Output Characteristics

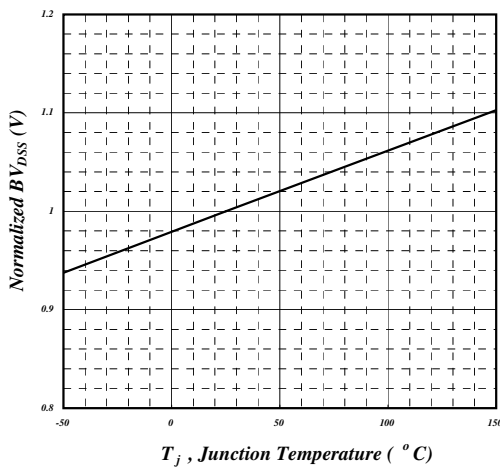


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

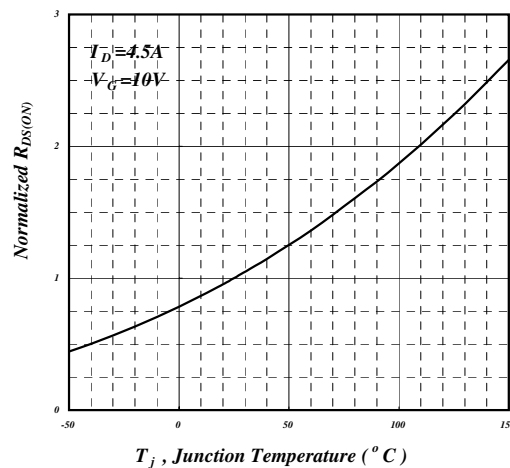


Fig 4. Normalized On-Resistance v.s. Junction Temperature

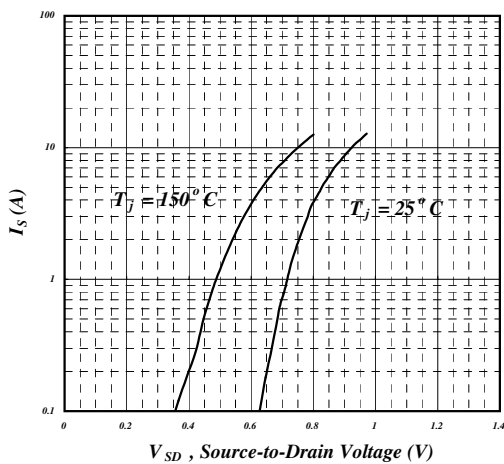


Fig 5. Forward Characteristic of Reverse Diode

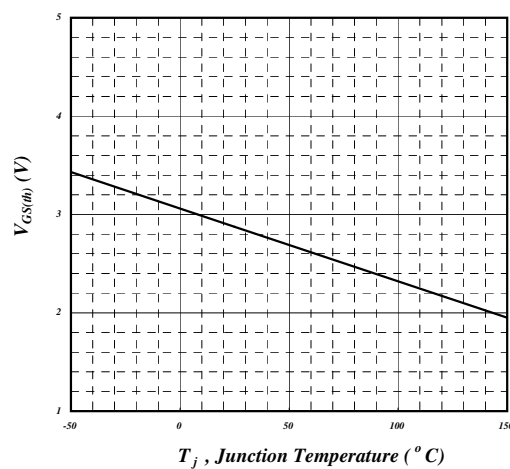


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

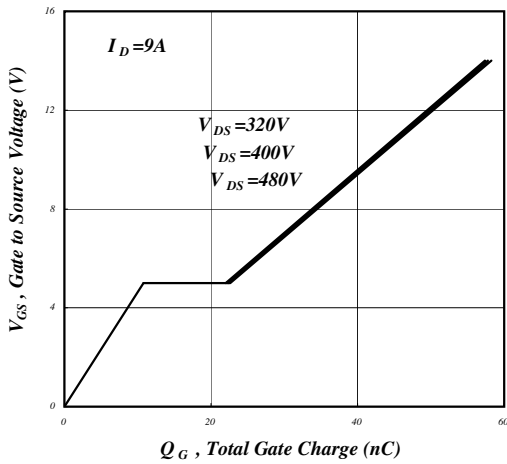


Fig 7. Gate Charge Characteristics

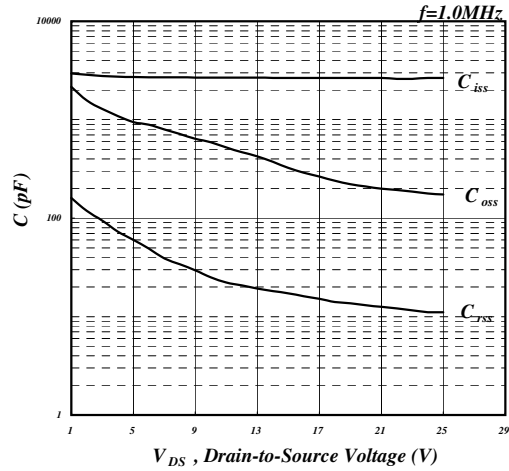


Fig 8. Typical Capacitance Characteristics

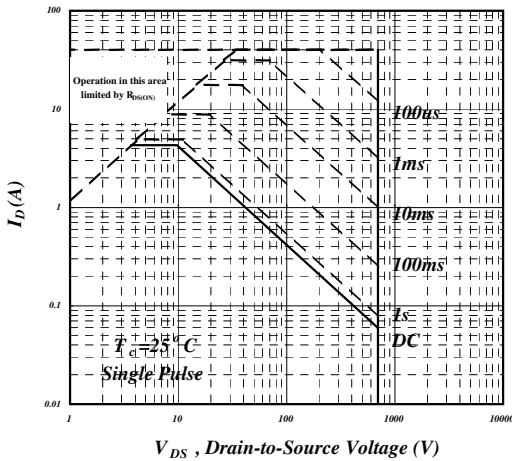


Fig 9. Maximum Safe Operating Area

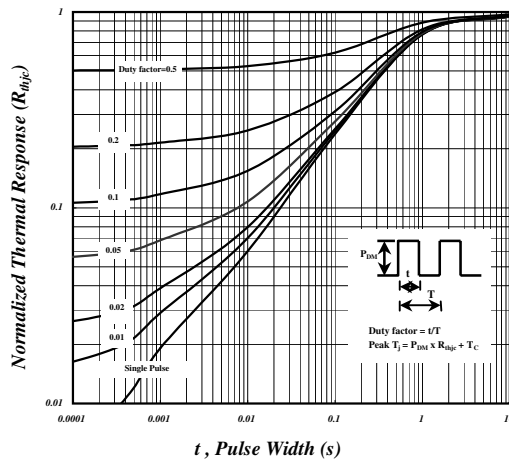


Fig 10. Effective Transient Thermal Impedance

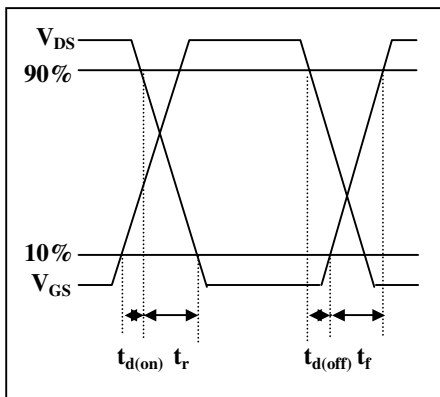


Fig 11. Switching Time Waveform

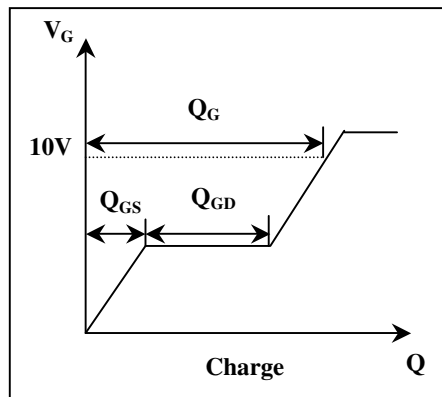


Fig 12. Gate Charge Waveform