Freescale Semiconductor
Advance Information

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MKW01Z128

Package Information

MKW01Z128

Highly-integrated, cost-effective single-package solution for sub-1 GHz applications

Ordering Information

Device	Device Marking	Package
MKW01Z128CHN	MKW01Z128CHN	LGA-60

1 Introduction

The MKW01Z device is highly-integrated, cost-effective, smart radio, sub-1 GHz wireless node solution composed of a transceiver supporting FSK, GFSK, MSK, or OOK modulations with a low-power ARM® Cortex M0+ CPU. The highly integrated RF transceiver operates over a wide frequency range including 315 MHz, 433 MHz, 470 MHz, 868 MHz, 915 MHz, 928 MHz, and 955 MHz in the license-free Industrial, Scientific and Medical (ISM) frequency bands. This configuration allows users to minimize the use of external components.

The MKW01Z128 is targeted for the following low-power wireless applications:

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

Freescale supplements the MKW01Z128 with tools and software that include hardware evaluation and

Contents

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development boards, software development IDE and applications, drivers, custom PHY usable with Freescale's IEEE 802.15.4 compatible MAC and SMAC.

2 Features

This section provides a simplified block diagram and highlights MKW01Z128 features.

2.1 Block Diagram

Figure 1 shows a simplified block diagram of the MKW01Z128.

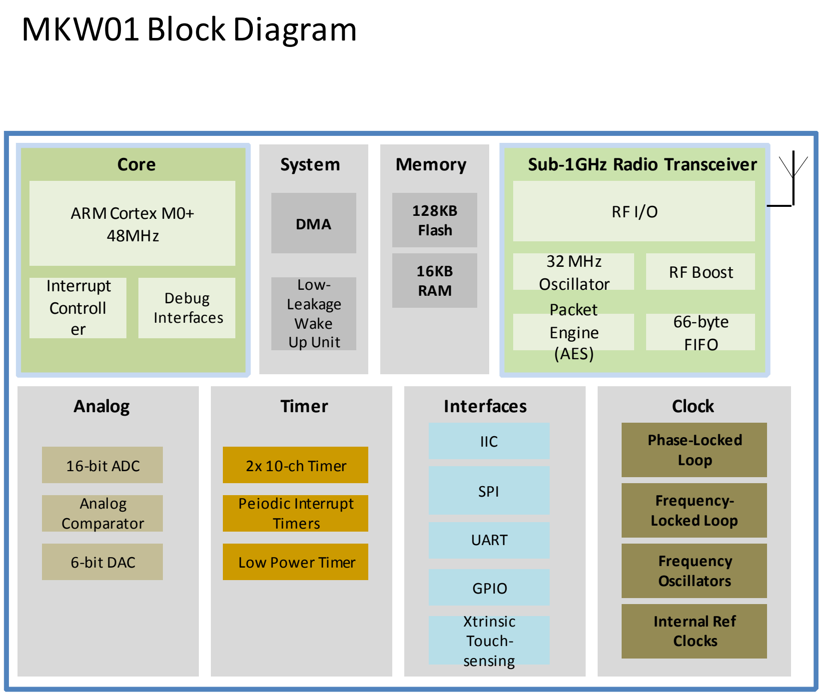


Figure 1. MKW01Z128 Simplified Block Diagram

2.2 Features Summary

- **RF Transceiver Features**
  - Operating Voltage from 1.8V to 3.6V.
  - Programmable bit rate up to 600kbps (FSK)
  - High Sensitivity: down to -120 dBm at 1.2 kbps
  - High Selectivity: 16-tap FIR Channel Filter
  - Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
  - Low current: Rx = 16mA, 100nA register retention

- Programmable Pout : -18 to +17 dBm in 1 dB steps
- Constant RF performance over voltage range of chip
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulations
- Built-in Bit Synchronizer performing Clock recovery
- Incoming Sync Word Recognition
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC, AES-128 encryption and 66-byte FIFO
- Built-in temperature sensor and Low battery indicator
- 32 MHz crystal oscillator clock source
- Dedicated I/O's for connection with an external 32 kHz crystal

- **MCU Features**

System**:**

- 48 MHz Max. Central Processor Unit (CPU) frequency
- 24 MHz Max. Bus frequency
- Vectored Interrupt Controller (NVIC) with 32 vectored interrupts with 4 programmable interrupt priority levels
- Wake-up Interrupt Controller (WIC)
- 4 channel Direct Memory Access (DMA)
- DMA request multiplex
- Non Maskable Interrupt (NMI)
- Software COP
- Low leakage Wake-up Unit (LLWU)
- Debug and Trace
  - 2-pin Serial Wire Debug (SWD)
  - Basic Branch Buffering (BBB)
- Boundary scan
- 80-bit wide ID number

Memory**:**

- 128 KB P-Flash with 64 byte flash cache
- 16 KB RAM
- Low Leakage Standby Memory:
  - 8KB in VLLS2 mode
  - 32 Register File Bytes in VLLS1 mode
  - Register File and PMC lose control and others in TBD in VLLS0
- 16-bit or 32-bit Cyclic Redundancy Check (CRC) with programmable generator polynominal

Clocks:

- External crystal oscillator or resonator:
  - 32 - 40 kHz low range, low power or full swing
  - 3 MHz - 32 MHz high range, low power or full swing
- DC - 48 MHz external square wave input clock
- Internal clock references:
  - 31.25 kHz to 39.063 kHz oscillator with +/- 2% max. deviation across temperature
  - 4 MHz oscillator with +/- 5% max. deviation across temperature
  - 1 kHz oscillator
- Phase Locked Loop (PLL) with up to 100 MHz VCO
- Frequency Locked Loop (FLL):
  - Range 1: 20 - 25 MHz
  - Range 2: 40 - 48 MHz

Analog:

- Power Management Controller (PMC) with low voltage warning (LVW) and detect with selectable trip points.
- 16-bit analog to digital converter
  - 16 single ended channels
  - 2 status, control and results registers
  - DMA support
- 1 High Speed Comparator (HSCMP) with internal 6-bit digital to analog converters (DAC)
- One 12-bit DAC with DMA support and 2 x 16 bit data buffer

Timers:

- 6 channel 16-bit flexible timer 0 (FTM0) / (LPTPM0) with basic TPM function and functional in STOP/VLPS modes
- 2 channel 16-bit FTM1 (LPTPM1) with basic TPM function and functional in STOP/VLPS modes.
- 2 channel 16-bit FTM2 (LPTPM2) with basic TPM function and functional in STOP/VLPS modes
- 2 channel 32-bit Programmable Input Timer (PIT)
- 24-bit counter System Tick Timer (SYSTIK)
- Independent Real Time Clock (SRTC) supporting an auxiliary supply, 32 kHz external oscillator and 32 Byte register file
- Low Power Timer (LPTMR) supporting 1 channel 16-bit pulse counter or periodic interrupt functional in all power modes except VLLS0.

Communication Interface:

- — Two Inter-Integrated Circuits (IIC's) with DMA support
- — One Universal Asynchronous Receiver / Transmitter 0 (UART0) / (LPSCIO) that supports standard features plus:
  - – Tx pin true open drain with enable / disable programmable
  - – x4, x8, x16 oversampling
  - – Functional in STOP / VLPS modes
  - – DMA support
  - – UART0 is clocked by the bus clock
- — UART1 (SCI) that supports standard features with DMA support
  - – UART1 is clocked by the core clock

Human Machine Interface (HMI)

- — General Purpose Input/Output (GPIO) supporting:
  - – 5 V Tolerant I/O
  - – Default to disabled (no leakage)
  - – 4 pins with 18 mA high current drive capability
  - – Hysteresis and configurable pull up device on all input pins
  - – Slew rate and drive strength fixed on all output pins
  - – Single cycle GPIO control via IOPORT
- — Touch Sensor Inputs (TSI)
  - – 16 - channel
  - – Selectable single channel wakeup source available in all modes
  - – DMA support
- — Pin Interrupt

Freescale will support the MKW01Z128 platform with:

- SMAC (Simple Media Access Controller) - This codebase provides simple communication and test apps based on drivers/PHY utilities available as source code. This environment is useful for hardware and RF debug, hardware standards certification, and developing proprietary applications.

The Freescale MKW01Z128 solutions are provided through a powerful software environment called the Freescale BeeKit Wireless Connectivity Toolkit. BeeKit is a comprehensive codebase of wireless networking libraries, application templates, and sample applications. The BeeKit Graphical User Interface (GUI), part of the BeeKit Wireless Connectivity Toolkit, allows users to create, modify, and update various wireless networking implementations.

3 Smart Radio Sub-1 GHz Wireless Node

The MKW01Z128 brings together a transceiver chip and an MCU chip on a single substrate to provide a small footprint, cost-effective sub-1 GHz wireless node. The transceiver is controlled by the MCU through a dedicated SPI interface. The SPI bus interface and some status signals are connected onboard the substrate to eliminate the need for external connections. The SPI supports bit order swapping providing hardware support for bit endianess reducing processing overhead.

3.1 RF Transceiver

The transceiver (see Figure 2) is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. Its advanced features set, including state of the art packet engine, greatly simplifies system design while the high level of integration reduces the external RF component bill of material (BOM) to a handful of passive de-coupling and matching components. It is intended for use as a high-performance, low-cost FSK, GFSK, MSK, GMSK, and OOK RF transceiver for robust, frequency agile, half-duplex bi-directional RF links.

The MKW01Z128 is intended for applications over a wide frequency range, including the 433 MHz, the 868 MHz European, and the 902-928 MHz North American ISM bands. Coupled with a link budget in excess of 135 dB, the transceiver advanced system features include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIO’s which greatly enhance system flexibility while at the same time significantly reducing MCU requirements. The transceiver complies with both ETSI and FCC regulatory requirements.

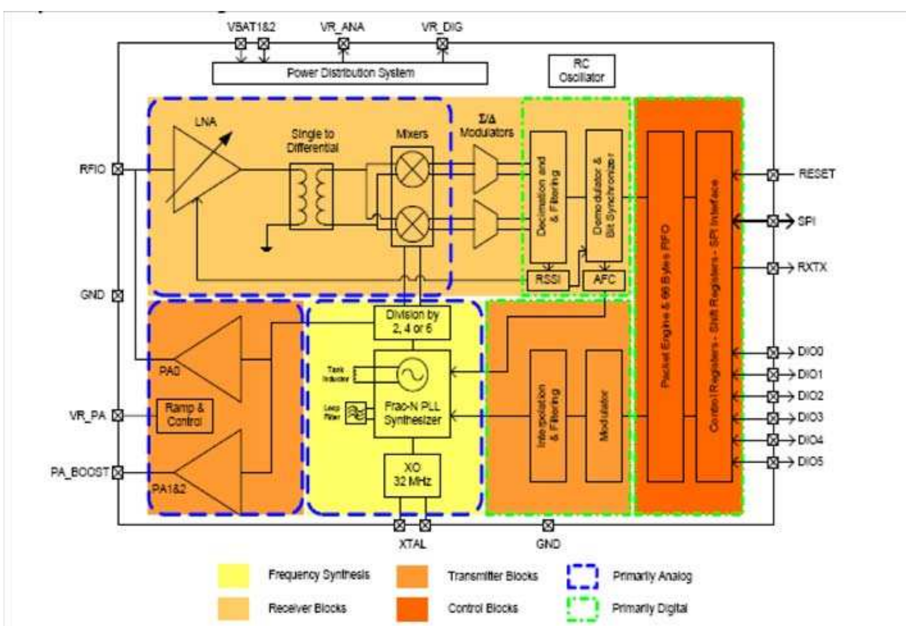


Figure 2. MKW01Z128 Transceiver Block Diagram

The major RF communication parameters of the MKW01Z128 transceiver are programmable and most can be dynamically set. This feature offers the unique advantage of programmable narrow-band and wide-band communication modes without the need to modify external components. The transceiver is also optimized for low power consumption while offering high RF output power and channelized operation.

3.2 ARM ® 32-bit Cortex M0+ CPU

The onboard MCU integrated circuit features an ARM ® Cortex M0+ CPU, up to 16 KB RAM, 128 KB Flash memory, and a rich set of peripherals (see Section 2.2, “Features Summary”). The RF transceiver is controlled through the MCU SPI port which is dedicated to the RF device interface. Two of the transceiver status IO lines are also directly connected to the MCU GPIO to monitor the transceiver operation. In addition, the transceiver reset and additional status can be connected to the MCU through external connections.

Operational modes of the MKW01Z128 are determined by the software running on the MCU. The MCU itself has a run mode as well as an array of low power modes that are coordinated by the PMC. The MCU in turn set the operational modes of the transceiver which include sleep, standby, and radio operational modes.

Two common application scenarios are:

- Low power, battery-operated standalone wireless node - a common example of this configuration would be a remote sensor monitor. The wireless node programmed for standalone operation, typically has a low active-mode duty cycle, and is designed for long battery life, i.e., lowest power.
- Communication channel to a higher level controller - in this example, the wireless node implements the lower levels of a communications stack and is subordinate to the primary controller. Typically the MKW01Z128 is connected to the controller through a command channel implemented via a UART/SCI port or other serial communication port.

3.3 System Clock Configuration

The MKW01Z128 device allows for various system clock configurations:

- Pins 46 & 47 are provided to input a 32 MHz crystal for the transceiver reference clock source (required) as shown in Figure 3.
- The transceiver can be programmed to provide a programmable frequency clock output (ClkOut Pin #54) that can be used as an external source to the CPU (see Figure 3 and Figure 4). As a result, a single crystal system clock solution is possible where the transceiver reference clock source can be divided by 2, 4, 8, 16 and 32.
- The MCU provides a trimmable internal reference clock and also supports an external clock source. An optional onboard frequency locked loop (FLL) can be used with either clock source to support a CPU clock as high as 48 MHz at 3.6 V.
- Pins 16 and 15 are available to provide an external 32.768kHz external clock source for the radio.

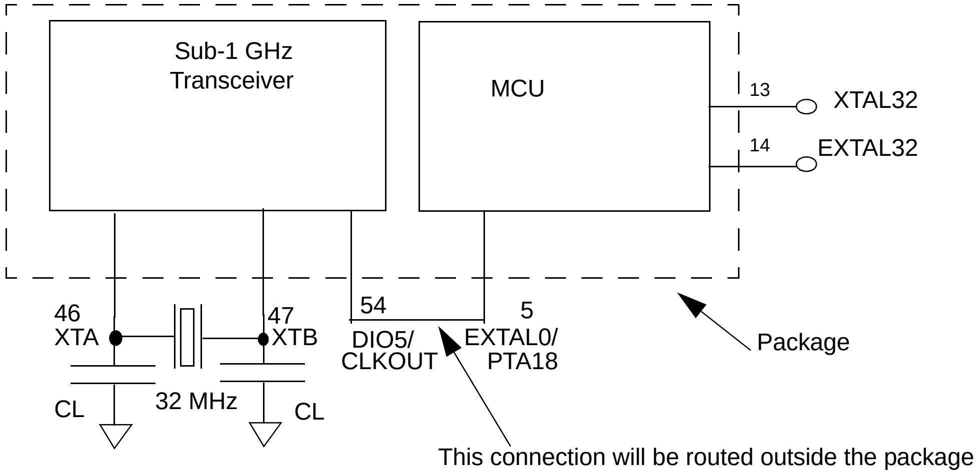


Figure 3. MKW01Z128 Single Crystal System Clock Connection

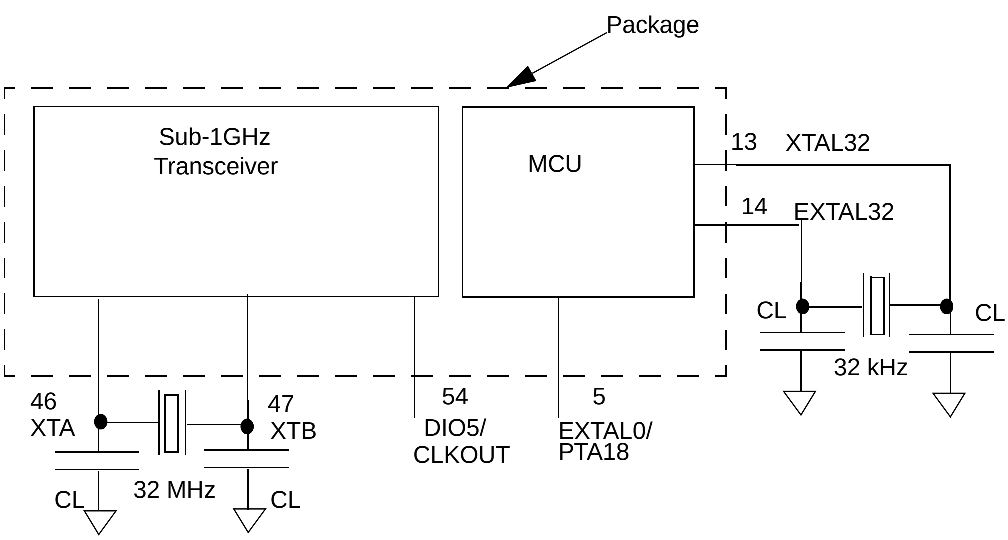


Figure 4. MKW01Z128 Two Crystal System Clock Connection

4 MKW01Z128 Pin Assignments and Connections

Figure 5 shows the MKW01Z128 pinout.

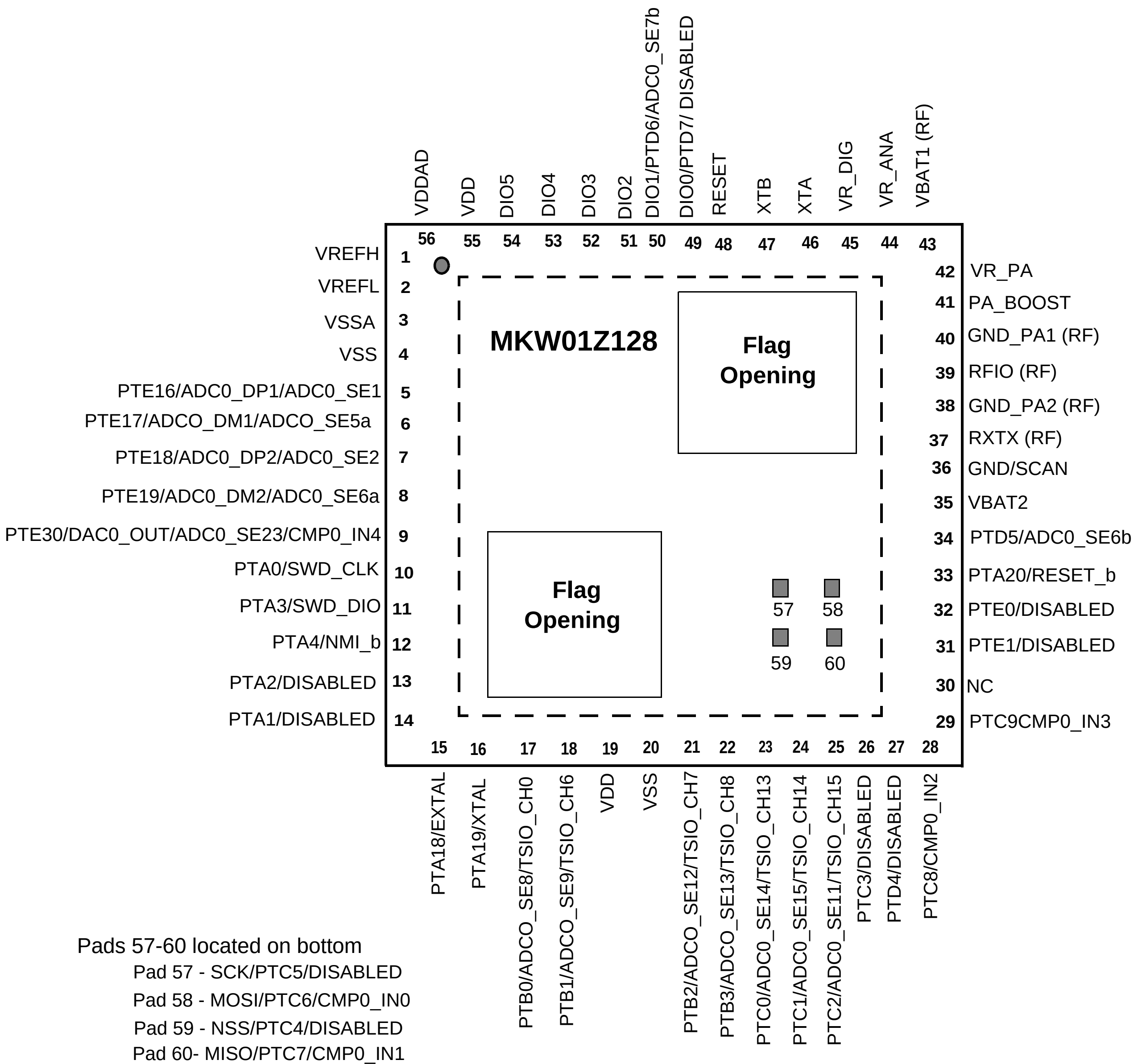


Figure 5. MKW01Z128 Pinout (Top View)

4.1 Pin Definitions

Table 1 details the MKW01Z128 pinout and functionality.

Table 1. Pin Function Description[1]

Pin #	Pin Name[1]	Type	Description	Functionality
1	VREFH	Input	MCU high reference voltage for ADC	
2	VREFL	Input	MCU low reference voltage for ADC	
3	VSSA	Power Input	MCU ADC Ground	Connect to ground
4	VSS	Power Input	MCU Ground	Connect to ground
5	PTE16/ADC0_DP1/ADCO_SE1/SPI0_PCS0/ FTM_CLKIN0	Digital Input / Output	MCU Port E Bit 16 / ADC0 Single Ended analog channel input DP1/ ADC0 Single Ended analog channel input SE1 / SPI module 0 PCS0 / Flex Timer module Clock In 0	
6	PTE17/ADC0_DM1/ADCO_SE5a/SPI0_SCK/ FTM_CLKIN1/LPTMR0_ALT3	Digital Input / Output	MCU Port E Bit 17 / ADC0 Single Ended analog channel input DM1/ ADC0 Single Ended analog channel input 5a / SPI module 0 SCK / Flex Timer module Clock In 1 / Low Power Timer Module 0 ALT3	
7	PTE18/ADC0_DP2/ADC0_SE2/SPI0_MOSI/IIC0_SDA/SPI0_MISO	Digital Input / Output	MCU Port E Bit 18 / ADC0 Single Ended analog channel input DP2/ ADC0 Single Ended analog channel input 2 / SPI module 0 MOSI / IIC0 Bus Data / SPI module 0 MISO	
8	PTE19/ADC0_DM2/ ADC0_SE6a/SPI0_MISO /IIC0_SCL/ SPI0_MOSI	Digital Input / Output	MCU Port E Bit 19 / ADC0 Single Ended analog channel input DM2/ ADC0 Single Ended analog channel input 6a / SPI module 0 MISO / IIC0 Bus Clock / SPI module 0 MOSI	
9	PTE30/DAC0_OUT/ ADCO_SE23/ CMP0_IN4/FMT0_CH3/FTM_CLKIN1	Digit-l Input / Output	MCU Port E Bit 30 / DAC0 Output/ ADC0 Single Ended analog channel input 23 / Comparator 0 Analog Voltage Input 4/ Flex Timer module 0 Channel 3 / Flex Timer module Clock In 1	
10	PTA0/SWD_CLK/TSIO_CH1/ FMT0_CH5	Digital Input / Output	MCU Port A Bit 0 / Serial Wire Data Clock / Touch Screen Interface Channel 1/Flex Timer module 0 Channel 5	
11	PTA3/SWD_DIO/TSIO_CH4/ IIC1_SCL/FMT0_CH0	Digital Input / Output	MCU Port A Bit 3 / Serial Wire Data DIO / Touch Screen Interface Channel 4 / IIC1 Bus Clock /Flex Timer module 0 Channel 0	

Pin #	Pin Name[1]	Type	Description	Functionality
12	PTA4/NMI_b/TSIO_CH5/ IIC1_SDA/FMT0_CH1	Digital Input / Output	MCU Port A Bit 4/ / Non Maskable Interrupt_ b/Touch Screen Interface Channel 5 /IIC1 Bus Data/Flex Timer module 0 Channel 1	
13	PTA2//DISABLED/TSIO_CH3/ UARTO_TX/FTM2_CH1	Digital Input / Output	MCU Port A Bit 2/Touch Screen Interface Channel 3/UART module 0 Transmit/Flex Timer module 2 Channel 1	
14	PTA1//DISABLED/TSIO_CH2/ UARTO_RX/FTM2_CH0	Digital Input / Output	MCU Port A Bit 1/Touch Screen Interface Channel 2/UART module 0 Receive/Flex Timer module Channel 0	
15	PTA18/EXTAL/UART1_RX/ FTM_CLKIN0	Digital Input / Output	MCU Port A Bit 18 / EXTAL/ UART module 1 Receive / Flex Timer module Clock In 0	
16	PTA19/XTAL/UART1_TX/FTM _CLKIN1/LPTMR0_ALT1	Digital Input / Output	MCU Port A Bit 19 / XTAL/ UART module 1 Transmit/ Flex Timer module Clock In 1 /Low Power Timer module 0 ALT1	
17	PTB0/ADC0_SE8/TSIO_CH0/ LLWU_P5/IIC0_SCL/ FMT1_CH0	Digital Input / Output	MCU Port B Bit 0 / ADC0 Single Ended analog channel input SE8 / Touch Screen Interface Channel 0/ Low Leakage Wake Up Port 5 / IIC0 Bus Clock / Flex Timer module 1 Channel 0	
18	PTB1/ADCO_SE9/TSIO_CH6 /LLWU_P5/IIC0_SDA/ FMT1_CH1	Digital Input / Output	MCU Port B Bit 1 / ADC0 Single Ended analog channel input SE9/ IIC0 Bus Data/Flex Timer module 1 Channel 1	
19	VDD	Power Input	MCU VDD supply input	Connect to system VDD supply
20	VSS	Power Input	MCU Ground	Connect to ground
21	PTB2/ADC0_SE12/TSIO_CH 7/LLWU_P5/IIC0_SCL/ FMT2_CH0	Digital Input/Output	MCU Port B Bit 2 / ADC0 Single Ended analog channel input SE12 / Touch Screen Interface Channel 7/ Low Leakage Wake Up Port 5 / IIC0 Bus Clock / Flex Timer module 2 Channel 0	
22	PTB3/ADC0_SE13/TSIO_CH 8/LLWU_P5/IIC0_SDA/ FMT2_CH1	Digital Input/Output	MCU Port B Bit 3 / ADC0 Single Ended analog channel input SE13 / Touch Screen Interface Channel 8 /Low Leakage Wake Up Port 5/ IIC0 Bus Data / Flex Timer module 2 Channel 1	
23	PTC0/ADC0_SE14/ TSIO_CH13/EXTRG_IN/ CMP0_OUT	Digital Input / Output	MCU Port C Bit 0 / ADC0 Single Ended analog channel input SE14/ Touch Screen Interface Channel 13/ ExternalTrigger Input/Comparator 0 Analog Voltage Output	

1.

Pin #	Pin Name[1]	Type	Description	Functionality
24	PTC1/ADC0_SE15/TSIO_CH 14/LLWU_P6/RTC_CLKIN/ IIC1_SCL/FMT0_CH0	Digital Input Output / Analog Input	MCU Port C Bit 1 /ADC0 Single Ended analog channel input SE15/ Touch Screen Interface Channel 14/ Low Leakage Wake Up Port 6 / Real Time Counter Clock Input/ IC1 Bus Clock/ Flex Timer module 0 Channel 0	
25	PTC2/ADC0_SE11/TSIO_CH 15/LLWU_P6/RTC_CLKIN/ IIC1_SDA/FMT0_CH1	Digital Input / Output / Analog Input	MCU Port C Bit 2 / ADC0 Single Ended analog channel input SE11/ / Touch Screen Interface Channel 15 / Low Leakage Wake Up Port 6/ Real Time Counter Clock Input/ IIC1 Bus Data / Flex Timer module 0 Channel 1	
26	PTC3/DISABLED/LLWU_P7/ UART1_RX/FMT0_CH2 /CLKOUTa	Digital Input / Output	MCU Port C Bit 3 / Low Leakage Wake Up Port 7 / UART module 1 Receive / Flex Timer module 0 Channel 2/ Clock OutA	
27	PTD4/DISABLED/LLWU_P14/ SPI1_PCS0/FMT0_CH4	Digital Input / Output	MCU Port D Bit 4 / Low Leak Wake Up Port 14/ SPI module 1 PCS0 / Flex Timer module 0 Channel 4	
28	PTC8/CMP0_IN2/IIC0_SCL /FTM0_CH4	Digital Input / Output / Analog Input	MCU Port C Bit 8 / Comparator 0 Analog Voltage Input 2 / IIC1 Bus Clock / Flex Timer module 0 Channel 4	
29	PTC9/CMP0_IN3/IIC0_SDA /FTM0_CH5	Digital Input / Output / Analog Input	MCU Port C Bit 9 / Comparator 0 Analog Voltage Input 3 / IIC0 Bus Data / Flex Timer module 0 Channel 5.	
30	NC		No Connect	
31	PTE1/DISABLED/SPI1_MOSI /UART1_RX/SPI1_MISO/ IIC1_SCL	Digital Input/Output	MCU Port E Bit 1/ SPI module 1 MOSI/UART module 1 Receive/SPI module 1 MISO/ IIC1 Bus Clock	
32	PTE0/DISABLED/UART1_TX/ RTC_CLKOUT/CMP0OUT/ IIC1_SDA	Digital Input/Output	MCU Port E Bit 0 / UART module 1 Transmit/Real Time Counter Clock Output/Comparator 0 Analog voltage Output/IIC1 Bus Data	
33	PTA20/RESETB	Digital Input/Output	MCU Port a Bit 20/MCU $\overline{\text{RESET}}$	
34	PTD5/ADC0_SE6b/ SPI1_SCK/ FTM0_CH5	Digital Input/Output	MCU Port D Bit 5 / ADC0 single ended analog channel input 6b / SPI module 1 SCK / Flex Timer module 0 Channel 5	
35	VBAT2	Power Input	Transceiver VDD	Connect to system VDD supply
36	GND/SCAN	Power Input	Transceiver Ground	Connect to ground
37	RXTX (RF)	Digital Output	Transceiver Rx / Tx RF Switch Control Output; high when in TX	
38	GND_PA2 (RF)	Power Input	Transceiver RF Ground	Connect to ground
39	RFIO (RF)	RF Input / Output	Transceiver RF Input / Output	

Pin #	Pin Name[1]	Type	Description	Functionality
40	GND_PA1 (RF)	Power Input	Transceiver RF Ground	Connect to ground
41	PA_BOOST	RF Output	Transceiver Optional High-Power PA Output	
42	VR_PA	Power Output	Transceiver regulated output voltage for VR_PA use.	De-coupling cap suggested.
43	VBAT1 (RF)	Power Input	Transceiver VDD for RF circuitry	Connect to system VDD supply
44	VR_ANA	Power Output	Transceiver regulated output voltage for analog circuitry.	Decouple to ground with 100 nF capacitor
45	VR_DIG	Power Output	Transceiver regulated output voltage for digital circuitry.	Decouple to ground with 100 nF capacitor
46	XTA	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
47	XTB	Xtal Osc	Transceiver crystal reference oscillator	Connect to 32 MHz crystal and load capacitor
48	RESET	Digital Input	Transceiver hardware reset input	Typically driven from MCU GPIO
49	DIO0 / PTD7/ DISABLED/SPI1_MISO / UART0_TX/SPI1_MOSI	Digital Input/Output	Transceiver GPIO Bit 0 / MCU Port D Bit 7 / SPI module 1 MISO/ UART module 0 Transmit/SPI module 1 MOSI	MCU IO and Transceiver IO connected onboard
50	DIO1/PTD6/ADC0_SE7b/ LLWU_P15/SPI1_MOSI/ UART0_RX/SPI1_MISO	Digital Input/Output	Transceiver GPIO Bit 1 / MCU Port D Bit 6 / ADC0 single ended analog channel input 7b / Low leakage Wake Up Port 15/ SPI module 1 MOSI / UART module 0 Receive/SPI module 1 MISO	MCU IO and Transceiver IO connected onboard
51	DIO2	Digital Input/Output	Transceiver GPIO Bit 2	
52	DIO3	Digital Input/Output	Transceiver GPIO Bit 3	
53	DIO4	Digital Input/Output	Transceiver GPIO Bit 4	
54	DIO5/CLKOUT	Digital Input/Output	Transceiver GPIO Bit 5 / ClkOut	Commonly programmed as ClkOut to supply MCU clock; connect to Pin 5
55	VDD	Power Input	MCU VDD supply	Connect to VDD supply
56	VDDAD	Power Input	MCU Analog supply	Connect to Analog supply
57	SCK / PTC5/DISABLED/LLWU_P9/ SPI0SCK/LPTMR0_ALT2/ CMP0_OUT	Digital Input/Output	SPI Port Clock driven from MCU Port C Bit 5/ MCU Port C Bit 5 / Low Leakage Wake UP Port 9/ SPI module 0 SCK/Low Power Timer module 0 ALT2/ Comparator 0 Analog voltage Output	• MCU IO and Transceiver IO connected onboard • MCU IO must be configured for this connection

Pin #	Pin Name[1]	Type	Description	Functionality
58	MOSI / PTC6 / CMP0_IN0/LLWU_P10/SPI0_MOSI/EXTRG_IN/SPI0_MISO	Digital Input/Output	SPI Port MOSI signal connected to MCU Port C Bit 6 / Comparator 0 Analog voltage Input 0/ Low Leakage Wake Up Port 10/ SPI module 0 MOSI/ External Trigger Input / SPI module 0 MISO	• MCU IO and Transceiver IO connected onboard • MCU IO must be configured for this connection
59	NSS / PTC4/ DISABLED/LLWU_P8/ SPI0_PCS0/UART1_TX/ FTM0_CH3	Digital Input/Output	SPI Port $\overline{\text{SS}}$ signal connected to MCU Port C Bit 4/Low leakage Wake Up Port 8/ SPI module 0 PCS/UART module 1Transmit/ Flex Timer module 0 Channel 3	• MCU IO and Transceiver IO connected onboard • MCU IO must be configured for this connection
60	MISO / PTC7 / CMP0_IN1/SPI0_MISO/ SPI0_MOSI	Digital Input/Output	SPI Port MISO signal connected to MCU Port C Bit 7/Comparator 0 Analog voltage Input 1/ SPI module 0 MISO/ SPI module 0 MOSI	• MCU IO and Transceiver IO connected onboard • MCU IO must be configured for this connection
FLAG	VSS	Power input	External package flag. Common VSS	Connect to ground.

1 Refer to ADD Table 1-3 for additional pin-out information on default and alternate setting selections.

4.2 Internal Functional Interconnects

The MCU provides control to the transceiver through the SPI Port and receives status from the transceiver from the DIOx pins. Certain interconnects between the devices are routed onboard the SiP. In addition, the signals are brought out to external pads.

Table 2. MKW01Z128 Internal Functional Interconnects

Pin #	MCU Signal	Transceiver Signal	Description
49	PTD7/SPI1_MISO SPI1_MOSI	DIO0	Transceiver DIO0 can be programmed to provide status to the MCU
50	PTD6/SPI1_MOSI SPI1_MISO	DIO1	Transceiver DIO1 can be programmed to provide status to the MCU
57	PTC5/SPI0SCK	SCK	MCU SPI connection must be initiated, not default
58	PTC6/SPI0_MOSI/ SPI0_MISO	MOSI	MCU SPI connection must be initiated, not default
59	PTC4/SPI0_PCS0	NSS	MCU SPI connection must be initiated, not default
60	PTC7/SPI0_MISO/ SPI0_MOSI	MISO	MCU SPI connection must be initiated, not default

NOTE

- As shown in Table 2, the MCU SPI Port pin selection must be configured by software.

- The transceiver DIO pins must be programmed to provide desired status

4.3 External Functional Interconnects

In addition to the onboard device interconnection, other external connections between the MCU and the transceiver are common:

1. Freescale recommends driving/controlling the transceiver reset from an MCU GPIO - This allows over-riding control of the transceiver from the system application.
2. The other DIO2-DIO4 status and RXTX signals can prove useful for monitoring the transceiver operation - the DIO2-DIO4 signals must be programmed to provide operational status. All signals must be connected externally to appropriate MCU GPIO for this function.

5 System and Power Management

The MKW01Z128 consists of an independent transceiver and MCU. The MCU controls the transceiver through programming of the SPI Port, and sets its operational mode through this control channel. Total current draw for the MKW01Z128 is dependent on the operation mode of both devices where different modes allow for different levels of power-down. Some additional features supported are:

- Transceiver Sleep with MCU set at the lowest power state.
- The transceiver mode selection being independent of the MCU's mode selection.
- The transceiver uses/powers-up the transmitter or receiver only as required.
- MCU peripheral control clock gating being disabled on a module-by-module basis to provide lowest power.
- RTC can be used as wake-up timer.
- LLWU (Low Leakage Wake-up Unit) available.

5.1 MCU Power Modes

The MCU has 10 different modes of operation to allow the user to optimize power consumption for the level of functionality needed. Depending on the STOP requirements of the user application, a variety of STOP modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. Table 3 outlines the various available power modes of MCU operation.

For each RUN mode there is a corresponding WAIT and STOP mode. WAIT modes are similiar to ARM sleep modes. STOP modes (VLPS, STOP) are similiar to ARM sleep deep mode. The very low power run (VLPR) operating mode can greatly reduce runtime power when the maximum bus frequency is not required to handle application needs. The 3 primary modes of operation are RUN, WAIT and STOP. The WFI instruction invokes both WAIT and STOP modes for the MCU. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 3. MCU power modes

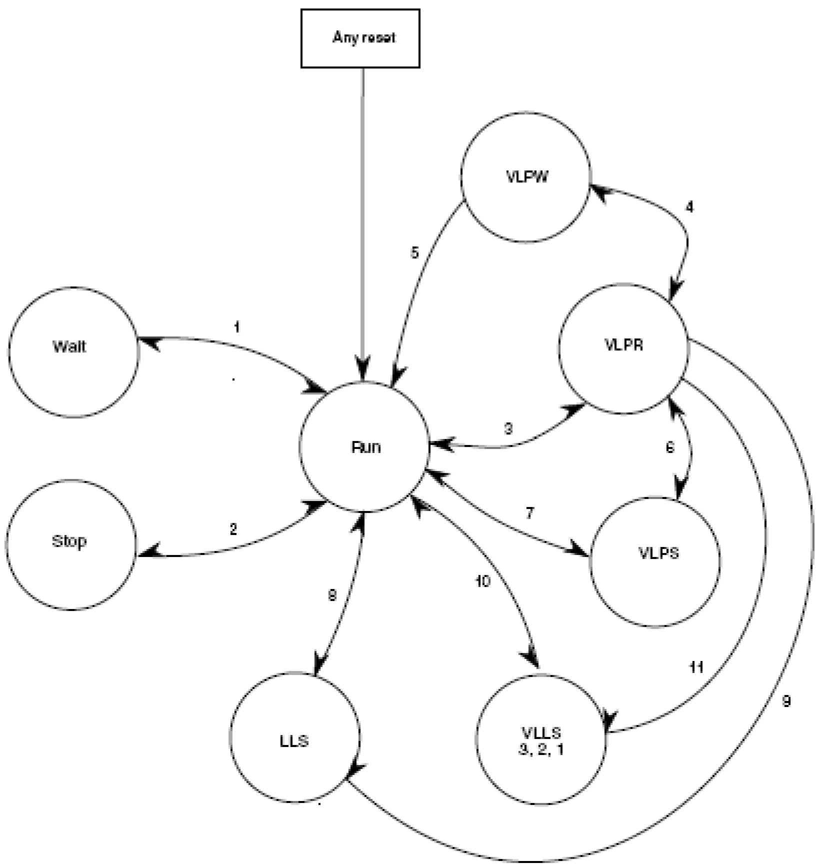
Power Mode	Description	Current[1]	Normal Recovery method	Recovery time
Normal RUN (all peripherals, “clock off”)	Allows maximum performance of chip.	125uA / MHz	—	—
Normal WAIT- via WFI	Allows peripherals to function while allowing the CPU to go to sleep reducing power.	TBD	Interrupt	0ns
Normal STOP- via WFI	Places chip in static state. Lowest power mode that retains all registers while amintaining LVD protection	127uA	Interrupt	4.3us
VLPR (Very Low Power RUN) (all peripherals off)	Reduced frequency (1MHz), Flash access mode, regulator in low power mode, LVD off. Internal oscillator can provide low power 4MHz source for the core. (Values at 2MHz core / 1MHz bus, module off, execution from flash).	100uA /MHz	Interrupt	4us
VLPW (Very Low Power WAIT) -via WFI (all peripherals off)	Similiar to VLPR, with CPU in sleep to further reduce power. (Values at 2MHz core /1MHz bus, module off).	TBD	Interrupt	4us
VLPS (Very Low Power STOP) -via WFI	Places MCU in static state, with LVD operation off, lowest power mode with ADC and all pin interrupt functional. LP timer, RTC CMP can be operational.	5.76uA	Interrupt	4.3us
LLS (Low Leakage STOP)	State retention power mode, LLWU, LPTimer, RTC, LCD,CMP can be operational	4.14uA	Wakeup Interrupt	4.6us
VLLS3 (Very Low Leakage STOP3)	Full SRAM retention. LLWU, LPTimer, RTC, LCD,CMP can be operational.	1.36uA	Wakeup Reset	53us
VLLS1 (Very Low Leakage STOP1) with LPTimer + LPO	All SRAM powered off. LLWU, LPTimer, RTC, CMP can be operational.	521nA	Wakeup Reset	115us
VLLS0 (Very Low Leakage STOP0)	Disable all analog modules in PMC and retains I/O state and DGO state. LPO shut down, optional POR brown-out detection, Pin interrupt only.	61nA	Wakeup Reset	115us

[1] Typical conditions

5.1.1 Power mode transitions

Figure 6 shows power mode transitions. Any reset always brings the MCU back to normal state run. In RUN, WAIT and STOP modes active power regulation is enabled. The VLPx modes are limited in frequency but offer a lower power operating power mode than normal modes. The LLS and VLLSx modes are the lowest power stop modes based on the amount of logic or memory that is required to be reatined by the application.

Figure 6. Power mode state transition diagram



5.2 Transceiver modes of operation.

The transceiver can be set in numerous modes of operation as described in Table 4. By default, when switching from one mode to another various features are selectively turned on coordinated by a pre-defined optimized sequence using the automatic sequencer. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer.

Table 4. Basic Transceiver modes

Selected Mode	Enabled blocks
Sleep	None
Stand-by	Main regulator and crystal osillator
Idle	Main regulator and RC osillator
FS	Frequency synthesizer
Transmit	Frequency synthesizer and transmitter
Receive	Frequency synthesizer and receiver
Listen	Periodical receive wake-up from Idle operation

An overview of the transceiver modes of operation is described below:

- Sleep - provides lowest power consumption and is the full power down state.
- Idle - provides very low standby power consumption and has the main voltage regulator and the RC oscillator enabled.
- Standby - similar to Idle with low standby power consumption but has the main voltage regulator and the crystal oscillator enabled.
- FS (Frequency synthesizer) - the frequency synthesizer is alive to shorten startup time to transmit or receive states.
- Transmit - transmitter is active.
- Receive - receiver is active.

5.3 System Protection

The MKW01Z128 provides numerous vehicles to maintain security or a high level of system robustness:

- Standard COP Watchdog reset with option to run from dedicated 1-kHz internal clock source or bus clock. The COP watchdog is intended to force a system reset when the application software fails to execute as expected.
- LVD protection with reset or interrupt; selectable trip points.
- HardFault exception on attempts to execute undefined instructions or access to undefined memory space.

- LOCKUP reset resource from core.
- Flash protection

6 Development Environment

Development support for the ARM® Cortex M0+ MCU on the MKW01Z128 is configured to provide maximum flexibility as allowed by the restrictions of the pinout and other available resources. One debug interface is supported:

- Two-wire Serial Wire Debug (SWD) interface

Table 5 presents a brief description of the serial wire debug description.

Table 5. Debug Components Description

Module	Type	Description
SWCLK	Input	Serial Wire Clock. This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.
SWDIO	Input /Output	Serial Wire debug data input / output. The SWDIO pin is used by an external debug tool for communication and devive control. This pin is pulled up internally.

7 System Electrical Specification

This section details maximum ratings for the 60 pin LGA package and recommended operating conditions, DC characteristics, and AC characteristics for the modem, and the MCU.

7.1 LGA Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 6 shows the maximum ratings for the 60 Pin LGA package.

Table 6. LGA Package Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Junction Temperature	T_J	95	°C
Storage Temperature Range	T_{stg}	-55 to 115	°C
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.8	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.3)	
RF Input Power	P_{max}	6	dBm

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

7.2 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with the JESD22 Stress Test Qualification for Commercial Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

All latchup testing is in conformity with the JESD78 IC Latch-Up Test.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin[1]	—	1	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin[1]	—	1	
Latch-up	Minimum input voltage limit		– 1.8	V
	Maximum input voltage limit		4.32	V

[1] This number represents a minimum number for both positive pulse(s) and negative pulse(s)

Table 8. ESD and Latc tection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 750	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	± 100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

7.3 Transceiver Electrical Characteristics

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2=VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, FRF = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

NOTE

Unless otherwise specified, the performances in the other frequency bands are similar or better.

7.3.1 Transceiver Recommended Operating Conditions

Table 9. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT})		1.8		3.6	Vdc
Operating Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	20% V_{BATT}	V
Logic Input Voltage High	V_{IH}	80% V_{BATT}	-	V_{BATT}	V
Logic Output Voltage Low (I_{max} = -1 mA)	V_{OL}	0	-	10% V_{BATT}	V
Logic Output Voltage High (I_{max} = 1 mA)	V_{OH}	90% V_{BATT}	-	V_{BATT}	V
Load capacitance on digital ports	C_L			25	pF
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-	0	dBm
Crystal Reference Oscillator Frequency	f_{ref}	32 MHz Only			

7.3.2 Transceiver Power Consumption

Table 10. Power Supply Current

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Supply current in Sleep mode		IDDSL	-	0.1	1	µA
Supply current in Idle mode	RC oscillator enabled	IDDIDLE	-	1.2	-	µA
Supply current in Standby mode	Crystal oscillator enabled	IDDST	-	1.25	1.5	mA
Supply current in Synthesizer mode		IDDFS	-	9	-	mA
Supply current in Receive mode		IDDR	-	16	-	mA
Supply current in Transmit mode with appropriate matching, stable across VDD range	RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFIO pin RFOP = +10 dBm, on RFIO pin RFOP = 0 dBm, on RFIO pin RFOP = -1 dBm, on RFIO pin	IDDT	- - - - -	95 45 33 20 16	- - - - -	mA mA mA mA mA

7.3.3 Transceiver Frequency Synthesis

Table 11. Frequency Synthesizer Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Synthesizer Frequency Range	Programmable	FR	290 424 862	- - -	340 510 1020	MHz MHz MHz
Crystal oscillator frequency		FXOSC	-	32	-	MHz
Crystal oscillator wake-up time		TS_OSC	-	250	500	µs
Frequency synthesizer wake-up time to PllLock signal	From Standby mode	TS_FS	-	80	150	µs
Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	TS_HOP	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	µs µs µs µs µs µs µs
Frequency synthesizer step	$FSTEP = FXOSC/2^{19}$	FSTEP	-	61.0	-	Hz
RC Oscillator frequency	After calibration	FRC	-	62.5	-	kHz
Bit rate, FSK	Programmable	BRF	1.2	-	600	kbps
Bit rate, OOK	Programmable	BRO	1.2	-	32.768	kbps
Frequency deviation, FSK	Programmable FDA + BRF/2 =< 500 kHz	FDA	0.6	-	300	kHz

7.3.4 Receiver

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in RegRxBw, receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit LnaZin in RegLna to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table 12. Receiver Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	RFS_F	- - -	-118 -114 -105	- - -	dBm dBm dBm
	FDA = 5 kHz, BR = 1.2 kb/s [1]		-	-120	-	dBm
OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	RFS_O	-	-112	-109	dBm
Co-Channel Rejection		CCR	-13	-10	-	dB
Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	ACR	- 37	42 42	- -	dB dB
Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	BI	- - -	-45 -40 -32	- - -	dBm dBm dBm
Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz		- - -	-36 -33 -25	- - -	dBm dBm dBm
AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	AMR	- - -	-45 -40 -32	- - -	dBm dBm dBm
2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP2	- -	+75 +35	- -	dBm dBm
3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	IIP3	- -23	+20 -18	- -	dBm dBm
Single Side channel filter BW	Programmable	BW_SSB	2.6	-	500	kHz
Image rejection in OOK mode	Wanted signal level = -106 dBm	IMR_ OOK	27	30	-	dB
Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE	- -	1.7 96	- -	ms µs
Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE_ AGC	-	3.0 163		ms µs
Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	TS_RE_ AGC&AFC		4.8 265		ms µs
FEI sampling time	Receiver is ready	TS_FEI	-	$4.T_{bit}$	-	-
AFC Response Time	Receiver is ready	TS_AFC	-	$4.T_{bit}$	-	-

Table 12. Receiver Specification

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
RSSI Response Time	Receiver is ready	TS_RSSI	-	$2.T_{bit}$	-	-
RSSI Dynamic Range	AGC enabled Min Max	DR_RSSI	- -	-115 0	- -	dBm dBm

[1] Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver

7.3.5 Transmitter

Table 13. Transmitter Specidication

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
RF output power in 50 ohms On RFIO pin	Programmable with 1dB steps Max Min	RF_OP	- -	+13 -18	- -	dBm dBm
Max RF output power, on PA_BOOST pin	With external match to 50 ohms	RF_OPH	-	+17	-	dBm
RF output power stability	From VDD=1.8V to 3.6V	ΔRF_OP	-	+/-0.3	-	dB
Transmitter Phase Noise	50 kHz Offset from carrier 868 / 915 MHz bands 434 / 315 MHz bands	PHN	- -	-95 -99	- -	dBc/Hz
Transmitter adjacent channel power (measured at 25 kHz offset)	BT=0.5 . Measurement conditions as defined by EN 300 220-1 V2.1.1	ACP	-	-	-37	dBm
Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10 µs, BR = 4.8 kb/s.	TS_TR	-	120	-	µs

7.4 MCU Electrical Characteristics

The following sections describe the electrical characteristics of the MKW01Z128 MCU.

7.4.1 MCU DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 14. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating Voltage				1.8[2]		3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T				2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C				1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	

Table 14. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T				2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C				1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
6	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} >1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}		0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	µA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	µA
11	P	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$\|I_{OZTOT}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	µA
12	P	Pull-up resistors	all digital inputs, when enabled	R_{PU}		17.5	—	52.5	kΩ
13	D	DC injection current [3, 4, 5]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
14	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
15	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
16	C	POR re-arm voltage[6]		V_{POR}		0.9	1.4	1.79	V

Table 14. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
17	D	POR re-arm time	t_{POR}		10	—	—	μs
18	P	Low-voltage detection threshold — high range[7]	V_{LVDH}[8]	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
19	P	Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
20	P	Low-voltage warning threshold — high range[7]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
21	P	Low-voltage warning threshold — low range[7]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
22	C	Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV
23	P	Bandgap Voltage Reference[9]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Low voltage detection and warning limits measured at 1 MHz bus frequency.

8 Run at 1 MHz bus frequency

9 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

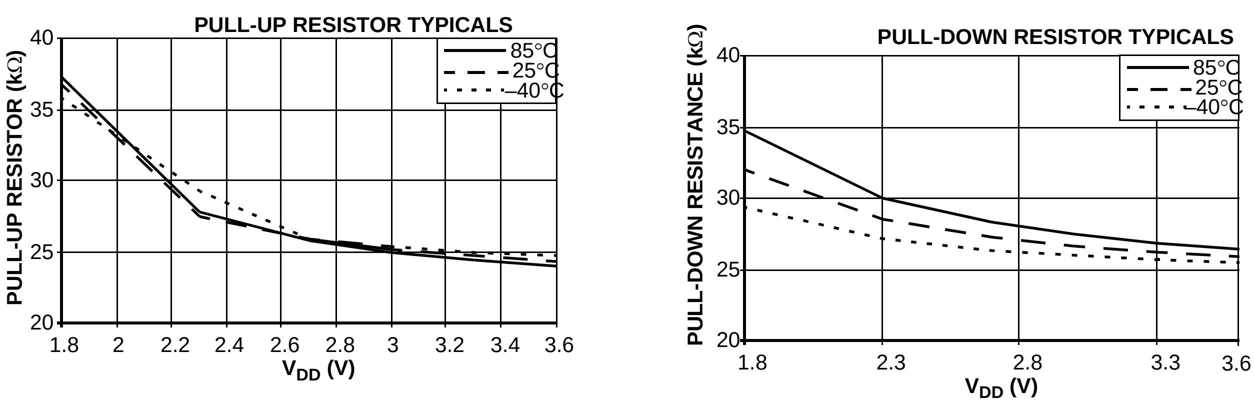


Figure 7. Pull-up and Pull-down Typical Resistor Values

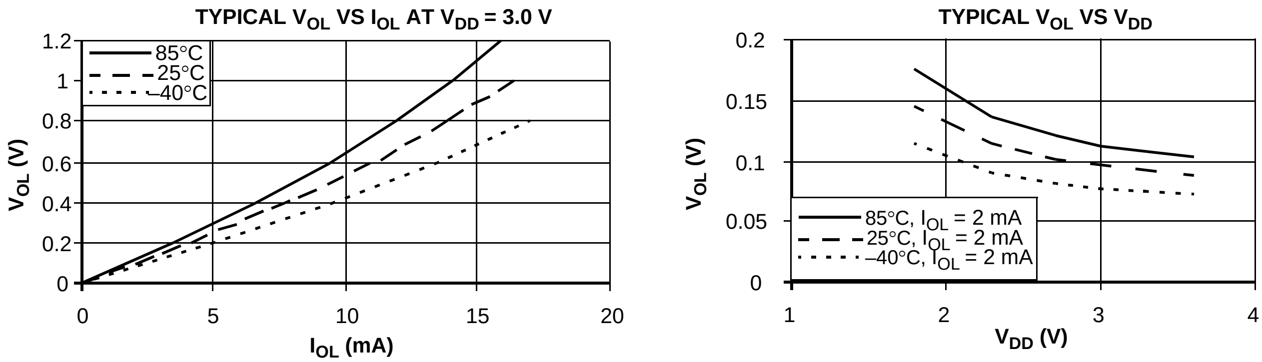


Figure 8. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

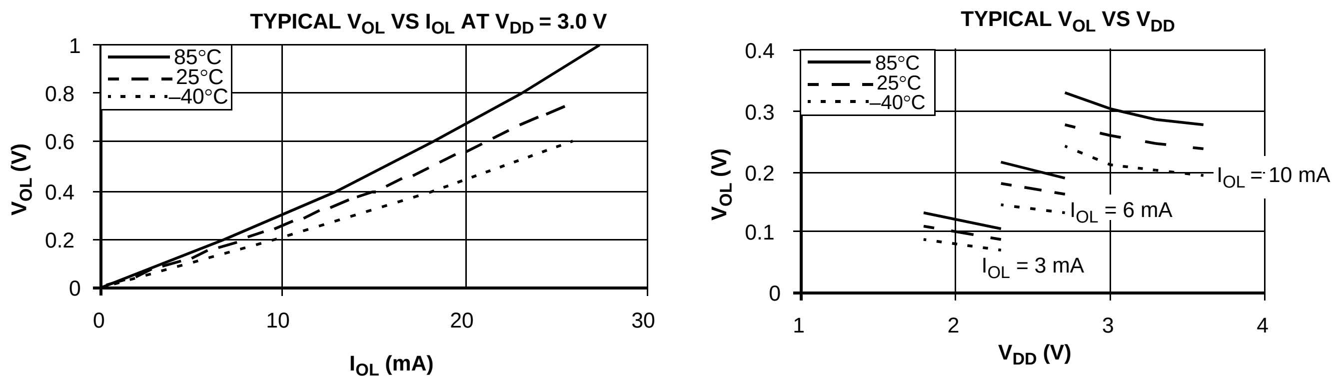


Figure 9. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

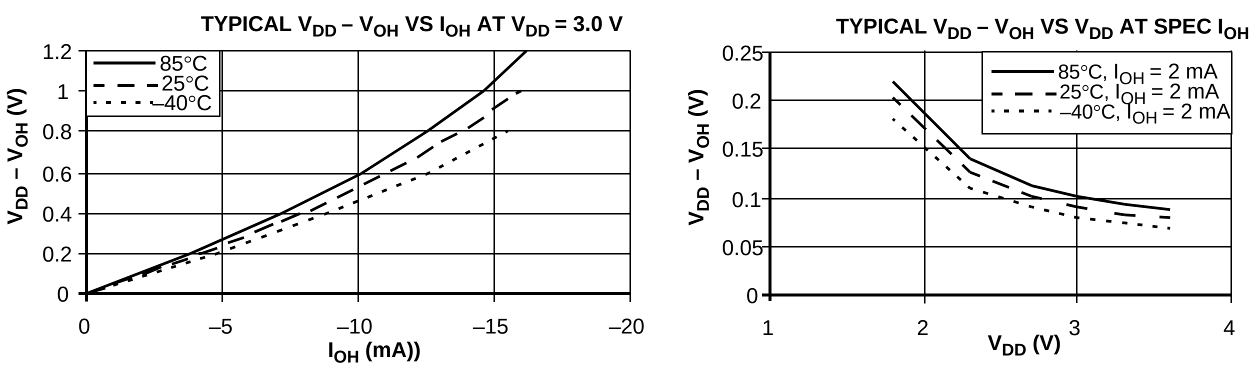


Figure 10. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

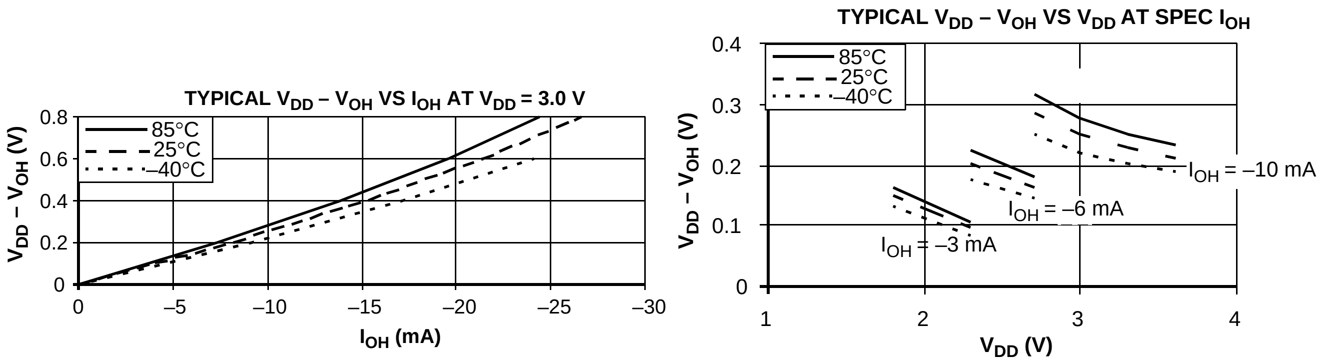


Figure 11. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

7.4.2 MCU Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 15. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	13	184	mA	–40 to 25
	P					14	15		85
	T			20 MHz		13.75	—		–40 to 85
	T			8 MHz		5.59	—		
	T			1 MHz		1.03	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPS=0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	µA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	0 to 70
							—		–40 to 85
	T	Run supply current LPS=1, all modules off, running from RAM				7.3	—		0 to 70
							—		–40 to 85
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6	mA	–-40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 15. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	n/a	3	0.35	0.65	µA	-40 to 25
	C						0.8	1.0		70
	P						2.0	4.5		85
	C					2	0.25	0.5		-40 to 25
	C						0.65	0.85		70
	C						1.5	3.5		85
7	P	Stop3 mode supply current No clocks active		$S3I_{DD}$	n/a	3	0.45	1.0	µA	-40 to 25
	C						1.5	2.3		70
	P						4	8		85
	C					2	0.35	0.7		-40 to 25
	C						1	2		70
	C						3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500		nA	-40 to 85
9	T		IREFSTEN=1		32 kHz		70		µA	
10	T		TPM PWM		100 Hz		12		nA	
11	T		SCI, SPI, or IIC		300 bps		15		µA	
12	T		RTC using LPO		1 kHz		200		µA	
13	T		RTC using ICSERCLK		32 kHz		1		µA	
14	T		LVD		n/a		100		µA	
15	T		ACMP		n/a		20		µA	

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 16. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	uA
6	T	ACMP[1]	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC[1]	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

1 Not available in stop2 mode.

7.4.3 External Oscillator (XOSCVLP) Characteristics

Reference Figure 12 and Figure 13 for crystal or resonator circuits.

Table 17. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f_{lo} f_{hi} f_{hi}	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 0 100 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	— — — —	200 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode FBELP mode	f_{extal}	0.03125 0	— —	40.0 50.33	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
3 See crystal or resonator manufacturer’s recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.

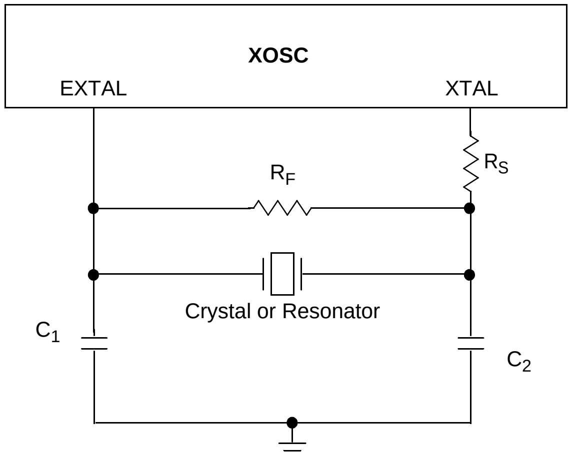


Figure 12. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

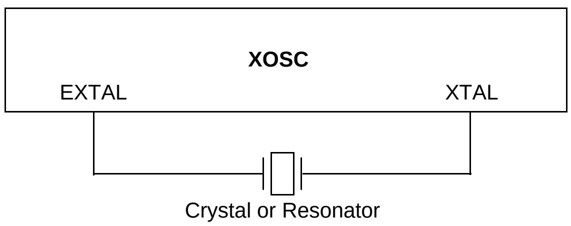


Figure 13. Typical Crystal or Resonator Circuit: Low Range/Low Gain

7.4.4 Internal Clock Source (ICS) Characteristics

Table 18. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25°C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	5	10	µs
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$

Table 18. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

[2] The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

[3] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[4] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

7.4.5 MCU Analog Characteristics

This section describes the following analog characteristics of the MCU system:

- 16-bit ADC
- High Speed Comparator (HSCMP) and 6-bit DAC
- 12-Bit DAC
- Power Management Controller (PMC) with with Low Voltage Warning (LVW) and detect.

7.4.5.1 ADC Characteristics

7.4.5.1.1 16-bit ADC Operating Conditions

These 16-bit specifications assume a separate VDDA supply for the ADC and an isolated pad segment for ADC supplies. Single ended (SE) channels meet 12-bit accuracy specifications.

Table 19. 16-bit ADC Operating Conditions

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})[2]	-100	0	+100	mV	
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	-100	0	+100	mV	
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	16 bit mode	—	8	10	pF	
		8/10/12 bit modes	—	4	5		
R_{ADIN}	Input Resistance		—	2	5	kΩ	

Table 19. 16-bit ADC Operating Conditions (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
R_{AS}	Analog Source Resistance	16 bit modes f_{ADCK} > 8 MHz f_{ADCK} = 4-8 MHz f_{ADCK} < 4 MHz	— — —	— — —	0.5 1 2	kΩ	External to MCU[3] Assumes ADLSMP=0
		13/12 bit modes f_{ADCK} > 16 MHz f_{ADCK} > 8MHz f_{ADCK} = 4-8 MHz f_{ADCK} < 4 MHz	— — — —	— — — —	0.5 1 2 5	kΩ	
		11/10 bit modes f_{ADCK} > 8 MHz f_{ADCK} = 4-8 MHz f_{ADCK} < 4 MHz	— — —	— — —	2 5 10	kΩ	
		11/10 bit modes f_{ADCK} > 8 MHz f_{ADCK} < 8 MHz	— —	— —	5 10	kΩ	
f_{ADCK}[4]	ADC Conversion Clock Freq.	ADLPC=0, ADHSC=1 16 bit modes < / = 13 bit modes	1.0 1.0	— —	TBD TBD	MHz	
		ADLPC=0, ADHSC=0 16 bit modes < / = 13 bit modes	1.0 1.0	— —	8.0 12.0	MHz	
		ADLPC=1, ADHSC=1 16 bit modes < / = 13 bit modes	1.0 1.0	— —	5.0 8.0	MHz	
		ADLPC=1, ADHSC=1 16 bit modes < / = 13 bit modes	1.0 1.0	— —	2.5 5.0	MHz	
		< / = 13 bit modes	1.0		18.0	MHz	
		16 bit modes	2.0		12.0	MHz	
C_{rate}	Conversion rate[5]	< / = 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	
		16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467		

1 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

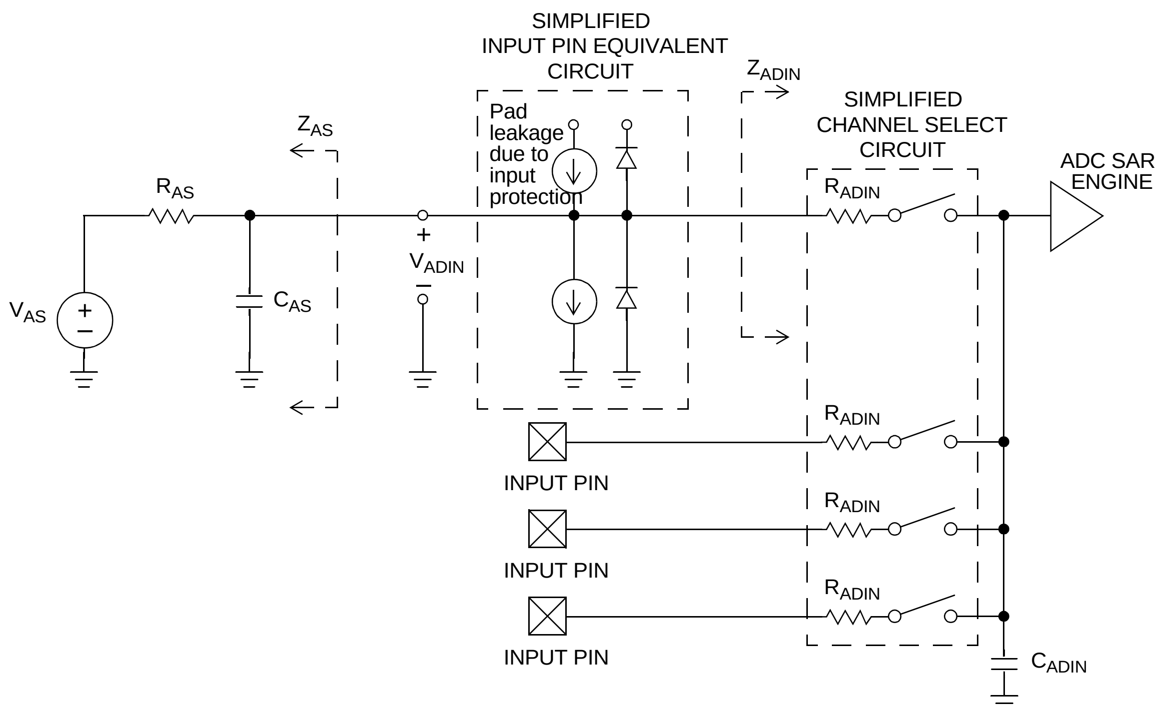
2 DC potential difference.

[3] This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this data sheet were derived from a system which has < 8 ohms analog source resistance. The R_{AS} / C_{AS} time constant should be kept < 1ns.

[4] To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.

[5] For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

Figure 14. ADC Input Impedance Equivalency Diagram



7.4.5.1.2 16-bit ADC Electrical Characteristics

Table 20. 16-Bit ADC characteristics (V_{REFH}=V_{DDA}, V_{REFL}=V_{SSA})

Symbol	Description	Conditions[1]	Min	Typ[2]	Max	Unit	Notes
I_{DDA_ADC}	Supply Current	ADLPC=1, ADHSC=0 ADLPC=1, ADHSC=1 ADLPC=0, ADHSC=0 ADLPC=0, ADHSC=1	— — — —	215 340 470 610	— — — —	µA	ADLSMP=0 ADCO=1
I_{DDA_ADC}	Supply Current	Stop, reset, module off	—	0.01	0.8	µA	ADLSMP=0 ADCO=1
I_{DDA_ADC}	Supply Current[3]		0.215	—	1.7	mA	
f_{ADACK}	ADC Asynchronous clock source	ADLPC=1, ADHSC=0 ADLPC=1, ADHSC=1 ADLPC=0, ADHSC=0 ADLPC=0, ADHSC=1	1.2 3.0 2.4 2.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz	t_{ADACK} = 1/f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
	Conversion Time	The ADC calculator tool can be used to determine ADC conversion times for different ADC configurations: http://cache/freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1					
TUE	Total Unadjusted Error	16 bit differential 16 bit single ended 13 bit differential 12 bit single ended 11 bit differential 10 bit single ended 9 bit differential 8 bit single ended	— — — — — — — —	+/- 14.0 +/- 13.0 +/- 1.5 +/- TBD +/- 0.8 +/- TBD +/- 0.5 +/- 0.5	+/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- 1.0 +/- 1.0	LSB[4]	5
		12 bit mode < 12 bit modes	— —	+/- 4.0 +/- 1.4	+/- 6.8 +/- 2.1		
DNL	Differential Non-Linearity	16 bit differential 16 bit single ended 13 bit differential 12 bit single ended 11 bit differential 10 bit single ended 9 bit differential 8 bit single ended	— — — — — — — —	+/- 2.5 +/- 2.5 +/- 0.7 +/- 0.7 +/- 0.5 +/- TBD +/- 0.2 +/- 0.2	+/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- 0.5 +/- 0.5	LSB[4]	5
		12 bit mode < 12 bit modes	— —	+/- 0.7 +/- 0.2	- 1.1 to +1.9 - 0.3 to +0.5		

Table 20. 16-Bit ADC characteristics (V_{REFH}=V_{DDA}, V_{REFL}=V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min	Typ[2]	Max	Unit	Notes
INL	Integral Non-Linearity	16 bit differential 16 bit single ended 13 bit differential 12 bit single ended 11 bit differential 10 bit single ended 9 bit differential 8 bit single ended	— — — — — — — —	-6 to +2.5 -2 to +12 +/- 1.0 +/- 1.0 +/- 0.5 +/- 0.5 +/- 0.3 +/- 0.3	+/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- TBD +/- 0.5 +/- 0.5	LSB[4]	5
		12 bit mode < 12 bit modes	— —	+/- 1.0 +/- 0.5	- 2.7 to +1.9 - 0.7 to +0.5		
E_{ZS}	Zero-Scale Error	16 bit differential 16 bit single ended 13 bit differential 12 bit single ended 11 bit differential 10 bit single ended 9 bit differential 8 bit single ended	— — — — — — — —	+/- 4.0 +/- 4.0 +/- 0.7 +/- 0.7 +/- 0.4 +/- 0.4 +/- 0.2 +/- 0.2	— — +/- TBD +/- TBD +/- TBD +/- TBD +/- 0.5 +/- 0.5	LSB[4]	V_{ADIN} = V_{SSA}
		< / = 13 bit mode < 12 bit modes	— —	+/- 0.7 +/- 0.4	+/- TBD +/- TBD		
E_{FS}[5]	Full-Scale Error	16 bit differential 16 bit single ended 13 bit differential 12 bit single ended 11 bit differential 10 bit single ended 9 bit differential 8 bit single ended	— — — — — — — —	0 to +10 0 to +14 +/- 1.0 +/- TBD +/- 0.4 +/- 0.4 +/- 0.2 +/- 0.2	— — +/- TBD +/- TBD +/- TBD +/- TBD +/- 0.5 +/- 0.5	LSB[4]	V_{ADIN} = V_{SSA}
		12 bit mode < 12 bit modes	— —	-4 -1.4	-5.4 -1.8		
E_Q	Quantization Errore	16 bit modes < / = 13 bit modes	— —	-1 to 0 —	— +/- 0.5	LSB[4]	

Table 20. 16-Bit ADC characteristics ($V_{REFH}=V_{DDA}$, $V_{REFL}=V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min	Typ[2]	Max	Unit	Notes
ENOB[6]	Effective Number of Bits	16 bit differential mode: Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1 16 bit single ended mode: Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	 12.8 12.7 12.6 12.5 11.8 TBD TBD TBD TBD TBD	 13.6 TBD 14.1 TBD 13.2 TBD TBD TBD TBD TBD	 15.0 14.6 14.3 13.9 13.0 TBD TBD TBD TBD TBD	bits	
		16 bit differential mode” Avg = 32 Avg = 4 16 bit single ended mode: Avg = 32 Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —		
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 x ENOB + 1.76			dB	
THD[7]	Total Harmonic Distortion	16 bit differential mode” Avg = 32 16 bit single ended mode: Avg = 32	 — —	 -94 -85	 — —	dB	
SFDR[7]	Spurious Free Dynamic range	16 bit differential mode” Avg = 32 16 bit single ended mode: Avg = 32	 82 78	 95 90	 — —	dB	
E_{IL}	Input Leakage Error		I_{In} * R_{AS}			mV	I_{In}= leakage current (refer to MCU voltage and current ratings)
m	Temp Sensor Slope	-40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp Sensor Voltage	25°C	—	719	—	mV	

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation, the ADLPC bit should be set, the HSC bit should be clear with 1 MHz ADC conversion clock speed.

4 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

5 ADC conversion clock <16MHz, Max. hardware averaging (AVGE = 1%, AVGS = 11%)

6 Input data is 100 Hz sine wave. ADC conversion clock <12 MHz.

7 Input data is 1 kHz sine wave. ADC conversion clock <12 MHz.

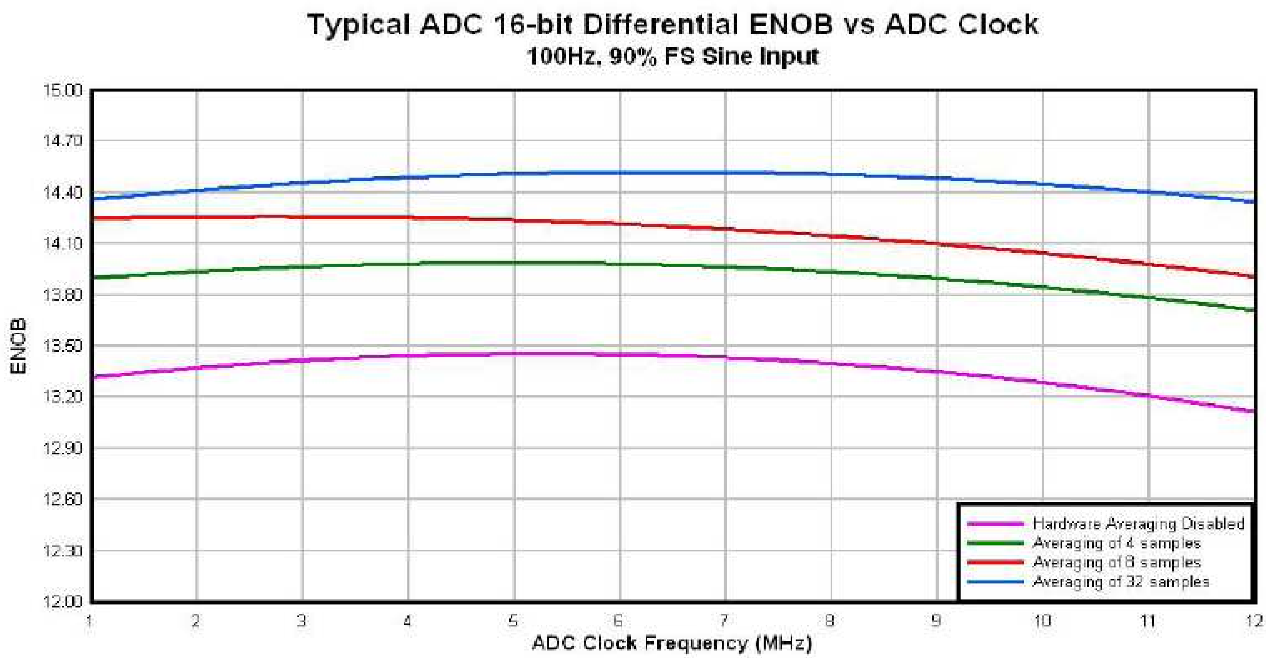


Figure 15. Typical ENOB Vs. ADC_CLK for 16-bit differential mode

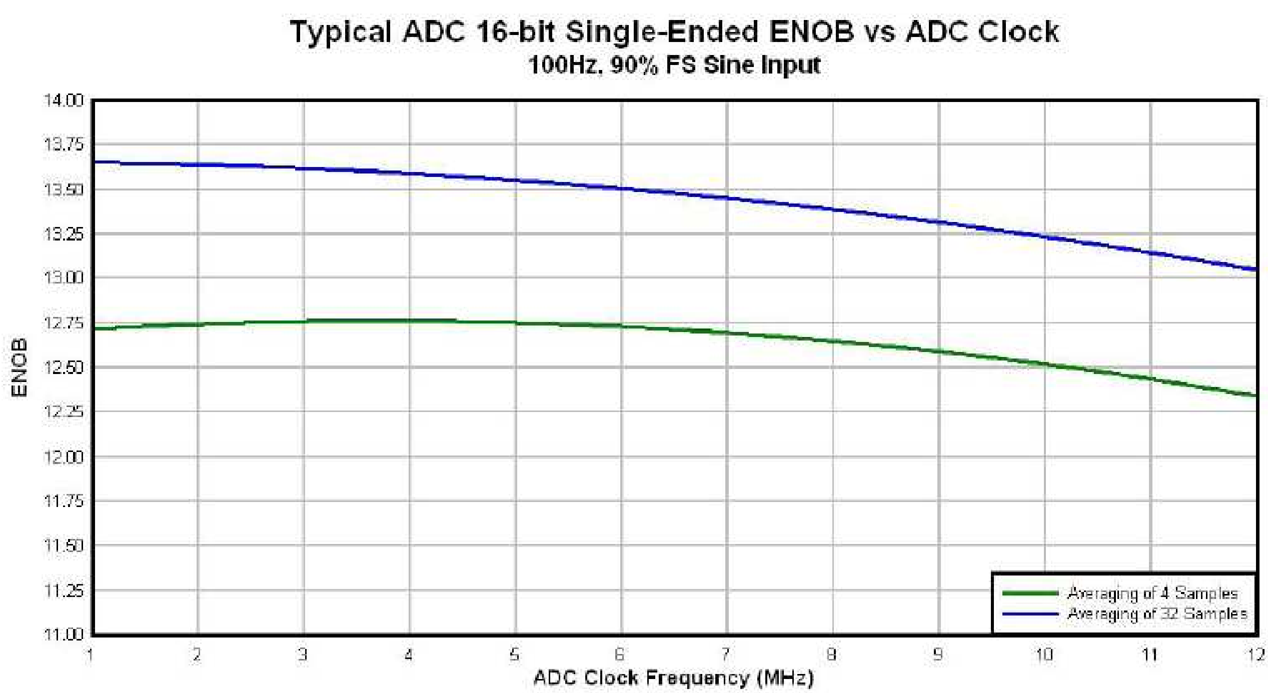


Figure 16. Typical ENOB Vs ADC_CLK for 16-bit single ended mode

7.4.5.2 High Speed Comparator (HSCMP) & 6-bit DAC electrical specifications

7.4.5.2.1 Overview

Figure 17 provides a block diagram of the modules configuration. The one (1) 12-bit DAC can be accessed through pins:

- CMP0 (Pins 9, 28, 29, 58 and 60)

Figure 17. CMP configuration

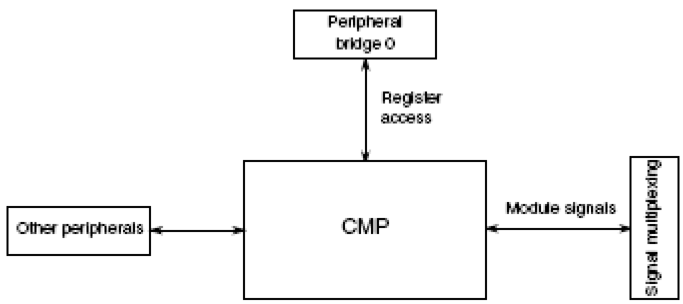


Table 21. High Speed Comparator (HSCMP) and 6-Bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
VDD	Supply voltage	1.71	—	3.60	V
I_{DDHS}	Supply current, High speed mode (EN=1, PMODE=1)	—	—	200	uA
I_{DDLS}	Supply current, Low speed mode (EN=1, PMODE=0)	—	—	20	uA
I_{DDOFF}	Supply current, OFF mode (EN=0)	—	—	100	nA
V_{AIN}	Analog voltage input	V_{SS} -0.3		V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hystersis[1]: CR0[HYSTCTR] = 00 CR0[HYSTCTR] = 01 CR0[HYSTCTR] = 10 CR0[HYSTCTR] = 11	 — — — —	 5 10 20 30	 — — — —	mV
V_{CMPOh}	Output high	V_{DD} -0.5	—	—	V
V_{CMPOL}	Output low	—	—	0.5	V
I_{ALKG}	Analog input leakage current	—	—	TBD	nA
t_{DHS}		20	50	200	ns
t_{DLS}		120	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	us
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	uA
	6-bit DAC reference input	TBD	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB[3]

1 Typical hysteresis is measured with input voltage range limited to 0.6V to V_{DD}-0.6V

2 Comparator initialization delay is defined as the time between software writes to change control bits (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL, see reference manual for details) and the comparator output settling to a stable level.

3 1 LSB = $V_{reference}$/64

Figure 18. Typical hysteresis Vs. Vin level (V_{DD} = 3.3V, PMODE = 0)

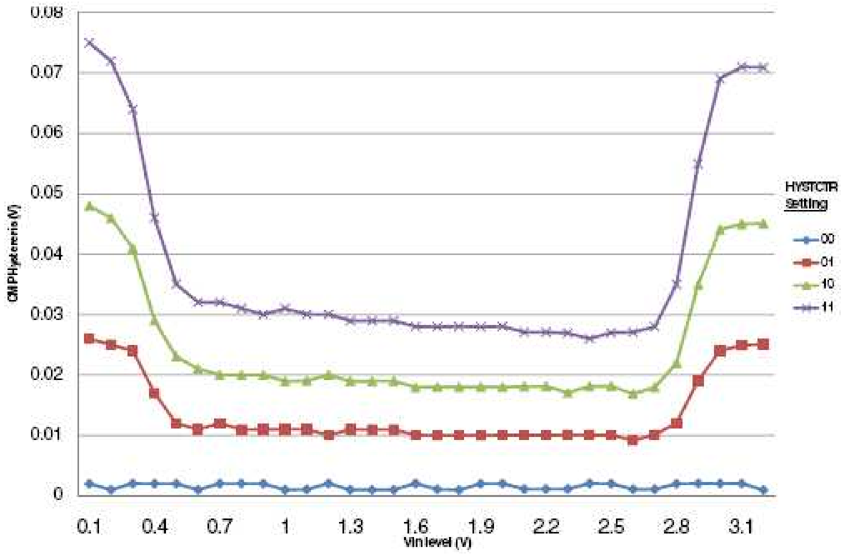
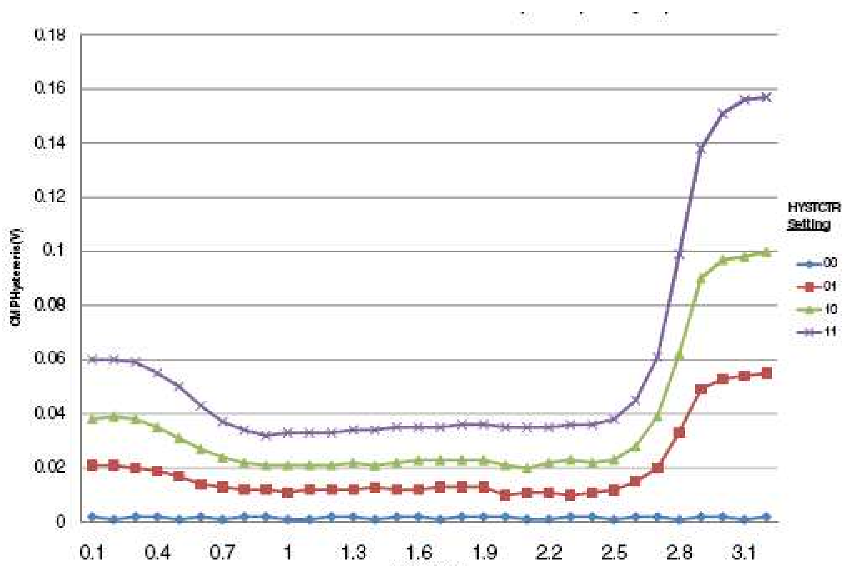


Figure 19. Typical hysteresis Vs. Vin level (V_{DD}= 3.3V, PMODE = 1)



7.4.5.3 12-bit DAC

12-bit digital-to-analog converter (DAC) includes a programmable reference generator output and has DMA support.

Table 22. 12-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
VDD	Supply voltage	1.71	—	3.60	V
I_{DACR}[1]	Reference voltage	1.13	—	3.60	V
T_A	Temperature	-40	—	105	C
C_L[2]	Output load capacitance	—	—	100	pF
I_L	Output load current	—	—	1	mA
I_{DDA_DACLP}	Supply current - low power mode	—	—	150	uA
I_{DDA_DACHP}	Supply current - high power mode	—	—	700	uA
t_{DACLP}[3]	Full-scale settling time - low power mode	—	100	200	us
t_{DACHP}[3]	Full-scale settling time - high power mode	—	15	30	us
$I_{CCDACLP}$[3]	Code-to-code settling time - low — high speed mode	—	0.7	1	us
$V_{dacoutl}$	DAC output voltage range low — high speed mode, no load.	—	—	100	mV
$V_{dacouth}$	DAC output voltage range high — high speed mode, no load.	V_{DACR} -100	—	V_{DACR}	mV
INL	Integral non-linearity error — high speed mode	—	—	+/- 8	LSB[4]
DNL	Differential non-linearity error — V_{DACR} > 2V	—	—	+/- 1	LSB[5]
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	+/- 1	LSB[6]
V_{OFFSET}	Offset error[7]	—	+/- 0.4		% FSR
E_G	Gain error[7]	—	+/- 0.1		% FSR
PSSR	Power Supply Rejection Ratio, V_{DDA} = 3V, T=25C	65	—	90	dB
PSSR	Power Supply Rejection Ratio, V_{DDA}> 2.4V	60	—	90	dB
R_{OP}	Output resistance load = 3 kohm	—	—	250	ohm
SR	Slew Rate • High power (SR_{HP}) • Low power (SR_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/us
CT	Channel to channel cross talk	—	—	-80	dB
BW	3dB bandwidth • High power (SR_{HP}) • Low power (SR_{LP})	 550 40	 — —	 — —	kHz

[1] The DAC reference can be VDDA or the voltage output of the VREF module (VREF_OUT)
[2] A small load capacitance (47pF) can improve the bandwidth performance of the DAC
[3] Settling within +/- 1 LSB
[4] The INL is measured for 0 + 100mV to V_{DACR} - 100mV
[5] The DNL is measured for 0 + 100mV to V_{DACR} - 100mV
[6] The DNL is measured for 0 + 100mV to V_{DACR} - 100mV with V_{DDA} > 2.4V
[7] Calculated by best fit curve from V_{SS} + 100mV to V_{DACR} - 100mV

7.4.5.4 Power Management Controller (PMC)

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed. Depending on the STOP requirements of the user application, a variety of STOP modes are available that provide state retention, partial power down of certain logic and/or memory. I/O states are held in all modes of operation. Both the MCU and transceiver MCU modes of operation are defined in Table 3 and Table 4.

7.4.5.4.1 Entering and exiting power modes

TheWFI instruction invokes WAIT and STOP modes for the SiP. The processor exits the low-power mode via an interrrupt. The wake-up flow from VLLSx is through reset. Once reset is engaged, the code execution begins, the I/O pins are held, RAM retained in VLLS3 only.

7.4.5.4.2 Operation in Low Power Modes

Table 23 outlines the functionality of each MCU module while in each of the low power modes. Terms used in the table are defined below.

- FF = Full functionality.
- static = Module register statesand associated memories retained
- powered = Memory is powered to reatin contents
- low power = Memory is powered to retain contents in a low power state
- OFF = Modules are powered off;module is in reset state upon wakeup
- wakup = Modules can serve as a wakeup source for the chip

Table 23. Module operation in low power modes

Modules	Stop	VLPR	VLPW	VLPS	LLS	VLLSx
NVIC	static	FF	FF	static	static	OFF
Mode Controller	FF	FF	FF	FF	FF	FF
LLWU[1]	static	static	static	static	FF	FF[2]
Regulator	ON	low power	low power	low power	low power	low power in VLLS3, OFF in VLLS0/1
LVD	ON	disabled	disabled	disabled	disabled	disabled
Brown-out detection	ON	ON	ON	ON	ON	ON in VLLS1/3, optionally disabled in VLLS0[3]
DMA	static	FF	FF	static	static	OFF
Watchdog	FF	FF	FF	FF	static	OFF
1kHz LPO	ON	ON	ON	ON	ON	ON in VLLS1/3, OFF in VLLS0
System oscillator (OSC)	OSCERCLK	OSCERCLK max. of 16MHz crystal	OSCERCLK max. of 16MHz crystal	OSCERCLK max. of 16MHz crystal	limited to low range / low power	limited to low range / low power in VLLS1/3, OFF in VLLS0
MCG	static - MCGIRCLK optional; PLL optionally on but gated	4MHz IRC	4MHz IRC	static - no clock output	static - no clock output	OFF
Core clock	OFF	4MHz max.	OFF	OFF	OFF	OFF
System clock	OFF	4MHz max.	4MHz max.	OFF	OFF	OFF
Bus clock	OFF	1MHz max.	1MHz max.	OFF	OFF	OFF
Flash	powered	1MHz max. access - no program	low power	low power	OFF	OFF
MGATE RAM	powered	powered	powered	powered	powered	powered in VLLS3
SRAM _U and SRAM_L	low power	low power	low power	low power	low power	low power in VLLS3, OFF in VLLS0/1
USB / FS/LS	static	static	static	static	static	OFF
USB Voltage regulator	optional	optional	optional	optional	optional	optional
UART0	FF with clocks	1 Mbps	1 Mbps	FF with clocks	static	OFF

Table 23. Module operation in low power modes

Modules	Stop	VLPR	VLPW	VLPS	LLS	VLLSx
UART1, UART2	static, wakeup on edge	1 Mbps	1 Mbps	static, wakeup on edge	static	OFF
SPI	static, slave mode receive	1 Mbps	1 Mbps	static, slave mode receive	static	OFF
I^2C	static, address match wakeup	100 kbps	100 kbps	static, address match wakeup	static	OFF
FTM	FF with clocks	FF	FF	FF with clocks	static	OFF
PIT	static	FF	FF	static	static	OFF
LPTMR	FF	FF	FF	FF	FF	FF[4]
RTC	FF	FF	FF	FF	FF	FF, OFF in VLLS0
16- bit ADC	ADC internal clock only	FF	FF	ADC internal clock only	static	OFF
CMP[5]	HS or LS compare	FF	FF	HS or LS compare	LS compare	LS compare in VLLS1/3, OFF in VLLS0
6-BIT dac	static	FF	FF	static	static	static, OFF in VLLS0
12-BIT dac	static	FF	FF	static	static	static
GPIO	wakeup	FF	FF	wakeup	static, pins latched	OFF, pins latched
TSI	wakeup	FF	wakeup	wakeup	wakeup	wakeup

1 Using the LLWU module, the external pins available do not require the associated peripheral function to be enabled. It only requires the function controlling the pin (GPIO or peripheral) to be configured as an input to allow a transition to occur to the LLWU.

2 Since LPO clock source is disabled, filters will be bypassed during VLLS0.

3 The VLLSCTRL [PORPO] bit in SMC module controls this option.

4 System OSC and LPO clock sources are not available in VLLS0 therefore pulse counting only.

5 CMP on STOP or VLPS supports high speed or low speed external pin to pin or external pin to DAC compares. CMP in LLS or VLLSx only supports low speed external pin to pin or external pin to DAC compares. Windowed, sampled and filtered modes or operation are not available while in STOP, VLPS or VLLSx modes.

7.4.6 MCU Timer characteristics

This section covers the timer characteristics of the MCU system:

- 16- bit Flexible Timer 0 (FTM0) / (LPTPM0)
  - – 6 channels, basic TPM function
  - – Functional in STOP/VPLS modes
- 16- bit Flexible Timer 1 (FTM1) / (LPTPM1)
  - – 2 channels, basic TPM function
  - – Functional in STOP/VPLS modes
- 16- bit Flexible Timer 2 (FTM2) / (LPTPM2)
  - – 2 channels, basic TPM function
  - – Functional in STOP/VPLS modes
- Low power timer (LPTMR)
  - – 1 channel, 16-bit pulse counter or periodic interrupt
  - – Functional in all power modes except VLLS0
- 2 channel 32-bit Programmable Interrupt Timer (PIT)
- Real Time Clock (SRTC)
- System Tick Timer (SYSTIK) with 24-bit counter

7.4.6.1 FTMx/LPTPMx Introduction

The FlexTimer is backwards compatible with the TPM (Timer PWM Module). The FlexTimer Module (FTM) is a two-to-eight channel timer that supports input capture, output compare and the generation of PWM signals. The FTM uses one input/output (I/O) pin per channel, CHn (FTM channel (n)) where n is the channel number. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter with programmable initial and final values and its counting can be up or up-down.

7.4.6.1.1 FTMx/LPTPMx Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 24. FTM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

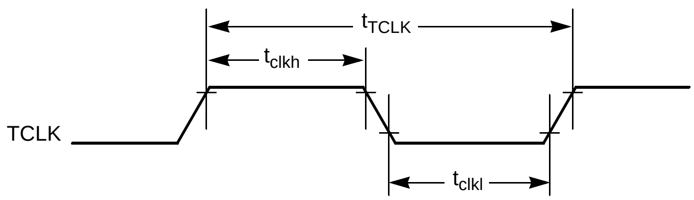


Figure 20. Timer External Clock

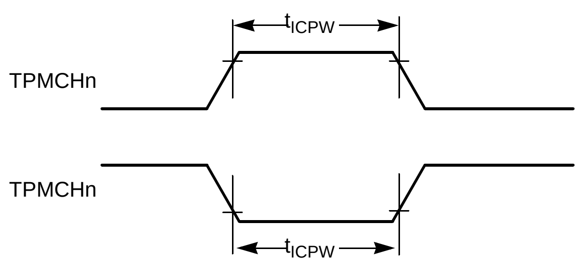
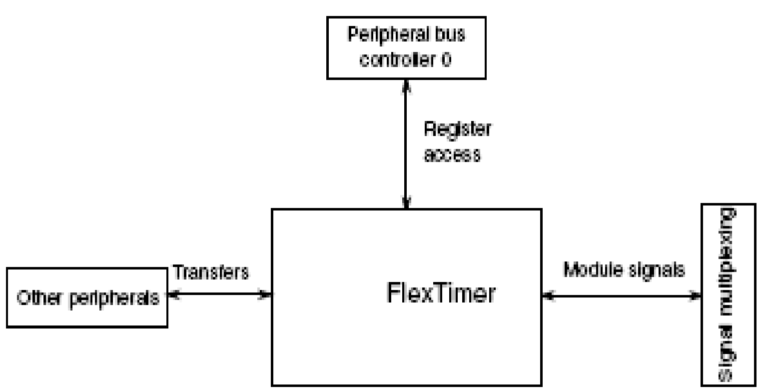


Figure 21. Timer Input Capture Pulse

By default each FTM is clocked by the internal bus clock (system clock) where each module has a register setting to allow an option of being clocked from an external module. The clock to each FlexTimer can be gated “on” or “off” to enable power reduction as required.

NOTE: FlexTimers must be no faster than 1/4 of the bus_clk frequency

Figure 22. FlexTimer configuration



7.4.6.1.2 Features

The FTM features include:

- FTM source clock is selectable:
  - Souce clock can be the system clock, the fixed frequency clock or an external clock.
  - Fixed frequency clock is an initial clock input to allow selection of an MCU clock souce other than the system clock
  - Selecting external clock connects FTM clock to a MCU input pin therefore allowing to synchronize the FTM counter with an off SiP clock source.
- Prescalar divide-by 1, 2, 4, 8, 16, 32, 64 or 128.
- 16-bit counter:
  - Can be free running counter or a counter with initial and final value
  - Counting can be up or up-down
- Each channel can be configured for input capture, output compare or edge-aligned PWM mode.
- In Input capture mode:
  - Capture can occur on rising edges, falling edges or both edges
  - An input filter can be selected for some channels
- In Output compare mode the output signal can be set, cleared or toggled on match.
- All channels can be configured for center-aligned PWM mode.
- Each pair of channels can be combined to generate a PWMsignal with independent control of both edges of PWM signal.
- The FTM channels can operate as pairs with equal outputs,pairs with complementary outputs or independent channels with independent outputs.
- The deadtime insertion is available for each complementary pair.
- Generation of matched triggers.
- Software control of PWM outputs.
- Up to 4 fault inputs for global fault control.
- Polarity of each channel is configurable.
- Generation of an interrupt per channel.
- Generation of an interrupt when the counter overflows.
- Generation of an interrupt when the fault condition is detected.
- Synchronized loading of write buffered FTM registers.
- Write protection for critical registers.

- Backwards compatible with TPM.
- Testing of input captures for a stuck at zero and one conditions.
- Dual edge capture for pulse and period width measurement.
- Quadrature decoder with input filters, relative position counting, interrupt on position count or capture of position count on external event.

7.4.6.2 Low Power Timer (LPTMR)

One 16-bit Low Power Timer is implemented to allow operation during all power modes including LLS and VLLSx with the exception of VLLS0 (Refer to Table 3 for MCU power modes) and can operate as either a Real Time Interrupt or as a pulse accumulator. It includes a 15-bit prescalar (Real Time Interrupt Mode) or glitch filter (Pulse Accumulator Mode) and can be clocked from the internal reference clock, the internal 1kHz LPO or an external 32.768kHz crystal. An interrupt is generated (and the counter can reset) when the counter equals the value in the 16-bit compare register.

7.4.6.2.1 Features

The features of the LPTMR module are:

- 16-bit counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wake-up from any low power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescalar/glitch filter
- Configurable input source for pulse counter
  - Rising or falling edge

Table 25 describes modes of operation of the LPTMR module.

Table 25. LPTMR modes of operation

Modes	Description
RUN	The LPTMR operates normally.
WAIT	The LPTMR continues to operate normally and may be configured to exit the low power mode by generating an interrupt request.
STOP	The LPTMR continues to operate normally and may be configured to exit the low power mode by generating an interrupt request.
Low-Leakage	The LPTMR continues to operate normally and may be configured to exit the low power mode by generating an interrupt request.
Debug	The LPTMR operates normally.

7.4.6.2.2 LPTMR power and reset

The LPTMR remains powered in all power modes, including low leakage modes. If the LPTMR is not required to remain operating during a low power mode, then it must be disabled before entering the mode.

The LPTMR is reset only on global Power On Reset (POR) or Low Voltage Detect (LVD). When configuring the LPTMR registers the CSR must be initially written with the timer disabled, before configuring the PSR and CMR.

7.4.6.3 Programmable Interrupt Timer (PIT)

This feature contains one PIT module with 2 channels. The device requires 32-bit PIT without RTI function. PIT is an array of timers that can be used to raise interrupts, trigger DMA channels and has no external pins. PIT trigger 0 and 1 are used as ADC hardware triggers. PIT can be used as generic timers to interrupt the CPU when the count expires allowing the system to have timed events.

7.4.6.3.1 Features

The main features of the PIT module are:

- Ability of timers to generate DMA trigger pulses.
- Ability of timers to generate interrupts.
- Maskable interrupts.
- Independent timeout periods for each timer.

7.4.6.3.2 PIT/DMA periodic trigger assignments

PIT generates periodic trigger events to the DMA channel mux as shown in Table 26.

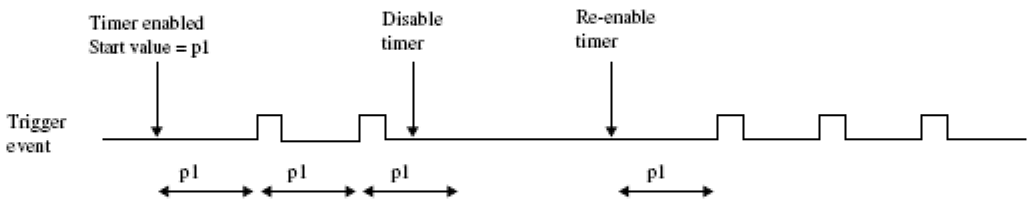
Table 26. PIT channel assignments for periodic DMA triggering

PIT Channel	DMA Channel Number
PIT Channel 0	DMA Channel 0
PIT Channel 1	DMA Channel 1

7.4.6.3.3 Functional Description

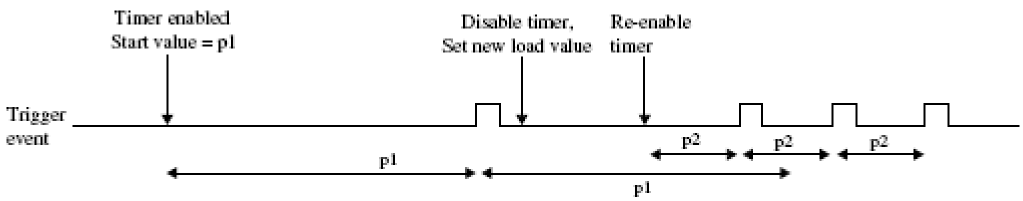
Each timer can be used to generate trigger pulses and interrupts where each interrupt is available on a separate interrupt line. The timers generate triggers at periodic levels, when enabled. The timers load the start values as specified in their LDVAL registers, count down to 0 and then load the respective start value again. Each time a timer reaches 0, it will generate a trigger plus and set the interrupt flag. All interrupts can be enabled or masked by setting TCTRLn[TIE]. A new interrupt can be generated only after the previous one is cleared. If desired, the current counter value of the timer can be read via the CVAL registers. The counter period can be restarted by first disabling and then enabling the timer with TCTRLn[TEN] (refer to Figure 23 for more detail).

Figure 23. Stopping and starting a timer



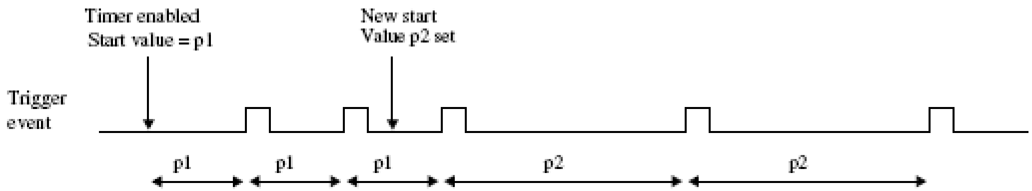
The counter period of a running timer can be modified by first disabling the timer, setting a new load value and then enabling the timer again (see Figure 24).

Figure 24. Modifying running timer period



It is also possible to change the counter period without restarting the timer by writing LDVAL with the new load value. This value will then be loaded after the next trigger event (see Figure 25).

Figure 25. Dynamically setting a new load value



In debug mode the timers will be frozen based on MCR[FRZ]. All timers support interrupt generation (refer to the RM for related vector addresses and priorities).

7.4.6.4 Real Time Clock (RTC)

The RTC operates in one (1) of two (2) modes of operation, chip power up and chip power down. During chip power down, RTC is powered from the backup power supply and is electrically isolated from the rest of the chip but continues to increment the timer counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible. During chip power-up, RTC remains powered from the backup battery supply. All RTC registers are accessible by software and all functions are operational. If enabled, the 32.768 kHz clock can be supplied to the rest of the chip or route the signal through pin #16 (XTAL). All registers must be accessed using 32-bit writes and all register accesses incur three (3) wait states.

7.4.6.4.1 RTC signal descriptions

Table 27. RTC signal descriptions

Signal	Description	I/O
EXTAL	32.768 kHz oscillator input	I
XTAL	32.768 kHz oscillator output	O
RTC_CLKOUT	1 Hz square-wave output	O
$\overline{\text{RTC\_WAKEUP}}$	Wakeup for external device	O

7.4.6.4.2 Power, clocking and reset functional Description

The time counter within the RTC is clocked by a 32.768 kHz clock and can supply this clock to other peripherals. The 32.768 kHz clock can only be sourced from an external crystal using the oscillator that is part of the RTC module. The RTC includes its own analog POR block, which generates a power-on-reset signal whenever the RTC module is powered up and initializes all RTC registers to their default state. A software reset bit can also initialize all RTC registers. The RTC also monitors the MCU power supply and electronically isolates itself when the rest of the chip is powered down. Any attempt to access an RTC register (except the access control registers) when VDD is powered down, when the RTC is electronically isolated, or when a VDD POR is asserted, will result in a bus error. Additional features supported are:

- Oscillator control
- Software reset
- Supervisor access

7.4.6.4.3 Time counter

The time counter consists of a 32-bit seconds counter that increments once every second and a 16-bit prescalar register that increments once every 32.768 kHz clock cycle.

7.4.6.4.4 Compensation

The compensation logic provides accurate and wide compensation range and can correct errors as high as 3906 ppm and as low as 0.12 ppm.

NOTE: The compensation factor must be calculated externally to the RTC and supplied by software to the register. The RTC itself does not calculated the amount of compensation that is required.

7.4.6.4.5 Time alarm

The time alarm register, SR[TAF] and IER[TAIE] allows the RTC to generate an interrupt at a predefined time. The 32-bit time alarm register is compared with the 32-bit time seconds register each time it increments. The SR[TAF] will set when the time alarm register equals the time seconds register and the time seconds register increments.

7.4.6.4.6 Update mode

An update mode bit is provided to configure software write access to the time counter enable bit. For more detail as to this features operation refer to the RM.

7.4.6.4.7 Register lock

The lock register can be used to block write accesses to certain registers until the next VBAT POR of software reset. Locking the control register will disable the software reset. Locking the lock register will block future updates to the lock register. Write accesses to a locked register are ignored and do not generate a bus error.

7.4.6.4.8 Access control

The read access and write access registers are implemented in the chip power domain and reset on the chip reset (they are not affected by the VBAT POR or the software reset). They are used to block read or write accesses to each register until the next chip system reset. When accesses are blocked the bus acess is not seen in the VBAT power supply and does not generate a bus error.

7.4.6.4.9 Interrupt

The RTC interrupt is asserted whenever a status flag and the corresponding interrupt enable bit is both set. It is always asserted on VBAT POR, software reset and when the VBAT power supply is powered down. The RTC interrupt is enabled at the chip level by enabling the chip specific RTC clock gate control bit. The RTC interrupt can be used to wakeup the chip from any low power mode. There is also an optional RTC seconds interrupt available where to obtain more detail on operation refer to the Reference Manual.

7.4.6.5 System Tick Timer (SYSTIK)

This module utilizes a 24-bit counter where the STCLK input to the ARM core system Tick Timer is driven with a divide-by-16 of the core clock, FCLK. The STCALIB inputs to the ARM core have no meaning in this device and are tied to logic 0. The CLKSOURCE bit in SysTick control and status register selects either the core clock, FCLK (when CLKSOURCE=1) or a divide-by-16 of the core clock, FCLK (when CLKSOURCE=0). Because the timing reference (FCLK) is a variable frequency, the TENMS bit in the SysTick Calibration Value Register is always zero.

7.4.7 Human Machine Interface

This section describes the following Human Machine Interface (HMI) features:

- GPIO
- Xtrinsic Touch Sensing Interface (TSI)

7.4.7.1 General Switching specifications

Table 28 describes general purpose specifications that apply to all signals configured for GPIO, UART, CMT and I^{2}C signals.

Table 28. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	FB_CLK high to GPIO output valid	—	16	ns	
	FB_CLK high to GPIO output invalid (output hold)	0	—	ns	
	GPIO input valid to FB_CLK high	14	—	ns	
	FB_CLK high to GPIO input invalid	—	2		
	GPIO pin interrupt pulse width (digital glitch filter disabled) – Synchronous path[1]	1.5	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) – Asynchronous path[2]	100	—	ns	
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) – Asynchronous path	100	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Mode select ($\overline{\text{EZP\_CS}}$) hold time after reset deassertion	2	—	Bus clock cycles	

1 The greater synchronous and asynchronous timing must be met.

2 This is the shortest pulse that is guaranteed to be recognized.

7.4.7.2 Touch Sensor Interface (TSI)

7.4.7.2.1 Overview and modes of operation

MKW01Z128 integrates a Touch Sensor Interface (TSI) module that is part of the Human Machine Interface (HMI). The touch sensing input (TSI) provides capacitive touch sensing detection with high sensitivity and enhanced robustness. Each TSI pin implements the capacitive measurement of an electrode having individual programmable detection thresholds and result registers. The TSI module can be functional in several low power modes with ultra low current adder and waking up the CPU in a touch event. It provides a solid capacitive measurement module to the implementation of touch keypad, rotaries and slider to support appliance and medical markets as examples. TSI module features include:

- Input capacitance touch sensing pins with individual result registers
- Automatic detection of electrode capacitance change in low power mode with programmable upper and lower threshold
- Automatic periodic scan unit with different duty cycles for run and low power modes.
- Fully supported SW library suite to implement keypads, rotaries and sliders.
- Operation across all low power modes: WAIT, STOP, VLPR,VLPW, VLPS LLS, VLLS.
- Capability to wake up the MCU from low power modes.
- Configurable interrupts:

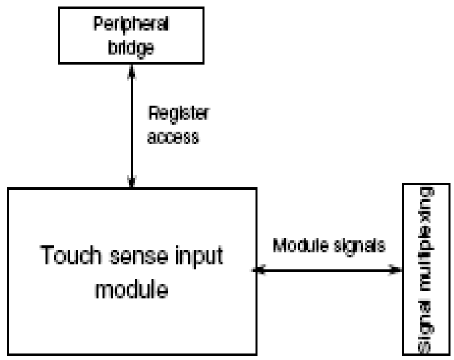
– End-of-scan or out-of-range interrupt

– TSI error interrupts: pad short to V_{DD}/V_{SS} or conversion overrun.

- Compensate temperature and supply voltage variations
- Stand alone operation not requiring any external crystal even in low power modes.
- Configurable integration of each electrode capacitive measurement for 1 to 4096 periods
- Programmable Electrode Oscillator and TSI Reference Oscillator allowing high sensitivity, small scan time and low power functionality.
- Only uses one pin per electrode implementation with no external hardware required.

The TSI feature is configured as shown in Figure 26

Figure 26. TSI configuration



The TSI module will run in all modes of operation as shown in Table 29. To support low power STOP modes (LLS, VLLSx) the TSI scan interval timer uses the LPO clock to save power. The internal TSI clock sources is used for input detection. Average power consumption for TSI in low power stop modes adds 1uA when enabled.

Table 29. TSI Module functionality in MCU operation modes

MCU operation mode	TSI clock sources	TSI operation mode when TSIEN = 1	Functional Electrode Pins	Required STPE state
RUN	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	Don’t care
WAIT	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	Don’t care
STOP	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	1
VLPRun	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	Don’t care
VLPWait	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	Don’t care
VLPStop	LPOCLK, MSGIRCLK, OSCERCLK	Active mode	All	1
LLS	LPOCLK, VLPOSCCLK		Determined by PEN[LPSP]	1
VLLS3	LPOCLK, VLPOSCCLK		Determined by PEN[LPSP]	1

Table 29. TSI Module functionality in MCU operation modes

MCU operation mode	TSI clock sources	TSI operation mode when TSIEN = 1	Functional Electrode Pins	Required STPE state
VLLS2	LPOCLK, VLPOSCCLK		Determined by PEN[LPSP]	1
VLLS1	LPOCLK, VLPOSCCLK		Determined by PEN[LPSP]	1

7.4.8 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section in the *Reference Manual*.

Table 30. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
P	Byte program time (random location)(2)	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)(2)	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time(2)	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	R_{IDDBP}	—	4	—	mA
	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

7.4.9 Communication Interfaces

7.4.9.1 Serial Peripheral Interface (SPI)

This feature contains two SPI modules that support 8-bit data length.

SPI0 is clocked on the bus clock. SPI1 is clocked from the system clock. SPI1 is therefore disabled in “Partial STOP Mode”.

The SPI supports DMA request and can operate in STOP/VLPS mode. When the SPI is operating in STOP/VLPS mode, it will operate as a slave.

SPI can wakeup the MCU from STOP/VLPS mode upon reception of SPI data in slave node.

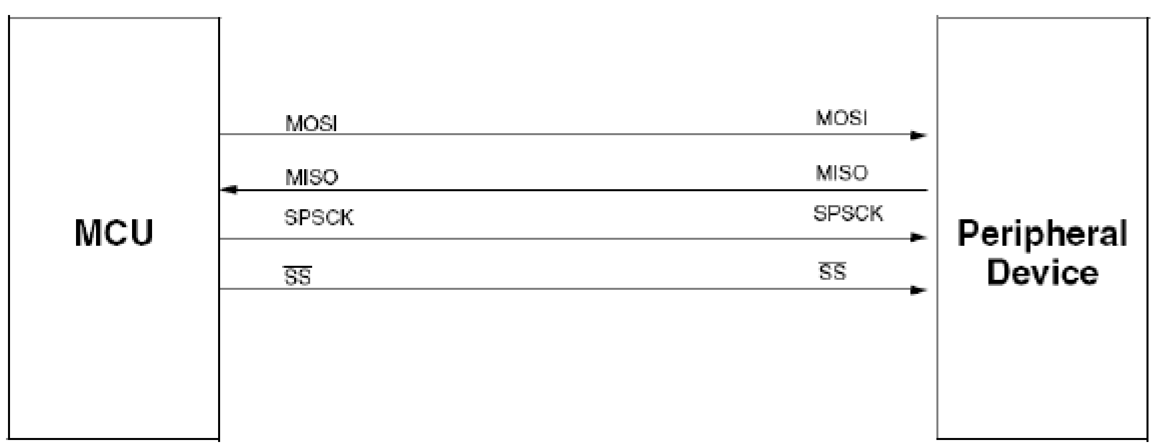
SPI0 will operate at maximum configurable speed — 12MHz in Master Mode (System clock/2).

SPI1 will not operate at maximum configurable speed — 24MHz in Master Mode (System clock/2).

7.4.9.1.1 SPI Use-case

SPI can be used several ways. Since the SPI is a standard interface this allows connection to a variety of devices like external SPI based memories, transmitters, basebands, PLM’s etc.

Figure 27. SPI usecase



7.4.9.1.2 Onboard System SPI Timing

Table 31. SPI Timing

No.	Function	Symbol	Min	Max	Unit
	Operating frequency Master	f_{op}	f_{Bus}/2048	10	MHz
1	SCK period Master	t_{SCK}	2	2048	t_{cyc}
2	Enable lead time Master	t_{Lead}	1/2	—	t_{SCK}
3	Enable lag time Master	t_{Lag}	1/2	—	t_{SCK}
4	Clock (SCK) high or low time Master	t_{WSCK}	62.5	1024 t_{cyc}	ns
5	Data setup time (inputs) Master	t_{SU}	15	—	ns
6	Data hold time (inputs) Master	t_{HI}	0	—	ns
7	Data valid (after SCK edge) Master	t_v	—	25	ns
8	Data hold time to transceiver	t_{HO}	250	—	ns
9	Slave Select high time between accesses	t_{nhigh}	20		ns

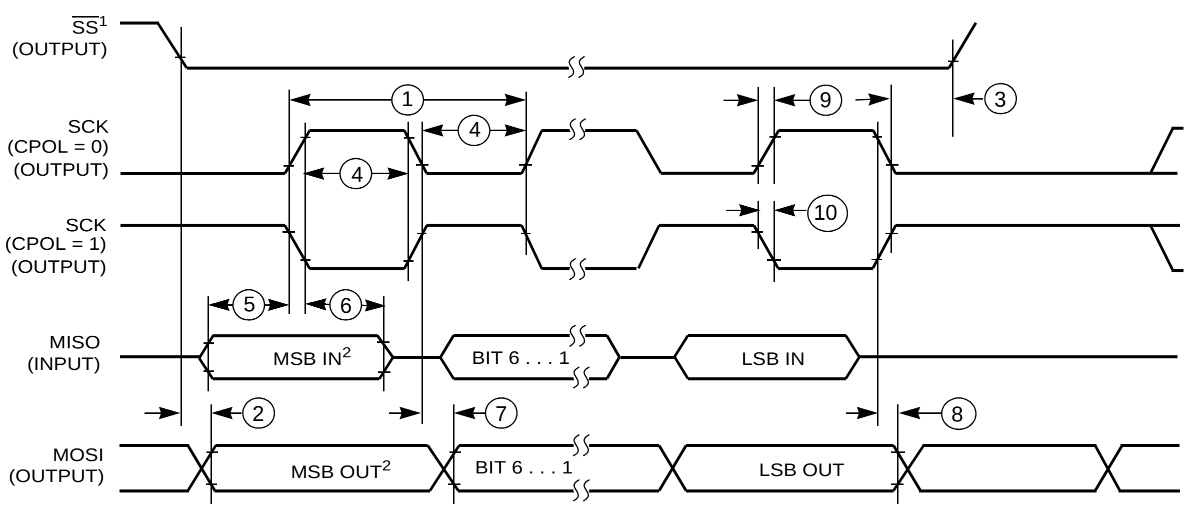


Figure 28. Onboard SPI Timing

7.4.9.2 Inter-Integrated Circuit (I2C)

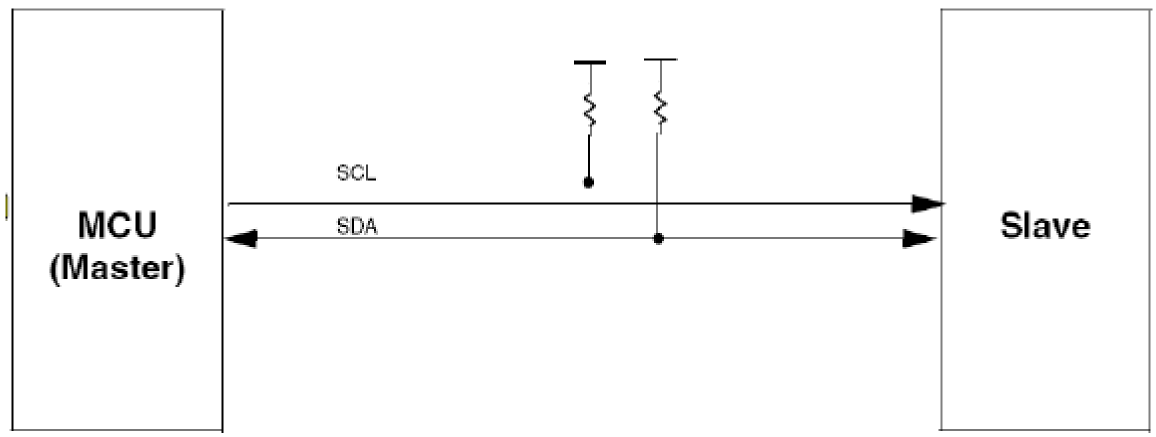
This feature has 2 IIC modules. Up to 400kbps ability is required at IIC bus heavy load conditions.

The IIC module includes SMBus support and DMA support. With the DMA implement, IIC must support auto transmission by DMA without any software operation. Optional on STOP/VLPS mode is wake up from STOP/VLPS.

7.4.9.2.1 IIC usecase

IIC being a standard interface allows connection to a variety of devices like external IIC based memories (EEPROM), sensors, etc.

Figure 29. IIC usecase



7.4.9.3 Universal Asynchronous Receive Transmit Port 0 (UART0)

7.4.9.3.1 UART0 overview

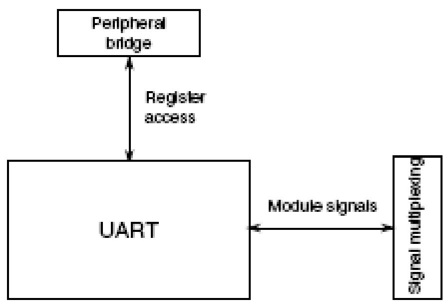
This feature contains one FSCI module. It is derived from the S08 SCI module and supports basic SCI, X4/X8/X16 oversampling of baud-rate, Smart card read and DMA.

The module is optional “on” in STOP/VLPS mode. FCSI is required run in STOP/VLPS modes and the clock source to FCSI is OSCOUT clock of XOSC, 32kHz that is mostly used in STOP/VLPS modes.

7.4.9.3.2 UART configuration

The UART modules 0 and 1 supported are configured as shown in Figure 30. UART1 is available in hardware, but is not supported by software.

Figure 30. UART configuration



UART1 allows asynchronous serial communication with peripheral devices and CPU’s. Just UART1 supports DMA and standard features.

7.4.9.3.3 Features

UART includes the following features:

- Full duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero (RZI) format with programmable pulse width
- 13-bit baud rate selection with /32 fractional divide, based on module clock frequency
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and recevier
- Programmable transmitter output polarity

- Programmable receive input polarity
- 13-bit break character option
- 11- bit break character detection option
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
  - IDLE line wakeup
  - Address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Hardware flow control support for request to sent (RTS) and clear to send (CTS) signals
- Support to interface with Smart cards
- Support for CEA709.1-B protocol used in building automation and home networking systems
- Interrupt-driven operation with 12 flags, not specific to ISO-7816 support
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- DMA interface

8 Typical Applications Circuit

Figure 31 show a MKW01Z128 typical applications circuit with and without use of an external power amplifier (PA) (driven by the RF power boost feature). Note a number of circuit features:

1. The two metal flags on the package bottom are independent (unconnected), and as a result, both must be connected to ground.
2. The topology of the external RF matching components is consistent across various frequency bandwidths. Only the component values differ as determined by the desired frequency range.
3. Freescale recommends using a single crystal design (as shown) to minimize systems costs - the circuit must connect transceiver signal DIO5/CLKOUT to the MCU EXTAL input to supply the MCU with a crystal accurate clock source. Also, the MCU initialization must enable the DIO5 pin as the ClkOut function.
4. Freescale also recommends that the transceiver RESET is driven by an MCU GPIO to provide total hardware control of the transceiver. Figure 31 shows GPIO PTC0 (preferred), but any GPIO can be used.

5. The MKW01Z128 provides onboard connection for the DIO1-DIO0 status to the MCU. External connection of DIO4-DIO2 status to MCU GPIO may be useful or required to implement a wireless node communication algorithm.
6. The transceiver reference oscillator uses the specified 32 MHz crystal (pins XTA and XTB).
7. A debug port connector is provided for programming the 9S08QE32 MCU FLASH and debugging code.
8. A simple UART interface (without flow control) is shown that is useful for a command/ communication channel interface or for system debug.

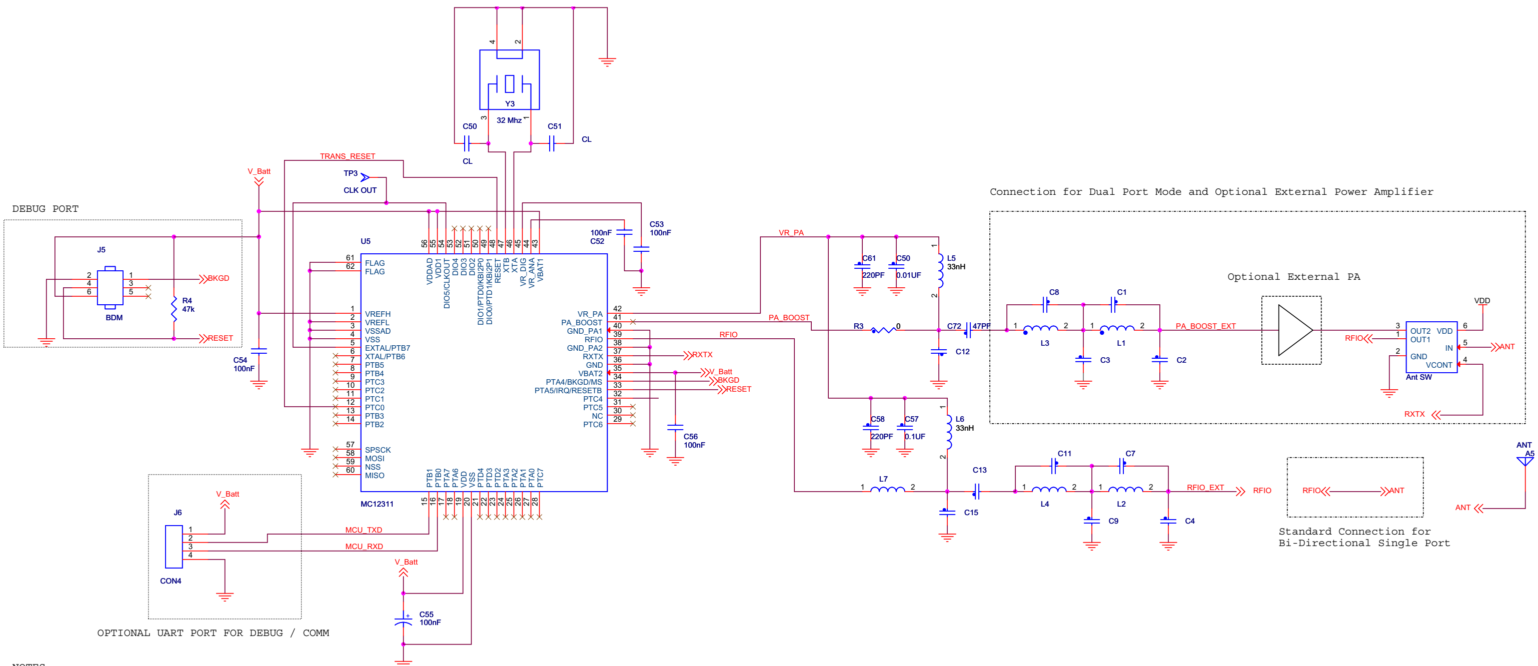
Two common RF wiring options are shown in Figure 31:

1. Bi-directional single port operation - this mode uses the bi-directional RF port pin of the MKW01Z128 designated as RFIO. The device transmits and receives through this single port.
   — Typical +13 dBm TX output power
   — Inductor L6 acts to provide DC power to the onboard transmitter while also acting as an AC signal block.
   — The circuit topology defined by inductors L7, L4 and L2 as well as capacitors C15, C13, C11, C7, C9, and C4 can provide:
     – Impedance matching between the RFIO port and the antenna
     – Low pass filtering for the onboard transmitter - when fully populated can implement an elliptic-function low pass filter.

NOTE

- The topology for the RF matching network can be used over the various bands of interest with changes in component values
- Not all indicated components are used at all frequencies
- Refer to *MKW01Z128 Sub 1 GHz Low Power Transceiver plus Microcontroller Reference Manual* (MKW01Z128RM.pdf) for additional information

2. Dual port operation with external amplification - this mode uses the RFIO port pin of the MKW01Z128 typically as the RX input and the auxiliary port PA_BOOST as the TX output. An external PA can optionally be inserted into the transmit path and an external antenna switch is also required.
   — The PA_BOOST has typical +17 dBm output power - this is +4 dBm higher than the RFIO and helps achieve higher power at the PA output
   — The PA_BOOST transmit path has a similar filter matching network discussed in the single-port to do low pass filtering and impedance match. The above note about components values also applies.
   — With separate transmit and receive paths, an antenna switch is required - the RXTX signal or another programmed GPIO can be used to switch paths depending on radio operation.
   — The receive side matching network can be simplified as no low pass filtering or harmonic trapping is required as with the transmit and single port networks



NOTES:

1) RF components determined by desired frequency range.
2) Recommend that ClkOut drive the MCU EXTAL input.
3) Recommend that transceiver RESET be driven from MCU GPIO (PTC0 shown).
3) Transceiver status DIO4-DIO2 may be monitored via external connection to MCU GPIO

Figure 31. MKW01Z128 Application Circuit Options

9 Mechanical Drawings

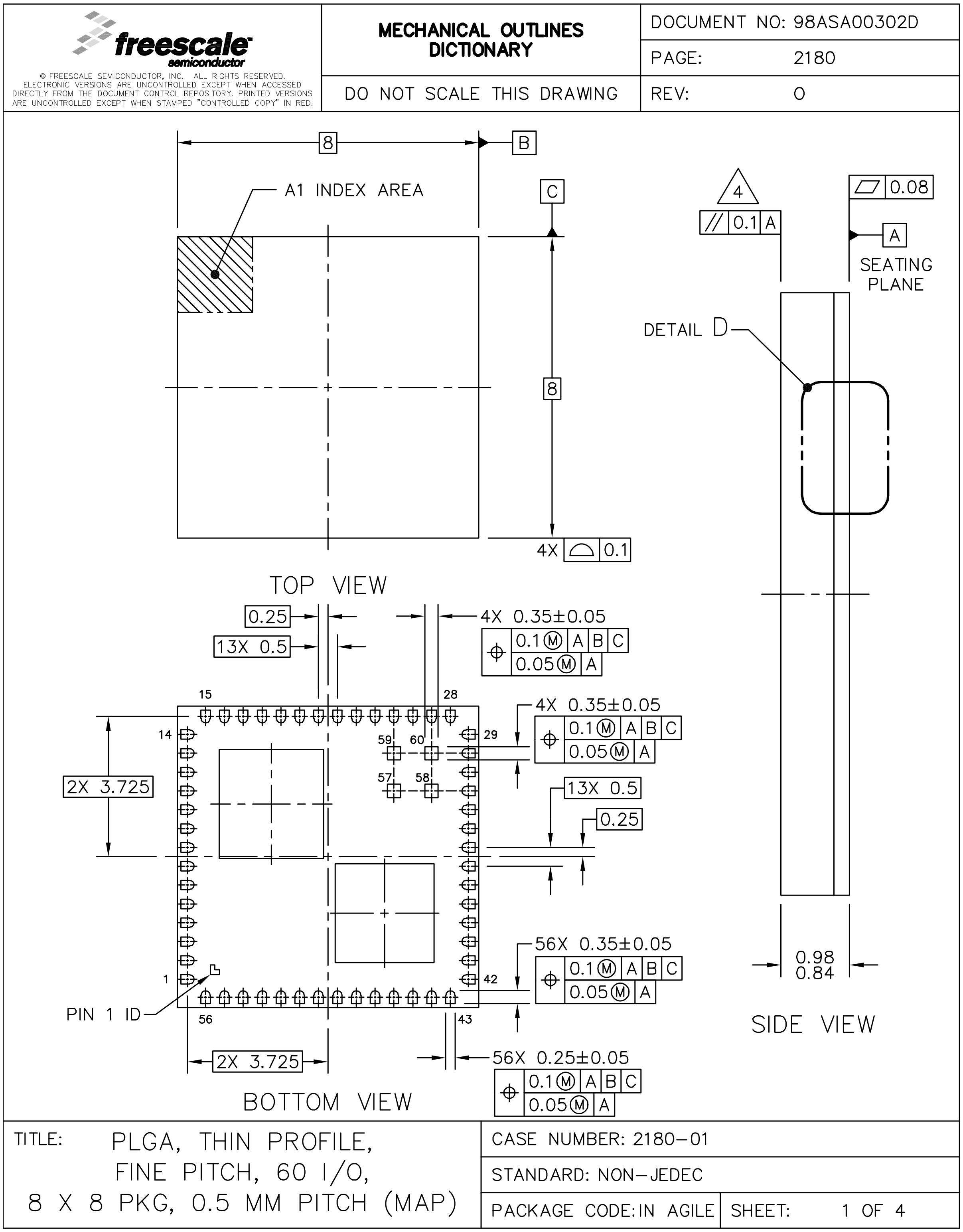


Figure 32. Mechanical Drawing (1 of 2)

freescale semiconductor 	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00302D
		PAGE: 2180
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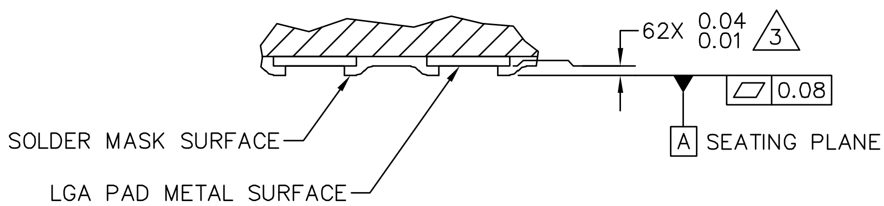
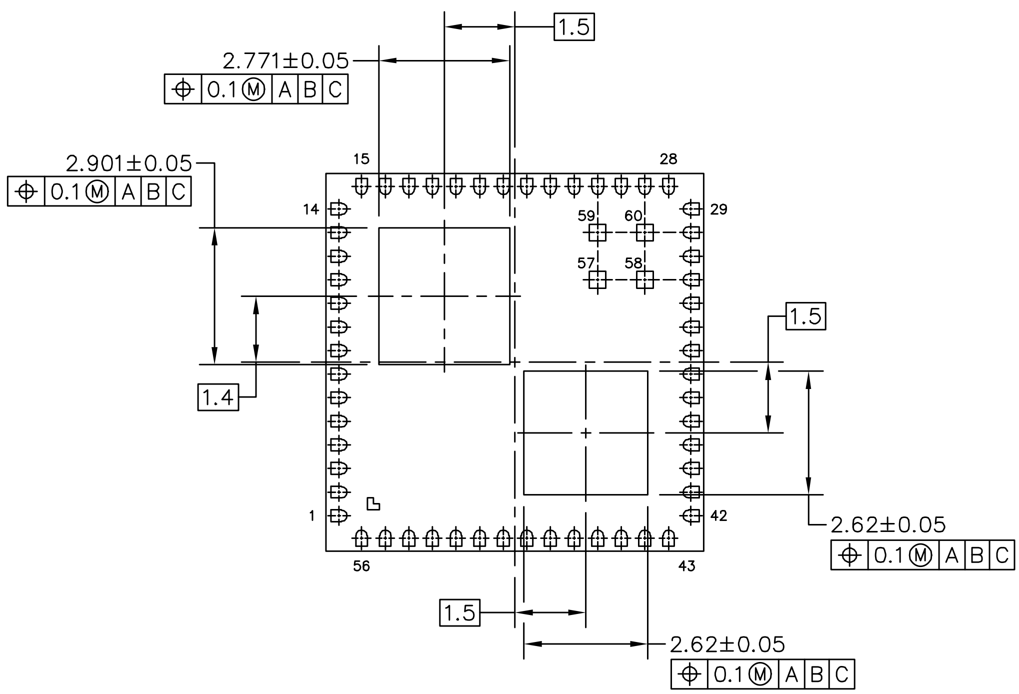


DETAIL D
VIEW ROTATED 90° CW



BOTTOM VIEW

TITLE: PLGA, THIN PROFILE, FINE PITCH, 60 I/O, 8 X 8 PKG, 0.5 MM PITCH (MAP)	CASE NUMBER: 2180–01	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: IN AGILE	SHEET: 2

Figure 33. Mechanical Drawing (2 of 2)

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