



# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

Designed for base station applications with frequencies from 728 to 768 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1400$  mA,  $P_{out} = 63$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency (MHz)	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
728	20.0	36.1	6.3	-38.1
748	20.2	36.0	6.4	-39.0
768	20.1	35.9	6.4	-38.7

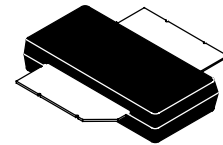
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 748 MHz, 360 Watts CW Output Power (3 dB Input Overdrive from Rated  $P_{out}$ ), Designed for Enhanced Ruggedness
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx$  260 Watts CW

### Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel.

**MRF8S7235NR3**

**728-768 MHz, 63 W AVG., 28 V  
 SINGLE W-CDMA  
 LATERAL N-CHANNEL  
 RF POWER MOSFET**



**OM-780-2  
 PLASTIC**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +70	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 63 W CW, 28 Vdc, $I_{DQ} = 1400$ mA, 728 MHz Case Temperature 82°C, 250 W CW, 28 Vdc, $I_{DQ} = 1400$ mA, 728 MHz	$R_{\theta JC}$	0.33 0.29	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 70\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 920\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.5	2.3	3.0	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_D = 1400\ \text{mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2.3	3.0	3.8	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.4\ \text{Adc}$ )	$V_{DS(on)}$	0.1	0.18	0.3	Vdc

**Functional Tests** <sup>(1)</sup> (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\ \text{mA}$ ,  $P_{out} = 63\ \text{W Avg.}$ ,  $f = 728\ \text{MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\ \text{MHz}$  Offset.

Power Gain	$G_{ps}$	18.8	20.0	21.8	dB
Drain Efficiency	$\eta_D$	34.5	36.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.8	6.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38.1	-35.5	dBc
Input Return Loss	IRL	—	-16	-10	dB

**Typical Broadband Performance** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\ \text{mA}$ ,  $P_{out} = 63\ \text{W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\ \text{MHz}$  Offset.

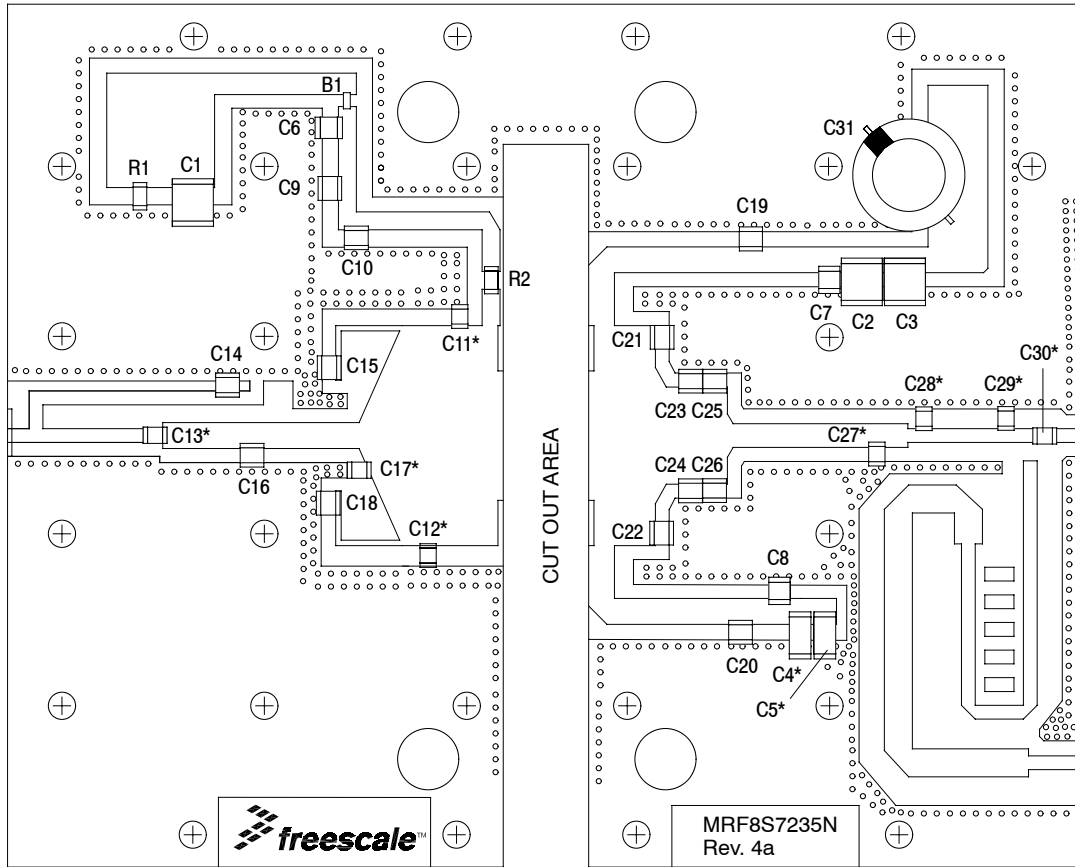
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
728 MHz	20.0	36.1	6.3	-38.1	-16
748 MHz	20.2	36.0	6.4	-39.0	-17
768 MHz	20.1	35.9	6.4	-38.7	-15

1. Part internally matched both on input and output.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ} = 1400$ mA, 728-768 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	260	—	W
IMD Symmetry @ 107 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30$ dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD <sub>sym</sub>	—	10	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	40	—	MHz
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 63$ W Avg.	G <sub>F</sub>	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.0124	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.005	—	dB/°C



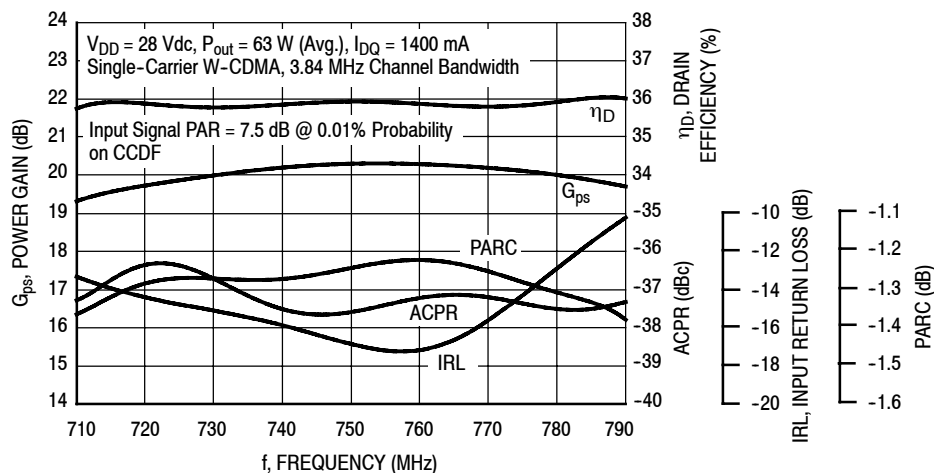
\*C4, C5, C11, C12, C13, C17, C27, C28, C29 and C30 are mounted vertically.

Figure 1. MRF8S7235NR3 Test Circuit Component Layout

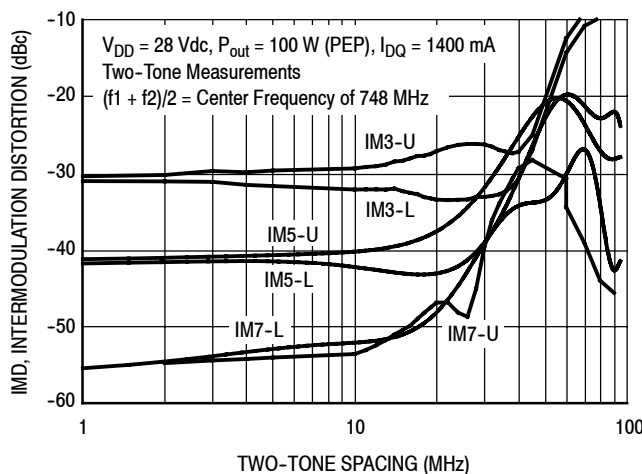
Table 6. MRF8S7235NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	MPZ2012S300A	Murata
C1, C2, C3, C4, C5	22 $\mu$ F Chip Capacitors	C5750KF1H226ZT	TDK
C6, C7, C8	3.3 $\mu$ F Chip Capacitors	C3225JB1H335MT	TDK
C9, C19, C20	68 pF Chip Capacitors	ATC100B680JT500XT	ATC
C10	12 pF Chip Capacitor	ATC100B120JT500XT	ATC
C11, C12	10 pF Chip Capacitors	ATC100B100CT500XT	ATC
C13	2.7 pF Chip Capacitor	ATC100B2R7CT500XT	ATC
C14	110 pF Chip Capacitor	ATC100B111JT500XT	ATC
C15, C16, C17, C18, C27	3.6 pF Chip Capacitors	ATC100B3R6CT500XT	ATC
C21, C22	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C23, C24	6.2 pF Chip Capacitors	ATC100B6R2CT500XT	ATC
C25, C26	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C28	3.3 pF Chip Capacitor	ATC100B3R3CT500XT	ATC
C29	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C30	39 pF Chip Capacitor	ATC100B390JT500XT	ATC
C31	470 $\mu$ F Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	27 K $\Omega$ , 1/4 W Chip Resistor	CRCW120627K0JNEA	Vishay
R2	4.75 $\Omega$ , 1/4 W Chip Resistor	CRCW12064R75FNEA	Vishay
PCB	0.030", $\epsilon_r = 3.5$	RF35-A2	Taconic

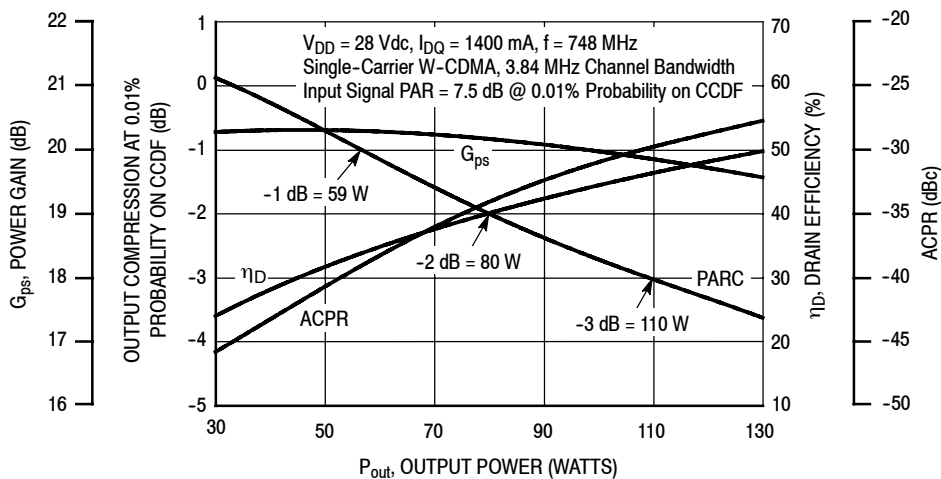
## TYPICAL CHARACTERISTICS



**Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 63$  Watts Avg.**

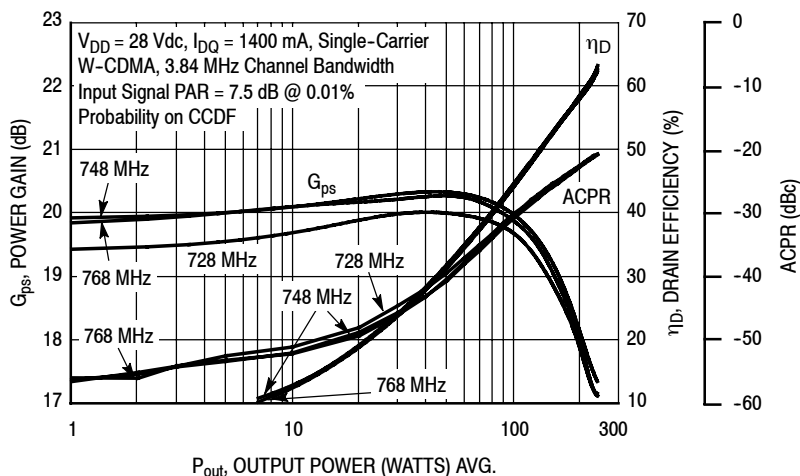


**Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing**

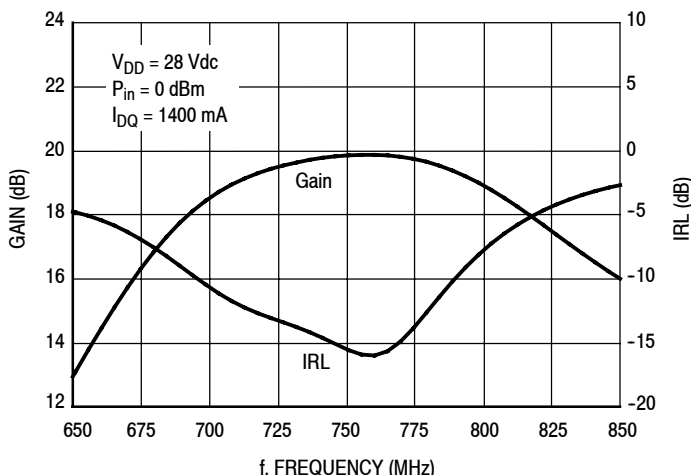


**Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS

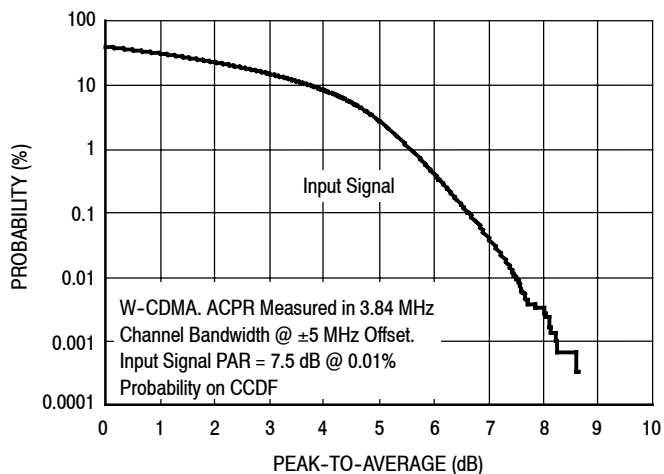


**Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

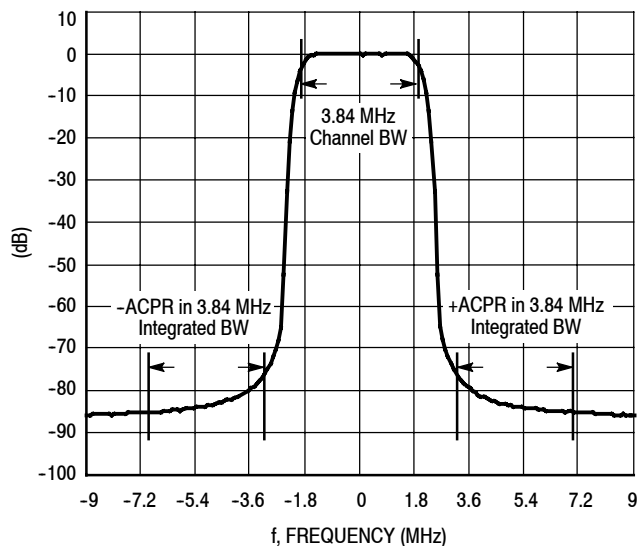


**Figure 6. Broadband Frequency Response**

### W-CDMA TEST SIGNAL



**Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



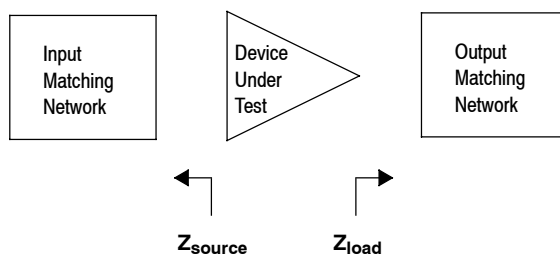
**Figure 8. Single-Carrier W-CDMA Spectrum**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1400 \text{ mA}$ ,  $P_{out} = 63 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
710	0.95 - j0.82	1.19 - j1.03
720	0.93 - j0.81	1.05 - j0.99
730	0.89 - j0.77	0.92 - j0.91
740	0.87 - j0.73	0.85 - j0.82
750	0.89 - j0.73	0.83 - j0.78
760	0.92 - j0.77	0.83 - j0.77
770	0.89 - j0.81	0.79 - j0.76
780	0.80 - j0.77	0.71 - j0.68
790	0.70 - j0.66	0.61 - j0.56

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.



**Figure 9. Series Equivalent Source and Load Impedance**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1200 \text{ mA}$ , Pulsed CW,  $10 \mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	$\eta_D$ (%)	(dBm)	(W)	$\eta_D$ (%)
728	1.00 - j0.80	0.50 - j0.70	55.3	339	54.1	56.2	417	57.2
748	0.70 - j1.10	0.50 - j0.60	55.4	347	53.9	56.2	417	56.9
768	0.80 - j1.25	0.50 - j0.60	55.3	339	53.5	56.1	407	56.9

(1) Load impedance for optimum P1dB power.

$Z_{\text{source}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Impedance as measured from drain contact to ground.

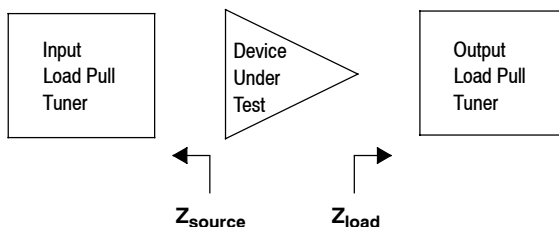


Figure 10. Load Pull Performance — Maximum P1dB Tuning

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1200 \text{ mA}$ , Pulsed CW,  $10 \mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	$\eta_D$ (%)	(dBm)	(W)	$\eta_D$ (%)
728	1.00 - j0.80	1.40 + j0.20	52.4	174	67.4	53.1	204	70.0
748	0.70 - j1.10	1.20 + j0.10	52.6	182	67.0	53.5	224	69.9
768	0.80 - j1.25	1.10 + j0.20	52.6	182	67.1	53.3	214	69.9

(1) Load impedance for optimum P1dB efficiency.

$Z_{\text{source}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Impedance as measured from drain contact to ground.

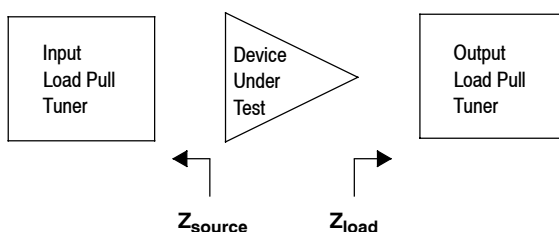
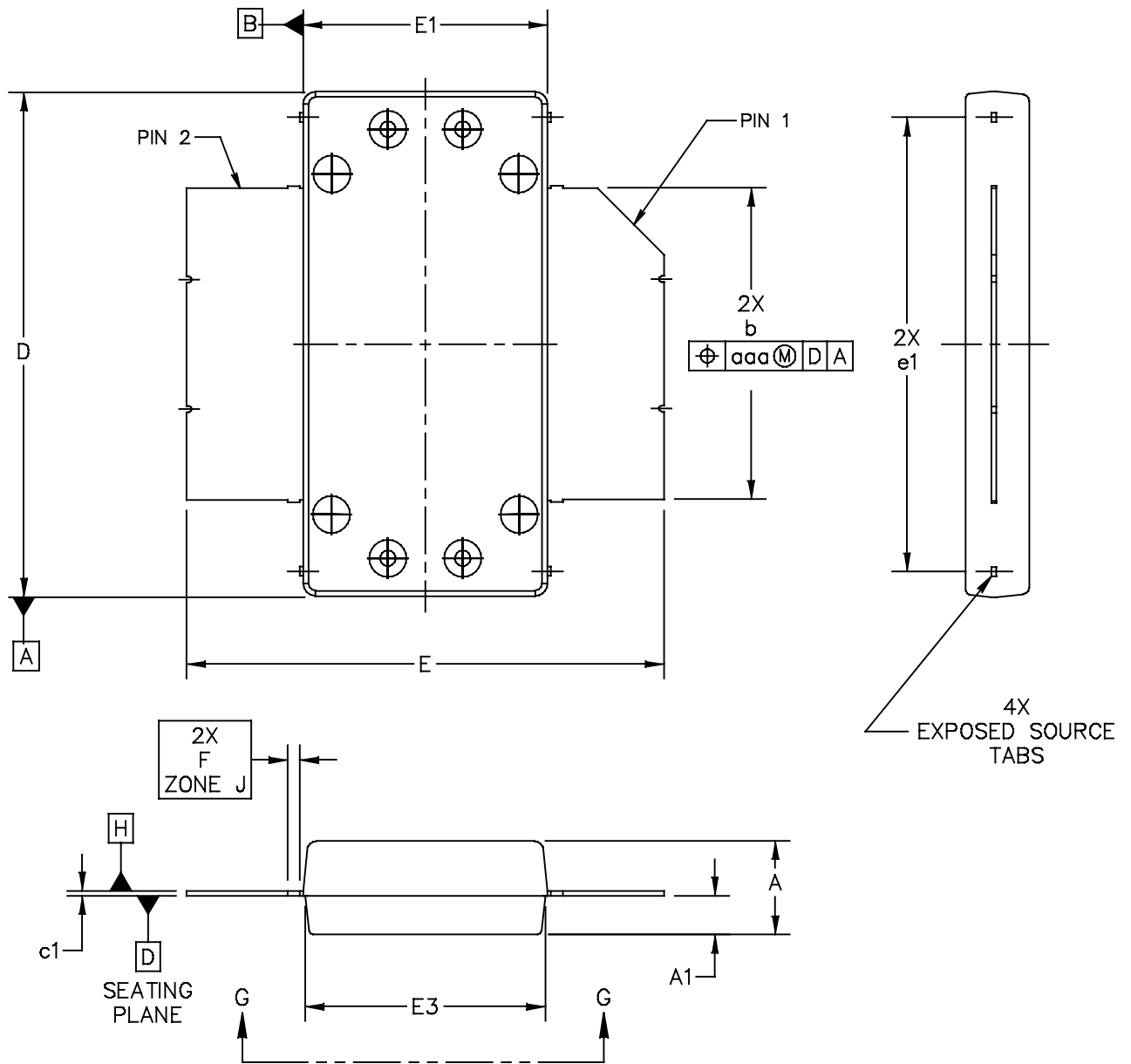


Figure 11. Load Pull Performance — Maximum Drain Efficiency Tuning

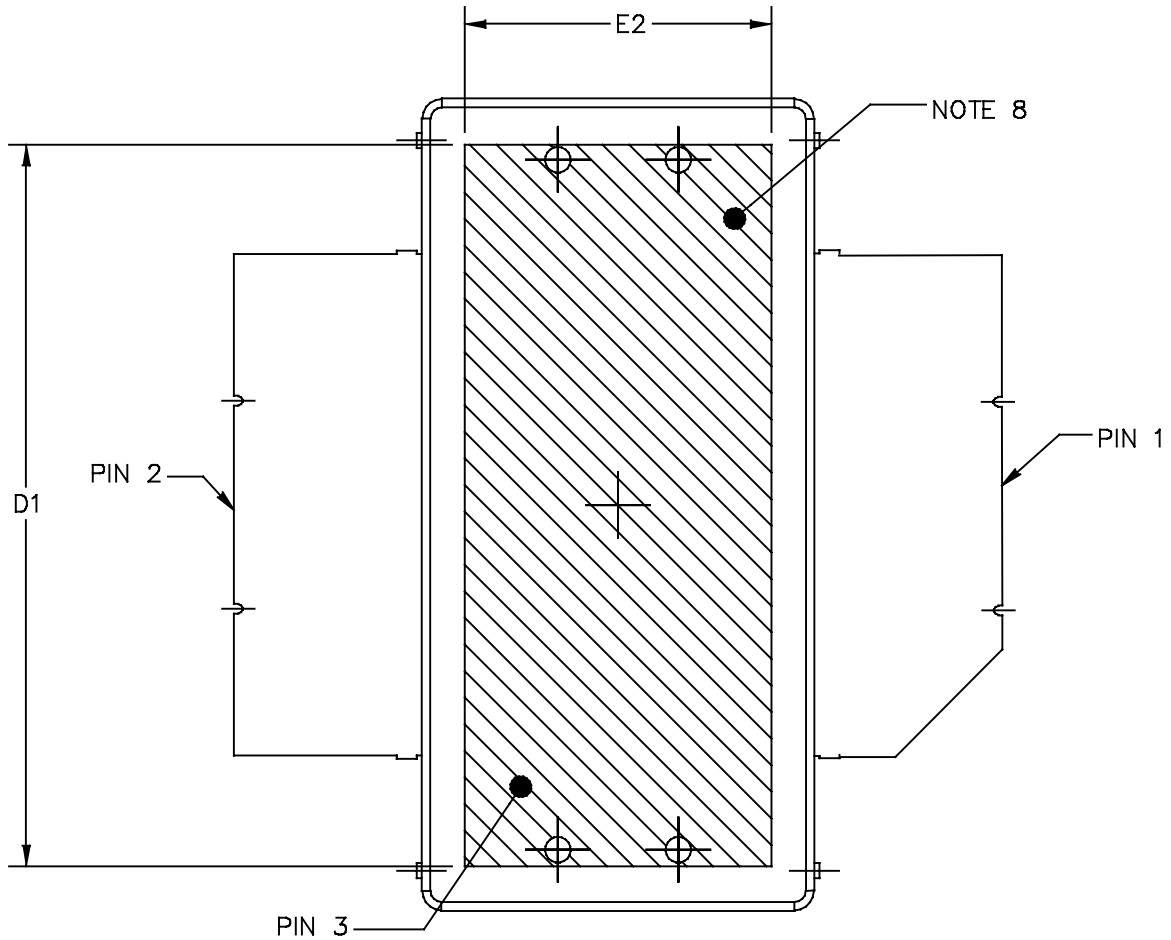


### PACKAGE DIMENSIONS



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	CASE NUMBER: 2021-03	22 OCT 2009	
	STANDARD: NON-JEDEC		

MRF8S7235NR3



BOTTOM VIEW  
VIEW G-G

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	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:  
 PIN 1 - DRAIN  
 PIN 2 - GATE  
 PIN 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

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		STANDARD: NON-JEDEC	

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

### Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2012	• Initial Release of Data Sheet

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