Freescale Semiconductor
Technical Data

Document Number: MML20242H
Rev. 0, 10/2012

RoHS

Enhancement Mode pHEMT Technology (E-pHEMT)

Low Noise Amplifier

MML20242HT1

1400-2800 MHz, 34 dB
24 dBm, 0.57 NF
E-pHEMT

CASE 2131-01
QFN 3x3
PLASTIC

The MML20242H is a 2-stage low noise amplifier (LNA) with active bias and high isolation for use in cellular infrastructure applications. It is designed for a range of low noise, high linearity applications such as picocell, femtocell, tower mounted amplifiers (TMA) and receiver front end circuits. It operates from a single voltage supply and is suitable for applications with frequencies from 1400 to 2800 MHz such as TD-SCDMA, W-CDMA, UMTS, PCS, LTE and BWA.

Features

- Low Noise Figure: 0.57 dB @ 1950 MHz
- Frequency: 1400-2800 MHz
- Unconditionally Stable over Temperature
- High Reverse Isolation: -51 dB @ 1950 MHz
- P1dB: 24 dBm @ 1950 MHz
- Small-Signal Gain: 34 dB @ 1950 MHz (adjustable externally)
- Third Order Output Intercept Point: 39.5 dBm @ 1950 MHz
- Active Bias Control (adjustable externally)
- Single 5 Volt Supply
- Supply Current: 160 mA
- 50 Ohm Operation (some external matching required)
- Cost-effective QFN Surface Mount Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7 inch Reel.

Table 1. Typical Performance (1)

Characteristic	Symbol	1400 MHz	1950 MHz	2800 MHz	Unit
Noise Figure (2)	NF	0.55	0.57	0.89	dB
Input Return Loss (S11)	IRL	-15	-18	-18	dB
Output Return Loss (S22)	ORL	-14	-15	-15	dB
Small-Signal Gain (S21)	G_p	38	34	31.5	dB
Power Output @ 1dB Compression	P1dB	23.5	24	24	dBm
Third Order Input Intercept Point	IIP3	1	5.5	8	dBm
Third Order Output Intercept Point	OIP3	39	39.5	39.5	dBm

1. V_{DD} = 5 Vdc, T_A = 25°C, 50 ohm system, application circuit tuned for specified frequency.
2. Noise Figure value calculated with connector losses removed.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Supply Current	I_{DD}	300	mA
RF Input Power	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature (3)	T_J	150	°C

3. For reliable operation, the junction temperature should not exceed 150°C.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (4)	Unit
Thermal Resistance, Junction to Case Case Temperature 95°C, 5 Vdc, 163 mA, no RF applied	$R_{\theta JC}$	40	°C/W

4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 4. Electrical Characteristics (V_{DD} = 5 Vdc, 2140 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21)	G_p	30.6	32.5	—	dB
Input Return Loss (S11)	IRL	—	-18	—	dB
Output Return Loss (S22)	ORL	—	-15	—	dB
Power Output @ 1dB Compression	P1dB	—	24	—	dBm
Third Order Input Intercept Point	IIP3	—	7	—	dBm
Third Order Output Intercept Point	OIP3	—	39.5	—	dBm
Reverse Isolation (S12)	|S12|	—	-50	—	dBm
Noise Figure (1)	NF	—	0.7	—	dB
Supply Current (2,3)	I_{DD}	117	160	207	mA
Supply Voltage (2)	V_{DD}	—	5	—	V

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	1	260	°C

1. Noise Figure value calculated with connector losses removed.
2. For reliable operation, the junction temperature should not exceed 150°C.
3. DC current measured with no RF signal applied.

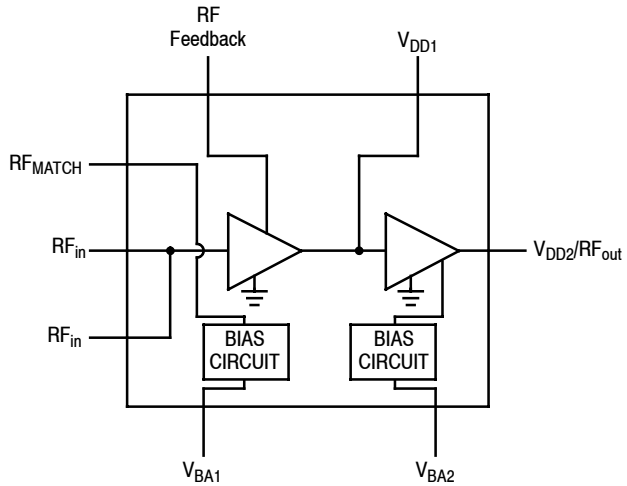
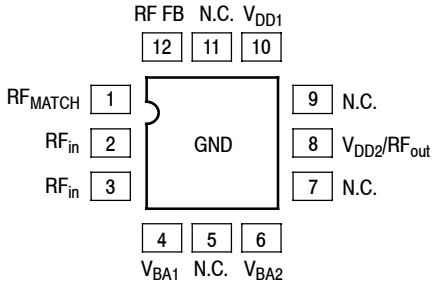


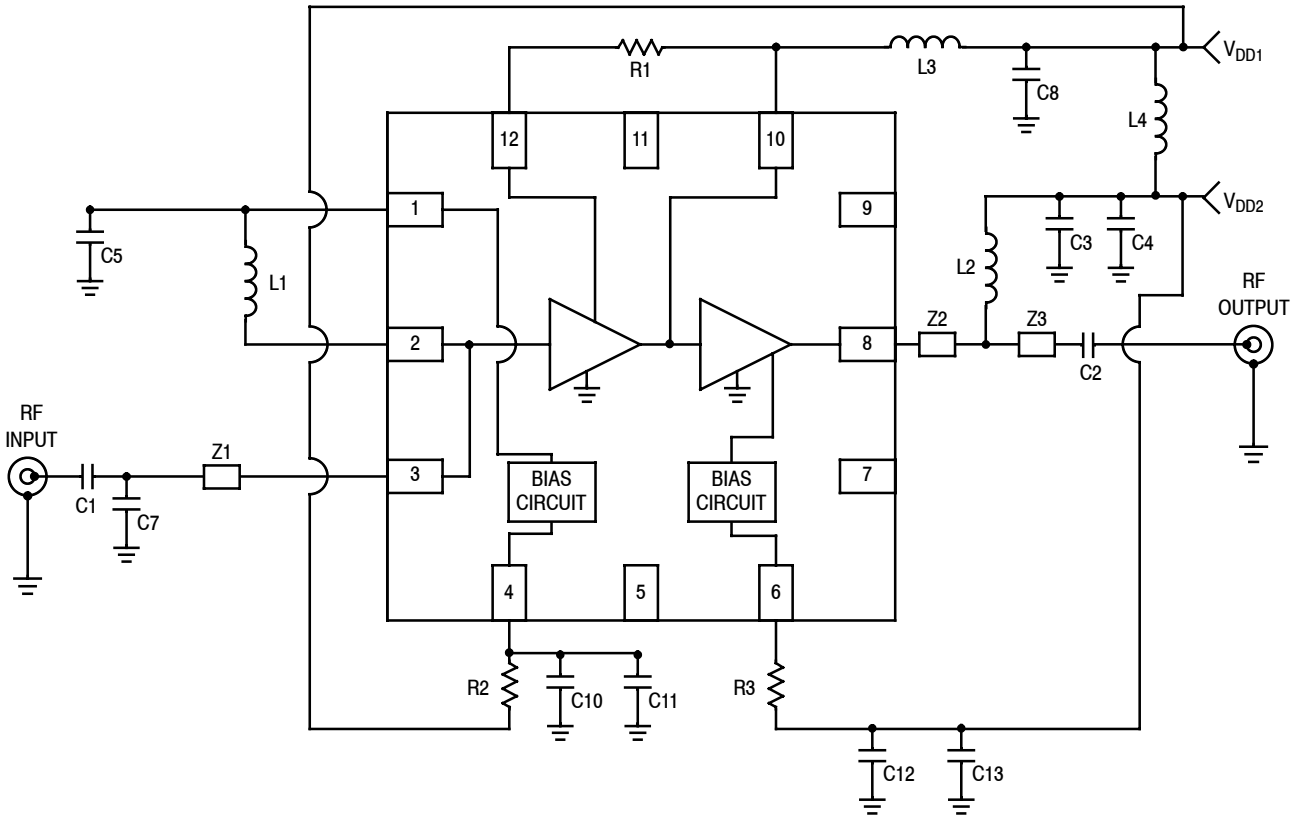
Figure 1. Functional Block Diagram



Note: Exposed backside of the package is DC and RF ground.

Figure 2. Pin Connections

50 OHM APPLICATION CIRCUIT: 1950 MHz



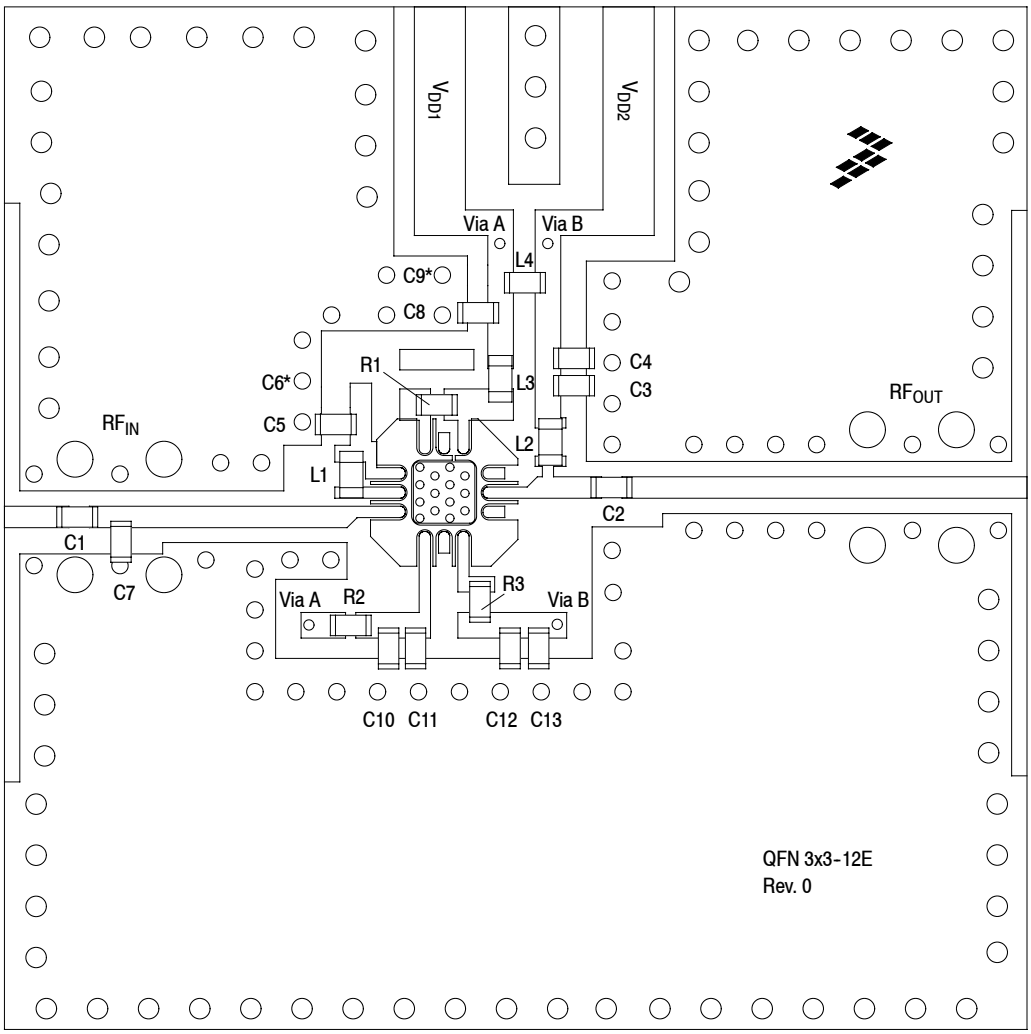
Z1 0.248″ × 0.021″ Microstrip
Z2 0.050″ × 0.021″ Microstrip
Z3 0.030″ × 0.021″ Microstrip

Figure 3. MML20242HT1 Test Circuit Schematic

Table 7. MML20242HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5	18 pF Chip Capacitors	GJM1555C1H180GB01	Murata
C2, C3, C8, C11, C12	18 pF Chip Capacitors	GRM1555C1H180JA01	Murata
C4, C10, C13	0.1 μF Chip Capacitors	GRM155R61A104K01	Murata
C6, C9	Components Not Used		
C7	0.6 pF Chip Capacitor	GJM1555C1HR60WB01	Murata
L1	3.3 nH Chip Inductor	0402HP-3N3XJLW	Coilcraft
L2, L4	10 nH Chip Inductors	0402CS-10NXJLW	Coilcraft
L3	2.2 nH Chip Inductor	0402CS-2N2XJLW	Coilcraft
R1	180 Ω Chip Resistor	RC0402FR-07-180RL	Yageo
R2, R3	1200 Ω Chip Resistors	RC0402FR-07-1K2RL	Yageo
PCB	0.010″, ε_r = 3.48, Multilayer	RO4350B	Rogers

50 OHM APPLICATION CIRCUIT: 1950 MHz



*C6 and C9 components are not used.

Figure 4. MML20242HT1 Test Circuit Component Layout

Table 7. MML20242HT1 Test Circuit Component Designations and Values

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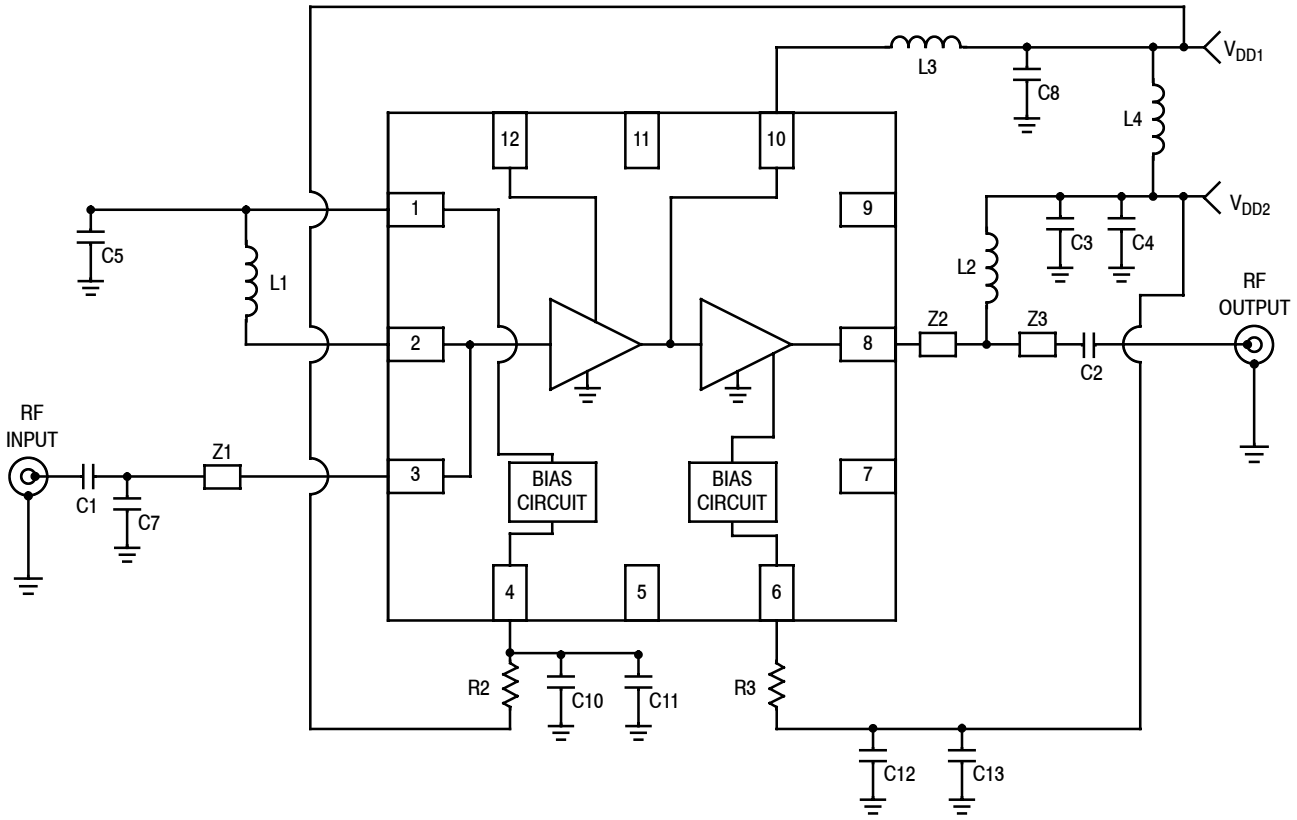
C4, C10, C13	0.1 μF Chip Capacitors	GRM155R61A104K01	Murata
C6, C9	Components Not Used		
C7	0.6 pF Chip Capacitor	GJM1555C1HR60WB01	Murata
L1	3.3 nH Chip Inductor	0402HP-3N3XJLW	Coilcraft
L2, L4	10 nH Chip Inductors	0402CS-10NXJLW	Coilcraft
L3	2.2 nH Chip Inductor	0402CS-2N2XJLW	Coilcraft
R1	180 Ω Chip Resistor	RC0402FR-07-180RL	Yageo
R2, R3	1200 Ω Chip Resistors	RC0402FR-07-1K2RL	Yageo
PCB	0.010″, ε_r = 3.48, Multilayer	RO4350B	Rogers

(Test Circuit Component Designations and Values repeated for reference.)

50 OHM APPLICATION CIRCUIT: 2535 MHz



Z1 0.248″ × 0.021″ Microstrip
Z2 0.050″ × 0.021″ Microstrip
Z3 0.030″ × 0.021″ Microstrip

Figure 5. MML20242HT1 Test Circuit Schematic

Table 8. MML20242HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
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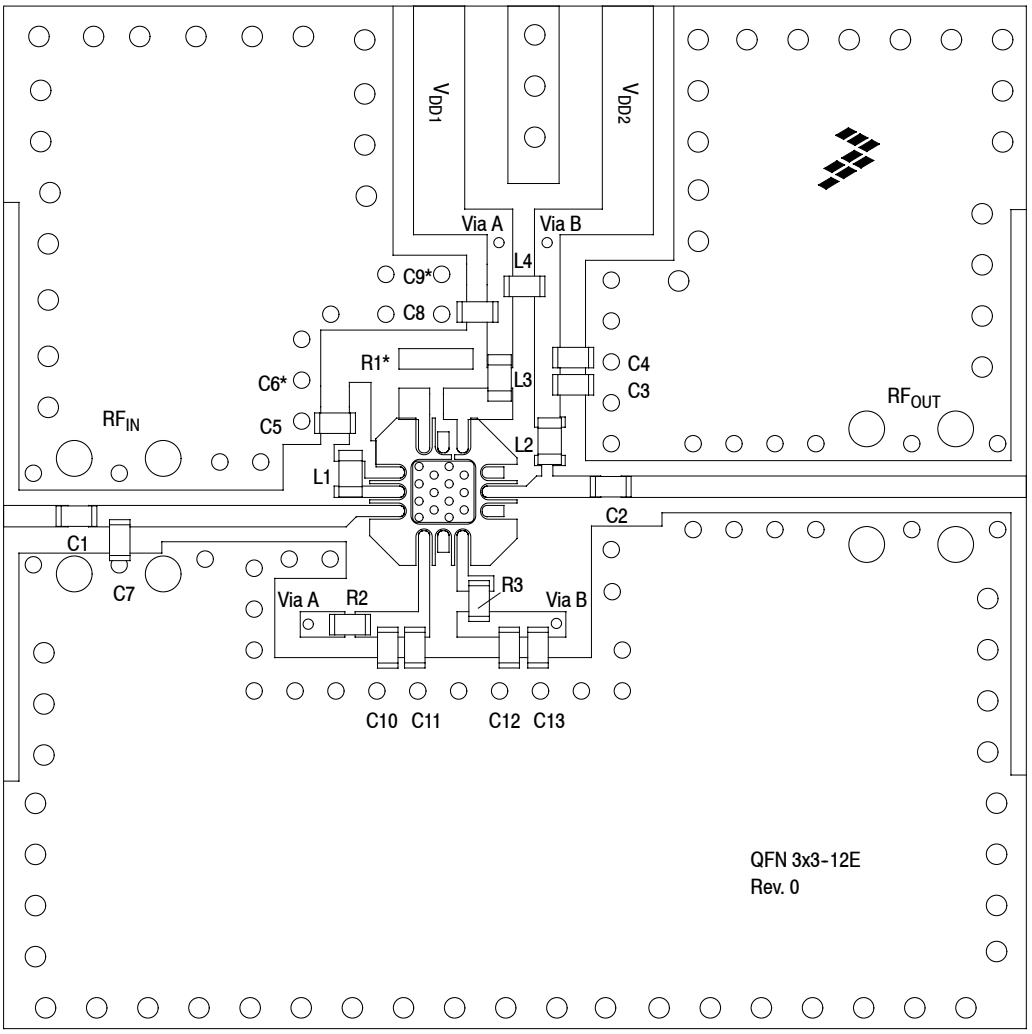
C4, C10, C13	0.1 μF Chip Capacitors	GRM155R61A104K01	Murata
C6, C9	Components Not Used		
C7	0.6 pF Chip Capacitor	GJM1555C1HR60WB01	Murata
L1	2.7 nH Chip Inductor	0402HP-2N7XJLW	Coilcraft
L2, L4	6.8 nH Chip Inductors	0402CS-6N8XJLW	Coilcraft
L3	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
R1	Component Not Used		
R2, R3	1200 Ω Chip Resistors	RC0402FR-07-1K2RL	Yageo
PCB	0.010″, ε_r = 3.48, Multilayer	RO4350B	Rogers

50 OHM APPLICATION CIRCUIT: 2535 MHz



*C6, C9 and R1 components are not used.

Figure 6. MML20242HT1 Test Circuit Component Layout

Table 8. MML20242HT1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5	18 pF Chip Capacitors	GJM1555C1H180GB01	Murata
C2, C3, C8, C11, C12	18 pF Chip Capacitors	GRM1555C1H180JA01	Murata
C4, C10, C13	0.1 μF Chip Capacitors	GRM155R61A104K01	Murata
C6, C9	Components Not Used		
C7	0.6 pF Chip Capacitor	GJM1555C1HR60WB01	Murata
L1	2.7 nH Chip Inductor	0402HP-2N7XJLW	Coilcraft
L2, L4	6.8 nH Chip Inductors	0402CS-6N8XJLW	Coilcraft
L3	1.0 nH Chip Inductor	0402CS-1N0XJLW	Coilcraft
R1	Component Not Used		
R2, R3	1200 Ω Chip Resistors	RC0402FR-07-1K2RL	Yageo
PCB	0.010″, ε_r = 3.48, Multilayer	RO4350B	Rogers

(Test Circuit Component Designations and Values repeated for reference.)

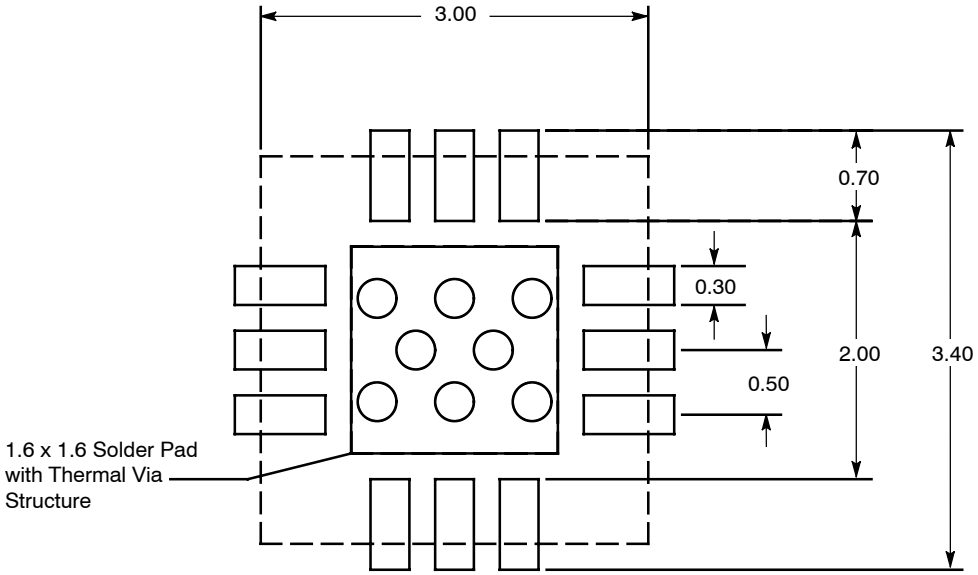
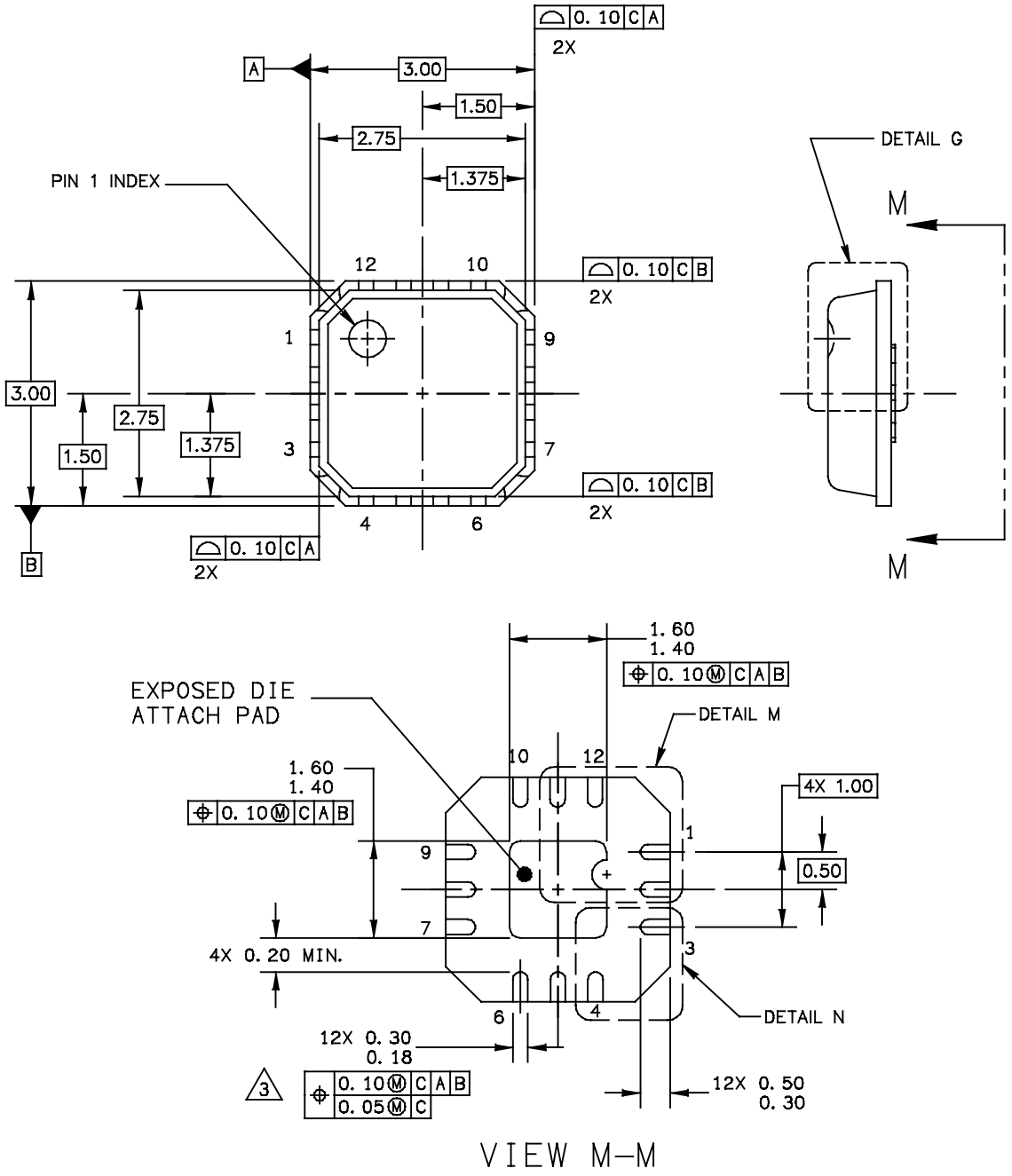


Figure 7. PCB Pad Layout for QFN 3x3

Figure 8. Product Marking

PACKAGE DIMENSIONS



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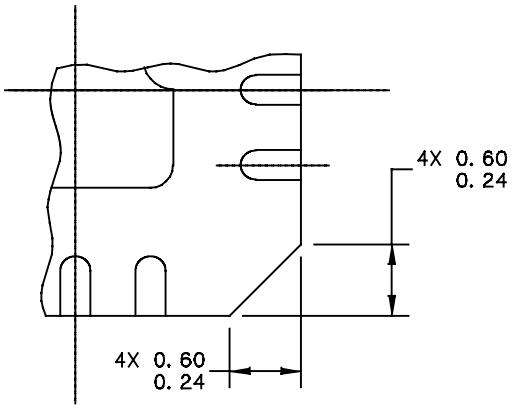
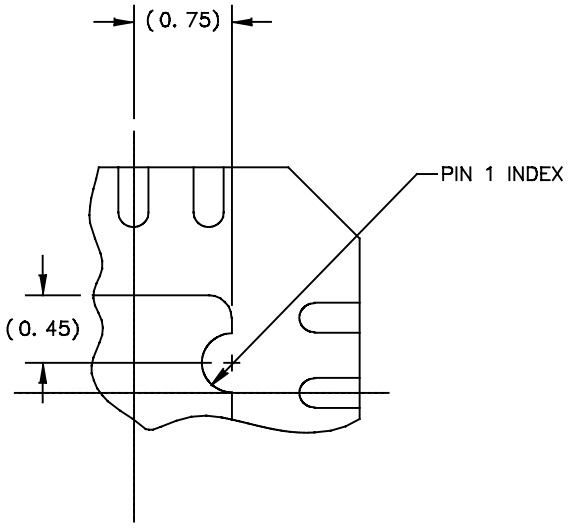
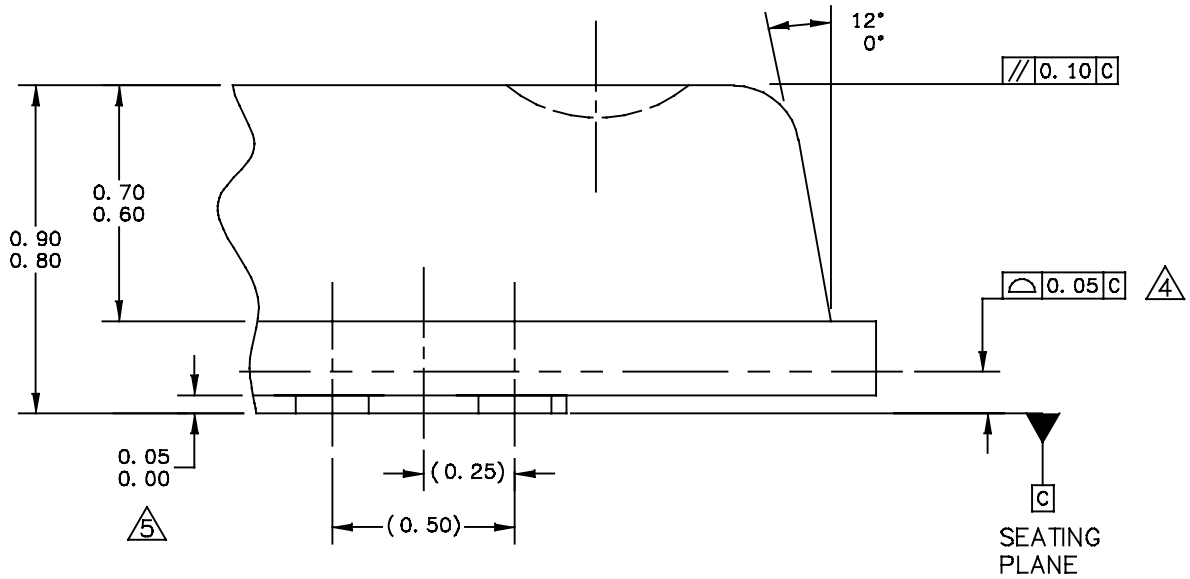
	CASE NUMBER: 2131–01	14 MAY 2010
	STANDARD: NON–JEDEC	



DETAIL N
CORNER CONFIGURATION



DETAIL M
PIN 1 BACKSIDE INDEX



DETAIL G
VIEW ROTATED 90° CW

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NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.

3. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

5. THIS DIMENSION APPLIED ONLY FOR TERMINALS.

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3100: General Purpose Amplifier and MMIC Biasing

Software

- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2012	• Initial Release of Data Sheet

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