

Features

- Fast access time: 15 ns
- Wide voltage range: 5.0 V ± 10% (4.5 V to 5.5 V)
- CMOS for optimum speed and power
- TTL compatible inputs and outputs
- Available in 24-pin DIP and 24-pin SOJ

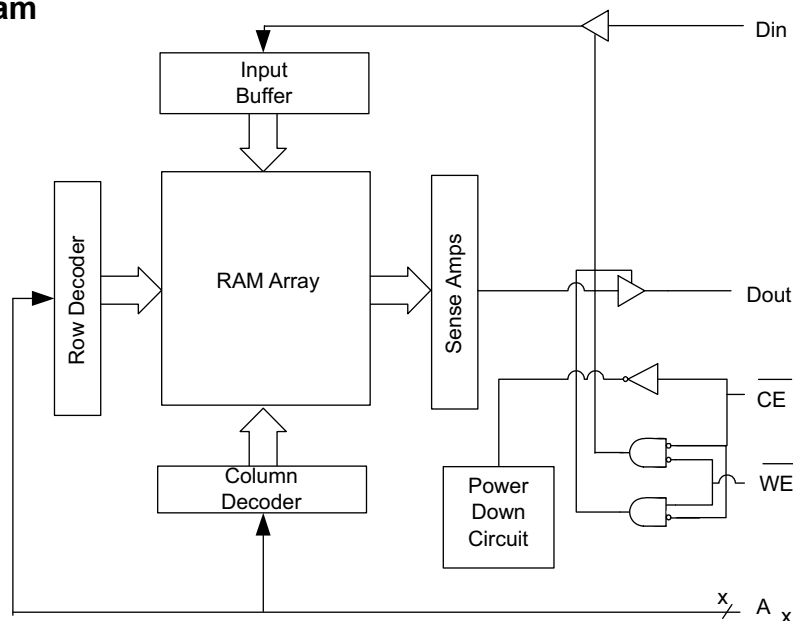
General Description ^[1]

The CY7C197BN is a high performance CMOS Asynchronous SRAM organized as 256 K × 1 bits that supports an asynchronous memory interface. The device features an automatic power down feature that significantly reduces power consumption when deselected.

See the [Truth Table on page 8](#) for a complete description of Read and Write modes.

The CY7C197BN is available in 24-pin DIP and 24-pin SOJ package(s).

Logic Block Diagram



Product Portfolio

Description	-15	-25	Unit
Maximum Access Time	15	25	ns
Maximum Operating Current	150	95	mA
Maximum CMOS Standby Current	10	10	mA

Note

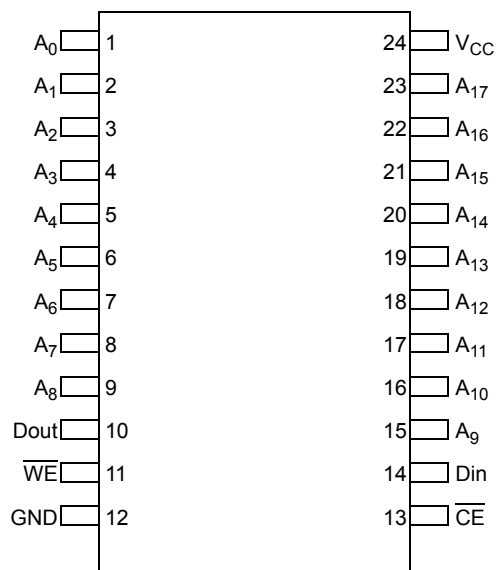
1. For best practice recommendations, refer to the Cypress application note [System Design Guidelines on www.cypress.com](#).

Contents

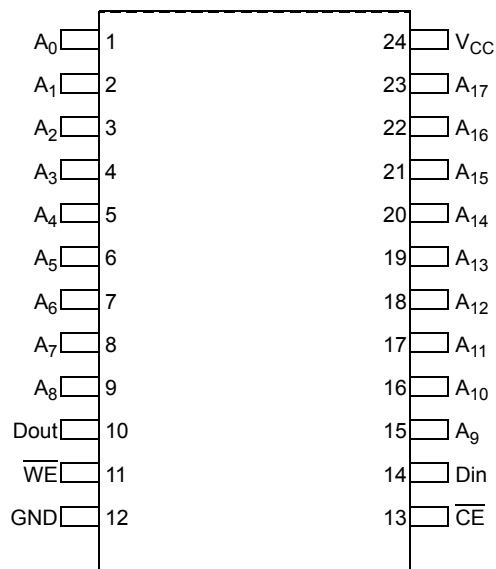
Pin Layout and Specification	3	Truth Table	8
Pin Description	3	Ordering Information	9
Maximum Ratings	4	Ordering Code Definitions	9
Operating Range	4	Package Diagrams	10
DC Electrical Characteristics	4	Acronyms	11
Capacitance	4	Document Conventions	11
Thermal Resistance	4	Units of Measure	11
AC Test Loads	5	Document History Page	12
AC Test Conditions	5	Sales, Solutions, and Legal Information	13
AC Electrical Characteristics	6	Worldwide Sales and Design Support	13
Timing Waveforms	6	Products	13
Read Cycle No. 1	6	PSoC Solutions	13
Read Cycle No. 2	7		
Write Cycle No. 1 ($\overline{WE}$ Controlled)	7		
Write Cycle No. 2 ($\overline{CE}$ Controlled)	8		

Pin Layout and Specification

24-pin DIP (6.6 × 31.8 × 3.5 mm)



24-pin SOJ (8 × 15 × 3.5 mm)



Pin Description

Pin	Type	Description	DIP	SOJ
A _x	Input	Address Inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 18, 19, 20, 21, 22, 23
$\overline{\text{CE}}$	Control	Chip Enable	13	13
Din	Input	Data Input Pins	14	14
Dout	Output	Data Output Pins	10	10
V _{CC}	Supply	Power (5.0 V)	24	24
$\overline{\text{WE}}$	Control	Write Enable	11	11

Maximum Ratings

Exceeding the maximum rating may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND -0.5 V to +7.0 V

DC Voltage Applied to Outputs
in High Z State^[2] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....2001 V
(per MIL-STD-883, Method 3015)

Latch Up Current > 200 mA

Operating Range

Range	Ambient Temperature ^[3]	V_{CC}
Commercial	0 °C to 70 °C	5.0 V ± 10%

DC Electrical Characteristics^[2]

Parameter	Description	Condition	15 ns		25 ns		Unit
			Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	—	0.4	—	0.4	V
I_{OZ}	Output Leakage Current	$GND \leq V_i \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	µA
I_{IX}	Input Leakage Current	$GND \leq V_i \leq V_{CC}$	-5	+5	-5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = F_{MAX} = 1/t_{RC}$	—	150	—	95	mA
I_{SB1}	Automatic $\overline{CE}$ Power Down Current TTL Inputs	$V_{CC} = \text{Max}, \overline{CE} \geq V_{IH}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = F_{MAX}$	—	30	—	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power Down Current CMOS Inputs	$V_{CC} = \text{Max}, \overline{CE} \geq V_{CC} - 0.3 \text{ V}, V_{IN} \geq V_{CC} - 0.3 \text{ V}$ or $V_{IN} < 0.3 \text{ V}, f = 0$	—	10	—	10	mA

Capacitance^[4]

Parameter	Description	Conditions	Max (ALL – PACKAGES)	Unit
C_{IN}	Input Capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	8	pF
C_{OUT}	Output Capacitance		10	

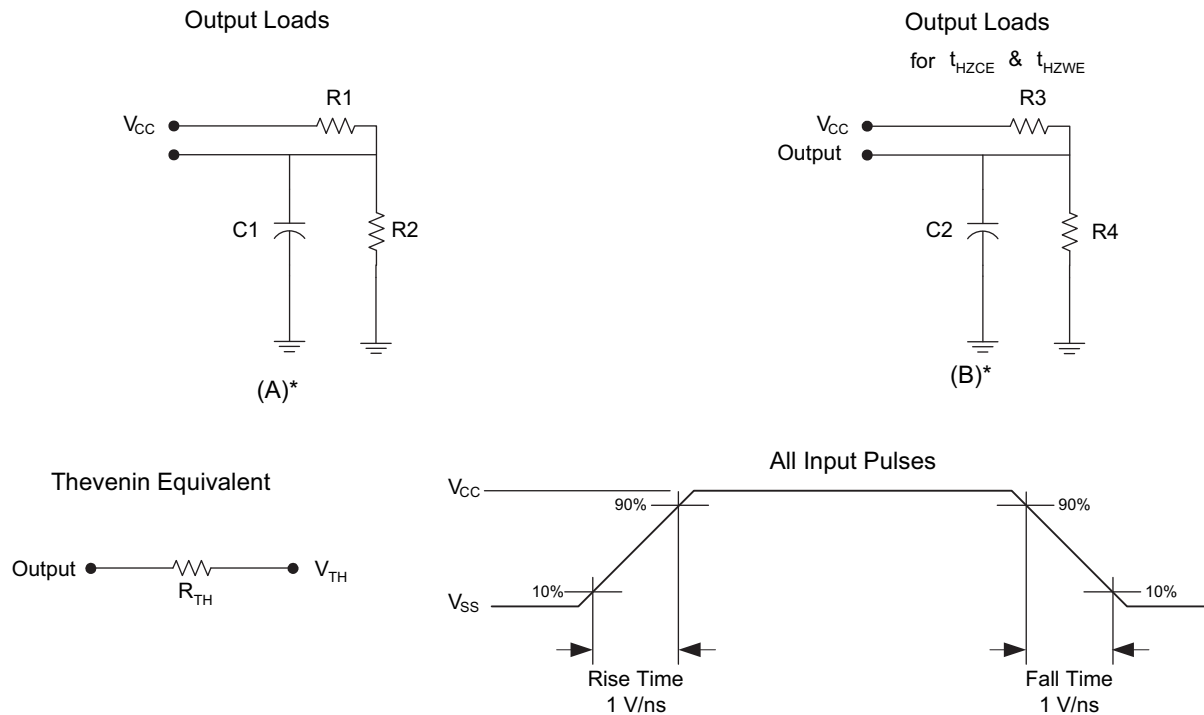
Thermal Resistance^[4]

Parameter	Description	Conditions	24-pin DIP	24-pin SOJ	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		33.80	37.56	

Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$ for pulse durations of less than 20 ns.
- T_A is the “instant on” case temperature.
- Tested initially and after any design or process change that may affect these parameters.

AC Test Loads^[5]



* including scope and jig capacitance

AC Test Conditions

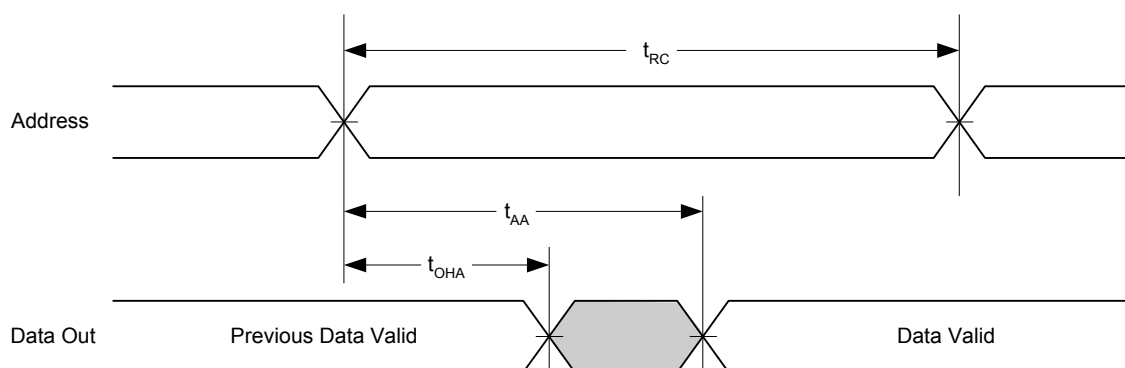
Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Note

5. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

AC Electrical Characteristics^[4, 6, 7, 8]

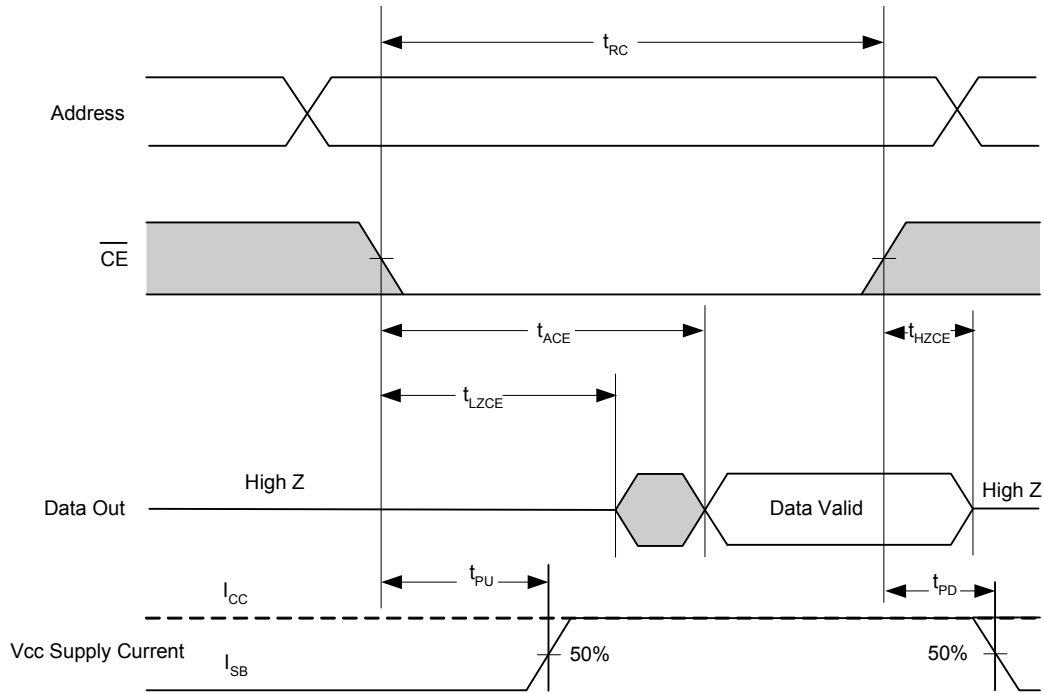
Parameter	Description	15 ns		25 ns		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15	–	25	–	ns
t_{AA}	Address to Data Valid	–	15	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	15	–	25	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	11	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	15	–	20	ns
t_{WC}	Write Cycle Time	15	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	20	–	ns
t_{AW}	Address Set-up to Write End	10	–	20	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	9	–	20	–	ns
t_{SD}	Data Set-Up to Write End	9	–	15	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	11	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2	–	3	–	ns

Timing Waveforms
Read Cycle No. 1 ^[9, 10]

Notes

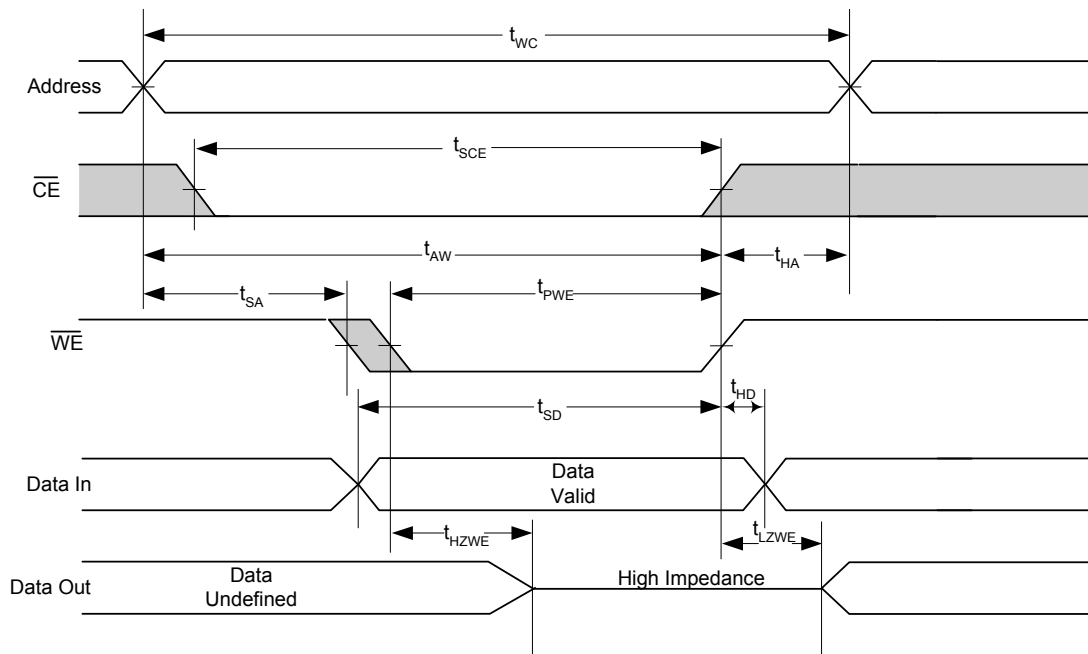
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. t_{HZCE} , t_{HZWE} are specified as in part (b) of the [AC Test Loads](#)^[5] on page 5. Transitions are measured ± 200 mV from steady state voltage.
9. Device is continuously selected. $\overline{CE} = V_{IL}$.
10. $\overline{WE}$ is HIGH for Read Cycle.

Timing Waveforms (continued)

Read Cycle No. 2 [11, 12, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [11, 14]

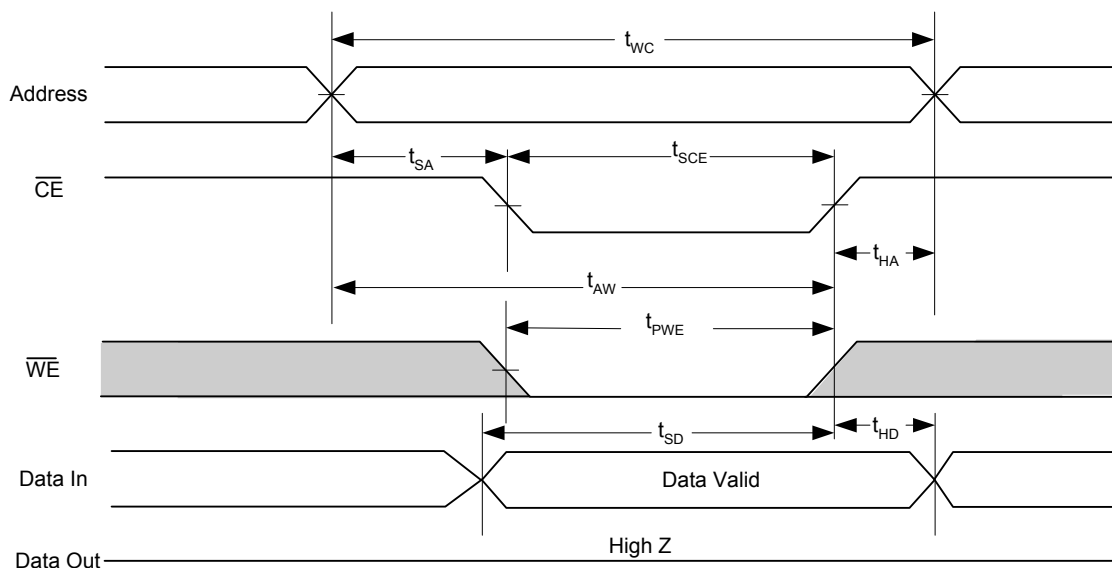


Notes

11. Tested initially and after any design or process change that may affect these parameters.
12. $\overline{WE}$ is HIGH in read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. The minimum write cycle time is the sum of t_{HZWE} and t_{SD} .

Timing Waveforms *(continued)*

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[15, 16]



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	I/Ox	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

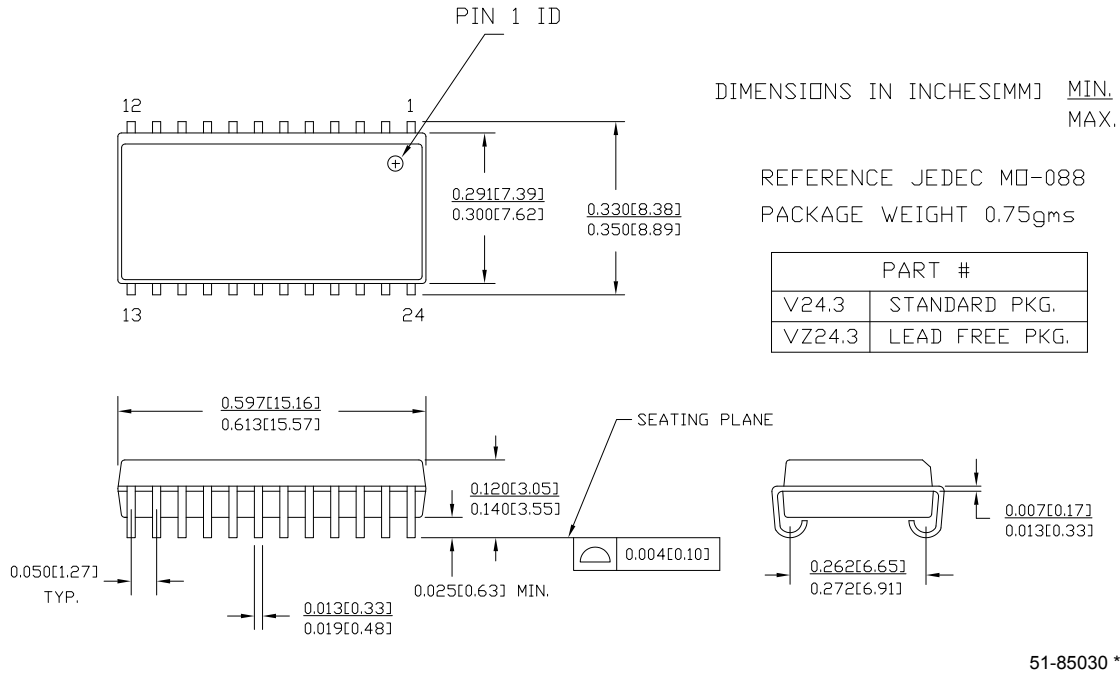
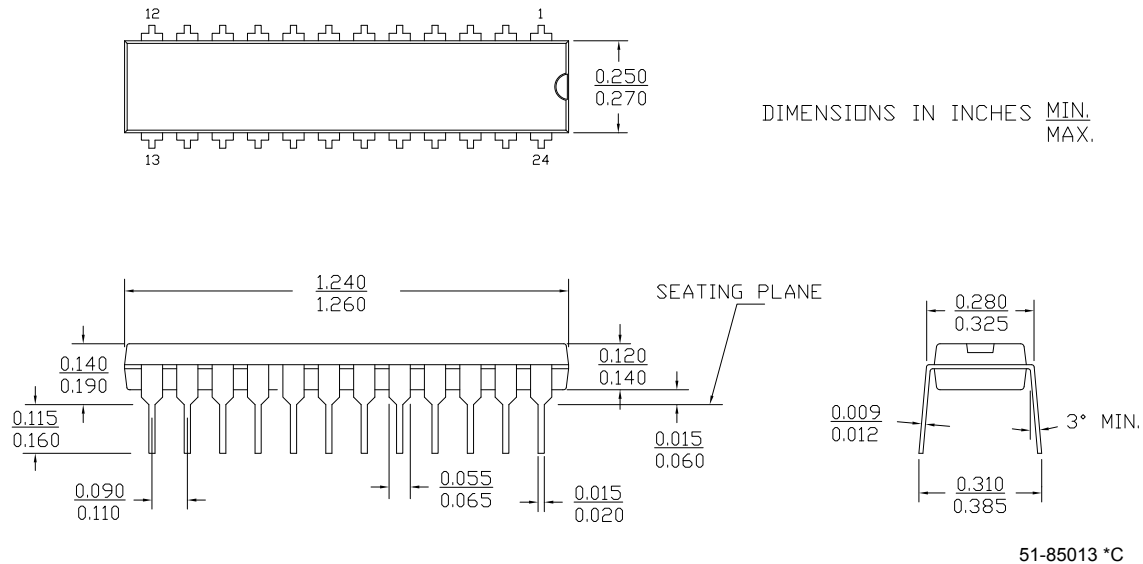
Notes

15. This cycle is $\overline{\text{CE}}$ controlled.

16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.



Package Diagrams

Figure 1. 24-pin (300-mil) SOJ, 51-85030

Figure 2. 24-pin DIP (6.6 × 31.8 × 3.5 mm), 51-85013


Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{\text{CE}}$	chip enable
DIP	dual in-line package
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
Ω	ohms
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
%	percent
$^{\circ}\text{C}$	degree Celcius

Document History Page

Document Title: CY7C197BN 256-Kb (256 K × 1) Static RAM Document Number: 001-06447				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	901742	See ECN	NXR	New Data Sheet
*A	2892510	03/18/2010	VKN	Removed 12ns speed bin Updated Ordering Information table Updated Package Diagrams Added Sales, Solutions, and Legal Information
*B	3108898	12/13/2010	AJU	Added Ordering Code Definitions .
*C	3217480	04/06/2011	PRAS	Added Acronyms and Units of Measure . Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2007-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.