CY7C1384D

18-Mbit (512 K × 32) Pipelined SRAM

Features

- Supports bus operation up to 166 MHz
- Available speed grades are 166 MHz
- Registered inputs and outputs for pipelined operation
- 3.3 V core power supply
- 2.5 V or 3.3 V I/O power supply
- Fast clock-to-output times
  - 3.4 ns (for 166 MHz device)
- Provides high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1384D is available in JEDEC-standard Pb-free 100-pin TQFP
- ZZ sleep mode option

Functional Description

The CY7C1384D SRAM integrates 524,288 × 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE_1}$), depth-expansion chip enables (CE_2 and $\overline{CE_3}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW_X}$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as they are controlled by the advance pin ($\overline{ADV}$).

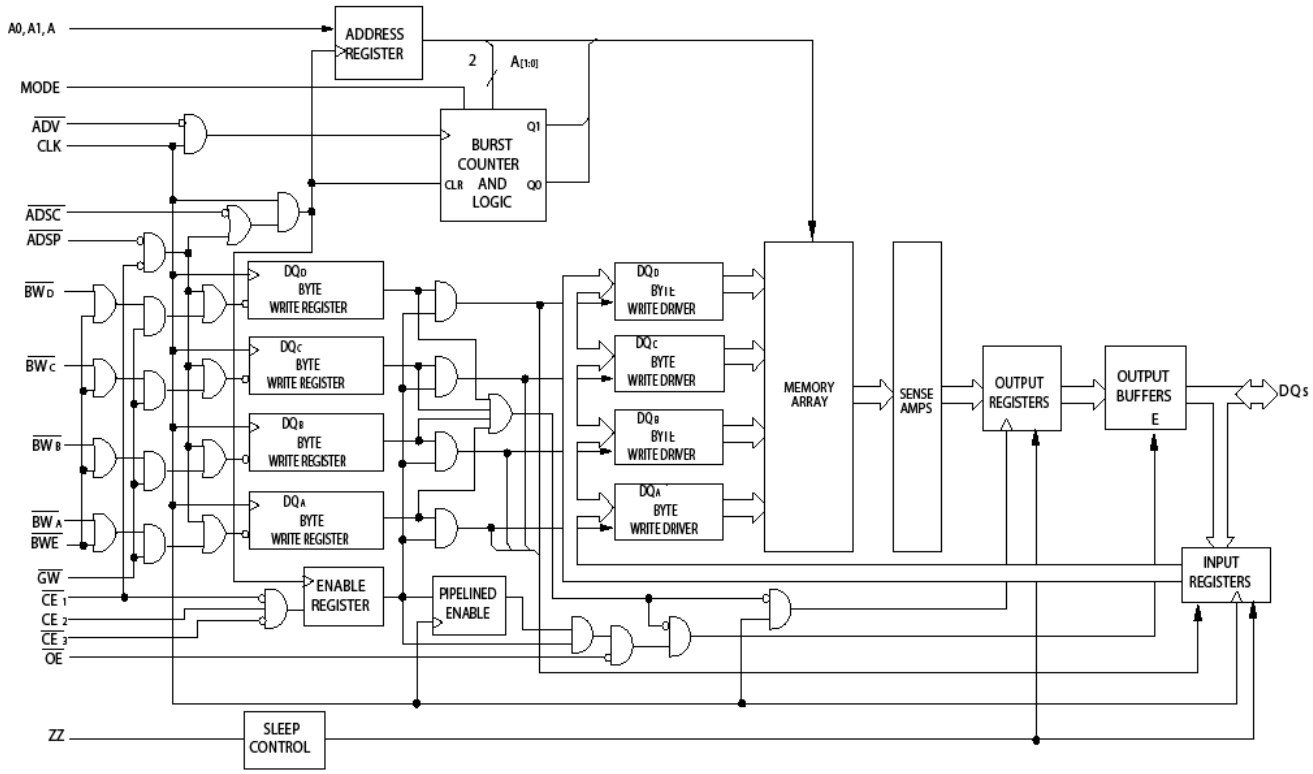
Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle.This part supports byte write operations (see Truth Table on page 7 for further details). Write cycles can be one to two or four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ when active LOW causes all bytes to be written.

The CY7C1384D operates from a +3.3 V core power supply while all outputs operate with a +2.5 or +3.3 V power supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

Selection Guide

Description	166 MHz	Unit
Maximum Access Time	3.4	ns
Maximum Operating Current	275	mA
Maximum CMOS Standby Current	70	mA

Logic Block Diagram – CY7C1384D

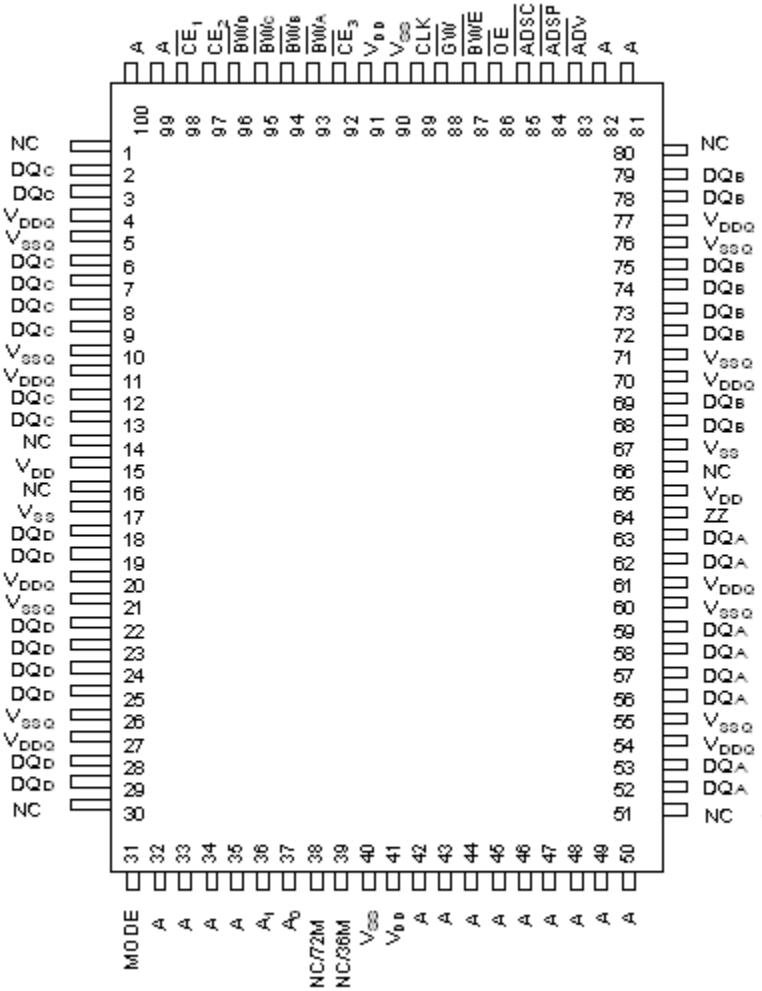


Contents

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enable)

CY7C1384D (512 K × 32)



Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.4 ns (166 MHz device).

CY7C1384D supports secondary cache in systems using a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence suits processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BWE}$) and byte write select ($\overline{BW_X}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is enabled to propagate to the input of the output registers. At the rising edge of the next clock, the data is enabled to propagate through the output register and onto the data bus within 3.4 ns (166 MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state; its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tri-states immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW and (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW_X}$ signals.

CY7C1384D provides byte write capability that is described in the write cycle descriptions table. Asserting the byte write enable input ($\overline{BWE}$) with the selected byte write ($\overline{BW_X}$) input, selectively writes to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

CY7C1384D is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deserted HIGH, (3) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

CY7C1384D is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

CY7C1384D provides a two-bit wraparound counter, fed by A1:A0, that implements an interleaved or a linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles

are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or VDD)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V	–	80	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The Truth Table for this data sheet follows. [1, 2, 3, 4, 5]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-state
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-state
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-state
WRITE Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
READ Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-state
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-state
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-state
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-state
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-state
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

1. X = Don't Care, H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more byte write enable signals, and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1384D follows. [6, 7]

Function (CY7C1384D)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A)	H	L	H	H	H	L
Write Byte B – (DQ_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes
6. X = Don't Care, H = Logic HIGH, L = Logic LOW.
7. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write is done based on which byte write is active.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. For user guidelines, not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.3 V to +V_{DD}

DC Voltage Applied to Outputs in tri-state .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....> 2001 V

Latch-up Current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [8]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [8]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	6.0-ns cycle, 166 MHz	–	275	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}	6.0-ns cycle, 166 MHz	–	140	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	All speeds	–	70	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = f_{MAX} = 1/t_{CYC}	6.0-ns cycle, 166 MHz	–	125	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speeds	–	80	mA

Notes
8. Overshoot: $V_{IH(AC)}$ < V_{DD} +1.5 V (pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than t_{CYC}/2).
9. TPower up: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

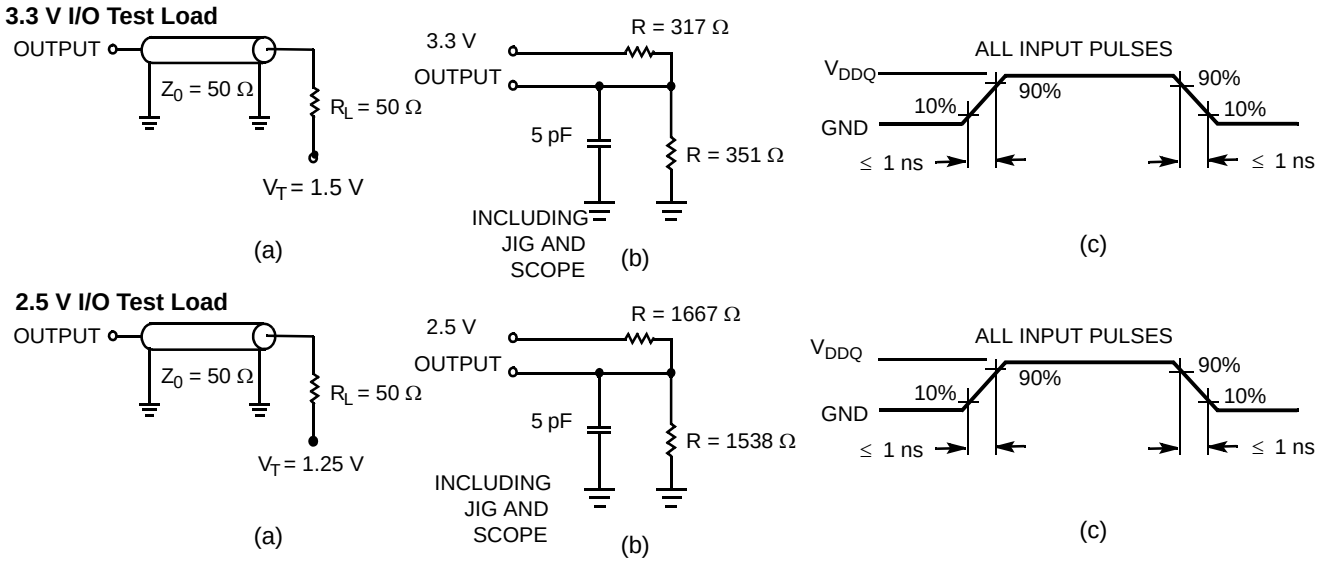
Parameter [10]	Description	Test Conditions	100-pin TQFP Package	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock Input Capacitance		5	pF
C_{IO}	Input/Output Capacitance		5	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
10. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

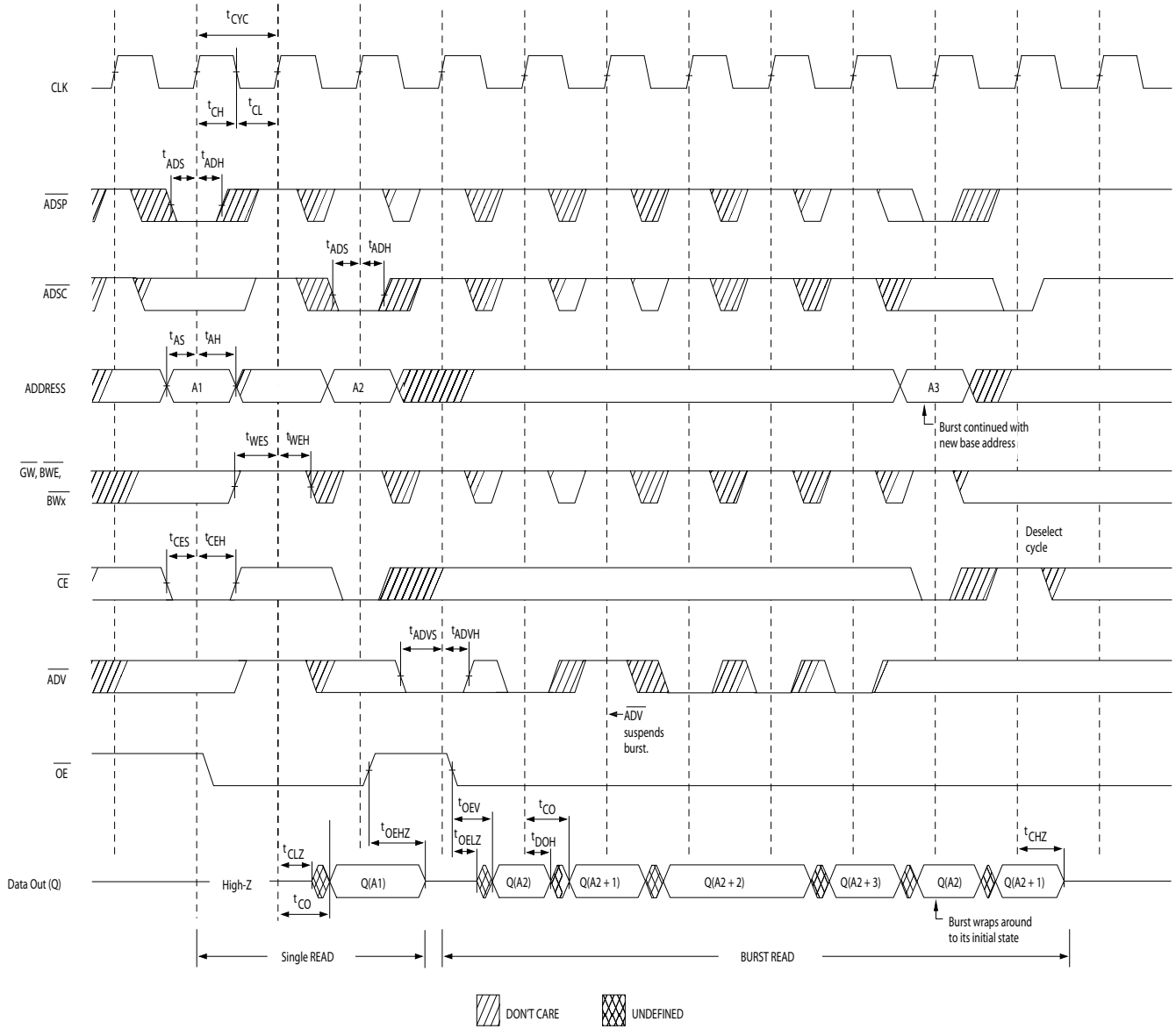
Parameter [11, 12]	Description	166 MHz		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [13]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	6	–	ns
t_{CH}	Clock HIGH	2.2	–	ns
t_{CL}	Clock LOW	2.2	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.3	–	ns
t_{CLZ}	Clock to low Z [14, 15, 16]	1.3	–	ns
t_{CHZ}	Clock to high Z [14, 15, 16]	–	3.4	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.4	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [14, 15, 16]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [14, 15, 16]	–	3.4	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ setup before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CES}	Chip enable setup before CLK rise	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

11. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
12. Test conditions shown in (a) of Figure 2 on page 10 unless otherwise noted.
13. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
14. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 10. Transition is measured ±200 mV from steady-state voltage.
15. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

Switching Waveforms

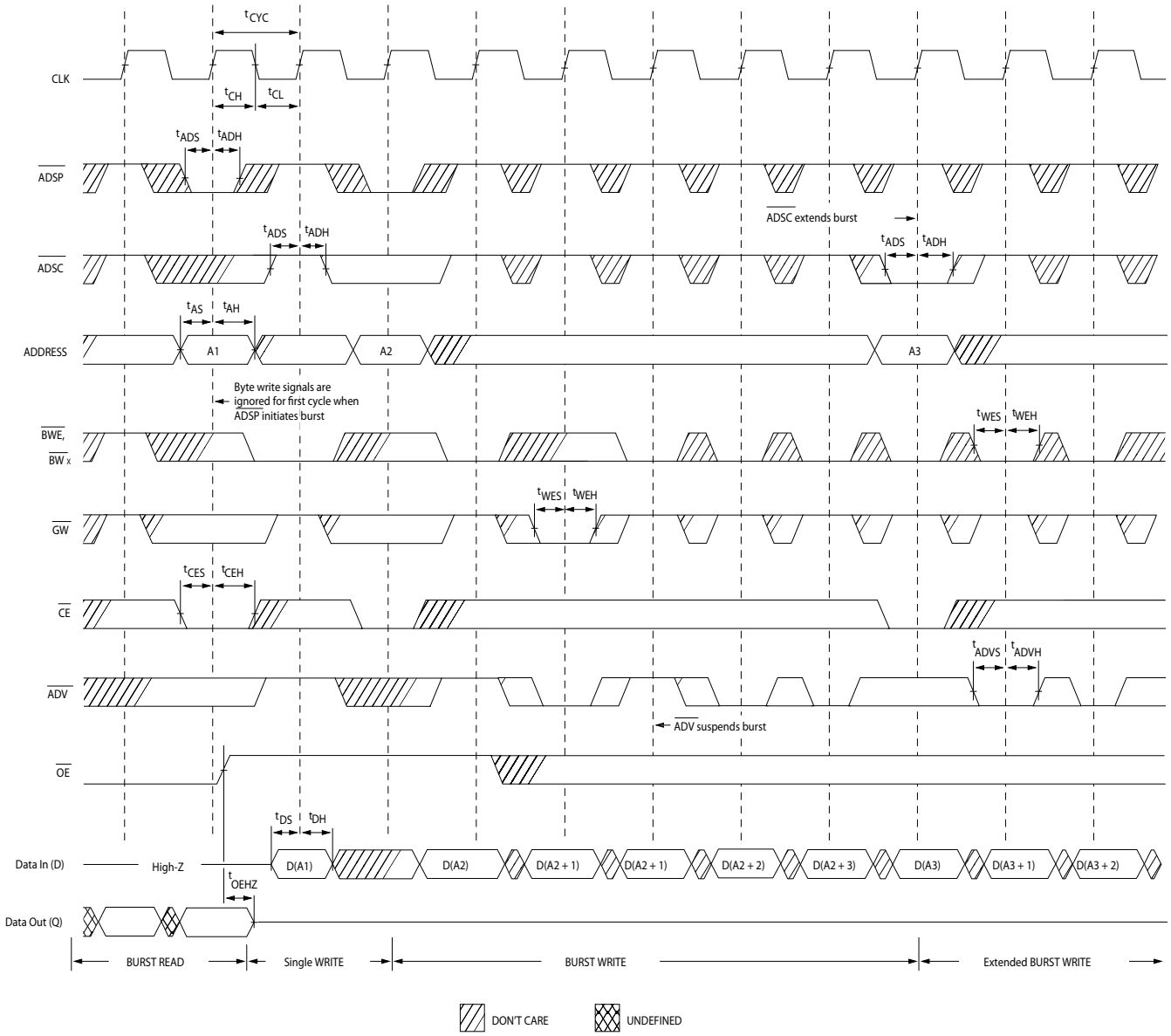
Figure 3. Read Cycle Timing [17]



Note
17. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms *(continued)*

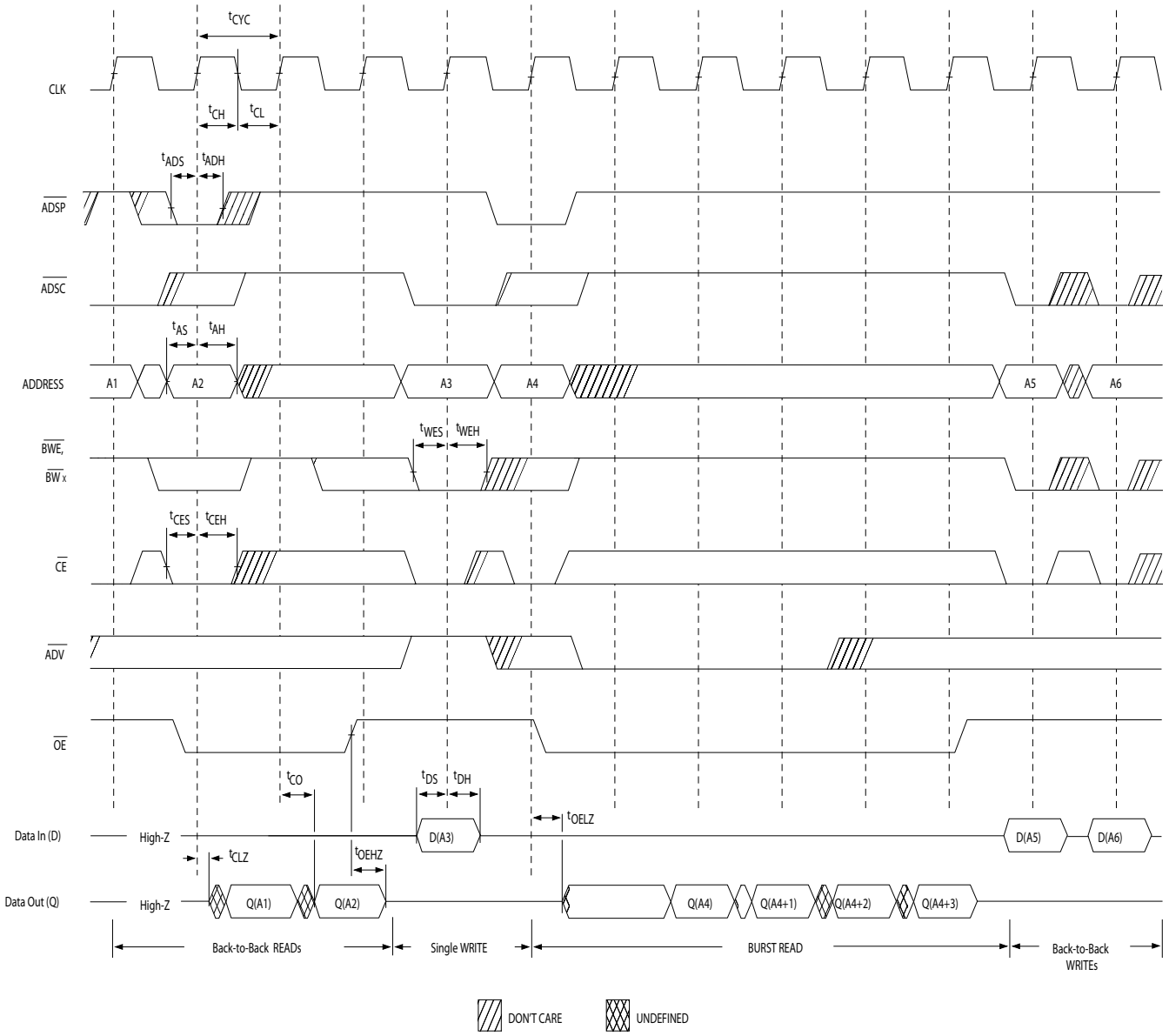
Figure 4. Write Cycle Timing [18, 19]



Notes
18. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
19. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Switching Waveforms *(continued)*

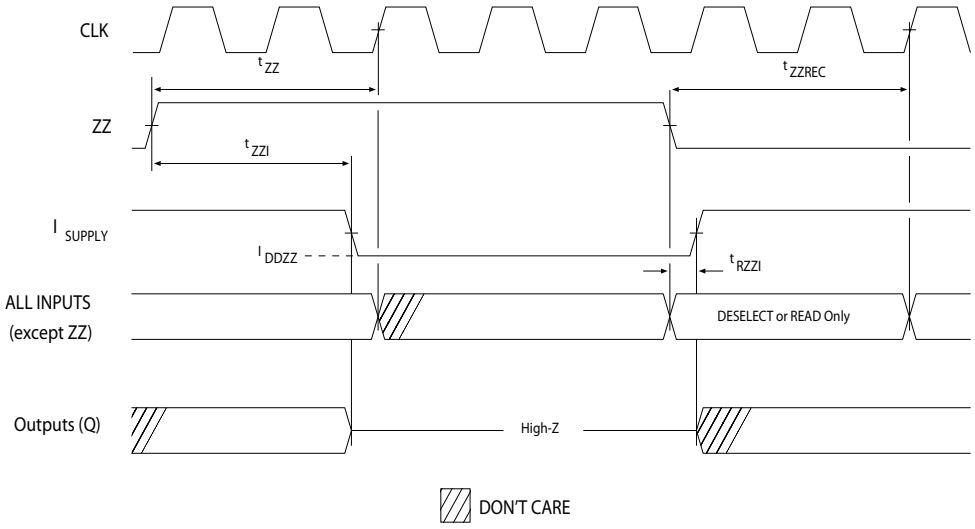
Figure 5. Read/Write Cycle Timing [20, 21, 22]



Notes
20. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
21. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
22. $\overline{GW}$ is HIGH.

Switching Waveforms *(continued)*

Figure 6. ZZ Mode Timing [23, 24]



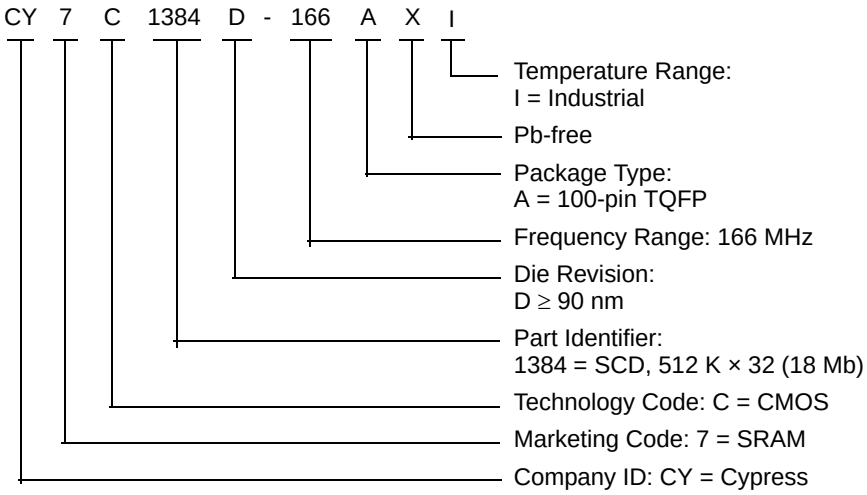
Notes
23. Device must be deselected when entering ZZ mode. See Truth Table on page 7 for all possible signal conditions to deselect the device.
24. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

The below table lists the key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

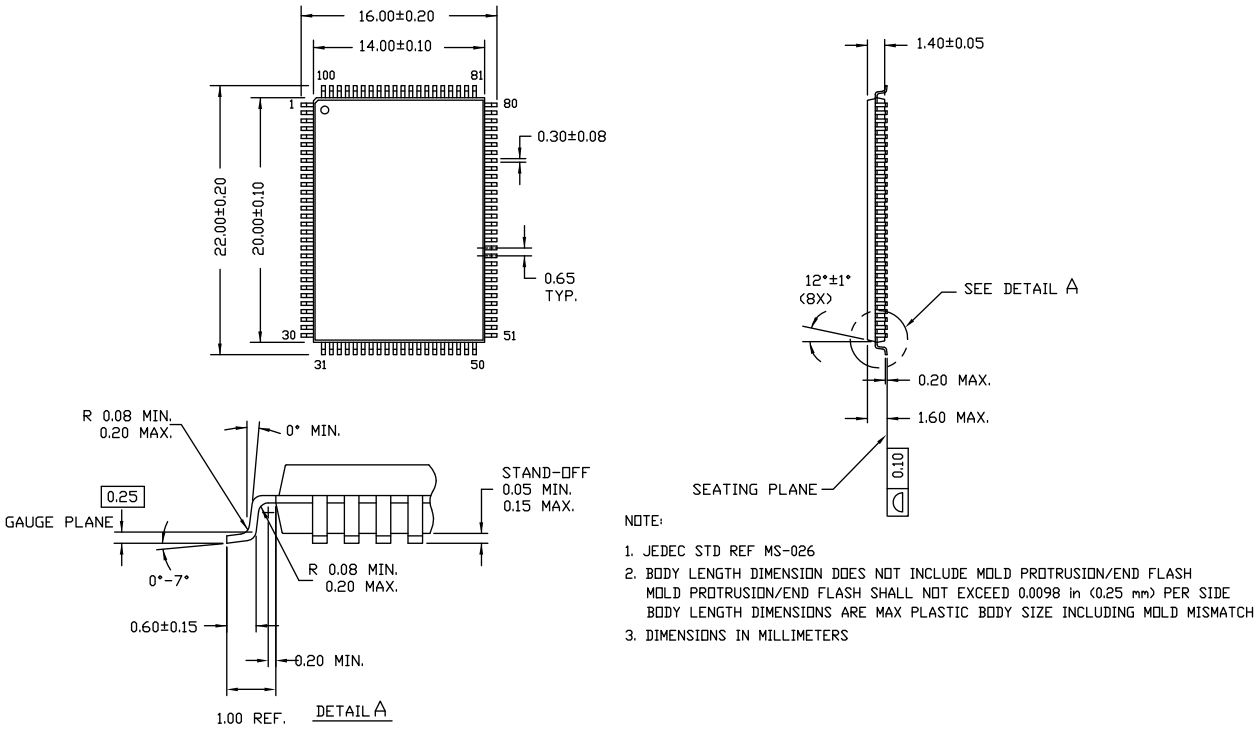
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
166	CY7C1384D-166AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
I/O	input/output
JEDEC	joint electron devices engineering council
$\overline{OE}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
℃	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

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Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3489511	01/10/2012	NJY	New datasheet
*A	3607309	05/03/2012	PRIT	Datasheet status moved from “Preliminary” to Final”

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