

MPEG Clock Generator with VCXO

Features

- Integrated phase locked loop (PLL)
- Low jitter, high accuracy outputs
- VCXO with analog adjust
- 3.3 V operation

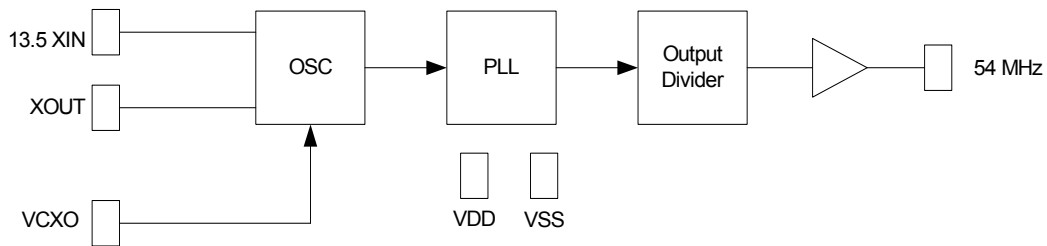
Benefits

- Highest performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Application compatibility for a wide variety of designs

Table 1. Frequency Table

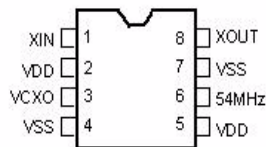
Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V8A-11	1	13.5 MHz pullable crystal input per Cypress specification	One copy of 54 MHz	linear	Pinout-compatible with CY2411

Block Diagram



Pin Configuration

Figure 1. CY241V8A-11 8-pin SOIC



Pin Descriptions

Name	Pin Number	Description
XIN	1	Reference crystal input
VDD	2, 5	Voltage supply
VCXO	3	Input analog control for VCXO
VSS	4, 7	Ground
54 MHz	6	54 MHz clock output
XOUT	8	Reference crystal output

Absolute Maximum Conditions

Supply voltage (V_{DD}) -0.5 to +7.0 V
 DC input voltage -0.5 V to $V_{DD} + 0.5$
 Storage temperature (Non-condensing) ... -55 °C to +125 °C

Junction temperature -40 °C to +125 °C
 Data retention at $T_j = 125$ °C > 10 years
 Package power dissipation 350 mW
 ESD (human body model) MIL-STD-883 > 2000 V

Pullable Crystal Specifications^[1]

Parameter	Description	Comments	Min	Typ	Max	Unit
F _{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C _{LNOM}	Nominal load capacitance		–	14	–	pF
R ₁	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R ₃ /R ₁	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R ₁ values are much less than the maximum spec	3	–	–	–
DL	Crystal drive level	No external series resistor assumed	150	–	–	μW
F _{3SEPHI}	Third overtone separation from 3 × F _{NOM}	High side	300	–	–	ppm
F _{3SEPLO}	Third overtone separation from 3 × F _{NOM}	Low side	–	–	–150	ppm
C ₀	Crystal shunt capacitance		–	–	7	pF
C ₀ /C ₁	Ratio of shunt to motional capacitance		180	–	250	–
C ₁	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V _{DD}	Operating voltage	3.135	3.3	3.465	V
T _A	Ambient temperature	0	–	70	°C
C _{LOAD}	Max load capacitance	–	–	15	pF
t _{PU}	Power-up time for all V _{DD} pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
I _{OH}	Output HIGH current	V _{OH} = V _{DD} – 0.5 V, V _{DD} = 3.3 V	12	24	–	mA
I _{OL}	Output LOW current	V _{OL} = 0.5 V, V _{DD} = 3.3 V	12	24	–	mA
C _{IN}	Input capacitance	Except XIN, XOUT pins	–	–	7	pF
V _{VCXO}	VCXO input range		0	–	V _{DD}	V
f _{ΔXO} ^[2]	VCXO pullability range	Low side	–	–	–115	ppm
		High side	115	–	–	ppm
I _{VDD}	Supply current		–	30	35	mA

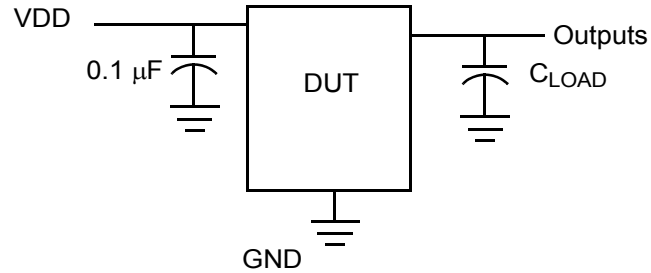
AC Electrical Specifications (V_{DD} = 3.3 V)^[3]

Parameter ^[3]	Name	Description	Min	Typ	Max	Unit
DC	Output duty cycle	Duty cycle is defined in Figure 2 on page 3 , 50% of V _{DD}	45	50	55	%
ER	Rising edge rate	Output clock edge rate, measured from 20% to 80% of V _{DD} , C _{LOAD} = 15 pF. see Figure 3 on page 3 .	0.8	1.4	–	V / ns
EF	Falling edge rate	Output clock edge rate, measured from 80% to 20% of V _{DD} , C _{LOAD} = 15 pF. see Figure 3 on page 3 .	0.8	1.4	–	V / ns
t _g	Clock jitter	Peak-to-peak period jitter	–	–	100	ps
t ₁₀	PLL lock time		–	–	3	ms

Notes

- Crystals that meet this specification include: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.
- 115/+115 ppm assumes 2.5 pF of additional board level load capacitance. This range will be shifted down with more board capacitance or shifted up with less board capacitance.
- Not 100% tested.

Test and Measurement Setup



Voltage and Timing Definitions

Figure 2. Duty Cycle Definition

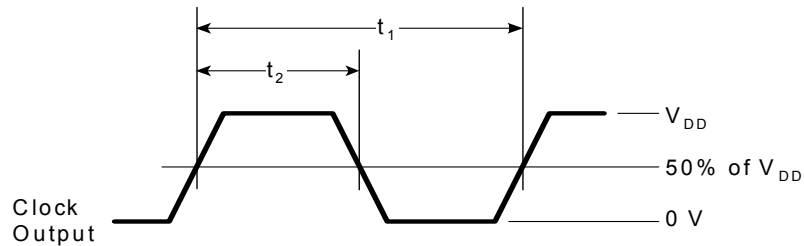
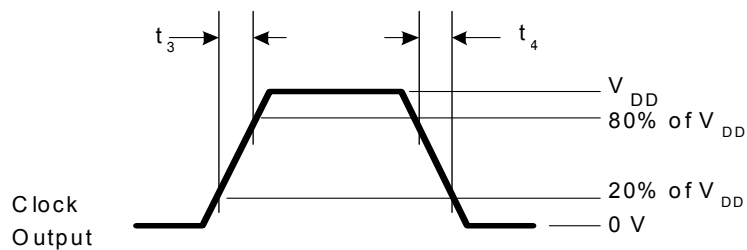


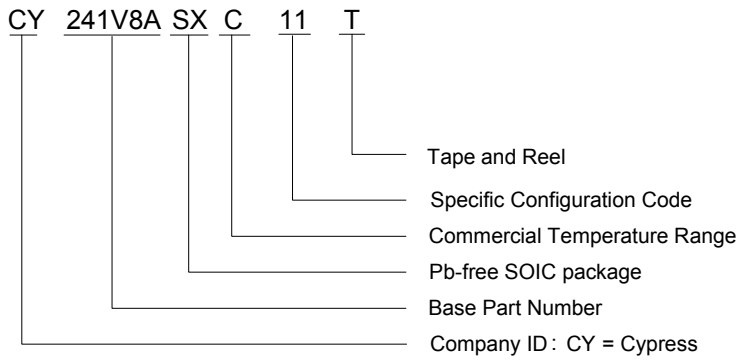
Figure 3. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$



Ordering Information

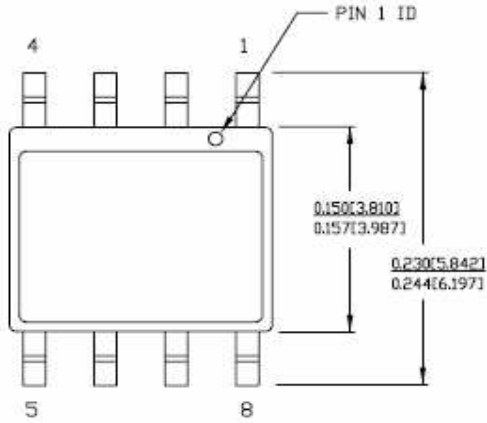
Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage	Features
CY241V8ASXC-11	S8	8-pin SOIC	Commercial	3.3 V	Linear VCXO control curve
CY241V8ASXC-11T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3 V	Linear VCXO control curve

Ordering Code Definition



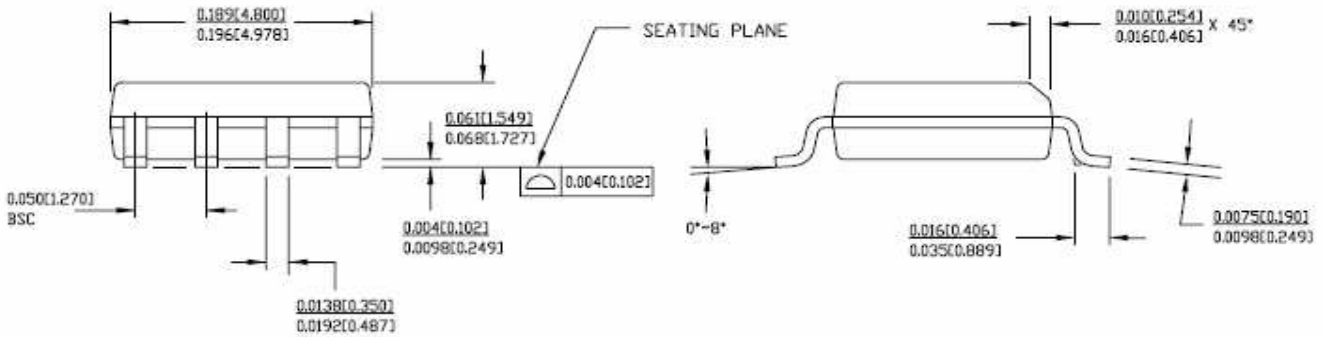
Package Drawing and Dimensions

Figure 4. 8 Pin (150 Mil) SOIC - S08



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG.
SZ08.15	LEAD FREE PKG.



51-85066 *D

Document History Page

Document Title: CY241V8A-11 MPEG Clock Generator with VCXO				
Document Number: 38-07654				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	214071	See ECN	RGL	New Data Sheet
*A	220461	See ECN	RGL	Minor Change: To post on web
*B	2896017	03/18/2010	CXQ	Inactive parts;obsolete datasheet
*C	3000820	08/06/2010	CXQ	Reinstatement of datasheet: Pb-free devices added to Ordering Information.

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