BTSD08 SerDes Test Device

Description

The adoption of serial link technology in VPX and ATCA poses significant debug, characterization, and test challenges. The BTSD08 is an ultra low cost multi-lane Gbps serial test device that achieves unprecedented density and performance. With the BTSD08, you do not need to purchase equipment such as oscilloscopes, pattern generators, jitter analyzers, BERTs, clock generators, and analog function generators for higher speed testing. The device allows the user to characterize the PCIe, Gig E, sRIO, XAUI, or SATA ports quickly and efficiently. Speeds to KX and KX-4 are currently covered by the module, with a roadmap to KR levels. The BTSD08 uses cabling in the VPX, ATCA or other architectures. The unit is connected to a VPX backplane using (2x) 12" VPX cable (full fat pipe connection wafer to SMA contacts and SMA adapter). For more information visit www.elmabustronic.com/cabling.html.

Features

- Multi-lane differential serial fabric test unit
- Flexible design allows signal analysis for various architectures (VPX, ATCA, VXS, etc.)
- Lab-on-board eliminates need for acquiring a whole rack of equipment
- Directly evaluate true Gbps serial link BER performance
- Test and characterize entire mutli-lane serial fabric (PCIe, sRIO, GigE) with one device
- Achieve lowest cost of test and fastest time to market
- Can be used for testing both line cards and backplanes
- Test up to 8 channels at once, up to 6.4 Gbps
- Perform pre-emphasis tuning

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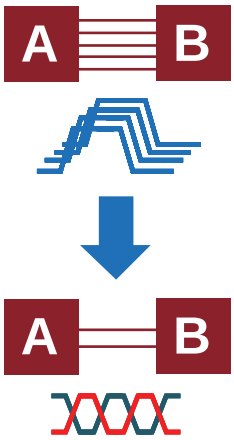
Cost + Time + Inaccuracy

- **Conventional equipment rack required for serial technology**
- **Capable of validating only a single-lane serial link**
- **Very capital-intensive**

The Need

- High speed serial across VPX, ATCA, MTCA, etc, will undoubtedly cause signal integrity issues.
- Customers/integrators need to understand where the fault lies. Vendors (board, backplane) need to know if their product works properly.
- Digital/chip evaluation today: what a logic analyzer was 20 years ago.
- Traditional test approach has too many problems.

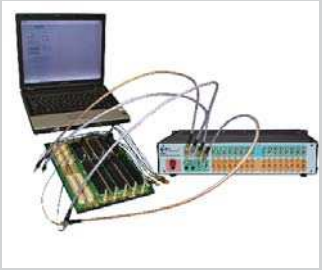


BTSD08 Benefits

- Significantly lower cost than traditional bench approach. Also, large labor cost savings.
- Easy to use, minimal training, CD of instructions available and user-friendly GUI software.
- Frees up time for expensive lab equipment, which typically have long queues. Allows quicker troubleshooting and time-to-market.
- Efficient testing of multiple channels, up to 8 at a time. Multiple units can cascade to 16 channels or more.
- Hits “sweet spot” of embedded market speeds of 3.125 to 6.4 Gbps.
- Other architectures available upon request. Consult factory.

BTSD08 Test Unit Features

• Pattern Generator	x8
• Oscilloscope	x8
• BERT	x8
• Jitter Injector	x8
• Jitter Tester	x8
• Single PC control	
• Ultimate Test Portability	



ORDER INFORMATION

Description	Channels	Model Number
BTSD08 Test Device with 2x VPX Cables (12", even row, wafer to SMA & SMA adapter)	8	1940000417-0000
BTSD08 Test Device without cables	8	1940000419-0000

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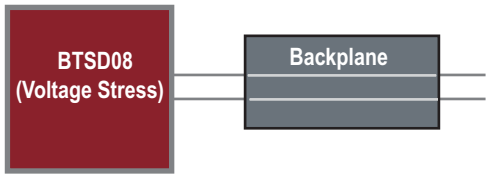
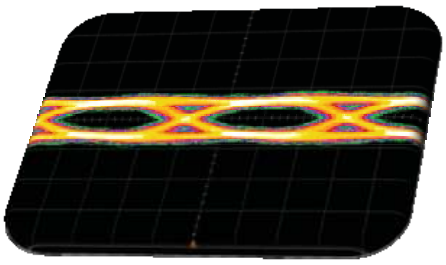
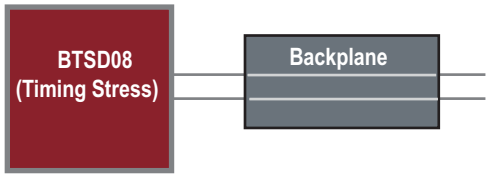
Overview of Capability

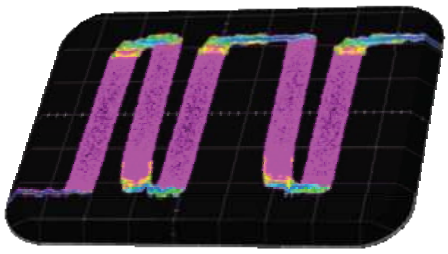


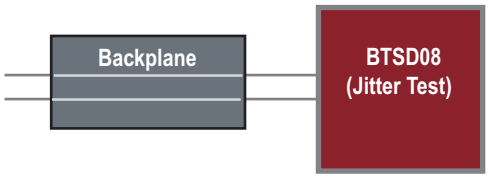
The BTSD08 creates test patterns and applies them directly onto the backplane connector. The differential voltage swing is programmed in order to stress the target receiver. The BER is computed against voltage stress.



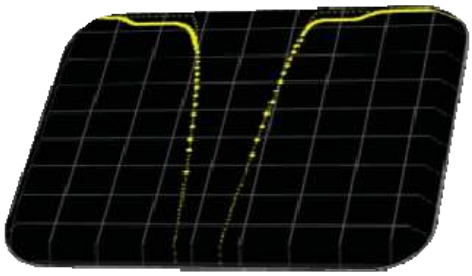


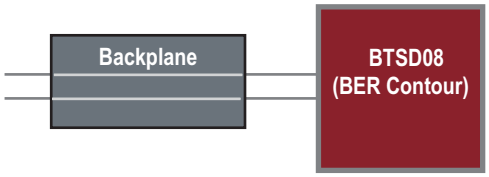
Just like voltage stress, the BTSD08 is capable of generating timing stress. This is useful for evaluating the jitter tolerance of target receivers. Jitter generation is performed internally to the BTSD08.



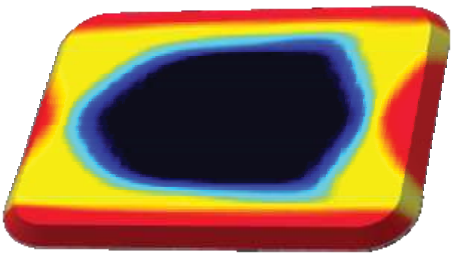


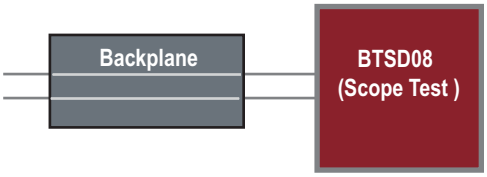
The BTSD08 incorporates sophisticated error counting and timing analysis hardware/software. This enables testing the jitter on transmitter outputs while they are installed in their target environment (the VPX chassis).





Just like timing measurement, the BTSD08 incorporates high resolution sampling hardware that enables direct BER measurement on the whole serial fabric. BER contour plots are also useful in verifying compliance to standards.





To assist in physical-layer debug, the BTSD08 offers an oscilloscope functionality. This allows for the visualization of signal parameters such as rise-time, fall-time, and voltage noise.