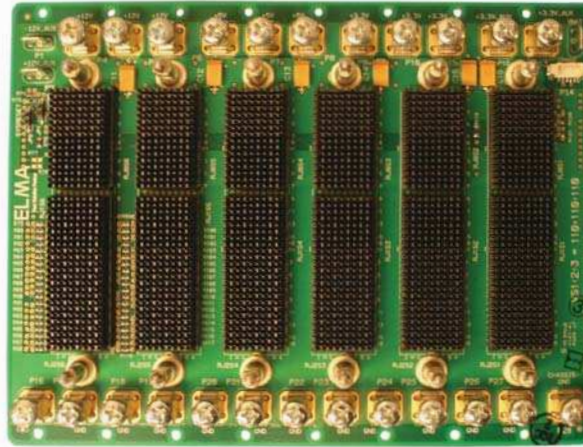


# 3U OpenVPX 6-slot BKP3-CEN06-15.2.12-n Backplane



## Description

Utilizing a twisted-ring topology versus a mesh topology allows for more I/O pins and ability to use mezzanines like XMC. A full mesh topology over 3U VPX would simply take up the vast majority of available pins. In the Elma Bustronic 3U VPX backplane (twisted ring versions), slot 6 has configurable thin pipe links for distributed Gigabit Ethernet to slot 1 through slot 5 and two fat pipes for rear I/O. In slots 1-5 any or all of the P1 thin pipes (x2 channels) assigned to the control channel star can be reconfigured as rear I/O by removing zero ohm SMT shunts. In slots 1-5 all P2 differential pairs are available on the rear side for I/O. In the "AX" part number version, slot 6 is not connected to the other slots, allowing undefined pins for an RTM slot. The only defined pins to the RTM are the 2x thin pipes for the control plane.

The VPX Gigabit Ethernet Control Plane adds a GigE switch, providing a separate star or dual star network for out-of-band communication. This can be particularly important for system management, software and firmware upgrades, and initiating new processes on specific boards.

The Elma Bustronic design solution offers 3.125 to 6.250Gbauds/performance in one PCB. This design provides maximum performance while saving you money. The central switch version of our 3U, 6-slot OpenVPX backplane features a fat pipe expansion plane, a fat pipe Star topology data plane, and an ultra thin pipe for the control plane. It is designed using Nelco-13SI PCB material.

## Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Channels A and B are arranged as 2 fat pipes (x4) channels configured as a twisted ring extending from slots 1 to 5
- Provides built in ESD ground protection in every slot
- Versions with or without GigE Control Plane
- Version with slot 6 not connected to other slots for use with RTM

## Board Specifications

- 22-layer stripline design
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB .212" thick

## Mechanical Specifications

- 3U height
- 6 slots
- MultiGig RT-2 connectors

Coming Soon!

Rear View



Close-up of Power studs and fast-on power blades

# 3U OpenVPX 6-slot BKP3-CEN06-15.2.12-n Backplane

## Line Drawing

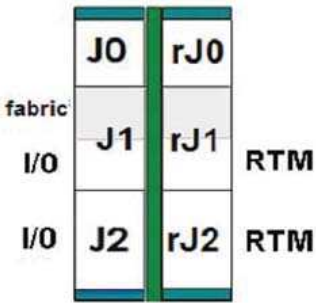
Coming Soon!

## ORDER INFORMATION

Height	Total Slots	Description	Profile Number	Part Number
3U	6	VPX central switch, payload in Slot 1 connected to slot 2, channel Gbaud rate up to 6.25	BKP3-CEN06-15.2.12-3	1OVX306JX6-1X11R
3U	6	VPX central switch, payload in Slot 1 connected to slot 2, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-CEN06-15.2.12-3	1OVX306JX6-1X10R

# 3U OpenVPX 6-slot BKP3-CEN06-15.2.12-n Backplane

## Connector Positions



## J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

## J1/P1 Payload Signal Assignments

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1	Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

J1/P1 Switch Signal Assignments

## J1/P1 Switch Signal Assignments

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1	Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10	GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11	UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12	GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14	GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16	GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

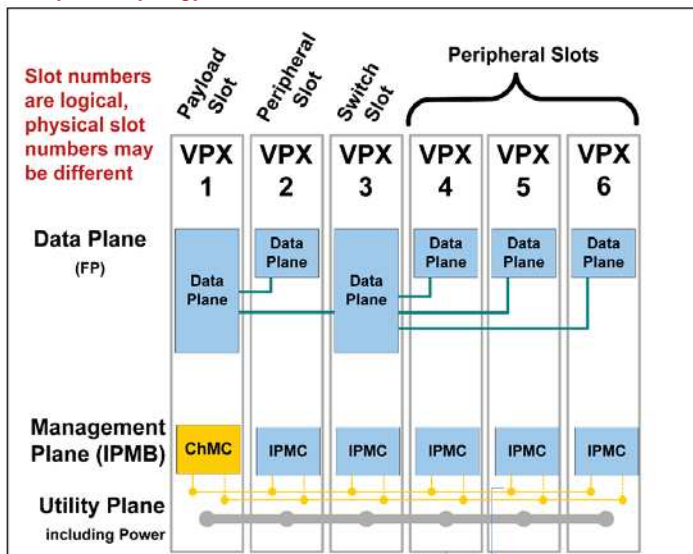
# 3U OpenVPX 6-slot BKP3-CEN06-15.2.12-n Backplane

## J1/P1 Peripheral Signal Assignments

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A
	Row i	Row h	Even Row g	Odd Row f	Row e	Row d	Even Row c	Odd Row b	Row a
1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7	Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

All J2/P2 slots = User Defined

## Backplane Topology

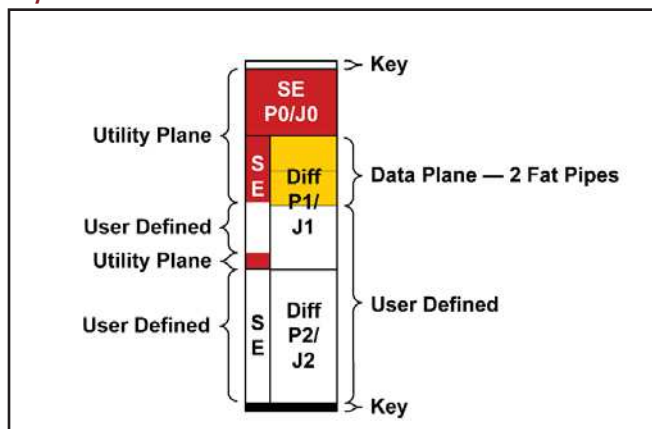


## Backplane Profile

Profile name	Mechanical		Slot Profiles and Section			Channel Gbaud Rate
	Pitch (in)	RTM Conn	VPX 1	VPX 3	VPX 2, 4 - 6	Data Plane
			Payload	Switch	Peripheral	
BKP3-CEN06-15.2.12-1	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-SWH-4F-14.4.4	SLT3-PER-1F-14.3.2	2.5
BKP3-CEN06-15.2.12-2	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-SWH-4F-14.4.4	SLT3-PER-1F-14.3.2	5.0
BKP3-CEN06-15.2.12-3	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-SWH-4F-14.4.4	SLT3-PER-1F-14.3.2	6.25

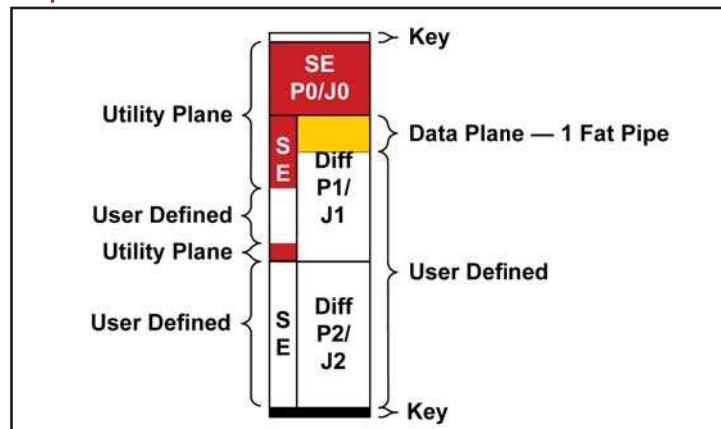
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## Payload Slot Profile



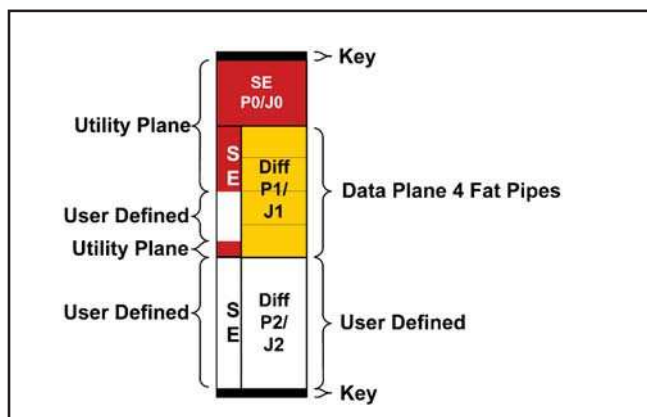
SLT3-PAY-2F-14.2.7

## Peripheral Slot Profile



SLT3-PER-1F-14.3.2

## Switch Slot Profile



SLT3-SWH-4F-14.4.4

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