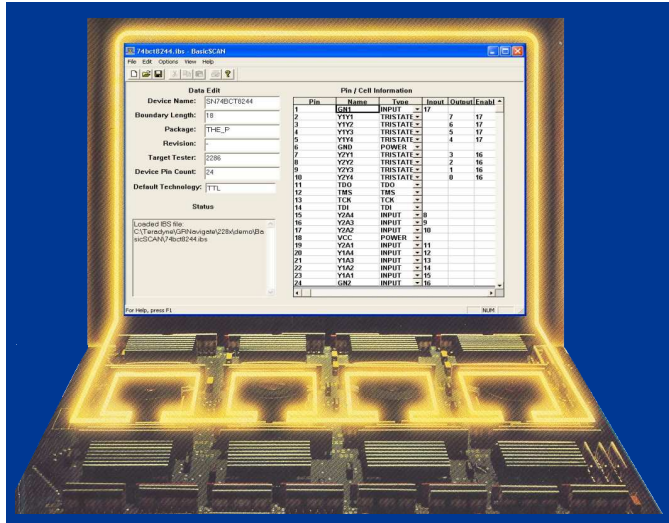


BasicSCAN™ Test Generator

A Boundary Scan Test Solution for 1149.1 Components

Key Features:

- *Boundary Scan Solution for 1149.1 Devices*
- *Available on any TestStation™ or GR228X test system*
- *Faster Test Program Development*
- *Better Process Fault Coverage*
- *Improved Throughput*
- *More Accurate Diagnostics*
- *Fast and Reliable Fault Detection*



BasicSCAN Test Generator- Speeds Test Development

Teradyne's BasicSCAN test generation tool is designed to significantly reduce the cost and time currently required to develop test programs for complex digital components. Applying Boundary Scan techniques, the BasicScan Test Generator, creates an effective test for all your IEEE 1149.1-compliant devices. Available on TestStation and GR228X systems, BasicScan simplifies test generation for Boundary Scan parts by providing a full access, digital test for process faults in a matter of minutes!

Complex components are predominant in printed circuit board design making reliable testing of those boards difficult at best. Test engineers, often presented with limited information about the functionality of these devices, previously had no choice but to get complex functional vectors from the designer or create the vector themselves. Either solution requires a considerable amount of time and expertise, significantly increasing the investment in test program development.

BasicSCAN is Teradyne's solution to reduce the cost and time associated with generating and debugging test programs for complex 1149.1-compliant components. The BasicSCAN Test Generator provides a comprehensive test for "stuck-at's" and opens.

It eliminates the need for complex tasks typically required when developing functional test vectors. In addition, using BasicSCAN will greatly reduce the number of test vectors required to test for process faults, reducing test program complexity and increasing throughput. Within minutes, test engineers can develop and debug a program that can detect and diagnose an open pin, a stuck-at pin, a missing component, or a wrong component fault.

The BasicSCAN software allows the user to simply import information directly from the component BSDL file, such as device name; Instruction register length; Instruction register capture value; Boundary Scan register length and, most importantly, input pin/cell information for each pin on the component.

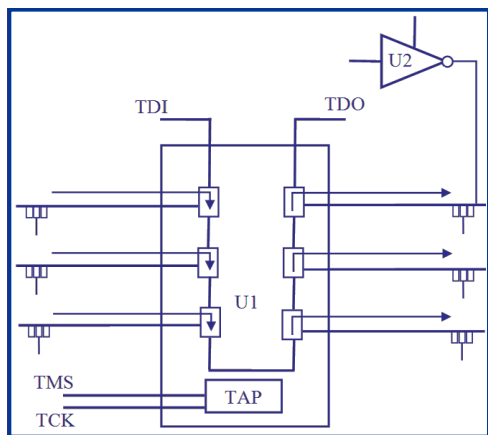
After the data is imported, BasicSCAN will automatically generate a Digital Test Source (.DTS) model. This model is then inserted into an user library within the Digital Test Library (.DTL) file to be accessed by the Automatic Test Generation (ATG) software of the test system.

The BasicSCAN models combine the device's built-in Boundary Scan features and the test system's resources to develop a high fault coverage test. The component is first initialized and placed in the Test-Logic-Reset state.

The BasicSCAN models combine the device's built-in Boundary Scan features and the test system's resources to develop a high fault coverage test. The component's Instruction register capture value is checked while the PRELOAD instruction is shifted in. The Boundary Register control cells are enabled and the device inputs are preloaded with alternating 1s and 0s using the PRELOAD instruction.

The test system's driver/sensor nails then present the opposite state to the component's inputs while shifting in the EXTEST instructions. The values driven by the outputs are then sensed. At the same time the component captures the values at the inputs. These captured values are shifted out and the complement of the previously loaded pattern is shifted in. The driver/sensor nails then drive the complement of their previous pattern. Again the values at the device's inputs are captured and the values at the output are sensed for comparison to the values previously loaded into the Boundary Scan output cells.

Finally, the captured values are shifted out to be compared to the pattern presented by the test system. This simple scenario will detect any open pins. Outputs never sensed high or low will also be found. This will also determine whether or not there are any stuck-at faults. From the information collected during these tests, faults are detectable to the pin level.



Automatic Test Generation uses BasicSCAN model information to isolate U1 from potential effects of U2.

Software Features:

- Available with TestStation software
- Operates on Windows operating systems
- Diagnostic to the pin level
- Easy to use Windows application
- Intuitive operation – minimum training required
- Capable of handling a variety of wiring configurations:
 - Un-nailed pins
 - Input Pins tied to one another
 - Pins tied to power
 - Output pins tied to one another
 - Output pins tied to input pins
- Intuitive operation – minimum training required
- Verifies Device IDCODE and runs optional Built-in-Self Tests
 - HIGHZ Disable;
 - EXTEST Inhibit/Disable
 - Non-Boundary Scan disables



Contact your Teradyne sales representative for more information or visit www.teradyne.com/atd.