



- Quartz SAW Stabilized Differential Output Technology
- Very Low Jitter Fundamental-Mode Operation at 644.53125 MHz
- Voltage Tunable for Phase Locked Loop Applications
- Timing Reference for 10G Optical Ethernet Communications Systems
- Complies with Directive 2002/95/EC (RoHS)



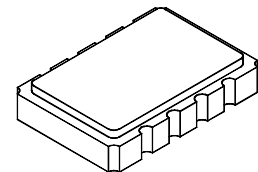
The OP4012B is a voltage-controlled SAW clock (VCSC) designed for phase-locked loop (PLL) applications in optical data communications systems. The differential outputs of the OP4012B are generated by high-Q, fundamental mode quartz surface acoustic wave (SAW) technology. This technique provides very low output jitter and phase noise, plus excellent immunity to power supply noise. The OP4012B differential outputs feature $\pm 1\%$ symmetry, and can be DC-configured to drive a wide range of high-speed logic families. The OP4012B is packaged in a hermetic metal-ceramic LCC.

Absolute Maximum Ratings

Rating	Value	Units
DC Supply Voltage	0 to 5.5	Vdc
Tuning Voltage	0 to 5.5	Vdc
Case Temperature	-55 to 100	°C

OP4012B

644.53125 MHz
Optical
Timing Clock



SMC-08

Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	Absolute Frequency	f_O	1	644.53125		MHz
			2	± 100		ppm
	Tuning Range		1	0	3.3	V
			1, 8	± 5		%
	Tuning Linearity		2	100	260	ppm/V
				125	265	kHz
Q and \bar{Q} Output	Voltage into 50 Ω (VSWR<1.2)	V_O	1, 3	0.60	1.1	V_{P-P}
				1, 3	2:1	
			3, 4, 5	49	51	%
			3, 4, 6		-30	dBc
			3, 4, 6, 7		-60	dBc
Phase Noise	@ 100 Hz offset		3, 6	-70		dBc/Hz
			3, 6	-100		dBc/Hz
			3, 6	-125		dBc/Hz
			3, 6	-150		dBc/Hz
Q and \bar{Q} Jitter	RMS Jitter		3, 4, 6, 7	2		ps
			3, 4, 6, 7	12		ps _{P-P}
			3	12		ps _{P-P}
Input Impedance (Tuning Port)			1			K Ω
Output DC Resistance (between Q & \bar{Q})		1, 3	50			K Ω
DC Power Supply	Operating Voltage	V_{CC}	1, 3	3.13	3.3 or 5.0	Vdc
	Operating Current	I_{CC}	1, 3		70	mA
Operating Case Temperature		T_C	1, 3	-40	+85	°C
Lid Symbolization (YY=Year, WW=Week)	RFM OP4012B YYWW					



CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.
COCOM CAUTION: Approval by the U.S. Department of Commerce is required prior to export of this device.

Notes:

1. Unless otherwise noted, all specifications include the combined effects of load VSWR, V_{CC} and T_C .
2. Net tuning range after tuning out the effects of initial manufacturing tolerances, VSWR pushing/pulling, V_{CC} , T_C and aging.
3. The internal design, manufacturing processes, and specifications of this device are subject to change without notice.
4. Specified only for a balanced load with a VSWR < 1.2 (50 ohms each side), and a V_{CC} = 3.0 Vdc.
5. Symmetry is defined as the width in (% of total period) measure at 50% of the peak-to-peak voltage of either output.
6. Jitter and other noise outputs due to power supply noise or mechanical vibration are not included in this specification except where noted.
7. Applies to period jitter of either differential output. Measured with a Tektronix CSA803 signal analyzer with at least 1000 sample.
8. One or more of the following United States patents apply: 4,616,197; 4,670,681; 4,760,352.

OP4012B Performance Parameters

The OP4012B has been developed to achieve high performance in five parameters critical to optical data communications applications:

Low Jitter and Phase Noise - low clock jitter (or low phase noise in the frequency domain) is critical to achieving low bit error rates in optical data communications systems. The OP4012B provides very low free-running jitter and phase noise as shown in Figures 1 and 2. This makes the OP4012B an excellent reference for the generation or regeneration of low-jitter clocks and data streams. The OP4012B achieves this performance over its full -40 to +85 °C operating temperature range using RFM's patented SAW oscillator architecture.

Single-Sideband Phase Noise

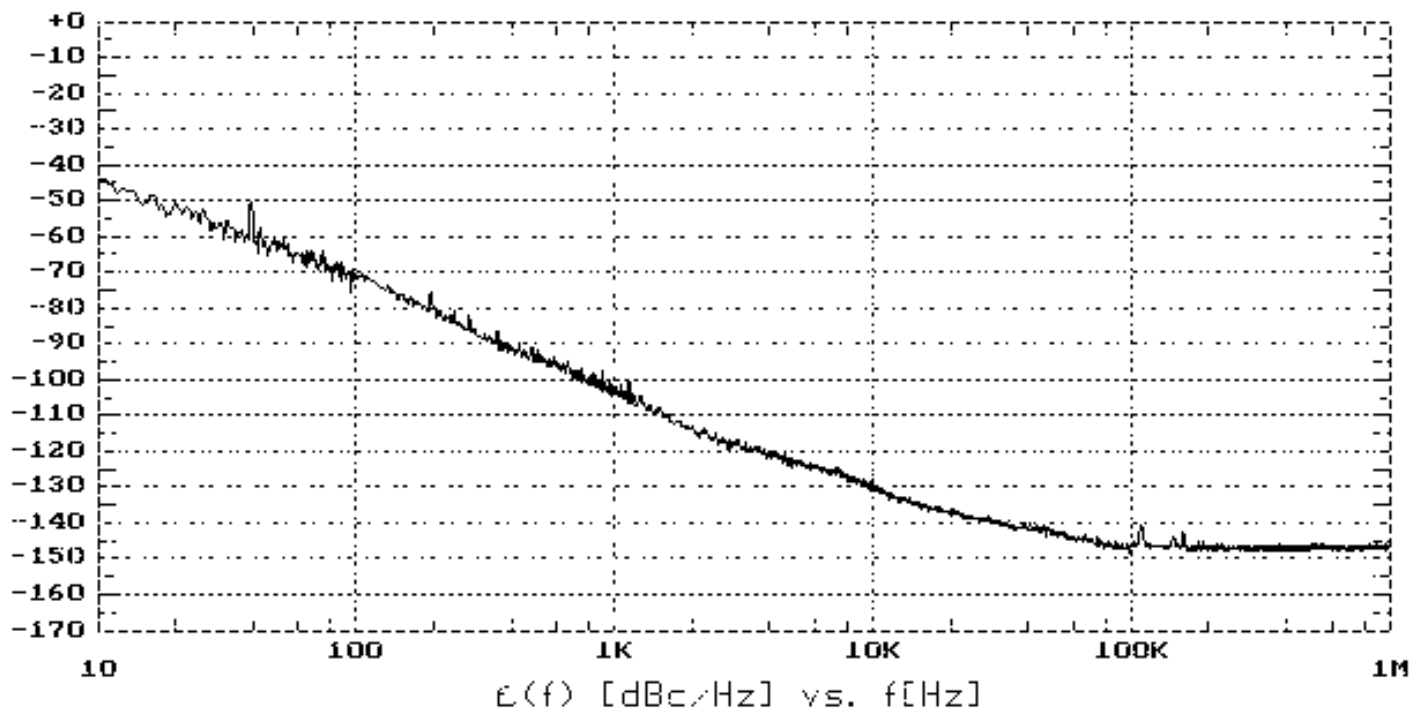
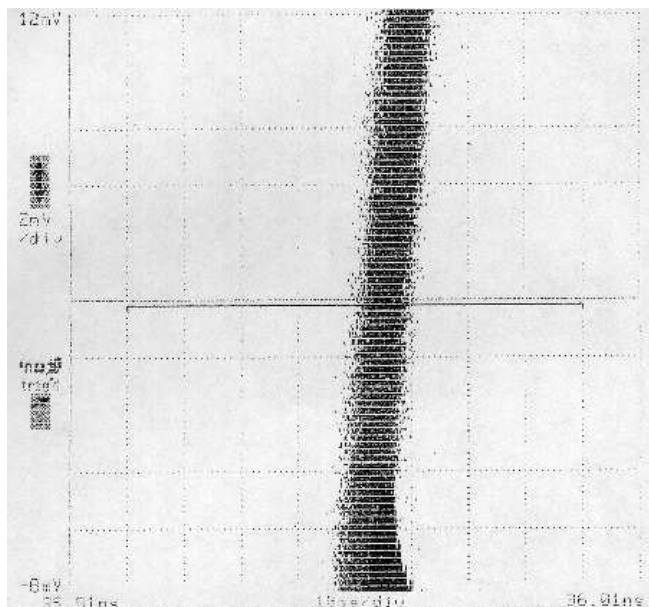


Figure 1

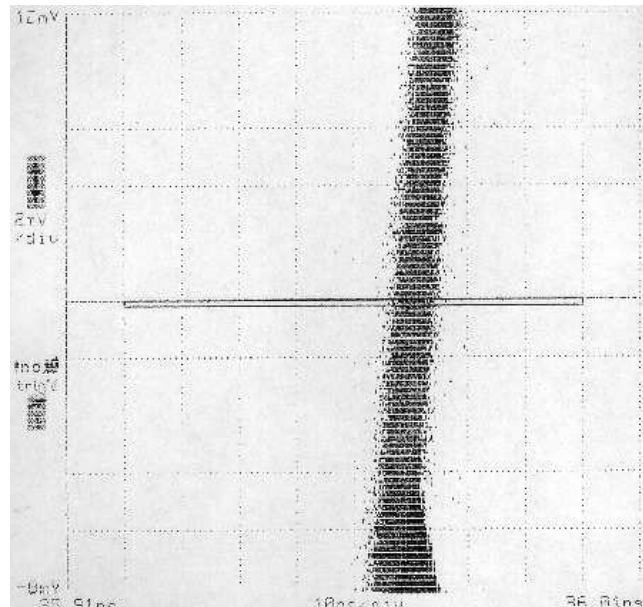
High Power Supply Noise Immunity - the OP4012B uses both differential active devices and differential SAW technology to minimize the effects of power supply noise on jitter and phase noise, as shown in Figures 2 and 3. Optical data communications circuits must switch relatively high levels of current, making power supply noise immunity an important clock requirement.

Controlled Tuning Characteristics - the OP4012B voltage tuning constant, K_V , is bounded between 100 and 260 ppm/V under locked conditions for reference signals with ± 100 ppm or better stability over the OP4012B's full operating temperature and supply voltage range. This allows a PLL based on the OP4012B to be designed with a well-controlled loop bandwidth and damping factor, avoiding problems such as jitter peaking, etc. The voltage tuning characteristic of the OP4012B is monotonic from 0 to 3.3 V, supporting reliable acquisition of phase lock. Figure 4 shows typical OP4012B tuning characteristics.

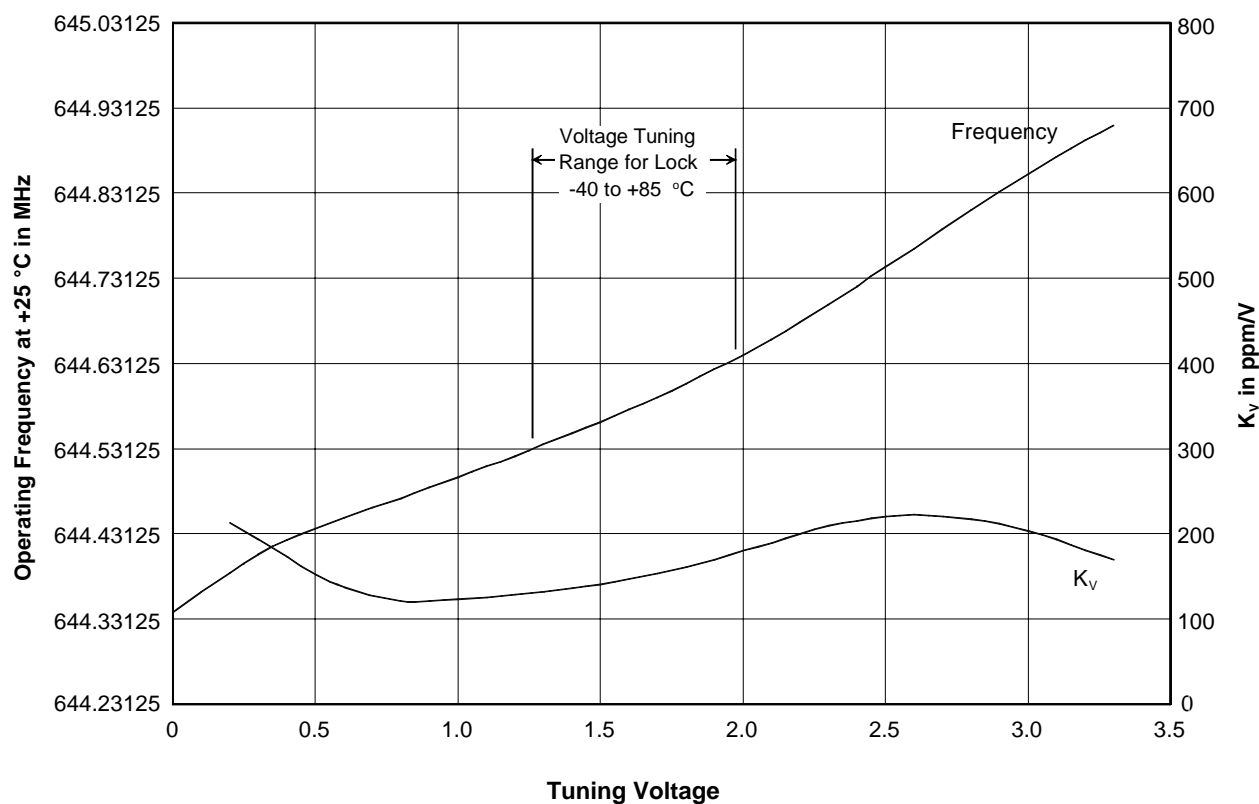
OP4012B Jitter Plot
No Power Supply Noise



OP4012B Jitter Plot
200 mV of Power Supply Noise



Typical OP4012B Tuning Characteristics



Differential Output Symmetry - for balanced output loads, the differential output symmetry of the OP4012B is $\pm 1\%$.

This differential output symmetry meets the requirements of the most demanding high-speed logic families.

Output DC Voltage Configurability - the OP4012B differential outputs can be DC-configured to support a wide range of high-speed logic families and ASIC drive requirements by the selection of four resistors (see Configuring the OP4012B DC Output Voltage below) and a logic supply voltage. Each differential output of the OP4012B is AC-coupled to provide this flexibility.

OP4005B Tuning Details

The frequency tuning of the OP4012B is characterized over a voltage range of 0 to 3.3 V. The tuning voltage applied to the OP4012B should be limited to this range. Figure 4 shows the typical locked tuning range for operation over -40 or $+85$ °C. The frequency shift of a quartz SAW frequency control device with temperature has the shape of an inverted parabola, with the highest frequency occurring around $+25$ °C. At both -40 and $+85$ °C, there will be a 170 ppm downward shift in the frequency of the SAW device compared to $+25$ °C. Tuning to compensate for this temperature shift is the same as tuning 170 ppm higher at $+25$ °C. This is well within the tuning range of the OP4012B, as shown in Figure 4. Note that the voltage tuning constant, K_V , is bounded between 140 and 300 ppm/V under locked conditions for any temperature within the OP4012B's specified operating range.

The OP4012B tuning port presents a input impedance greater than 100 kilohms from DC to 50 kHz, and at least 1 kilohm for any RF frequency up to the operating frequency of the OP4012B. Most operational amplifiers used in active loop filters will be stable when driving the tuning port directly. Special care should be taken to avoid ground loops in the path from the output of the phase detector through the loop filter to the tuning input of the OP4012B. For most applications, the bandwidth of the loop filter in a OP4012B PLL will be less than 50 Hz, as discussed in the example OP4012B PLL application section below.

Configuring the OP4012B DC Output Voltage

Each differential output of the OP4012B is AC coupled, allowing the static DC level at each output to be set with a resistive divider to match the logic family being driven by the clock. The parallel-equivalent resistance of the two resistors in each divider should be approximately 50 ohms. The supply voltage to the dividers, V_{LOAD} , should be two to three times the value of the static DC voltage, V_{DC} .

Referring to the accompanying figure:

$$V_{DC} = V_{LOAD} * R1 / (R1 + R2)$$

and

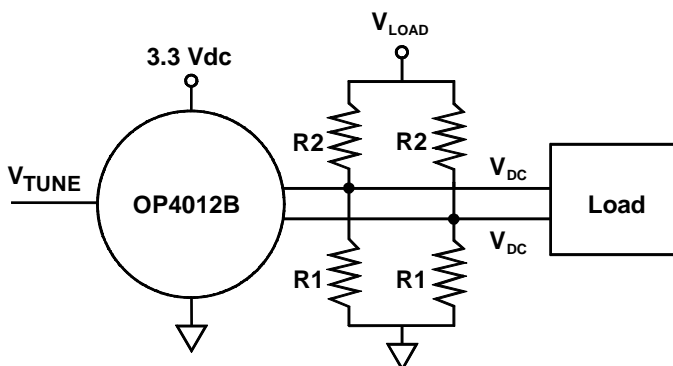
$$50 = R1 * R2 / (R1 + R2)$$

The values of the resistors $R2$ and $R1$ are given directly as:

$$R2 = 50 * V_{LOAD} / V_{DC}$$

$$R1 = 1 / (0.02 - (1/R2))$$

OP4012B DC Output Voltage Adjustment



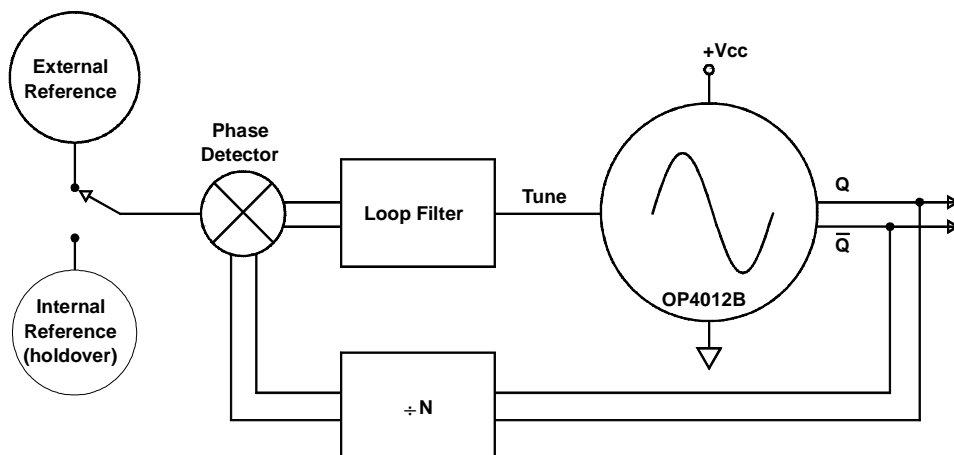
The following table provides R1 and R2 values for six high-speed logic families commonly used in optical data communications systems. Note that the OP4012B can be used with logic families that run from a negative power supply voltage by simply using a negative V_{LOAD} voltage.

Load Type	V_{DC}	R1	R2	V_{LOAD}
10K 3.3 V PECL	1.95	120	91	3.3 V
100K 3.3 V PECL	1.88	120	91	3.3 V
10K 5 V PECL	3.65	180	68	5.0 V
100K 5 V PECL	3.58	180	68	5.0 V
10K -5 V NECL	-1.30	240	62	-5.0 V
100K -5 V NECL	-1.42	240	62	-5.0 V

OP4012B Enable/Disable

Pin 3 on the OP4012B is the enable/disable control pin for the clock outputs. When Pin 3 is grounded, full output power is available from the clock. When Pin 3 is pulled to V_{CC} , the power on the clock outputs is decreased at least 25 dB.

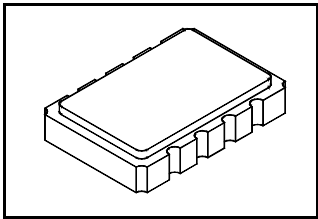
PLL for Generating a High Stability 644.53125 MHz Clock



Example OP4012B Phase-Locked Loop Application

One of the most important applications for the OP4012B is in a PLL circuit used to generate a very high quality 644.53125 MHz clock. The PLL combines the long-term stability of a precision external or internal 20.1416 MHz reference clock with the very low jitter and phase noise of the OP4012B. A block diagram of the PLL is shown in Figure 6. A sample of the OP4012B output is divided by 32 and is compared to 20.1416 MHz reference clock in the phase detector. The loop filter at the output of the phase detector is set to a very low bandwidth (less than 50 Hz typical). This imparts the long-term stability of the precision 20.1416 MHz reference to the OP4012B without degrading the OP4012B's low jitter and phase noise.

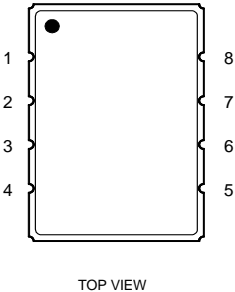
SMC-8 8-Terminal Surface Mount Case



Dimension	mm		Inches	
	MIN	MAX	MIN	MAX
A	13.46	13.97	0.530	0.550
B	9.14	9.66	0.360	0.380
C	1.93 Nominal		0.076 Nominal	
D	3.56 Nominal		0.141 Nominal	
E	2.24 Nominal		0.088 Nominal	
F	1.27 Nominal		0.050 Nominal	
G	2.54 Nominal		0.100 Nominal	
H	3.05 Nominal		0.120 Nominal	
J	1.93 Nominal		0.076 Nominal	
K	5.54 Nominal		0.218 Nominal	
L	4.32 Nominal		0.170 Nominal	
M	4.83 Nominal		0.190 Nominal	
N	0.50 Nominal		0.020 Nominal	

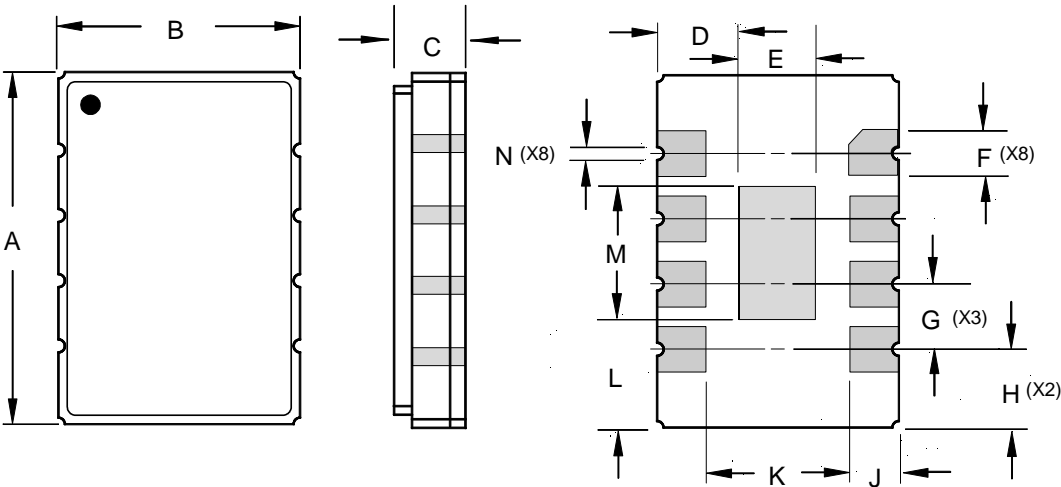
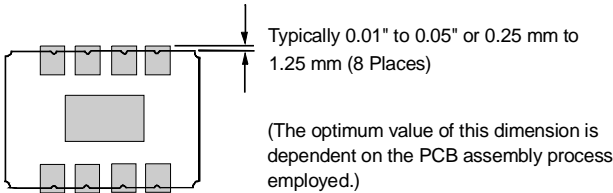
ELECTRICAL CONNECTIONS

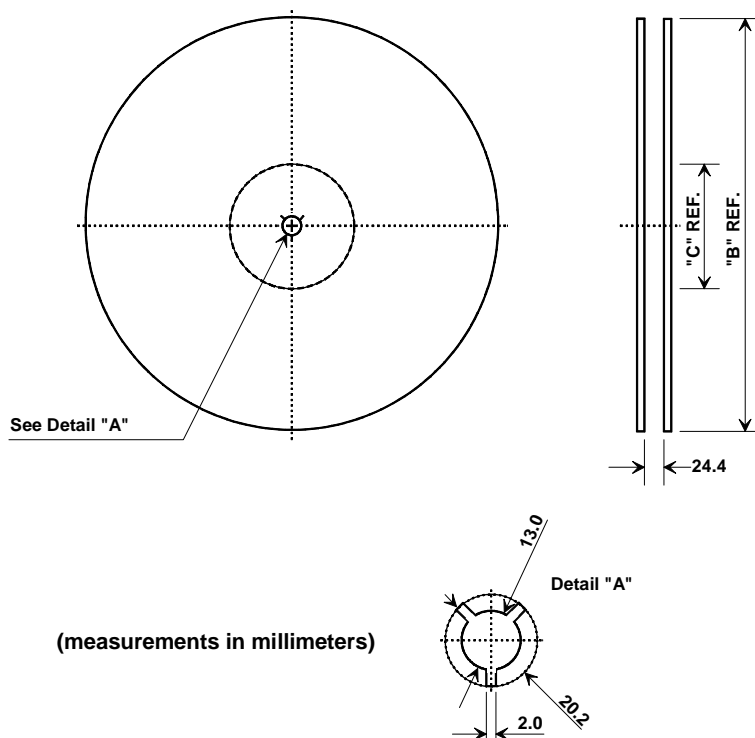
Terminal Number	Connection
1	V _{CC}
2	Ground
3	Enable/Disable
4	Q Output
5	\overline{Q} Output
6	Ground
7	
8	Tuning Input
LID	Ground



Typical Printed Circuit Board Land Pattern

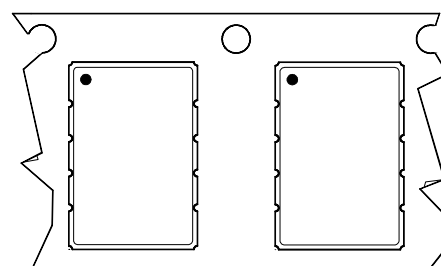
A typical land pattern for a circuit board is shown on the right.
Grounding of the metallic center pad is optional.





SMC-08 Case

Reel Size			Quantity Per Reel	
"B" Nominal	"C" Nominal		Min	Max
13 Inch	330 mm	100 mm	200	1000



Orientation in Tape Carrier as Shipped

Dimensions

Carrier Tape Dimensions		Cover Tape
Ao	.383 ± .004 (9.7 mm)	21.3 mm
Bo	.554 ± .004 (14.1 mm)	
Ko	.130 ± .004 (3.3 mm)	
P	12mm	
W	24mm	
Tape Length	60M	
Pockets/m	83	

