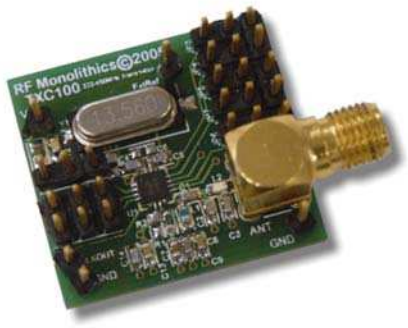
DR-TXC100
315 & 433.92 MHz
Development Kits

RF Monolithics, Inc.

Complies with Directive 2002/95/EC (RoHS)
ETSI Compliant



Evaluation Board

I. Product Overview

The DR-TXC100-315 and DR-TXC100-433 Evaluation Boards allow for evaluation of the RF performance of the TXC100 300-450MHz Transmitter at 315 MHz and 433.92 MHz, respectively. The board is designed to serve as a standalone evaluation platform or to be incorporated on a user's design simply by soldering directly to the prototype PCB via standard .025" square header pins. All configurable functions of the TXC100 are accessible for the user to directly interface to any embedded microcontroller design.

The DR-TXC100 RF output uses an end launch SMA connector for quick and convenient connection to an external antenna or spectrum analyzer or the connector may be removed and replaced with a λ/4 monopole antenna soldered to the center pin. The output is optimized for two common frequencies of 315MHz and 433.92MHz. The 433.92MHz evaluation board is ETSI compliant. All matching components are accessible for optimization at other frequencies of interest.

The DR-TXC100 serves as a guide to PCB layout. Placement and routing can be easily duplicated for quick design-in and proven performance, speeding product time-to-market and reducing
design efforts.

II. Key Features

- Operating Frequency Range: 300-450 MHz
- Modulation Types: OOK/ASK/FSK
- Operation supply voltage: 2.1V - 3.6V
- High Date rate:
  - ASK: 100 kbps
  - FSK: 20 kbps
- Low current consumption:
  - ASK mode: 7 mA typical
  - FSK mode: 10 mA typical
- Low Stand by current: < 1 nA
- Adjustable Output power: -10dBm to +10dBm
- Adjustable FSK Shift
- Programmable Clock Output

Electrical Characteristics

Characteristics	Sym	Min	Typical	Max	Units
Operating Frequency	fo	300		450	MHz
Modulation Types			OOK/ASK/ FSK		
ASK Data Rate				100	Kbps
FSK Data Rate				20	Kbps
Peak RF Output Power			+10		dBm
Standby Current				1	nA
Supply Voltage Range	V_{DD}	2.1		3.6	Vdc
Operating Temperature	Ta	-40		+125	°C

Reference Crystal Parameters

Characteristics	Sym	Min	Typical	Max	Units
Crystal Frequency	fc		fo/32		MHz
Load Capacitance	Cl			3	pF
Motional Capacitance	Cm	9		10	fF
Tolerance	Tol		±30		ppm

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III. Schematic Diagram

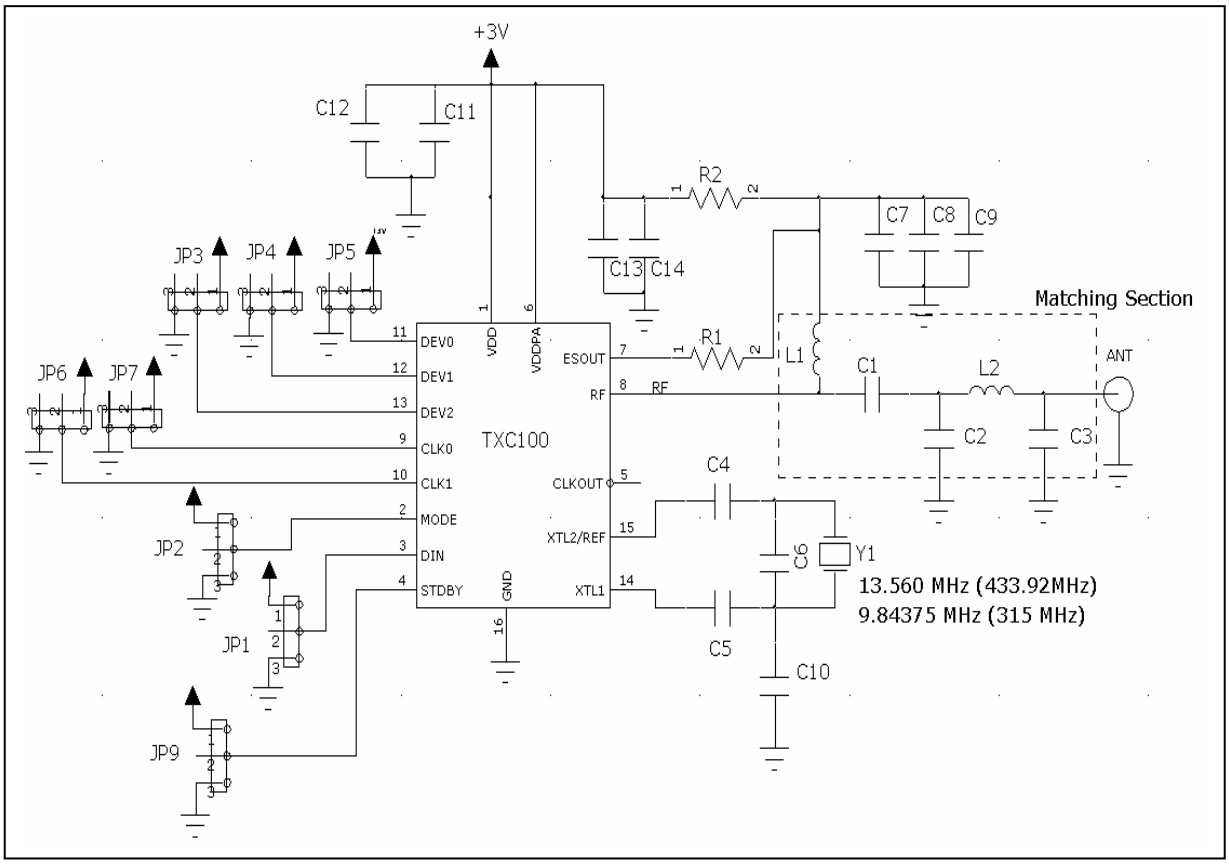


Table 1: Bill of Material for the DR-TXC100

Ref Des	315MHz Band	433MHz Band‡
C4,C5,C9	100pF	100pF
C10*	.01uF	.01uF
C6	**DNP**	**DNP**
C11,C13	1uF	1uF
C12,C14	.01uF	.01uF
C8	220pF	220pF
C7	680pF	680pF
C1[1]	15pF	3.3pF
C3[1]	15pF	12pF
C2[1]	22pF	5.6pF
L1[12]	27nH	22nH
L2[12]	22nH	18nH
R1	**DNP**	0 Ohm
R2	0 Ohm	**DNP**
Y1	9.84375 ∞	13.560 ◊

[1]Matching Components
[2]Use wirewound inductors ONLY for best performance
* Install for External Reference ONLY
‡ ETSI COMPLIANT
∞ Hong Kong Crystal P/N SSL9843750E03FAFR800
◊ Hong Kong Crystal P/N SSM1356000E03FAFR800

IV. Connections and Quick Start

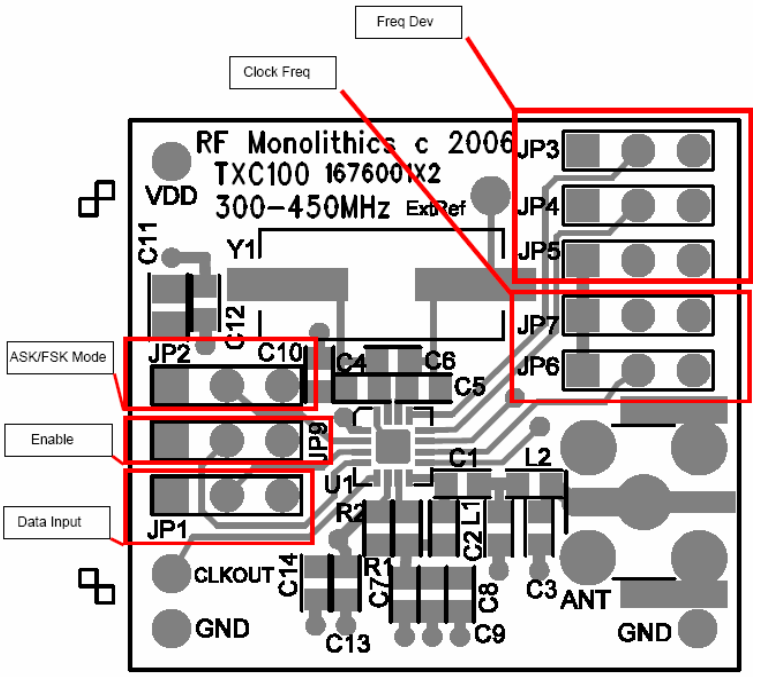
Test Equipment Needed:

- Spectrum Analyzer
- Regulated, Variable Power Supply
- Digital Multimeter (DMM)

Setup

1) Turn on power supply set to +3V and then turn off.
2) Connect GND lead to any GND pin.
3) Connect +lead of power supply to +input of DMM.
4) Connect COM lead of DMM to VCC of DR-TXC100.
5) Turn DMM to mA setting.
6) Connect the ANT connection (SMA connector) to the spectrum analyzer and set to 315MHz or 433.92MHz with Span = 1MHz.
7) Turn on power supply. The spectrum analyzer should show a peak of about +10dBm at the set frequency (315MHz or 433.92MHz).
8) Observe the current draw on the DMM.
9) Vary the power supply from +2.1V to +3.6V and observe the output power vs. current.

V. Jumper Descriptions



Jumpers
The DR-TXC100 functions can be tested by configuring the jumper settings or applying external stimulus from a pulse/function generator to pin 2 of the respective jumper. Table 2 shows the jumper designations and associated functions.

NOTE: Pin 1 (VCC) denoted by square pad.

Data Pin
The TXC100 transmits ASK or FSK data at 100kbps and 20kbps, respectively. JP1 controls whether a logic '1' or logic '0' is applied. For ASK, a logic '1' will turn on the power amplifier. For FSK, a logic '1' will shift the carrier to the higher deviation frequency specified by JP3, JP4, JP5. For ASK, a logic '0' will turn off the power amplifier. For FSK, a logic '0' will shift the output to the fundamental carrier frequency. An external modulating signal can be applied to JP1-2 by removing the jumper and clipping onto the center pin directly and observing the output modulation on the spectrum analyzer.

TABLE 2: Jumper Designations

JUMPER	Position	Description
JP1	1-2	Data '1'
	2-3	Data '0'
JP2	1-2	FSK Mode
	2-3	ASK Mode
JP3	1-2	FreqDev(2) '1'
	2-3	FreqDev(2) '0'
JP4	1-2	FreqDev(1) '1'
	2-3	FreqDev(1) '0'
JP5	1-2	FreqDev(0) '1'
	2-3	FreqDev(0) '0'
JP6	1-2	CLK(1) '1'
	2-3	CLK(1) '0'
JP7	1-2	CLK(0) '1'
	2-3	CLK(0) '0'
JP9	1-2	Enabled
	2-3	Power Down

Mode Pin
Jumper JP2 sets the modulation mode, either ASK or FSK.

Deviation Setting
The FSK deviation is set by jumpers JP3-JP5. The position of these jumpers sets 1 of 8 possible deviation settings. The maximum deviation is highly dependent on the crystal as is the carrier frequency desired. For 315MHz the max deviation is approximately 55kHz. For 433.92MHz the max deviation is approximately 80kHz. The frequency deviation is affected by the motional capacitance of the crystal. For larger deviations, a crystal with a larger motional capacitance should be used. See Table 3 for jumper deviation settings.

TABLE 3: Jumper Deviation Settings

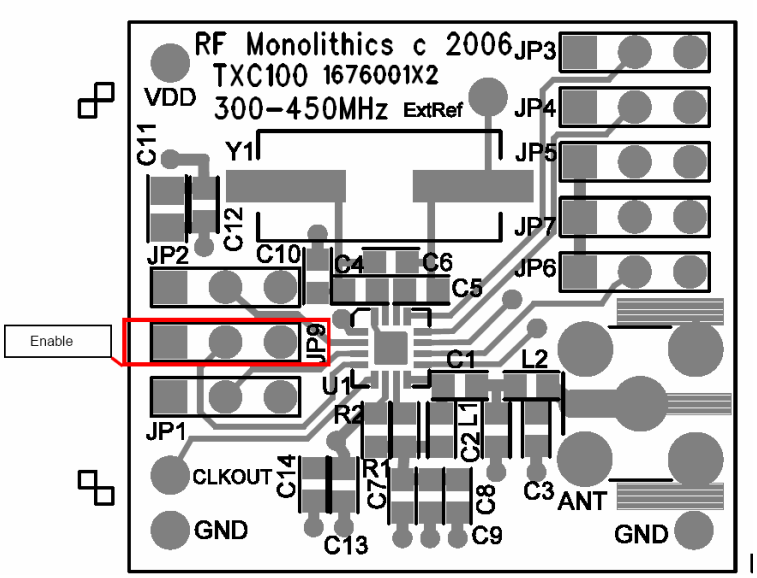
JP3 (bit2)	JP4 (bit1)	JP5 (bit0)	Logic	Description
1-2	1-2	1-2	111	Max Deviation
1-2	1-2	2-3	110	7/8 x Max Dev
1-2	2-3	1-2	101	3/4 x Max Dev
1-2	2-3	2-3	100	5/8 x Max Dev
2-3	1-2	1-2	011	1/2 x Max Dev
2-3	1-2	2-3	010	3/8 x Max Dev
2-3	2-3	1-2	001	1/4 x Max Dev
2-3	2-3	2-3	000	1/8 x Max Dev

Clock Output
The clock output frequency is set by jumpers JP6-JP7. The clock can be used for an on-board microcontroller or as an external timing reference. The clock frequency is the crystal frequency divided by 4, 8, and 16. Table 4 shows the jumper setting to configure the clock frequency.

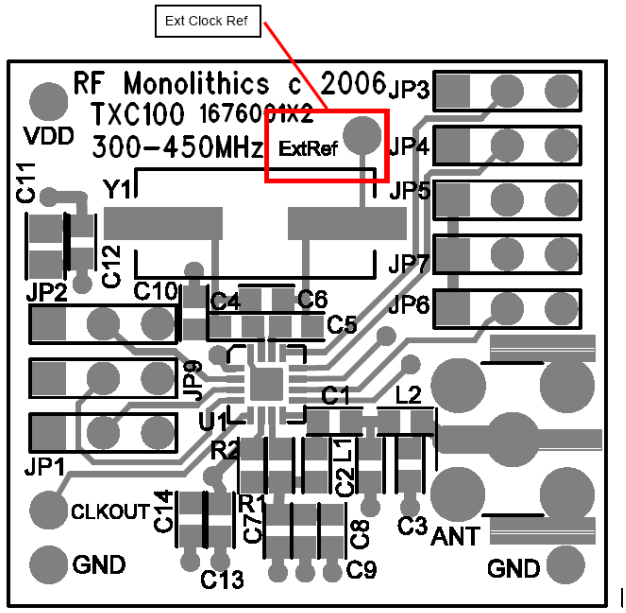
TABLE 4: Jumper Settings for Clock Frequency

JP6 (bit1)	JP7 (bit0)	Logic	Description
1-2	1-2	11	Xtal/16
1-2	2-3	10	Xtal/8
2-3	1-2	01	Xtal/4
2-3	2-3	00	Logic '0' Output

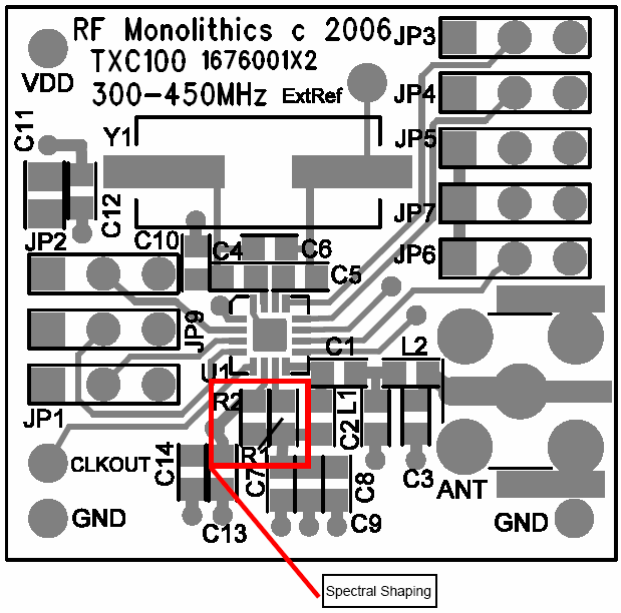
Chip Enable/Standby
The chip can be enabled or put into standby mode by setting jumper JP9. In standby mode the current usage drops to <1nA for ultra low power standby. This pin is internally pulled low so removal of the shunt will automatically put the chip in standby mode. To enable the chip place the shunt jumper across JP9(1-2).



External Reference Input
It is possible to input a custom reference frequency if it is not available as a standard crystal frequency. A test point is provided to apply this frequency from an external source such as a low phase noise RF signal generator. The crystal must be removed to inject this signal. Add .01uF capacitors to C5 and C10 and insert a 0-Ohm, 0603 resistor at C4.



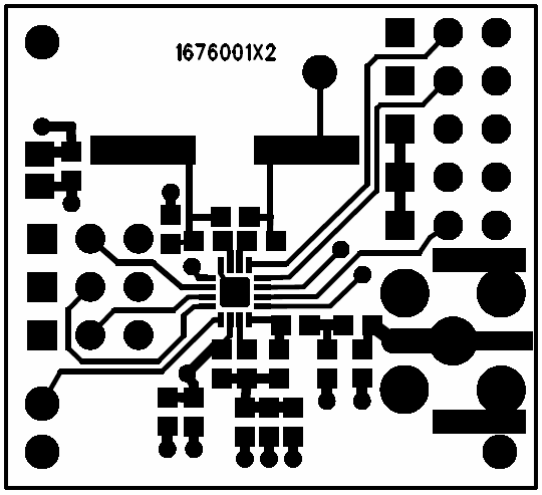
Spectral Shaping Select
Spectral Shaping is used to reduce the sideband noise and harmonics associated with fast switching input data signals. To reduce stray inductance the selection for this option is a soldered component. R1 and R2 select either spectral shape biasing or regular power supply biasing. The DR-TXC100 comes with a 0-Ohm resistor soldered into R2, which selects no spectral shaping. Simply remove R2 and solder in a 0-Ohm, 0603 resistor to R1 to select spectral shaping.

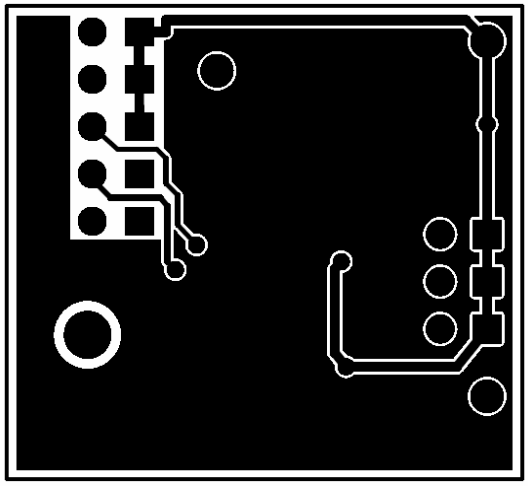


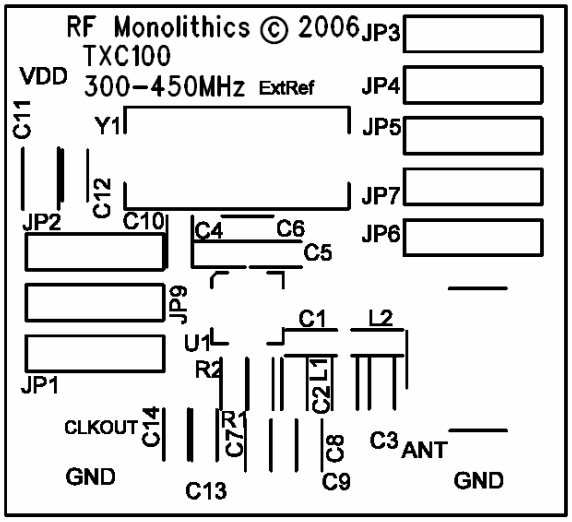
VI. Recommended Layout

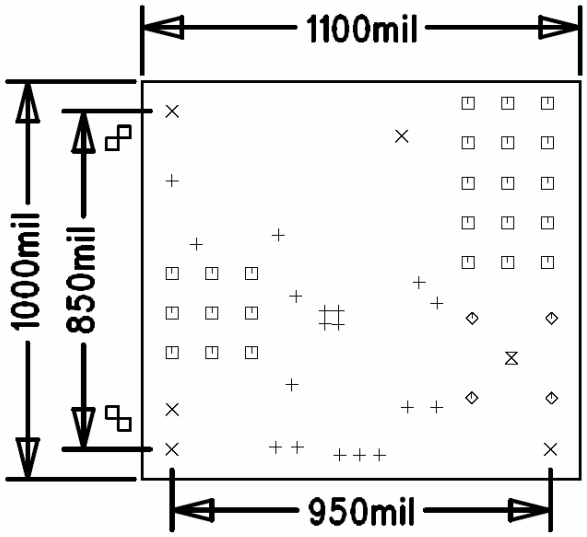
Layout considerations should be addressed for two key areas: crystal and RF output. The crystal is a critical part to the accuracy of the output frequency. Its distance from the chip introduces additional parasitic capacitance to the load capacitance of the crystal. This has the effect of reducing the output frequency slightly. The best approach is to put the crystal as close as possible to the chip to avoid adding additional stray capacitance as much as possible.

The RF output power is heavily dependent upon the matching circuit components and the distance the signal has to travel. By keeping all components related to the RF output as close as possible minimizes any loss associated with long runs to the output connector. Always use a ground plane under any RF signal to keep the impedance constant. Place decoupling capacitors to GND on all VCC pins.









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DR-TXC100 11107
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