2.5V, 3.3V LVCMOS 1:10 Clock Fanout Buffer
AK8180A

Features

- Configurable 3-bank 10 LVCMOS outputs
- Selectable two LVCMOS inputs
- Single, dual and mixed voltage supply available on 2.5V and 3.3V
- Clock output frequency up to 250MHz
- Output-to-output skew : 200ps max
- Tri-state outputs
- Enable to drive up to 20 series terminated clock lines
- Operating Temperature Range: -40 to +85℃
- Package: 32-pin LQFP (Pb free)
- Pin compatible with MPC9446

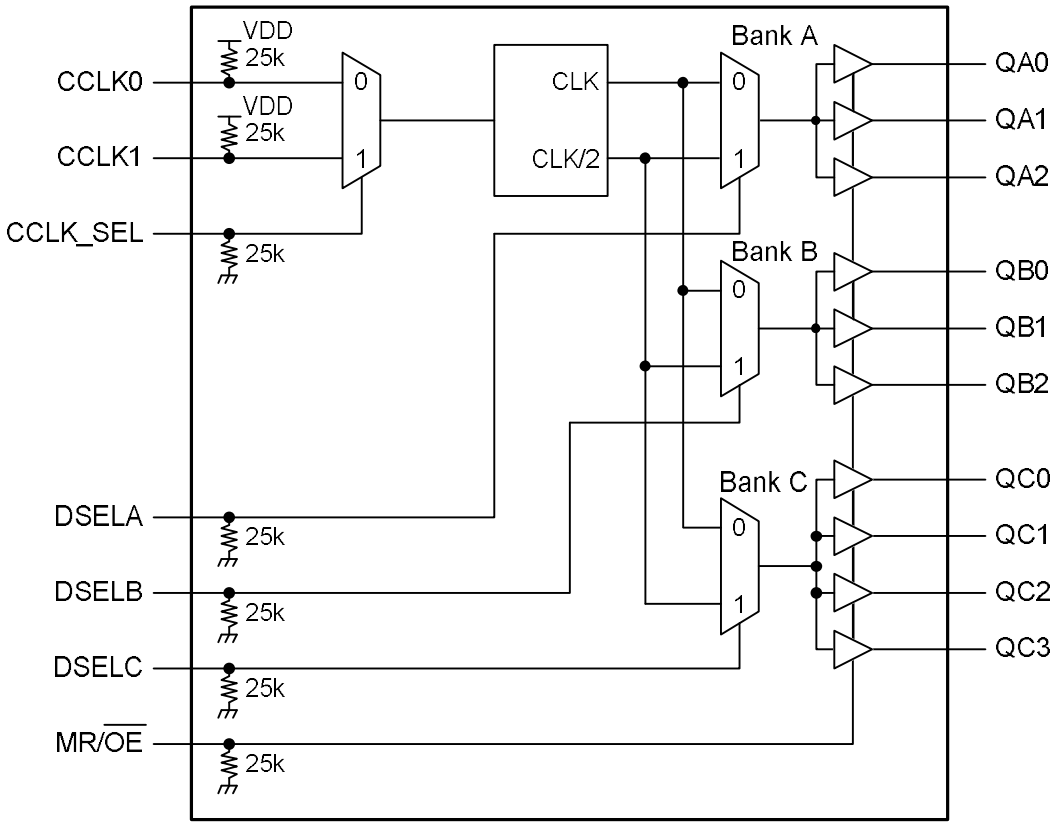
Description

The AK8180A is a member of AKM's LVCMOS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew.

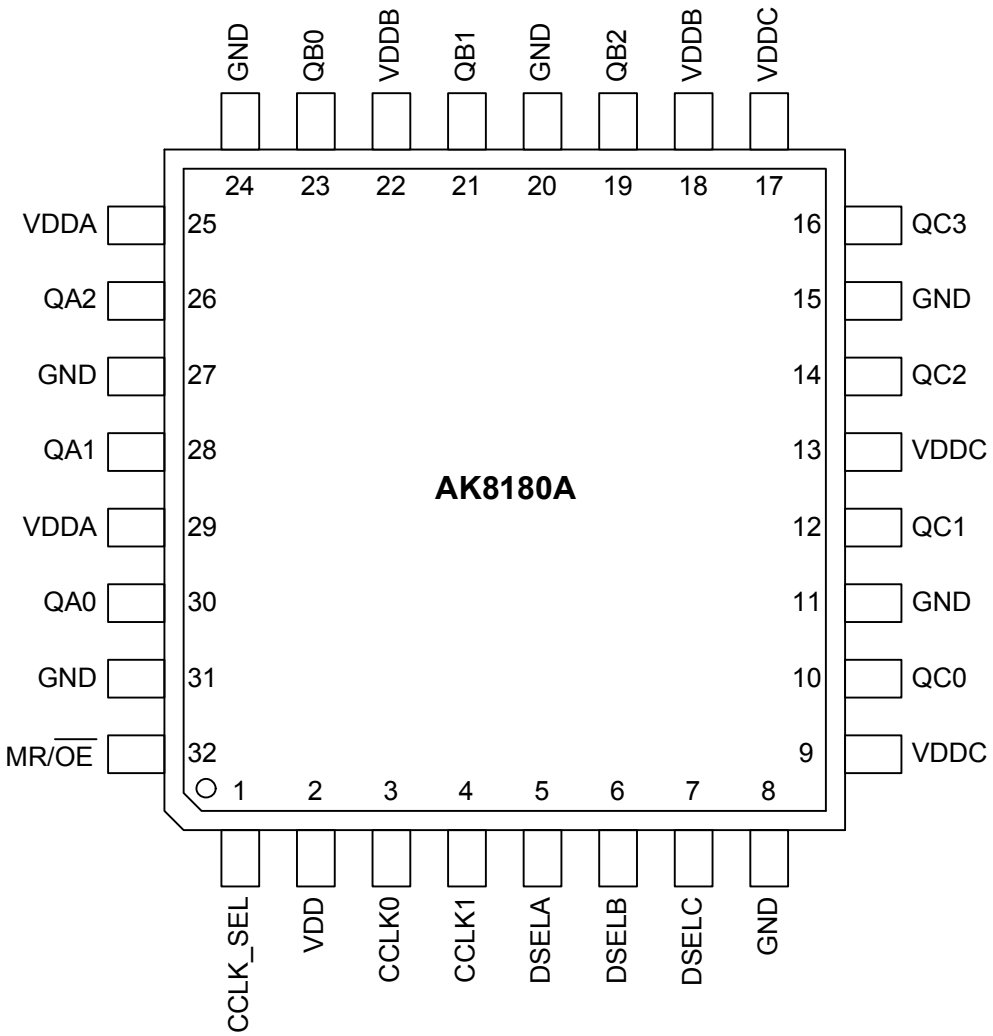
The AK8180A distributes 10 buffered clocks configured by pin-setting per bank. Each bank has the selected output divided by one or two through DSELx pin. Each of 3-bank outputs operate at 2.5V or 3.3V respectively. The 10 outputs can drive terminated 50 Ω transmission lines.

The AK8180A is available in a 7mm x 7mm 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
1	CCLK_SEL	IN	PD	CCLK Select Input.
2	VDD	--	--	Power Supply for Core
3	CCLK0	IN	PU	Clock Inputs
4	CCLK1	IN	PU	Clock Inputs
5	DSELA	IN	PD	Divide Select Input for Output Bank A
6	DSELB	IN	PD	Divide Select Input for Output Bank B
7	DSELC	IN	PD	Divide Select Input for Output Bank C
8,	GND	--	--	Ground
9	VDDC	--	--	Power Supply for Output bank C
10	QC0	OUT	---	Clock output Bank C
11	GND	--	--	Ground
12	QC1	OUT	---	Clock output Bank C

(continued on next page)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
13	VDDC	--	--	Power Supply for Output bank C
14	QC2	OUT	---	Clock output Bank C
15	GND	--	--	Ground
16	QC3	OUT	---	Clock output Bank C
17	VDDC	--	--	Power Supply for Output bank C
18	VDDB	--	--	Power Supply for Output bank B
19	QB2	OUT	---	Clock output Bank B
20	GND	--	--	Ground
21	QB1	OUT	---	Clock output Bank B
22	VDDB	--	--	Power Supply for Output bank B
23	QB0	OUT	---	Clock output Bank B
24	GND	--	--	Ground
25	VDDA	--	--	Power Supply for Output bank A
26	QA2	OUT	---	Clock output Bank A
27	GND	--	--	Ground
28	QA1	OUT	---	Clock output Bank A
29	VDDA	--	--	Power Supply for Output bank A
30	QA0	OUT	---	Clock output Bank A
31	GND	--	--	Ground
32	MR/$\overline{OE}$	IN	PD	Master Reset and Output Enable (Output disable = High impedance)

PU: Pull up PD: Pull down

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8180A	AK8180A	Tape and Reel	32-pin LQFP	-40 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	GND-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD, VDDA	±5%	2.375	2.5	2.625	V
	VDDB, VDDC		3.135	3.3	3.465	

(1) Supply voltages require to be supplied from each single source of 2.5V or 3.3V. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Supported VDD Supply Voltage Configurations

Supply Voltage Configuration	VDD	VDDA	VDDB	VDDC	GND
3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
3.3 V and 2.5 V	3.3 V	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V or 2.5 V	0 V
2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

General Specification

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Termination Voltage	VTT			VDD/2		V
ESD Protection 1	MM	Machine model	200			V
ESD Protection 2	HBM	Human Body Model	2000			V
Latch-Up Immunity	LU		200			mA
Input Capacitance	C_{IN}			4.0		pF

Power Supply Current <3.3V>

VDD=VDDA=VDDB=VDDC= 3.3V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=250MHz CCLK1=H		84	105	mA
Quiescent state (1)	IDD2	CCLK0=H CCLK1=H		0.8	1.7	mA

(1) The outputs have no loads. CCLK_SEL=L, DSELA=DSELB=DSELC=L, MR/$\overline{OE}$ =L

DC Characteristics <3.3V>

All specifications at VDD=VDDA=VDDB=VDDC= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	2.0		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.8	V
Input Current (1)	I_L1	Vin=GND or VDD	-200		+200	μA
High Level Output Voltage	V_{OH}	I_{OH}= -24mA (2)	2.4			V
Low level Output Voltage	V_{OL}	I_{OL}= +24mA (2) I_{OL}= +12mA			0.55 0.30	V
Output Impedance	Z_{OUT}			14-17		Ω

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180A is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

AC Characteristics <3.3V> (1)

All specifications at VDD=VDDA=VDDB=VDDC= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency (2)	f_{IN}	CCLK0,1			250	MHz
Input Pulse Width	t_{pwIN}	CCLK0,1	1.4			ns
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	CCLK0,1 0.8 to 2.0V			1.0	ns
Output Frequency (2)	f_{OUT}	DSELA,B,C= 0 x1 output DSELA,B,C= 1 x1/2 output			250 125	MHz
Propagation Delay	t_{PLH} t_{PHL}	CCLK0,1 to any Q CCLK0,1 to any Q	1.15 1.15	2.0 2.0	3.4 3.4	ns
Output Disable Time	t_{PLZ},t_{PHZ}				10	ns
Output Enable Time	t_{PZL},t_{PZH}				10	ns
Output-to-Output Skew	$t_{sk(O)}$	Within one bank Any output, same output divider Any output, Any output divider			150 200 350	ps
Device-to-Device Skew	t_{skPP}				2.25	ns
Output Pulse Skew (4)	$t_{sk(P)}$				200	ps
Output Duty Cycle (5)	DC_{OUT}	DC_{REF}= 50% x1 output DC_{REF}= 25-75% x1/2 output	45 47	50 50	55 53	%
Output Rise/Fall Time	t_r, t_f	0.55 to 2.4V	0.1		1.0	ns

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) The AK8180A is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times:| t_{PLH} - t_{PHL} |.

(5) Output duty cycle is frequency dependent (= 0.5 ± t_{skO} x fout). For example at fout = 125 MHz the output duty cycle limit is 50% ± 2.5%.

Power Supply Current <2.5V>

VDD=VDDA=VDDB=VDDC= 2.5V±5%, Ta: -40 to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full operation (1)	IDD1	CCLK0=250MHz CCLK1=H		62	75	mA
Quiescent state (1)	IDD2	CCLK0=H CCLK1=H		0.5	1.0	mA

(1) The outputs have no loads. CCLK_SEL=L, DSELA=DSELB=DSELC=L, $\overline{MR/OE}$ =L

DC Characteristics <2.5V>

All specifications at VDD=VDDA=VDDB=VDDC= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	LVCMOS	1.7		VDD+0.3	V
Low Level Input Voltage	V_{IL}	LVCMOS	-0.3		0.7	V
Input Current (1)	I_L1	Vin=GND or VDD	-200		+200	μA
High Level Output Voltage	V_{OH}	I_{OH}= -15mA (2)	1.8			V
Low level Output Voltage	V_{OL}	I_{OL}= +15mA (2)			0.6	V
Output Impedance	Z_{OUT}			17-20		Ω

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180A is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

AC Characteristics <2.5V> (1)

All specifications at VDD=VDDA=VDDB=VDDC= 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency (2)	f_{IN}	CCLK0,1			250	MHz
Input Pulse Width	t_{pwIN}	CCLK0,1	1.4			ns
Input Rise/Fall time (3)	t_{rIN},t_{fOUT}	CCLK0,1 0.7 to 1.7V			1.0	ns
Output Frequency (2)	f_{OUT}	DSELA,B,C= 0 x1 output DSELA,B,C= 1 x1/2 output			250 125	MHz
Propagation Delay	t_{PLH} t_{PHL}	CCLK0,1 to any Q CCLK0,1 to any Q	1.3 1.3	2.4 2.4	4.3 4.3	ns
Output Disable Time	t_{PLZ},t_{PHZ}				10	ns
Output Enable Time	t_{PZL},t_{PZH}				10	ns
Output-to-Output Skew	$t_{sk(O)}$	Within one bank Any output, same output divider Any output, Any output divider			150 200 350	ps
Device-to-Device Skew	t_{skPP}				3.0	ns
Output Pulse Skew (4)	$t_{sk(P)}$				200	ps
Output Duty Cycle	DC_{OUT}	DC_{REF}= 50% x1 or 1/2 output	45	50	55	%
Output Rise/Fall Time	t_r, t_f	0.6 to 1.8V	0.1		1.0	ns

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) The AK8180A is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

AC Characteristics <mixed with 3.3V and 2.5V> (1)(2)

All specifications at VDD=3.3V±5%, VDDA, VDDB, VDDC=2.5V±5%, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Propagation Delay	t_{PLH}	CCLK0,1 to any Q	1.2	2	3.7	ns
	t_{PHL}	CCLK0,1 to any Q	1.2	2	3.7	
Output-to-Output Skew	$t_{sk(O)}$	Within one bank			150	ps
		Any output, same output divider			250	
		Any output, Any output divider			350	
Device-to-Device Skew	t_{skPP}				2.5	ns
Output Pulse Skew (3)	$t_{sk(P)}$				250	ps
Output Duty Cycle	DC_{OUT}	DC_{REF}= 50% x1 or 1/2 output	45	50	55	%

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) For all other AC specifications, refer to 2.5V and 3.3V tables according to the supply voltage of the output bank.

(3) Output pulse skew t_{skO} is the absolute difference of the propagation delay times:| t_{PLH} - t_{PHL} |.

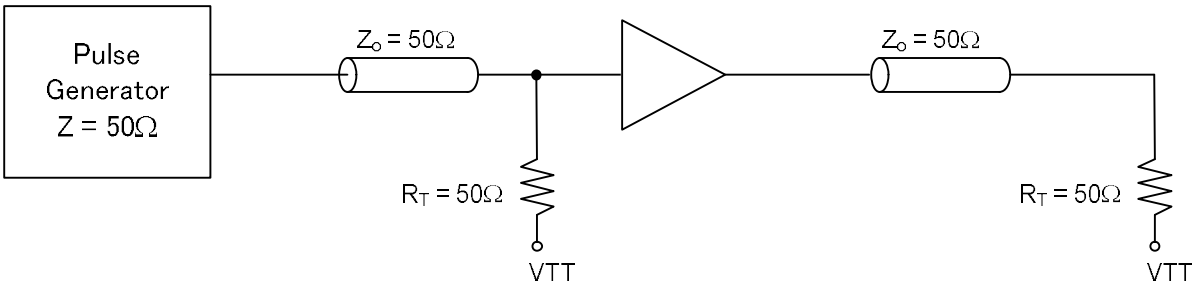


Figure 1 CCLK0,1 AC Test Reference

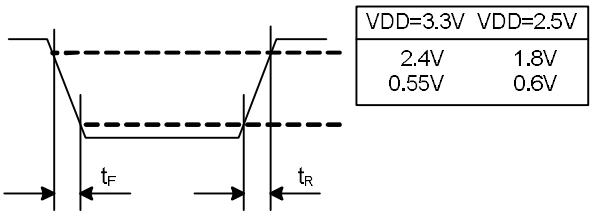


Figure 2 Output Translation Time Test Reference

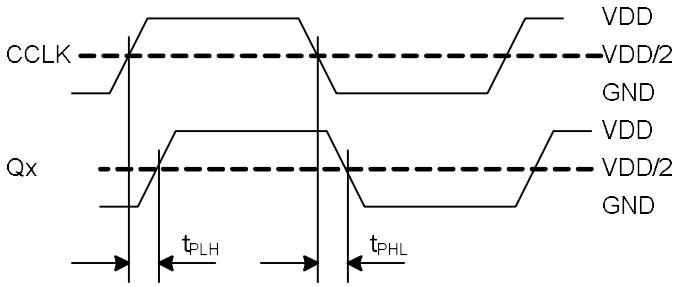
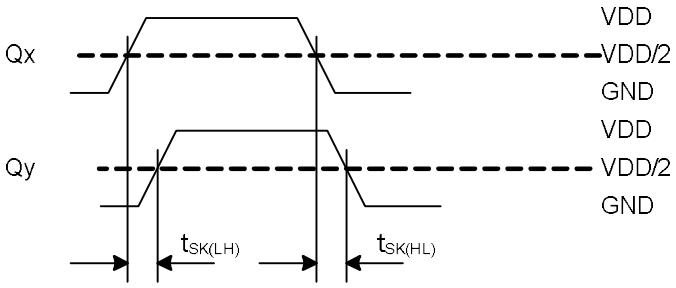
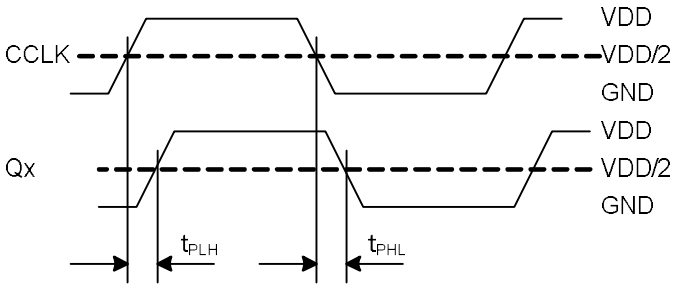


Figure 3 Propagation Delay Test Reference



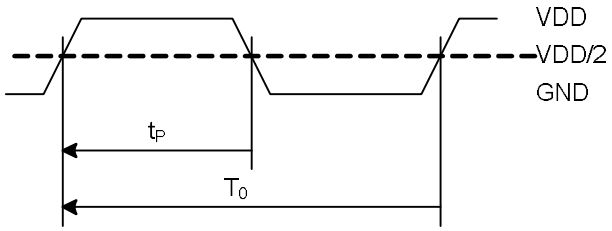
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.

Figure 4 Output-to-Output Skew



$t_{skP} = | t_{PLH} - t_{PHL} |$

Figure 5 Output Pulse Skew Test Reference



$DC = t_P / T_0 \times 100\%$

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 6 Output Duty Cycle (DC)

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

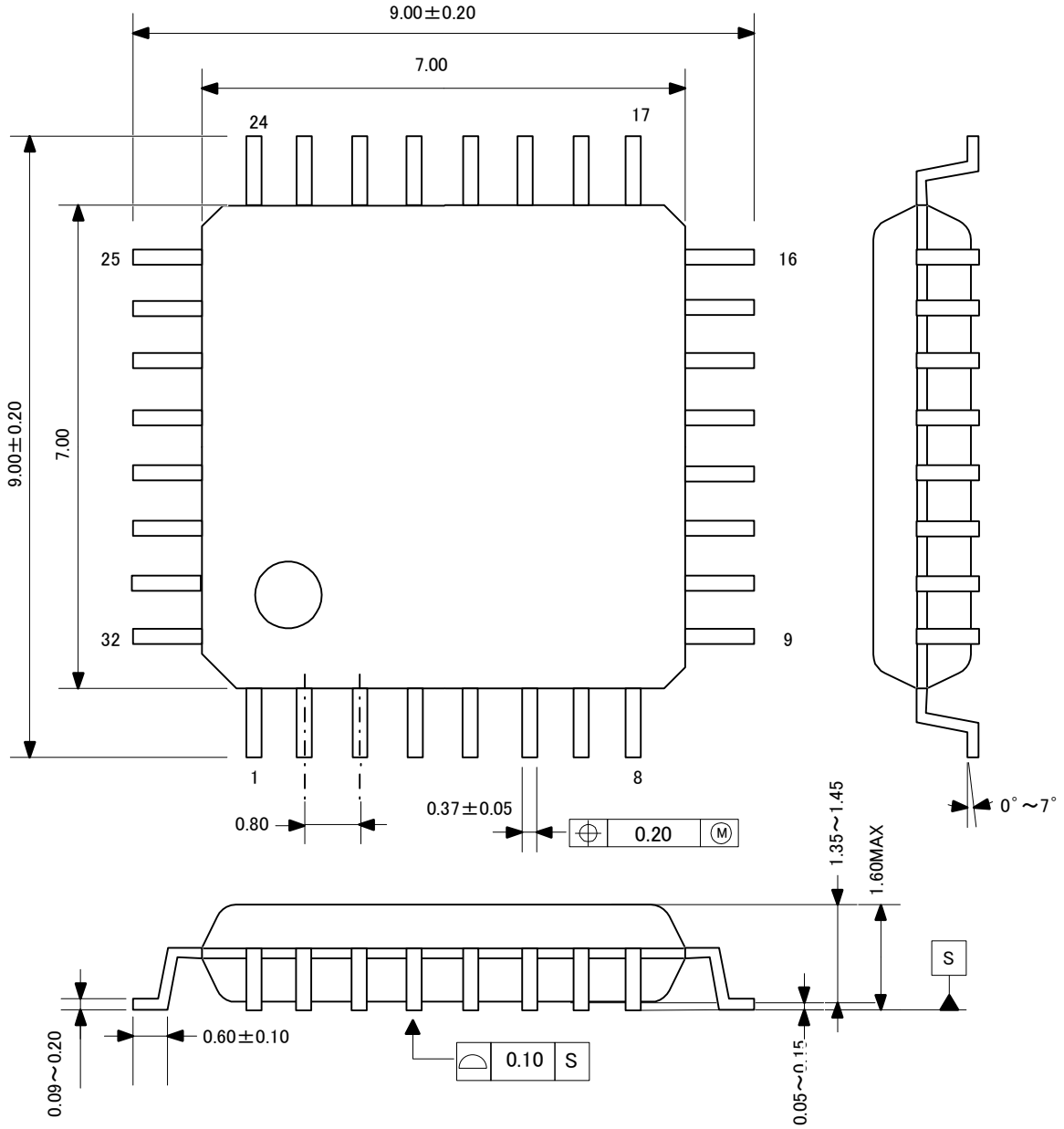
Table 1: Control-Pin-Setting Function Table

Control Pin	Default	0	1
CCLK_SEL	0	CCLK0	CCLK1
DSELA	0	QA0-2 = REFCLK x 1	QA0-2 = REFCLK x 1/2
DSELB	0	QB0-2 = REFCLK x 1	QB0-2 = REFCLK x 1/2
DSELC	0	QC0-3 = REFCLK x 1	QC0-3 = REFCLK x 1/2
MR/$\overline{OE}$	0	Output enabled	Internal reset. Outputs disabled. (High impedance)

REFCLK is the selected input clock through the CCLK_SEL pin.

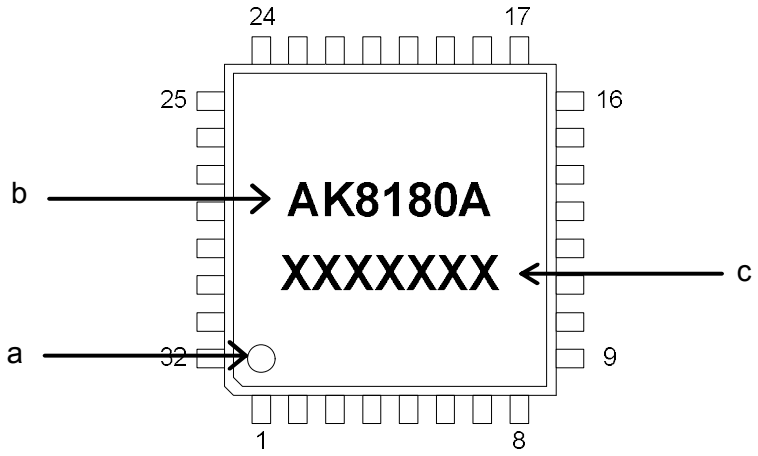
Package Information

- **Mechanical data : 32-lead LQFP**



- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)



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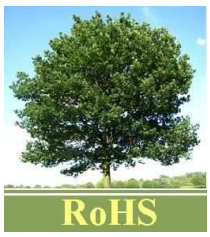
- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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