AK8857VQ
Dual Channel Digital Video Decoder

Overview

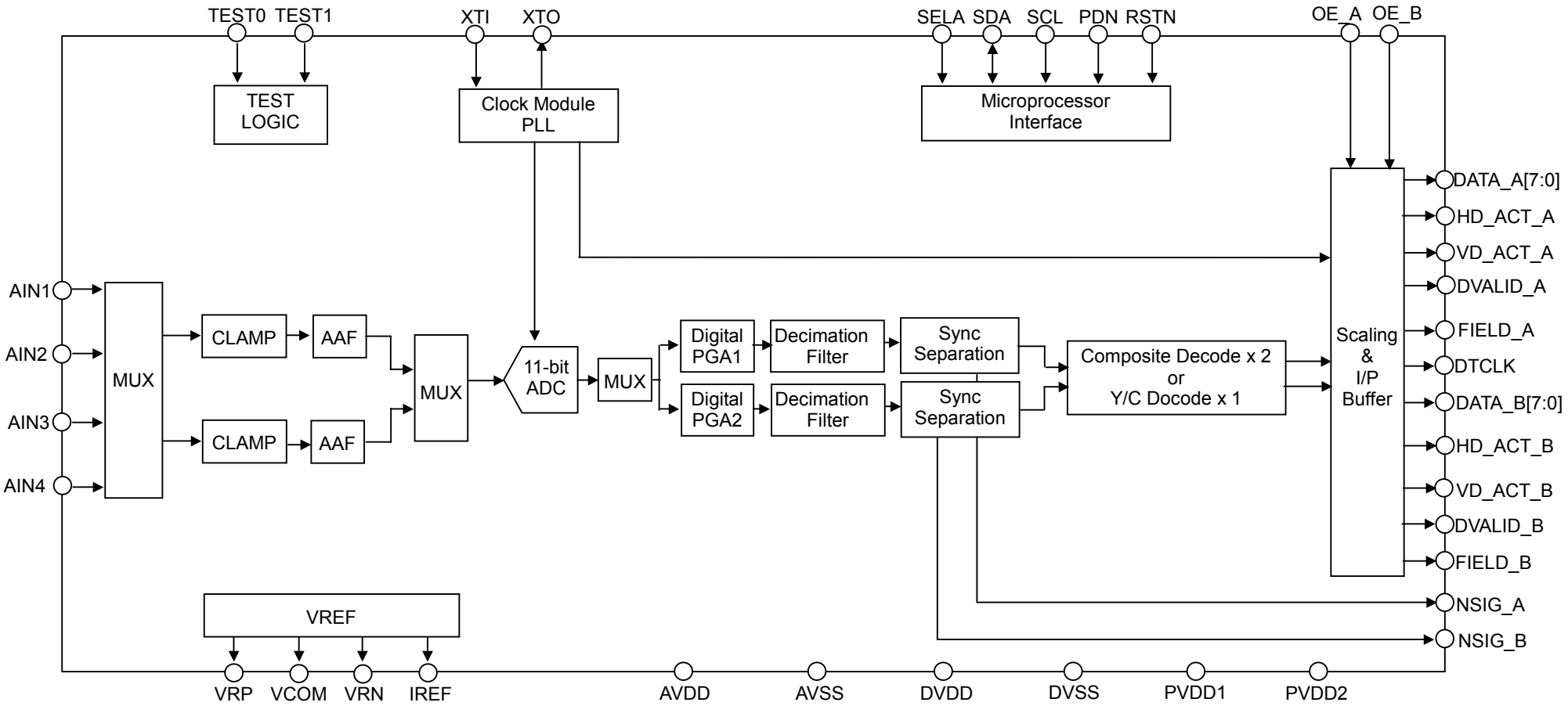
The AK8857VQ is a single-chip digital video decoder for composite and s-video video signals. In case of composite video signal, it can decode two inputs at the same time. Its output data is in YCbCr format, compliant with ITU-R BT.601. Its output interface is ITU-R BT.656 compliant. A simple IP conversion function is built internally and the output pixel size also can easily be changed using this function. The operating temperature range is −40°C to 85°C. The package is 64-terminal LQFP.

Features

- Decodes two inputs of composite video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM at the same time.
- Decodes S-video video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM.
- Four input channels, with internal video switch.
- 11-bit 54Mhz ADC 1 channel.
- Digital PGA.
- Adaptive automatic gain control (AGC).
- Auto Color Control (ACC)
- Simple IP conversion function (Line repeating process).
- Image adjustment (contrast, saturation, brightness, hue, sharpness).
- Automatic input signal detection.
- Adaptive 2-D Y/C separation.
- ITU-R BT.656 and ITU-R BT.601 format output (with 4:2:2_8 bit parallel_EAV/SAV).
- Supported output pixel size : 720x487, 720x576, WVGA, VGA, WQVGA, QVGA
- SYNC signal timing for external output : HSYNC/HACT, VSYNC/VACT, FIELD, DVALID
- Closed-caption signal decoding (output via register).
- VBID(CGMS-A) signal decoding (CRCC decode) (output via register).
- WSS signal decoding (output via register).
- Power down function.
- I^2C control.
- 1.70~2.00 V core power supply.
- 1.70~3.60 V interface power supply.
- Operating temperature range: −40°C to 85°C.
- 64-pin LQFP package.

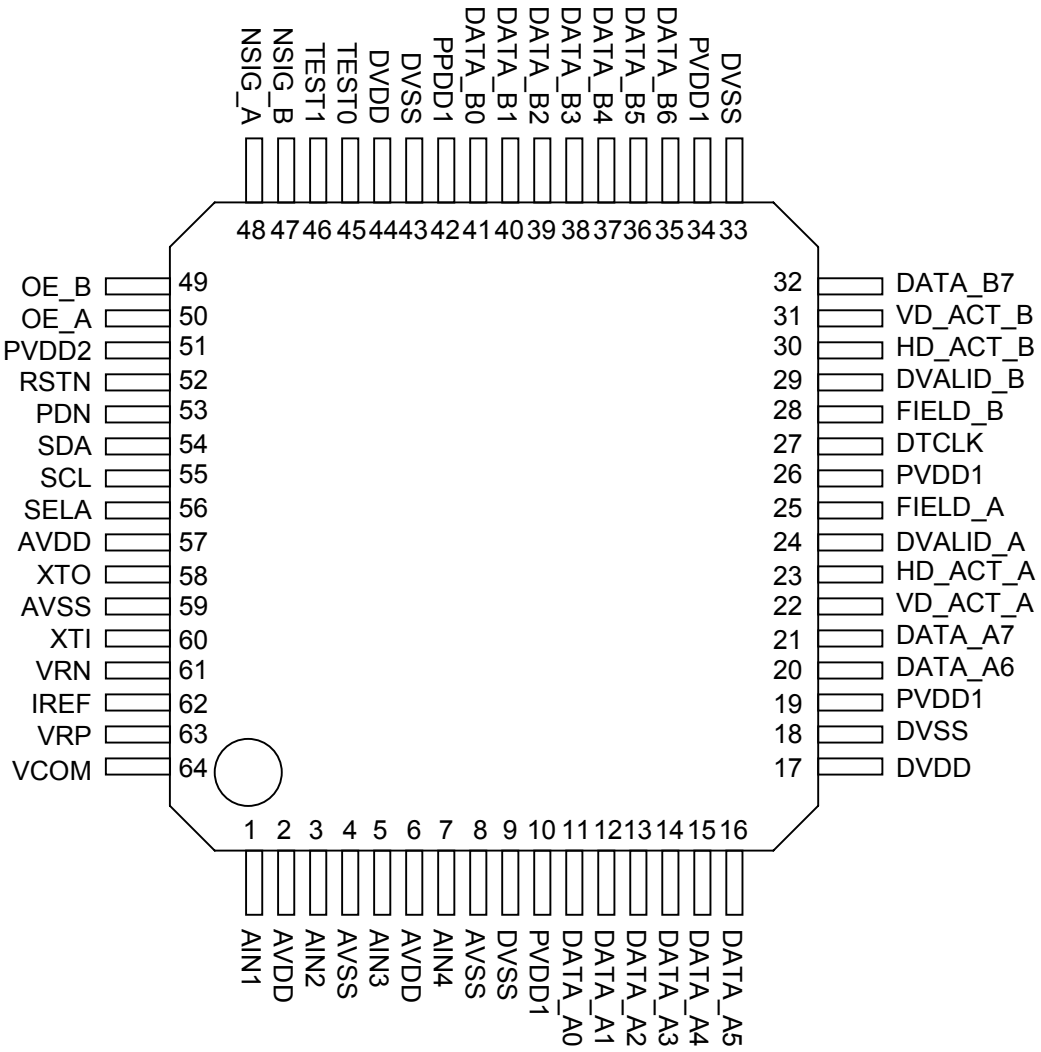
*Because the data is sampling to a fixed clock, it may not fullfilled the ITU-R BT.656 standard interface.

1.Functional Block Diagram



In this specification, the output pins above the DTCLK pin on the right side of this block diagram is called [A BLOCK] and the output pins below the DTCLK pin is called [B BLOCK].

2.Pin assignment – 64 pins LQFP



3.Pin Functions

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
1	AIN1	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
2	AVDD	A	P	Analog ground pin.
3	AIN2	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
4	AVSS	A	G	Analog ground pin.
5	AIN3	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
6	AVDD	A	P	Analog ground pin.
7	AIN4	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 121. If it is not used, connect to NC.
8	AVSS	A	G	Analog ground pin.
9	DVSS	D	G	Digital ground pin.
10	PVDD1	P1	P	I/O power supply pin.
11	DATA_A0	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
12	DATA_A1	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
13	DATA_A2	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
14	DATA_A3	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
15	DATA_A4	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
16	DATA_A5	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
17	DVDD	D	P	Digital power supply pin.
18	DVSS	D	G	Digital ground pin.
19	PVDD1	P1	P	I/O power supply pin.
20	DATA_A6	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
21	DATA_A7	P1	O (I)	A block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
22	VD_ACT_A	P1	O (I)	A block VD(Vertical Drive) / VACT(Vertical Active) signal output pin. VD signal output / VACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
23	HD_ACT_A	P1	O (I)	A block HD(Horizontal Drive) / HACT(Horizontal Active) signal output pin. HD signal output / HACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
24	DVALID_A	P1	O (I)	A block DVALID signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
25	FIELD_A	P1	O (I)	A block FIELD signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_A, PDN and RSTN pin status.
26	PVDD1	P1	P	I/O power supply pin.
27	DTCLK	P1	O	Data clock output pin. Approx. 27 MHz clock output. See Table below for relation of output to OE_A, OE_B, PDN and RSTN pin status.
28	FIELD_B	P1	O (I)	B block FIELD signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
29	DVALID_B	P1	O (I)	B block DVALID signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
30	HD_ACT_B	P1	O (I)	B block HD(Horizontal Drive) / HACT(Horizontal Active) signal output pin. HD signal output / HACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
31	VD_ACT_B	P1	O (I)	B block VD(Vertical Drive) / VACT(Vertical Active) signal output pin. VD signal output / VACT signal output can be selected by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
32	DATA_B7	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
33	DVSS	D	G	Digital ground pin.
34	PVDD1	P1	P	I/O power supply pin.
35	DATA_B6	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
36	DATA_B5	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
37	DATA_B4	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
38	DATA_B3	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
39	DATA_B2	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
40	DATA_B1	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
41	DATA_B0	P1	O (I)	B block data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE_B, PDN and RSTN pin status.
42	PVDD1	P1	P	I/O power supply pin.
43	DVSS	D	G	Digital ground pin.
44	DVDD	D	P	Digital power supply pin.
45	TEST0	P2	I	Pin for test mode setting. Connect to DVSS.
46	TEST1	P2	I	Pin for test mode setting. Connect to DVSS.
47	NSIG_B	P2	O (I)	Shows status of synchronization with input signal of B block. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE_B, PDN, RSTN pin status.
48	NSIG_A	P2	O (I)	Shows status of synchronization with input signal of A block. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE_A, PDN, RSTN pin status.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
49	OE_B	P2	I	B block Output Enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE_B pin is prohibited.
50	OE_A	P2	I	A block Output Enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE_A pin is prohibited.
51	PVDD2	P2	P	Microprocessor I/F power supply pin.
52	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. L: Reset. H: Normal operation.
53	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. L: Power-down. H: Normal operation.
54	SDA	P2	I/O	I^2C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when RSTN=L. Will not accept SDA input during reset sequence.
55	SCL	P2	I	I^2C clock input pin. Use PVDD2 or lower for input. Hi-z input possible when PDN=L. Will not accept SCL input during reset sequence.
56	SELA	P2	I (O)	I^2C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]
57	AVDD	A	P	Analog power supply pin.
58	XTO	A	O	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 10. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
59	AVSS	A	G	Analog ground pin.
60	XTI	A	I	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 10. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
61	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via ≥0.1 μF ceramic capacitor.
62	IREF	A	O	Reference current setting pin. Connect to ground via 6.8 kΩ (≤1% accuracy) resistor.

Pin No.	Symbol	P/S[1]	I/O[2]	Functional Description
63	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via ≥0.1 μF ceramic capacitor.
64	VCOM	A	O	Common internal voltage for AD convertor. Connect to AVSS via ≥0.1 μF ceramic capacitor.

[1]Power supply A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[2]Input/Output O: output pin, I: intput pin, I/O:input/output pin, P: power supply pin,G:ground connection pin.

Output pin status as determined by OE_A, OE_B, PDN, and RSTN pin status.

OE_A, OE_B (*2)	PDN	RSTN	Output1 (*2)	Output2 (*2)
L	x	x	Hi-Z output	L output
H	L	x	L output	L output
H	H	L	L output	L output
		H	Default Data Out (*3)	Default Data Out (*3)

[2]Output1:

(A Block) DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A

(B Block) DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B

DTCLK.

If OE_A and OE_B both are in Low condition, the DTCLK pin output is Hi-Z.

Output2: NSIG_A, NSIG_B

If (OE_A=H or OE_B=H) and PDN=H just after power is turned on, output pin status will be indefinite until internal state is determined by reset sequence.

[3]In the absence of AIN signal input, output will be black data ((Y=0x10, Cb/Cr=0x80).
(Blueback output can be obtained by register setting.)

4.Electrical specifications

(1) Absolute maximum ratings

Parameter	Min	Max	Units	Notes
Supply voltage AVDD, DVDD, PVDD1, PCDD2	 −0.3 −0.3	 2.2 4.2	 V V	
Analog input pin voltage A (VinA)	−0.3	AVDD + 0.3 (≤2.2)	V	
Digital output pin voltage P1 (VioP1)	−0.3	PVDD1 + 0.3 (≤4.2)	V	(*1)
Digital output pin voltage P2 (VioP2)	−0.3	PVDD2 + 0.3 (≤4.2)	V	(*2)
Input pin current (Iin) (except for power supply pin)	−10	10	mA	
Storage temperature	−40	125	ºC	

*The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above for the digital output pin.

(*1) DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A,
DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, DTCLK.

(*2) OE_A, OE_B, SELA, PDN, RSTN, SDA, SCL, NSIG_A, NSIG_B, TEST0, TEST1.

(2) Recommended operating conditions

Parameter	Min	Typ	Max	Units	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/O supply voltage (PVDD1) MPU I/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1≥DVDD PVDD2≥DVDD
Operating temp. (Ta)	−40		85	ºC	

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage).

All power supply grounds (AVSS, DVSS) should be at the same electric potential.

(3) DC characteristics

Where no specific condition is indicated in the following table, the supply voltage range is the same as that shown for the recommended operating conditions in 4-2 above.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage	VPIH	0.8PVDD2			V	Case *1
		0.7PVDD2			V	Case *2
Digital P2 input low voltage	VPIL			0.2PVDD2	V	Case *1
				0.3PVDD2	V	Case *2
Digital input leak current	IL			±10	uA	
Digital P1 output high voltage	VP1OH	0.8PVDD1			V	IOH = -600uA
Digital P1 output low voltage	VP1OL			0.2PVDD1	V	IOL = 1mA
Digital P2 output high voltage	VP2OH	0.8PVDD2			V	IOH = -600uA
Digital P2 output low voltage	VP2OL			0.2PVDD2	V	IOL = 1mA
I^2C (SDA)L output	VOLC			0.4 0.2 PVDD2	V	IOLC = 3mA PVDD2≥2.0V PVDD2<2.0V

*1: < DVDD = 1.70V~2.00V, DVDD≤PVDD1<2.70V, DVDD≤PVDD2<2.70V, Ta: -40~85˚C >

*2: < DVDD = 1.70V~2.00V, 2.70V≤PVDD1≤3.60V, 2.70V≤PVDD2≤3.60V, Ta: -40~85˚C >

Definition of above input/output terms

Digital P2 input : Collective term for SDA, SCL, SELA, OE_A, OE_B, PDN, RSTN, TEST0, TEST1 pin inputs.

Digital P1 output : Collective term for DATA_A[7:0], HD_ACT_A, VD_ACT_A, DVALID_A, FIELD_A, DATA_B[7:0], HD_ACT_B, VD_ACT_B, DVALID_B, FIELD_B, DTCLK pin outputs.

Digital P2 output : Collective term for NSIG_A, NSIG_B pin outputs.

SDA pin output: Not termed digital pin output unless otherwise specifically stated.

(4) Analog characteristics (AVDD=1.8V, Temp.25˚C)

Selector clamp

Parameter	Symbol	Min	Typ	Max	Units	Condition
Maximum input range	VIMX	0	0.50	0.60	V_{PP}	ADC output data is fullcode when input range is 0.6Vpp input.

AD converter

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES		11		bit	
Operating clock frequency	FS		27		MHz	ADC:54MHz
Integral nonlinearity	INL		±2.0	+4.0 -4.0	LSB	FS=27MHz, Input range = 0.5Vpp
Differential nonlinearity	DNL		±0.5	+1.5 -1.0	LSB	FS=27MHz, Input range = 0.5Vpp
S/N	SN		54		dB	Fin=1MHz*, FS=27MHz, Input range = 0.5Vpp
S/(N+D)	SND		52		dB	
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.28		V	
ADC internal negative VREF	VRN		0.64		V	

*Fin = AIN input signal frequency

AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	-1		+1	dB	6MHz
Stop band blocking	Gs	20	35		dB	27MHz

(5) Current consumption (at DVDD = AVDD = PVDD1 = PVDD2 = 1.8V, Ta = −40 ~ 85˚C) (*1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						
Total	IDD1		86	130	mA	CVBS : 2ch
	IDD2		63		mA	CVBS : 1ch (*2)
	IDD3		75	112	mA	S-Video (*2)
Analog block	AIDD		39		mA	CVBS : 2ch With Xtal crystal connected.
Digital block	DIDD		34		mA	CVBS : 2ch
I/O block	PIDD		13		mA	Load condition: CL=12pF, 24pF* (*DTCLK pin)
(Power down mode)						PDN=L(DVSS) (*3)
Total	SIDD		≤ 1	20	uA	
Analog block	ASIDD		≤ 1		uA	
Digital block	DSIDD		≤ 1		uA	
I/O block	PSIDD		≤ 1		uA	

(*1) With NTSC-J 100% color bar input.

(*2) Reference Value. During A Block is set to output, B Block is set to [No Decode].

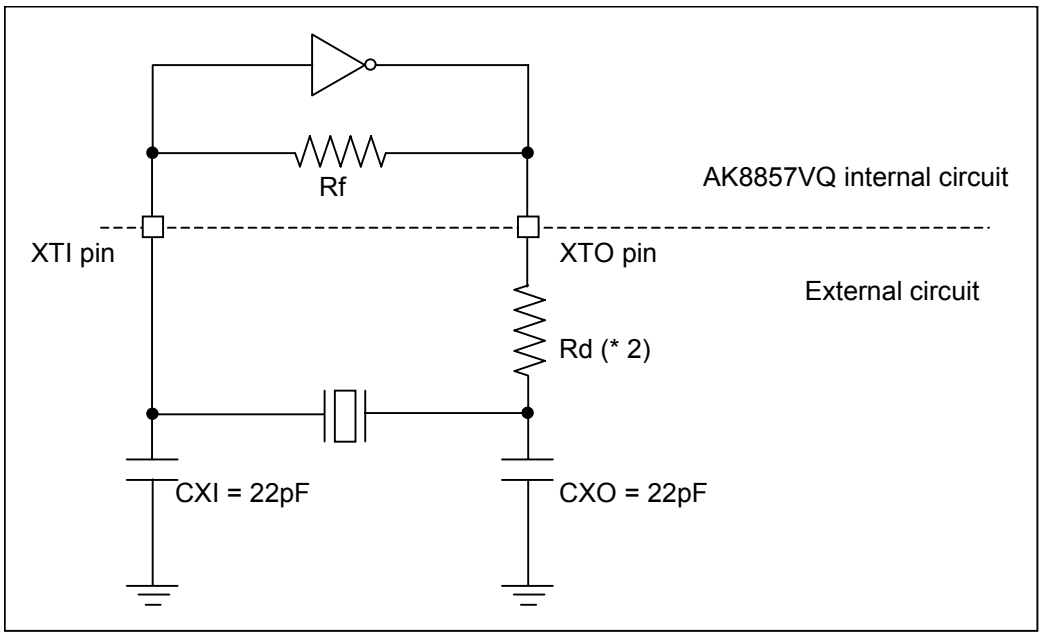
(*3)To perform power-down, OE_A, OE_B and RSTN pins must always be brought to the voltage polarity to be used or to ground level.

(6) **Crystal circuit block** (Ta : -40~85˚C)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Frequency	f_0		27		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	CL=15pF

(*1) Effective equivalent resistance generally may be taken as $Re = R1 \times (1+CO/CL)^2$, where R1 is the crystal series equivalent resistance.

Example connection



(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

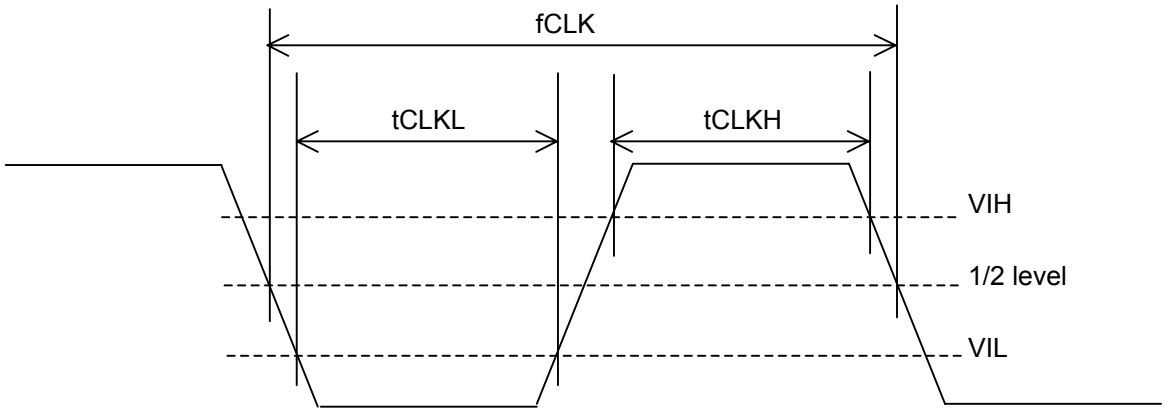
AK8857VQ is hereafter the “AK8857”.

5. **AC Timing**

(DVDD=1.70V~2.00V, PVDD1=DVDD~3.60V, PVDD2=DVDD~3.60V, -40~85˚C)
Load condition: CL=12pF, 24pF(DTCLK pin)

(1) Clock Input

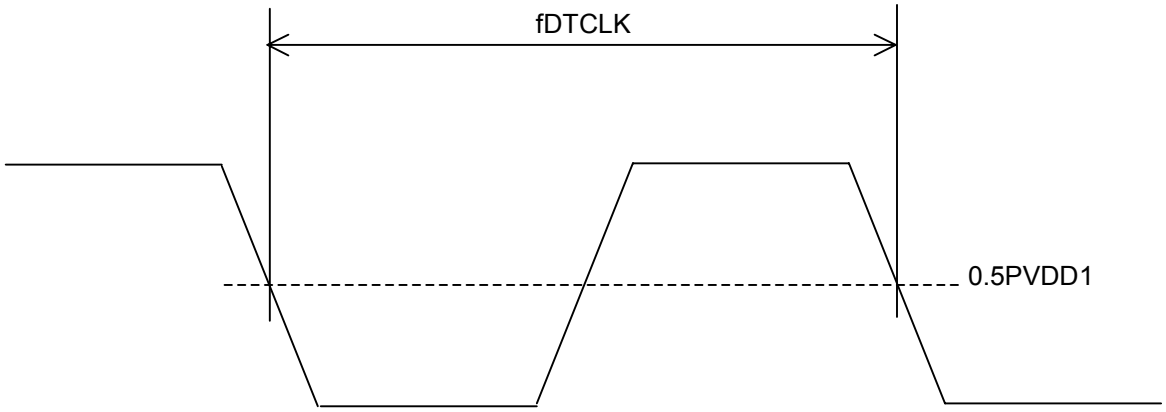
Set AK8857 clock input as follows.



Parameter	Symbol	Min	Typ	Max	Units
Input CLK	fCLK		27		MHz
CLK pulse width H	tCLKH	15			nsec
CLK pulse width L	tCLKL	15			nsec
Frequency tolerance				±100	ppm

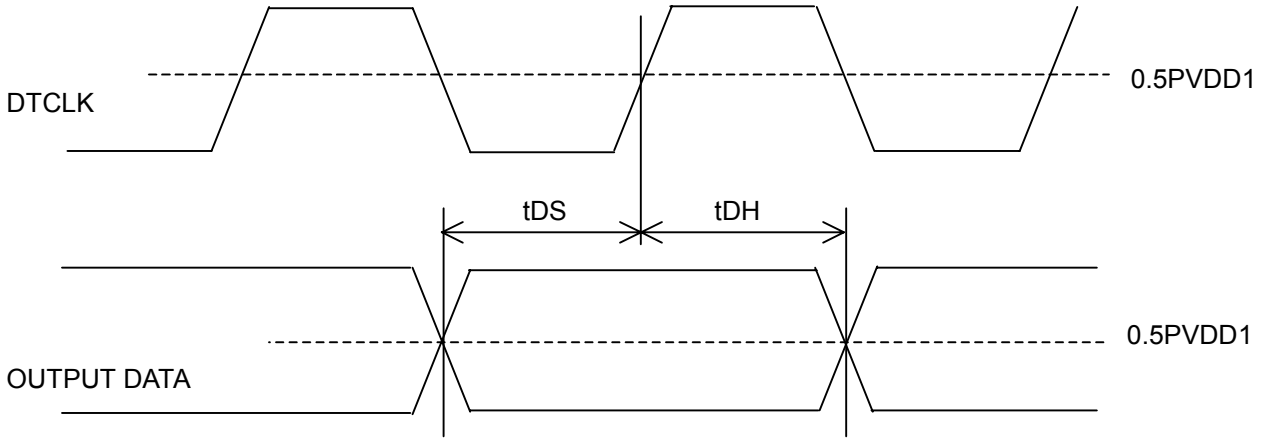
(2) Clock Output (DTCLK output)

Parameter	Symbol	Min	Typ	Max	Units	Output Data Format
DTCLK	fDTCLK		54		MHz	601,VGA, WVGA progressive output.
			27			601,VGA, WVGA other than progressive output.



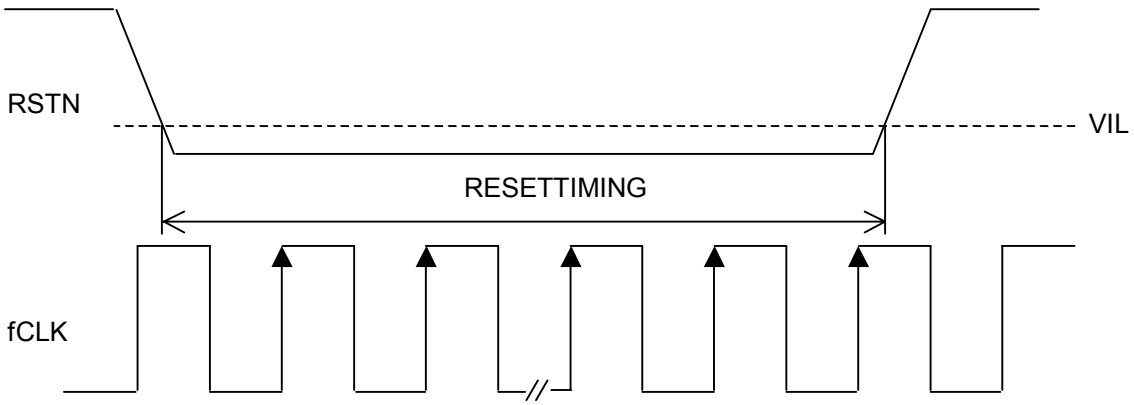
(3) Output Data Timing

DATA_A[7:0], HD_ACT_A, VD_ACT_A, FIELD_A, DVALID_A, DATA_A[7:0], HD_ACT_A, VD_ACT_A, FIELD_A, DVALID_A



Parameter	Symbol	Min	Typ	Max	Units	DTCLK
Output Data Setup Time	tDS	10			nsec	27MHz
		5			nsec	54MHz
Output Data Hold Time	tDH	10			nsec	27MHz
		5			nsec	54MHz

(4) Register reset timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
RSTN pulse width	RESETTIMING	100 (3.7)			CLK (usec)	Based on clock leading edge

Note. Clock input is necessary for reset operation.
RSTN pin must be pulled low following clock application.