

AsahiKASEI

ASAHI KASEI EMD

AK8853XQ/ VN

NTSC/PAL/SECAM Digital Video Decoder

Overview

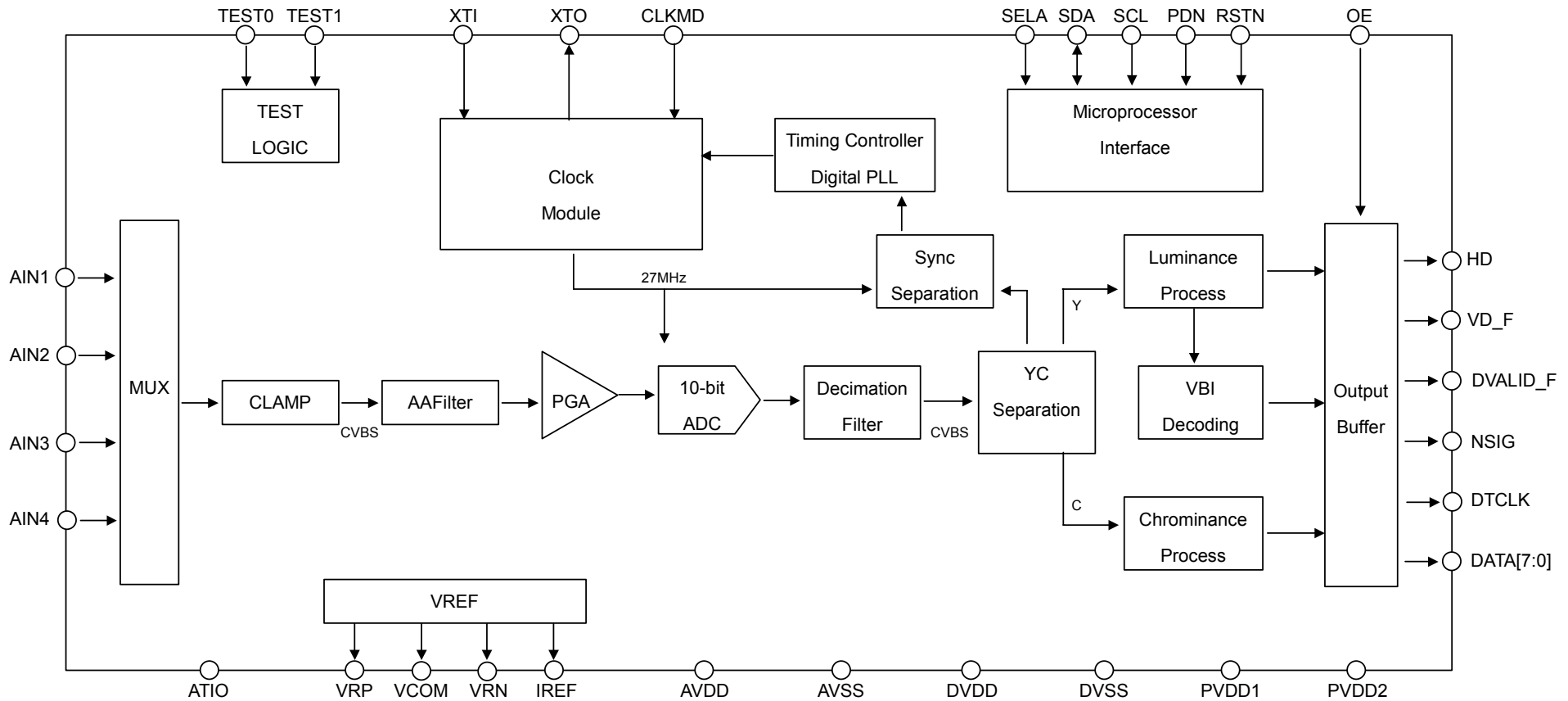
The AK8853 is a single-chip digital decoder for NTSC, PAL, and SECAM composite video signals. Its output data is in YCbCr format, compliant with ITU-R BT.601. Its pixel clock, with a generated clock rate of 27 MHz, synchronizes with the input signal. Its output interface is ITU-R BT.656 compliant. Closed-caption, VBID, and WSS encoded information in the input signal is externally accessible. Microprocessor access is via a I²C interface.

Features

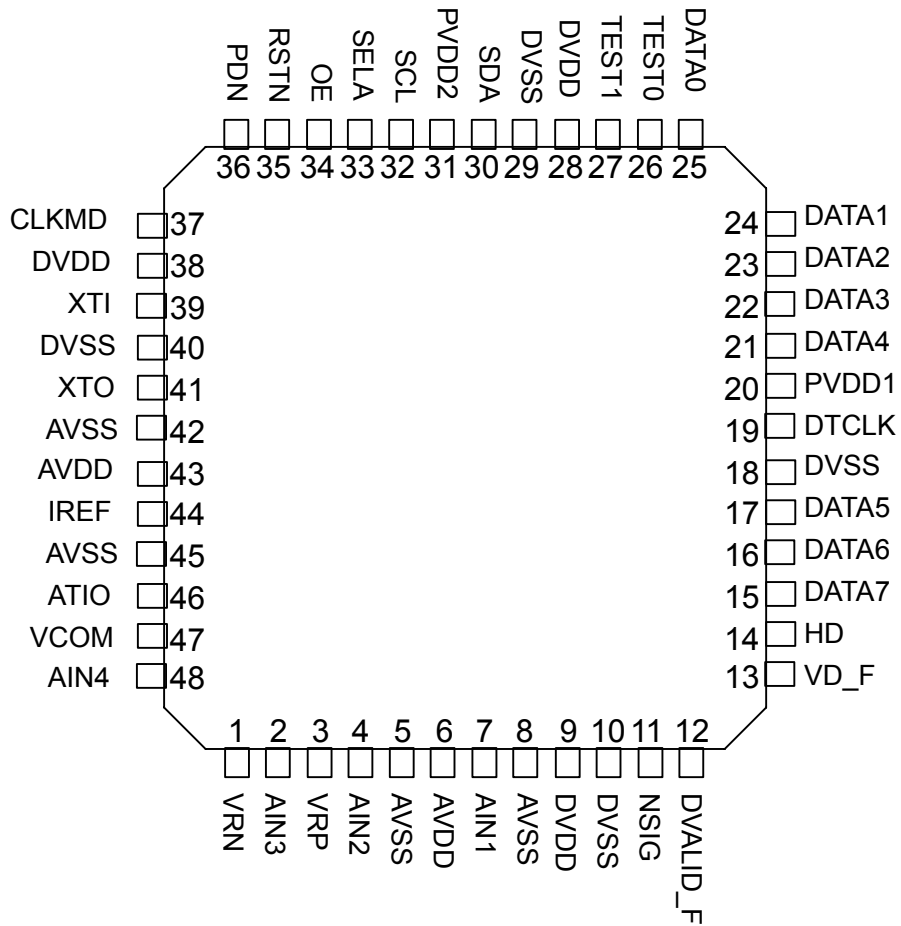
- Decodes composite video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM.
- Four input channels, with internal video switch.
- 10-bit ADC 1 channel.
- Internal line-locked and frame-locked PLLs for generation of clock synchronized with input signal.
- Internal PGA (-6 dB to 6 dB).
- Adaptive automatic gain control (AGC).
- Auto color control (ACC).
- Image adjustment (contrast, saturation, brightness, hue, sharpness).
- Automatic input signal detection.
- Adaptive 2-D Y/C separation.
- PAL decoding phase correction.
- ITU-R BT.656 format output (with 4:2:2_8 bit parallel_EAV/SAV)
- Closed-caption signal decoding (output via register).
- WSS signal decoding (output via register).
- Macrovision signal detection (Macrovision certification).
- Power down function.
- I²C control.
- 1.70~2.00 V core power supply.
- 1.70~3.60 V interface power supply.
- Operating temperature range: -40°C to 105°C. (AK8853XQ)
- Operating temperature range: -40°C to 85°C. (AK8853VN)
- 48-pin LQFP package. (AK8853XQ)
- 48-pin QFN package. (AK8853VN)

(Note) The difference between AK8853XQ and AK8853VN is operating temperature range and package type.

1. Functional block diagram



2. Pin assignment – 48 pins LQFP/ 48 pins QFN



3. Pin functions

Pin No.	Symbol	P/S ¹	I/O ²	Description
1	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via $\geq 0.1 \mu\text{F}$ ceramic capacitor.
2	AIN3	A	I	Analog video signal input pin. Connect via $0.033 \mu\text{F}$ capacitor and voltage-splitting resistors as shown in Sec. 11.
3	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via $\geq 0.1 \mu\text{F}$ ceramic capacitor.
4	AIN2	A	I	Analog video signal input pin. Connect via $0.033 \mu\text{F}$ capacitor and voltage-splitting resistors as shown in Sec. 11.
5	AVSS	A	G	Analog ground pin.
6	AVDD	A	P	Analog power supply pin.
7	AIN1	A	I	Analog video signal input pin. Connect via $0.033 \mu\text{F}$ capacitor and voltage-splitting resistors as shown in Sec. 11.
8	AVSS	A	G	Analog ground pin.
9	DVDD	D	P	Digital power supply pin.
10	DVSS	D	G	Digital ground pin.
11	NSIG	P1	O	Shows status of synchronization with input signal. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE, PDN, RSTN pin status.
12	DVALID_F	P1	O (I/O)	DVALID/FIELD signal output pin. DVALID and FIELD output signals switched by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.
13	VD_F	P1	O	Vertical timing/ field timing signal output pin. VD and FIELD output signals switched by register setting. See Table below for relation of output to OE, PDN, RSTN pin status.
14	HD	P1	O (I/O)	Horizontal timing signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.
15	DATA7	P1	O (I/O)	Data output pin. (MSB) Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.
16	DATA6	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.
17	DATA5	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.
18	DVSS	D	G	Digital ground pin.
19	DTCLK	P1	O	Data clock output pin. Approx. 27 MHz clock output. See Table below for relation of output to OE, PDN, RSTN pin status.
20	PVDD1	P1	P	I/O power supply pin.
21	DATA4	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN, RSTN pin status.

¹Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.

²Input/Output: O, output pin; I, input pin; I/O, input/output pin; P, power supply pin; G, ground connection pin.

Pin No.	Symbol	P/S ¹	I/O ²	Description
22	DATA3	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See table below for relation of output to OE, PDN, RSTN pin status.
23	DATA2	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See table below for relation of output to OE, PDN, RSTN pin status.
24	DATA1	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See table below for relation of output to OE, PDN, RSTN pin status.
25	DATA0	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See table below for relation of output to OE, PDN, RSTN pin status.
26	TEST0	D	I	Pin for test mode setting. Connect to DVSS.
27	TEST1	D	I	Pin for test mode setting. Connect to DVSS.
28	DVDD	D	P	Digital power supply pin.
29	DVSS	D	G	Digital ground pin.
30	SDA	P2	I/O	I ² C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L. Will not accept SDA input during reset sequence.
31	PVDD2	P2	P	Microprocessor I/F power supply pin.
32	SCL	P2	I	I ² C clock input pin. Use PVDD2 or lower for input. Hi-z input possible when PDN=L. Will not accept SCL input during reset sequence.
33	SELA	P2	I	I ² C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]
34	OE	P2	I	Output enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE pin is prohibited.
35	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. L: Reset. H: Normal operation.
36	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. L: Power-down. H: Normal operation.
37	CLKMD	D	I	Clock mode selection pin. Connect to DVDD or DVSS. DVSS connection: For crystal. DVDD connection: For quartz generator or other external clock input; not for crystal.
38	DVDD	D	P	Digital power supply pin.
39	XTI	D	I	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 11. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.

¹Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.

²Input/Output: O, output pin; I, input pin; I/O, input/output pin; P, power supply pin;
G, ground connection pin.

Pin No.	Symbol	P/S ¹	I/O ²	Description
40	DVSS	D	G	Digital ground pin.
41	XTO	D	O	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 11. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
42	AVSS	A	G	Analog ground pin.
43	AVDD	A	P	Analog power supply pin.
44	IREF	A	O	Reference current setting pin. Connect to ground via 6.8 kΩ (≤1% accuracy) resistor.
45	AVSS	A	G	Analog ground pin.
46	ATIO	A	I/O	Analog test pin. For normal operation, connect to AVSS.
47	VCOM	A	O	Common internal voltage for AD convertor. Connect to AVSS via ≥0.1 μF ceramic capacitor.
48	AIN4	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in Sec. 11.

¹Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.

²Input/Output: O, output pin; I, input pin; I/O, input/output pin; P, power supply pin;
G, ground connection pin.

Output pin status as determined by OE, PDN, and RSTN pin status.

OE	PDN	RSTN	Output1 ¹	Output2 ¹
L	x	x	Hi-z output	L output
H	L	x	L output	L output
H	H	L	L output	L output
		H	Default Data Out ²	Default Data Out ²

¹Output1: DATA[7:0], HD, VD_F, DVALID_F, DTCLK

Output2: NSIG

If OE=H and PDN=H just after power is turned on, output pin status will be indefinite until internal state is determined by reset sequence.

²In the absence of AIN signal input, output will be black data ((Y=0x10, Cb/Cr=0x80).
(Blueback output can be obtained by register setting.)

4. Electrical specifications

4.1 Absolute maximum ratings

Parameter	Min	Max	Units	Notes
Supply voltage DVDD, AVDD PVDD1, PVDD2	-0.3 -0.3	2.2 4.2	V V	-
Analog input pin voltage A (VinA)	-0.3	AVDD + 0.3 (≤ 2.2)	V	-
Digital input pin voltage D (VinD)	-0.3	DVDD + 0.3 (≤ 2.2)	V	XTI, XTO, CLKMD, TEST0, TEST1
Digital output pin voltage P1 (VoutP)	-0.3	PVDD1 + 0.3 (≤ 4.2)	V	DTCLK, DATA[7:0], HD, VD_F, DVALID_F, NSIG
Digital input pin current P2 (VinP)	-0.3	PVDD2 + 0.3 (≤ 4.2)	V	OE, SELA, PDN, RSTN, SDA, SCL
Input pin current (Iin) (except for power supply pin)	-10	10	mA	-
Storage temperature	-40	125	°C	-

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage). All power supply grounds (AVSS, DVSS) should be at the same electric potential.

If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above for the digital output pin.

4.2 Recommended operating conditions

Parameter	Min	Typ	Max	Units	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/O supply voltage (PVDD1) MPU I/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1 \geq DVDD PVDD2 \geq DVDD
Operating temp. (Ta)	-40	-	105	°C	AK8853XQ
	-40	-	85	°C	AK8853VN

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage). All power supply grounds (AVSS, DVSS) should be at the same electric potential.

4.3 DC characteristics

Where no specific condition is indicated in the following table, the supply voltage range is the same as that shown for the recommended operating conditions in 4-2 above.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage	VIH	0.8PVDD2	–	–	V	Case 1 ^a
		0.7PVDD2	–	–	V	Case 2 ^b
Digital P2 input low voltage	VIL	–	–	0.2PVDD2	V	Case 1 ^a
		–	–	0.3PVDD2	V	Case 2 ^b
Digital D input high voltage	VDIH	0.8DVDD	–	–	V	–
Digital D input low voltage	VDIL	–	–	0.2DVDD	V	–
Digital input leak current	IL	–	–	±10	uA	–
Digital output high voltage	VOH	0.7PVDD1	–	–	–	IOH = -600uA
Digital output low voltage	VOL	–	–	0.3PVDD1	–	IOL = 1mA
I ² C (SDA)L output	VOLC	–	–	0.3 PVDD2	V	IOLC = 3mA

^aDVDD = 1.70V~2.00V, 1.70V≤PVDD1<2.70V, 1.70V≤PVDD2<2.70V, Ta: Recommended Operating Temp.

^bDVDD = 1.70V~2.00V, 2.70V≤PVDD1≤3.60V, 2.70V≤PVDD2≤3.60V, Ta: Recommended Operating Temp.

Definition of above input/output terms

Digital P2 input: Collective term for SDA, SCL, SELA, OE, PDN, RSTN pin inputs.

Digital D input: Collective term for CLKMD, TEST0, TEST1 pin inputs.

Digital output: Collective term for DTCLK, DATA[7:0], HD, VD_F, DVALID_F, NSIG pin outputs.

SDA pin output: Not termed digital pin output unless otherwise specifically stated.

4.4 Analog characteristics (AVDD=1.8V, Temp.25°C)

Selector clamp

Parameter	Symbol	Min	Typ	Max	Units	Condition
Maximum input range	VIMX	0	0.50	0.60	V _{PP}	Max value at minimum PGA_GAIN setting

PGA

Parameter	Symbol	Min	Typ	Max	Units
Resolution		–	7	–	bits
Minimum gain	GMN	–	–6	–	dB
Maximum gain	GMX	–	6	–	dB
Gain step	GST	–	0.094	0.235	dB

AD converter

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES	10			bits	–
Operating clock frequency	FS	–	27	–	MHz	–
Integral nonlinearity	INL	–	1.0	3.0	LSB	FS = 27 MHz, PGA_GAIN default setting
Differential nonlinearity	DNL	–	0.5	1.5	LSB	FS = 27 MHz, PGA_GAIN default setting
S/N	SN	–	53	–	dB	Fin = 1 MHz*, FS = 27 MHz, PGA_GAIN default setting
S/(N+D)	SND	–	51	–	dB	Fin=1MHz*, FS=27MHz PGA_GAIN default setting
ADC internal common voltage	VCOM	–	0.9	–	V	–
ADC internal positive VREF	VRP	–	1.1	–	V	–
ADC internal negative VREF	VRN	–	0.7	–	V	–

*Fin = AIN input signal frequency

AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	–1		+1	dB	6 MHz
Stop band blocking	Gs	10	22	–	dB	27 MHz

4.5 Current consumption (at DVDD = AVDD = PVDD1 = PVDD2 = 1.8V, Ta = Recommended Operating Temp.)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						a
Total	IDD		58	76	mA	With crystal connected Load condition: CL=15pF
Analog block	AIDD		35		mA	
Digital block	DIDD		19		mA	
I/O block	PIDD		4		mA	
(Power down mode)						
Total	SIDD		≤1	200	uA	
Analog block	ASIDD		≤1		uA	
Digital block	DSIDD		≤1		uA	
I/O block	PSIDD		≤1		uA	

^aWith NTSC-J 100% color bar input.

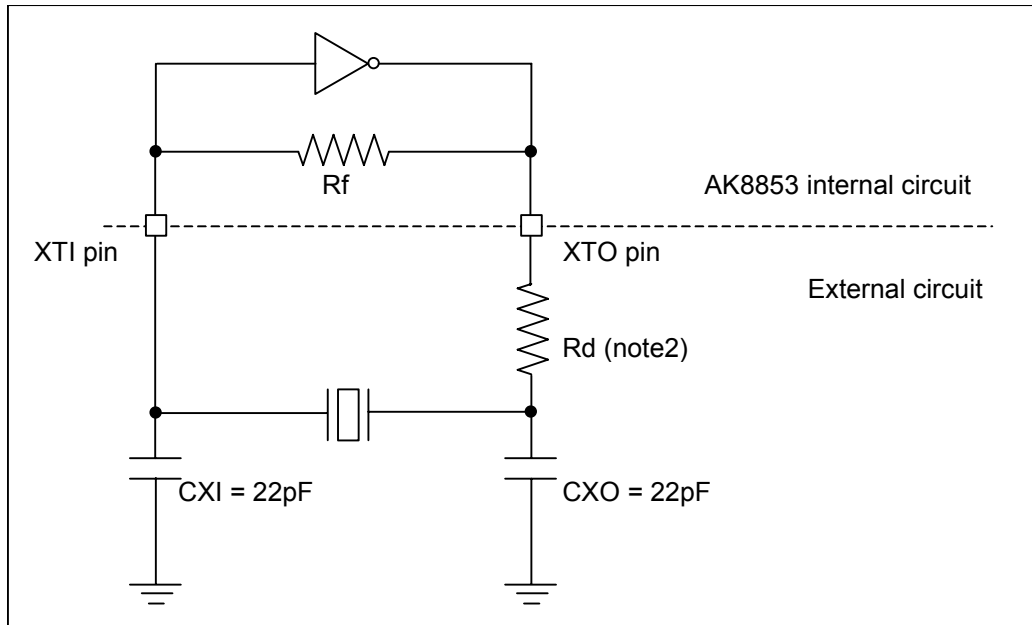
4.6 Crystal circuit block

(Ta: Recommended Operating Temp.)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Frequency	f_0	–	24.576	–	MHz	–
Frequency tolerance	$\Delta f/f$	–		± 100	ppm	–
Load capacitance	CL	–	15	–	pF	–
Effective equivalent resistance	Re	–	–	100	Ω	See note 1
Crystal parallel capacitance	CO	–	0.9	–	pF	–
XTI terminal external connection load capacitance	CXI	–	22	–	pF	If CL=15 pF
XTO terminal external connection load capacitance	CXO	–	22	–	pF	If CL=15 pF

(note1) Effective equivalent resistance generally may be taken as $R_e = R_1 \times (1 + CO/CL)^2$, where R_1 is the crystal series equivalent resistance.

Example connection

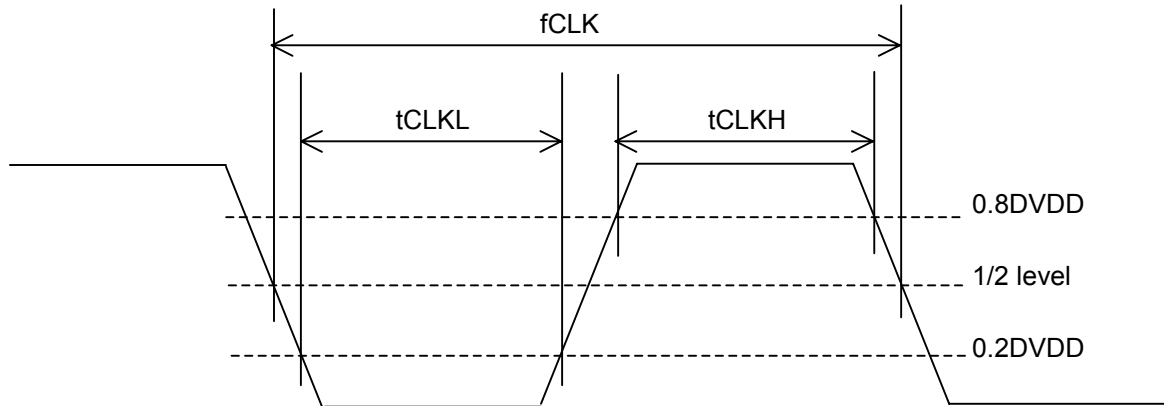


(note2) Determine need for and appropriate value of limiting resistance (R_d) in accordance with the crystal specifications.

5. AC timing (DVDD=1.70V~2.00V, PVDD1=PVDD2=1.70V~3.60V, Recommended Operating Temp.)
 Load condition: CL=15pF

5.1 Clock input

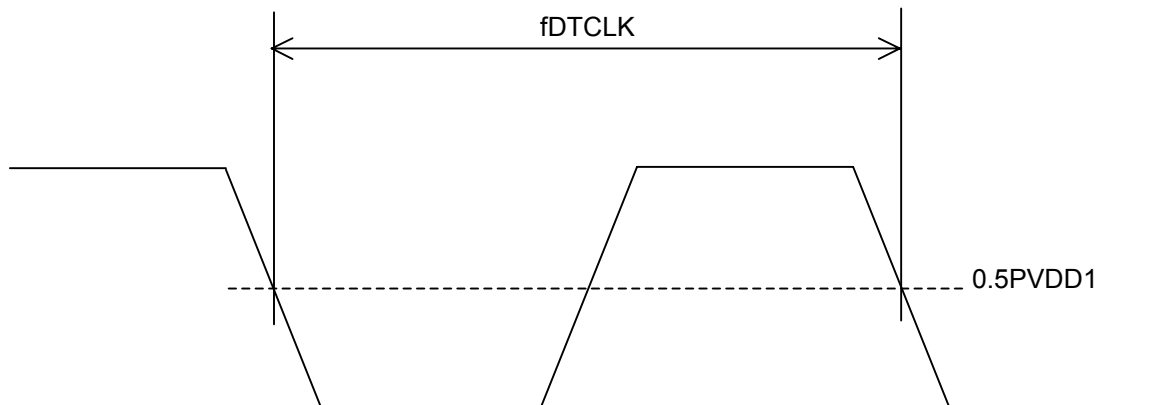
Set AK8853 clock input as follows.



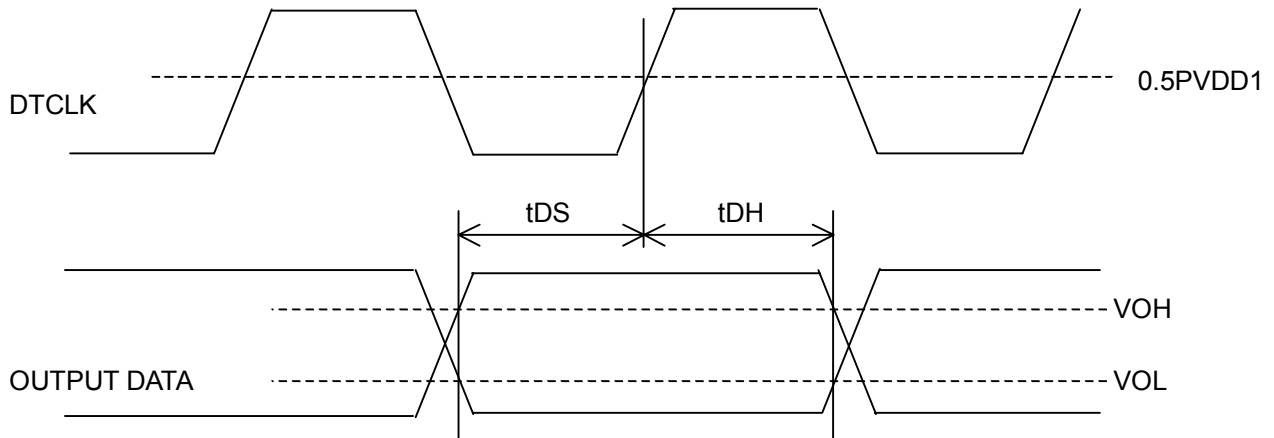
Parameter	Symbol	Min	Typ	Max	Units
Input CLK	f_{CLK}	–	24.576	–	MHz
CLK pulse width H	t_{CLKH}	16	–	–	ns
CLK pulse width L	t_{CLKL}	16	–	–	ns
Frequency tolerance	–	–	–	± 100	ppm

5.2 Clock output (DTCLK output)

Parameter	Symbol	Min	Typ	Max	Units
DTCLK	f_{DTCLK}	–	27	–	MHz

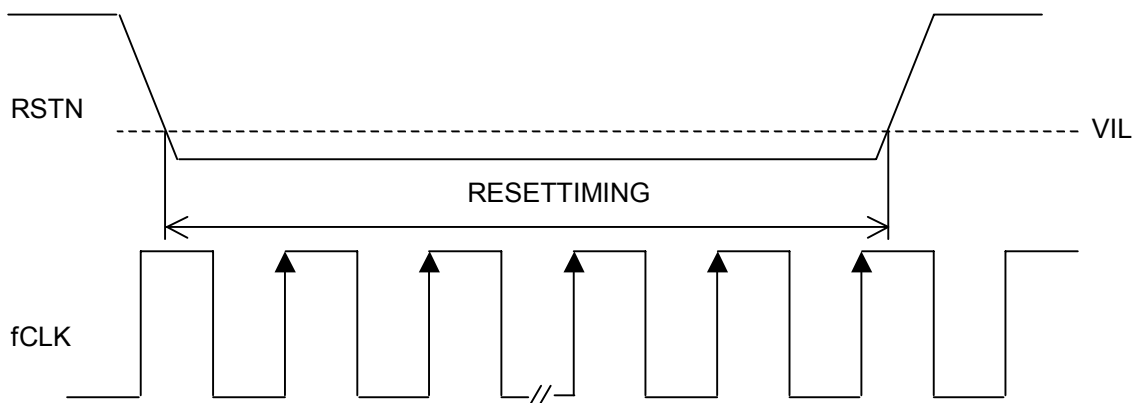


5.3 Output data (DATA[7:0], HD, VD_F, DVALID_F) timing



Parameter	Symbol	Min	Typ	Max	Units
Output Data Setup Time	tDS	10			nsec
Output Data Hold Time	tDH	10			nsec

5.4 Register reset timing

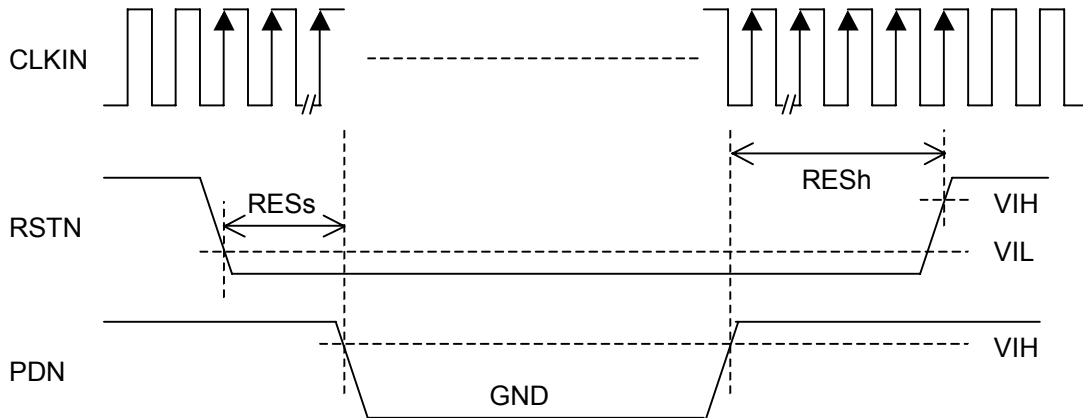


Parameter	Symbol	Min	Typ	Max	Units	Notes
RSTN pulse width	RESETTIMING	100 (4.1)	-	-	CLK (μ sec)	Based on clock leading edge

Note. Clock input is necessary for reset operation.
RSTN pin must be pulled low following clock application.

5.5 Power-down sequence and Reset sequence after power-down

Reset must be applied for at least 2048 clock cycles (or 83.33 μ s) before setting PDN (PDN=Low).
 Reset must be applied for at least 10 ms after PDN release (PDN=Hi).



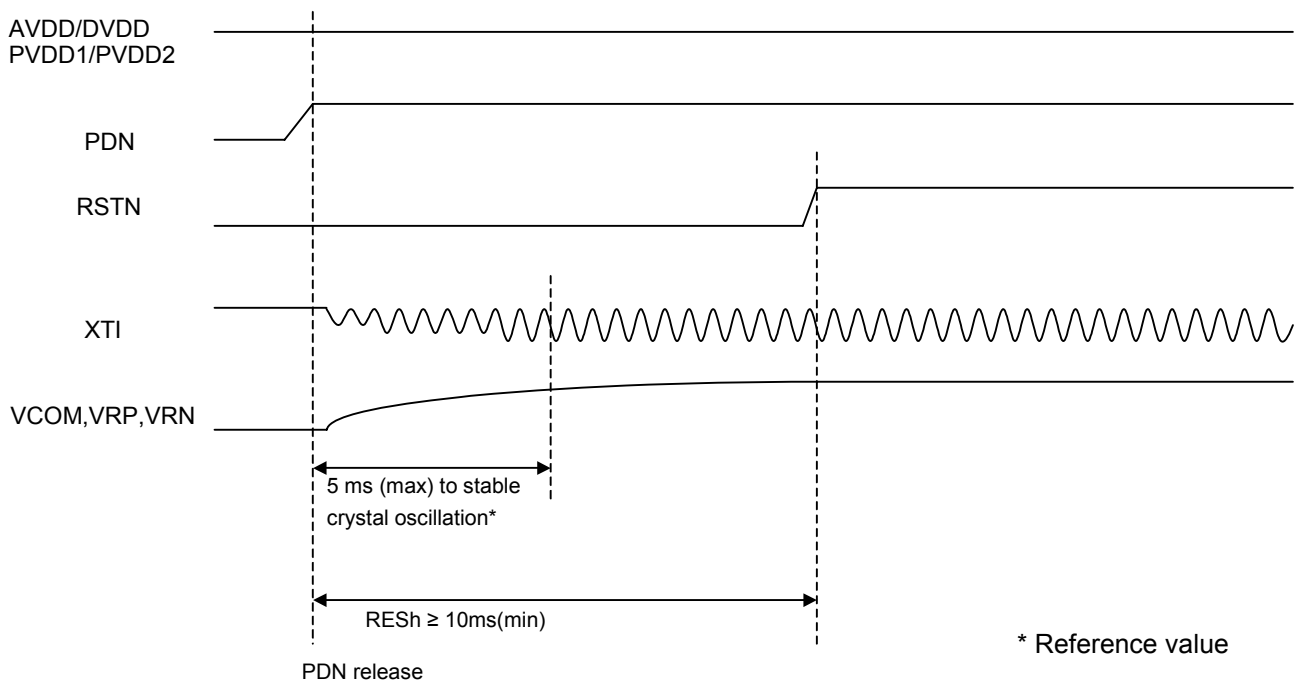
Parameter	Symbol	Min	Typ	Max	Units
Reset width before setting PDN	RESs	2048 (83.33)	-	-	CLK (μ s)
Reset width after PDN release	RESH	10	-	-	ms

To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.

For any power supply removal, all power supplies must be removed.

Clock input is necessary for resetting.

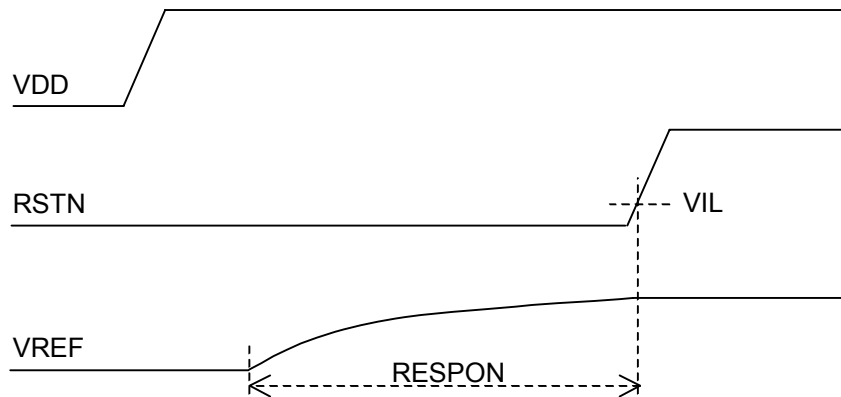
The power-down sequence for connection of the crystal is as follows.



* Reference value

5.6 Power-on reset

At power-on, reset must be applied until the analog reference voltage and current have stabilized.¹ AVDD/DVDD/PVDD1/PVDD2 should be raised simultaneously at power-on.²



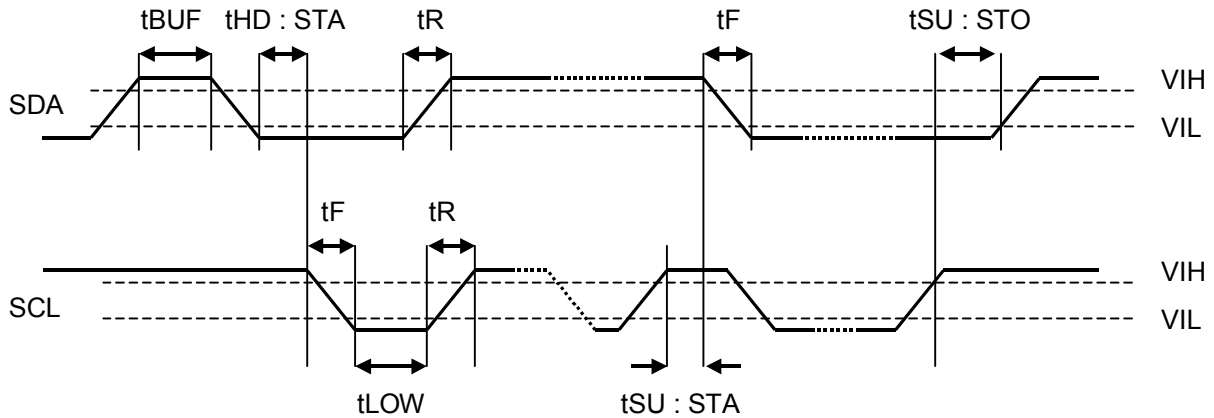
Parameter	Symbol	Min	Typ	Max	Units
RSTN pulse width	RESPON	10			ms

¹Clock input is necessary for resetting.

²If not simultaneous, then raise in the order PVDD2 -> AVDD/DVDD -> PVDD1.

5.7 I²C bus input timing (DVDD=1.70V~2.00V, PVDD1=PVDD2=1.70V~3.60V, Recommended Operating Temp.)

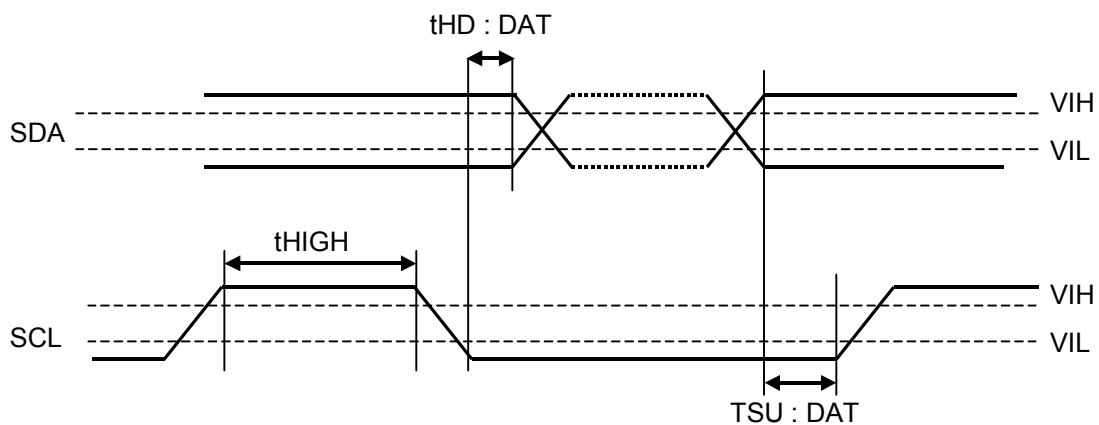
5.7.1 Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

Note. The timing relating to the I²C bus is as stipulated by the I²C bus specification, and not determined by the device itself. For details, see I²C bus specification.

5.7.2 Timing 2



Parameter	Symbol	Min	Typ	Units
Data Setup Time	tSU:DAT	100 ¹		nsec
Data Hold Time	tHD:DAT	0.0	0.9 ²	usec
Clock Pulse High Time	tHIGH	0.6		usec

¹ If I²C is used in standard mode, tSU: DAT ≥ 250 ns is required.

² This condition must be met if the AK8853 is used with a bus that does not extend tLOW (to use tLOW at minimum specification).