



AK4957

24bit Stereo CODEC with MIC/SPK/VIDEO-AMP & LDO

GENERAL DESCRIPTION

The AK4957 is a 24bit stereo CODEC with a microphone, speaker, video amplifiers and LDO. The input circuits include a microphone amplifier and the output circuits include a speaker amplifier. It is suitable for portable application with recording/playback function. A one channel composite In/Out video amplifier is also integrated. The AK4957 is available in a small 32pin QFN (4mm x 4mm, 0.4mm pitch), saving mounting area on the board.

FEATURES

1. Recording Functions

- Stereo Single-ended input with two Selectors
- MIC Amplifier (+21dB/+18dB/+16dB/+14dB/+8dB/0dB)
- Digital ALC (Automatic Level Control)
(Setting Range: +36dB ~ -54dB, 0.375dB Step)
- ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)
S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- Microphone Sensitivity Compensation
- 5 Band Notch Filter
- Stereo Separation Emphasis Circuit
- Digital MIC Interface

2. Playback Functions

- Soft Mute
- Digital ALC (Automatic Level Control)
(Setting Range: +36dB ~ -54dB, 0.375dB Step)
- Digital Volume Control (+12dB ~ -115dB, 0.5dB Step & Mute)
- Stereo Separation Emphasis Circuit
- Stereo Line Output
 - Output Voltage: 1Vrms (AVDD= 3.3V)
 - S/(N+D): 85dB
 - S/N: 92dB
- Mono Mixing Output
- Mono Speaker-Amplifier
 - S/(N+D): 65dB@150mW, 60dB@250mW,
 - S/N: 90dB
 - BTL Output
 - Output Power: 400mW@8Ω (AVDD=3.3V)
- Analog Mixing: BEEP Input

3. Master Clock:
 - (1) PLL Mode
 - Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
32fs or 64fs (BICK pin)
 - (2) External Clock Mode
 - Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
 - Output Master Clock Frequency: 32fs/64fs/128fs/256fs
4. Sampling Frequencies
 - PLL Slave Mode (MCKI pin):
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - PLL Master Mode:
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - EXT Master/Slave Mode:
7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 13kHz (1024fs)
5. μ P I/F: 3-wire Serial, I²C Bus (Ver 1.0, 400kHz Fast-Mode)
6. Master/Slave Mode
7. Audio Interface Format: MSB First, 2's complement
 - ADC: 24bit MSB justified, 16/24bit I²S
 - DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 24bit I²S
8. Video Functions
 - One Composite Signal Input
 - Video Amplifier for Composite Signal Output
Gain: +6 / +9 / +12 / +16.5dB
 - Low Pass Filter
9. Ta = -30 ~ 85°C
10. Power Supply:
 - Analog Power Supply (AVDD): 2.8 ~ 3.6V
 - Digital Power Supply (DVDD): 1.6 ~ 2.0V
 - Digital I/O Power Supply (TVDD): 1.6 or DVDD - 0.2 ~ 3.6V
11. Package: 32pin QFN (4.0 x 4.0 mm, 0.4mm pitch)

■ Block Diagram

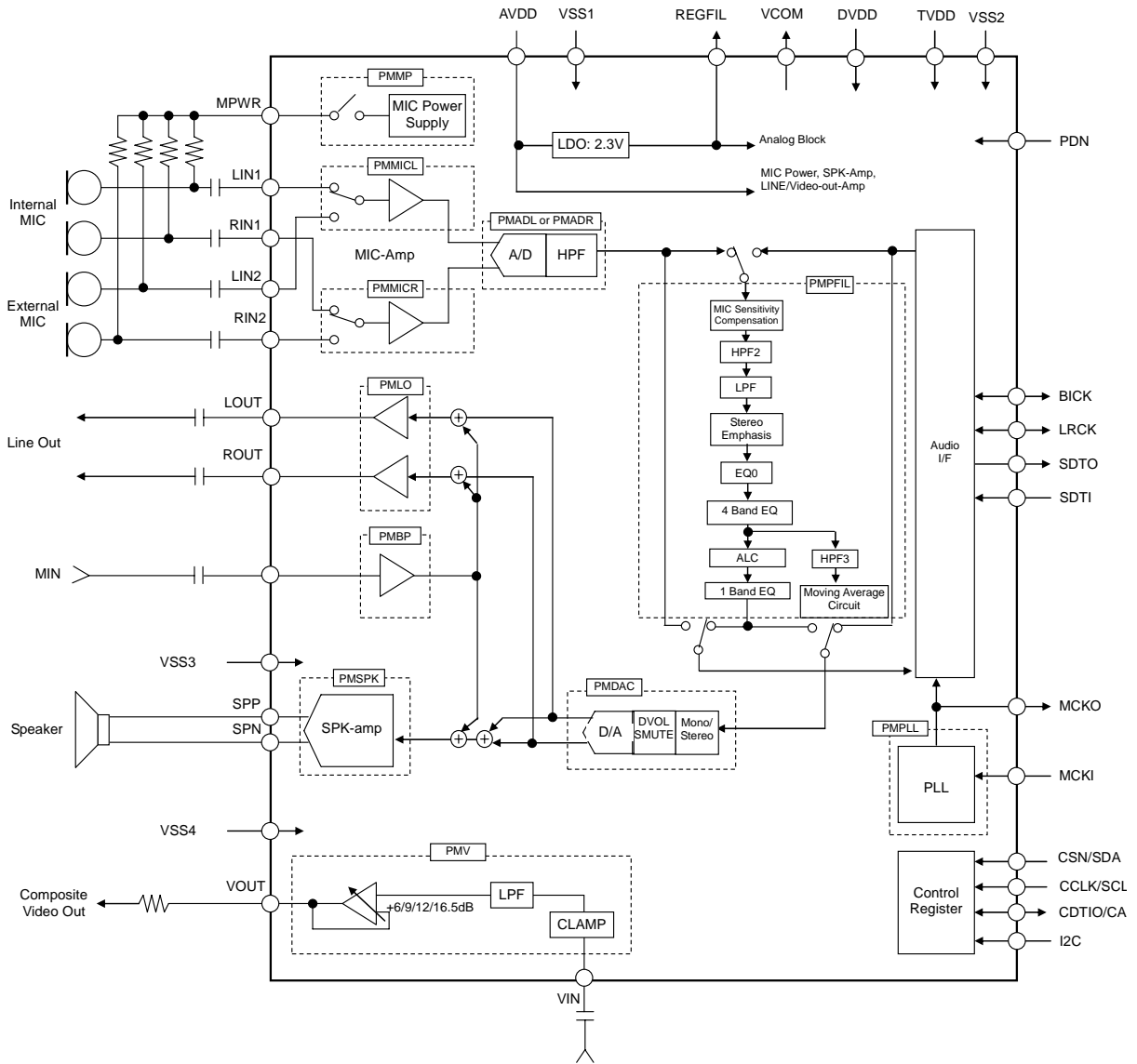


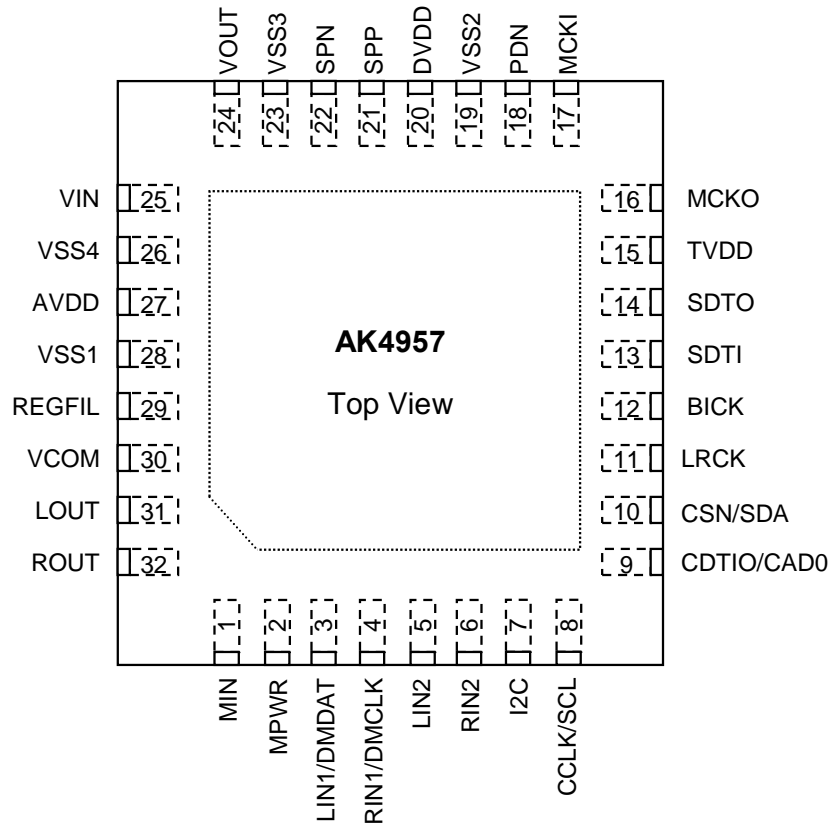
Figure 1. Block Diagram

■ Ordering Guide

AK4957EN
AKD4957

-30 ~ +85°C 32pin QFN (0.4mm pitch)
Evaluation board for AK4957

■ Pin Layout



PIN/FUNCTION

No	Pin Name	I/O	Function
Power Supply			
27	AVDD	-	Analog Power Supply Pin, 2.8 ~ 3.6V This pin must be connected to VSS1 through a 0.1μF ceramic capacitor.
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 through a 2.2μF ±50% capacitor.
28	VSS1	-	Ground 1 Pin
20	DVDD	-	Digital Power Supply Pin, 1.6 ~ 2.0V This pin must be connected to VSS2 through a 0.1μF ceramic capacitor.
15	TVDD	-	Digital Interface Supply Pin, 1.6 or DVDD-0.2V ~ 3.6V
29	REGFIL	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to VSS1 through a 2.2μF ±50% capacitor.
19	VSS2	-	Ground 2 Pin
23	VSS3	-	Ground 3 Pin
26	VSS4	-	Ground 4 Pin
Audio Interface			
17	MCKI	I	Master Clock Input Pin (Note 1)
16	MCKO	O	Master Clock Output Pin
11	LRCK	I/O	Channel Clock Pin (Note 1)
12	BICK	I/O	Audio Serial Data Clock Pin (Note 1)
13	SDTI	I	Audio Serial Data Input Pin (Note 1)
14	SDTO	O	Audio Serial Data Output Pin
Control Register Interface			
10	CSN	I	Chip Select Pin (I2C pin = "L") (Note 1)
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H") (Note 1)
8	CCLK	I	Control Data Clock Pin (I2C pin = "L") (Note 1)
	SCL	I	Control Data Clock Pin (I2C pin = "H") (Note 1)
9	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L") (Note 1)
	CAD0	I	Chip Address Select Pin (I2C pin = "H") (Note 1)
7	I2C	I	Control Mode Select Pin "H": I ² C Bus, "L": 3-wire Serial

Note 1. All input pins except analog input pins (MIN, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

No	Pin Name	I/O	Function
MIC Block			
3	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1") (Note 1)
4	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock Pin (DMIC bit = "1")
5	LIN2	I	Lch Analog Input 2 Pin
6	RIN2	I	Rch Analog Input 2 Pin
2	MPWR	O	MIC Power Supply Pin for Microphone
MIN Block			
1	MIN	I	Mono Analog Signal Input Pin
Lineout Block			
31	LOUT	O	Lch Analog Output Pin
32	ROUT	O	Rch Analog Output Pin
Speaker Block			
21	SPP	O	Speaker Amp Positive Output Pin
22	SPN	O	Speaker Amp Negative Output Pin
Video Block			
25	VIN	I	Composite Video Input Pin
24	VOUT	O	Composite Video Output Pin
Other Functions			
18	PDN	I	Reset & Power-down Pin (Note 1) "L": Reset & Power-down, "H": Normal Operation

Note 1. All input pins except analog input pins (MIN, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, LOUT, ROUT, MIN, RIN2, LIN2, VIN, VOUT	These pins must be open.
	LIN1/DMDAT, RIN1/DMCLK	DMIC bit = "0", and these pins must be open.
Digital	MCKO, SDTO	These pins must be open.
	MCKI, SDTI	These pins must be connected to VSS2.
	LRCK, BICK	M/S bit = "0", and these pins must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	2.5	V
	Digital I/O	TVDD	-0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage	(Note 4)	VIND	-0.3	TVDD+0.3	V
	(Note 6)	VIND	-0.3	6.0	V
Ambient Temperature (powered applied)		Ta	-30	85	°C
Storage Temperature		Tstg	-65	150	°C
Maximum Power Dissipation (Note 6)		Pd1	-	390	mW

Note 2. All voltages are with respect to ground. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.

Note 3. MIN, LIN1, RIN1, LIN2, RIN2, VIN, I2C pins

Note 4. PDN, CDTIO, SDTI, LRCK, BICK and MCKI pins

Note 5. CSN/SDA and CCLK/SCL pins

Note 6. In case that PCB wiring density is over 200%. This power is the AK4957 internal dissipation that does not include power dissipation of externally connected speakers.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 7)	Analog	AVDD	2.8	3.3	3.6	V
	Digital	DVDD	1.6	1.8	2.0	V
	Digital I/O (Note 8)	TVDD	1.6 or DVDD-0.2	1.8	3.6	V

Note 2. All voltages are with respect to ground.

Note 7. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be “L” upon power up, and should be changed to “H” after all power supplies are supplied to avoid an internal circuit error.

Note 8. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When TVDD is powered ON and the PDN pin is “L”, AVDD and DVDD can be powered ON/OFF. When the AK4957 is powered ON from power-down state, the PDN pin must be “H” after all power supplies (AVDD, DVDD and TVDD) are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=3.3V, TVDD= 1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=48kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins					
Input Resistance		22	33	44	kΩ
Gain	MGAIN2-0 bits = "000"	-1	0	+1	dB
	MGAIN2-0 bits = "001"	+7	+8	+9	dB
	MGAIN2-0 bits = "010"	+13	+14	+15	dB
	MGAIN2-0 bits = "011"	+15	+16	+17	dB
	MGAIN2-0 bits = "100"	+17	+18	+19	dB
	MGAIN2-0 bits = "101"	+20	+21	+22	dB
MIC Power Supply: MPWR pin					
Output Voltage	MICL bit = "0"	2.2	2.4	2.6	V
	MICL bit = "1"	1.8	2.0	2.2	V
Output Noise Level (A-weighted)		-	-108	-	dBV
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)		-	100	-	dB
ADC Analog Input Characteristics					
: LIN1/RIN1/LIN2/RIN2 pins → ADC (Programmable Filter = OFF)					
Resolution		-	-	24	Bits
Input Voltage (Note 9)	(Note 10)	-	0.261	-	Vpp
	(Note 11)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)	(Note 10)	73	83	-	dBFS
	(Note 11)	-	85	-	dBFS
D-Range (-60dBFS, A-weighted)	(Note 10)	78	88	-	dB
	(Note 11)	-	96	-	dB
S/N (A-weighted)	(Note 10)	78	88	-	dB
	(Note 11)	-	96	-	dB
Interchannel Isolation	(Note 10)	75	90	-	dB
	(Note 11)	-	100	-	dB
Interchannel Gain Mismatch	(Note 10)	-	0	0.5	dB
	(Note 11)	-	0	0.5	dB
PSRR (Sine Wave = 500mVpp, fin = 1kHz)		-	80	-	dB

Note 9. Vin = 0.9 x 2.3Vpp (typ) @MGAIN2-0 bits = "000" (0dB)

Note 10. MGAIN2-0 bits = "110" (+18dB)

Note 11. MGAIN2-0 bits = "000" (0dB)

Parameter	min	typ	max	Unit	
DAC Characteristics:					
Resolution	-	-	24	Bits	
Stereo Line Output Characteristics: DAC → LOOUT, ROOUT pins, ALC=OFF, DVOL=OVOL =0dB, R _L =10kΩ, PMBP bit = "0", LVCM1-0 bits = "01"					
Output Voltage (0dBFS)(Note 12)	LVCM0 bit = "0" AVDD = 2.8V	-	2.26	-	V _{pp}
	LVCM0 bit = "1"	-	1.00	-	V _{rms}
Output Voltage (-3dBFS) (Note 12)	LVCM0 bit = "0" AVDD = 2.8V	1.44	1.60	1.76	V _{pp}
	LVCM0 bit = "1"	1.82	2.00	2.22	V _{pp}
S/(N+D) (-3dBFS)	75	85	-	dBFS	
S/N (A-weighted)	82	92	-	dB	
Interchannel Isolation	85	100	-	dB	
Interchannel Gain Mismatch	-	0	0.8	dB	
Load Resistance	10	-	-	kΩ	
Load Capacitance	-	-	30	pF	
PSRR (Sine Wave = 500mV _{pp} , fin = 1kHz)	-	80	-	dB	
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL =0dB, R _L =8Ω, BTL					
Output Voltage					
	SPKG1-0 bits = "00", -0.5dBFS (Po=150mW)	-	3.18	-	V _{pp}
	SPKG1-0 bits = "01", -0.5dBFS (Po=250mW)	3.20	4.00	4.80	V _{pp}
	SPKG1-0 bits = "11", -1.8dBFS (Po=400mW)	-	1.79	-	V _{rms}
S/(N+D)					
	SPKG1-0 bits = "00", -0.5dBFS (Po=150mW)	-	65	-	dB
	SPKG1-0 bits = "01", -0.5dBFS (Po=250mW)	20	60	-	dB
	SPKG1-0 bits = "11", -1.8dBFS (Po=400mW)	-	20	-	dB
S/N	SPKG1-0 bits = "01", -0.5dBFS (Po=250mW) (A-weighted)	80	90	-	dB
Load Resistance	6.8	-	-	-	Ω
Load Capacitance	-	-	100	-	pF
PSRR (Sine Wave = 500mV _{pp} , fin = 1kHz)	-	60	-	-	dB

Note 12. The output voltage does not track the AVDD.

Parameter		min	typ	max	Unit
Mono Input: MIN pin, External Resistance mode (PMBP bit = "1", BPM bit = "1", BPVCM bit = "0", BPLVL3-0 bits = "0000"), External Input Resistance= 66kΩ					
Maximum Input Voltage		-	-	1.54	Vpp
Gain (Note 14)					
MIN → LOUT	LVCM1-0 bits = "00"	-4.5	0	+4.5	dB
	LVCM1-0 bits = "01"	-	+2.0	-	dB
	LVCM1-0 bits = "10"	-	+2.0	-	dB
	LVCM1-0 bits = "11"	-	+4.0	-	dB
MIN → SPP/SPN					
	ALC bit = "0", SPKG1-0 bits = "00"	+1.6	+6.1	+10.6	dB
	ALC bit = "0", SPKG1-0 bits = "01"	-	+8.1	-	dB
	ALC bit = "0", SPKG1-0 bits = "10"	-	+10.1	-	dB
	ALC bit = "0", SPKG1-0 bits = "11"	-	+12.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "00"	-	+8.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "01"	-	+10.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "10"	-	+12.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "11"	-	+14.1	-	dB
Mono Input: MIN pin, Internal Resistance Mode (PMBP bit = "1", BPM bit = "0", BPVCM bit = "0", BPLVL3-0 bits = "0000")					
Input Resistance		46	66	86	kΩ
Maximum Input Voltage (Note 13)		-	-	1.54	Vpp
Gain					
MIN → LOUT	LVCM1-0 bits = "00"	-1	0	+1	dB
	LVCM1-0 bits = "01"	-	+2.0	-	dB
	LVCM1-0 bits = "10"	-	+2.0	-	dB
	LVCM1-0 bits = "11"	-	+4.0	-	dB
MIN → SPP/SPN					
	ALC bit = "0", SPKG1-0 bits = "00"	+4.1	+6.1	+8.1	dB
	ALC bit = "0", SPKG1-0 bits = "01"	-	+8.1	-	dB
	ALC bit = "0", SPKG1-0 bits = "10"	-	+10.1	-	dB
	ALC bit = "0", SPKG1-0 bits = "11"	-	+12.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "00"	-	+8.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "01"	-	+10.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "10"	-	+12.1	-	dB
	ALC bit = "1", SPKG1-0 bits = "11"	-	+14.1	-	dB

Note 13. The maximum value is AVDD Vpp when BPVCM bit = "1". However, it must be set as the amplitude after MIN-Amp is less than 0.1Vpp. (set by BPLVL3-0 bits)

Note 14. The gain is in inverse proportion to external input resistance.

Parameter		min	typ	max	Unit
Video Signal Input					
External Resistor (Note 16)	R1 (Figure 2)	0.075	-	1.6	kΩ
External Capacitor	C1 (Figure 2)	0.02	0.047	0.2	μF
Maximum Input Voltage: VG1-0 bits = "00" (+6dB)		-	1.2	-	Vpp
Pull Down Current		-	0.125	-	μA
Video Analog Output (Figure 3)					
Output Gain fin = 100kHz Sine wave Input (Note 15)	VG1-0 bits = "00", 1.0Vpp Input	5.5	6.0	6.5	dB
	VG1-0 bits = "01", 0.7Vpp Input	8.5	9.0	9.5	
	VG1-0 bits = "10", 0.5Vpp Input	11.5	12.0	12.5	
	VG1-0 bits = "11", 0.3Vpp Input	16	16.5	17	
Clamp Level (Note 15)		-	50	100	mV
S/N (Note 17) VG1-0 bits = "00" (+6dB)	BW = 100kHz ~ 6MHz, S = 0.7Vpp Input	60	70	-	dB
Maximum Output Voltage (Note 15)	fin = 100kHz (Sine wave)	2.54	-	-	Vpp
Secondary Harmonic Distortion VG1-0 bits = "00" (+6dB) fin = 3.58MHz	860mVpp: -20 ~ 100IRE, Sine Wave Input (Flat Field = 100 IRE Burst = -20IRE)	-	-45	-35	dB
Load Resistance		140	150	-	Ω
Load Capacitance	C2 (Figure 3)	-	-	15	pF
	C3 (Figure 3)	-	-	400	pF
PSRR VG1-0 bits = "00" (+6dB)(Note 18)	fin = 10kHz	-	60	-	dB
	fin = 100kHz	-	45	-	dB
LPF for VIN signal : (Note 15)					
Frequency Response (fin = 100kHz, 1.0Vpp, Sine wave Input)					
	Response at 6.75MHz	-3.0	-0.5	+2.0	dB
	Response at 27MHz	-	-47	-20	
Group Delay	GD3MHz-GD6MHz	-	15	100	ns

Note 15. This is a value at measurement point in Figure 3. 1.0Vpp input is the value when VG1-0 bit = "00". Input amplitude is in inverse proportion to the gain. S/N and Secondary Harmonic Distortion values are measured at measuring point 2.

Note 16. PMV bit must be set to "0" if the resistor value exceeds the range from 0.075 to 1.6kΩ in case of the input signal is stopped or the input circuit of the VIN pin is powered down.

Note 17. S/N = 20xlog (Output Voltage[Vpp]/Noise Level[Vrms]). Output Voltage = 0.7 [Vpp].

Note 18. PSRR is applied to AVDD with 500mVpp sine wave when DC level of -20IRE, 0IRE and 100IRE are input to the VIN pin.

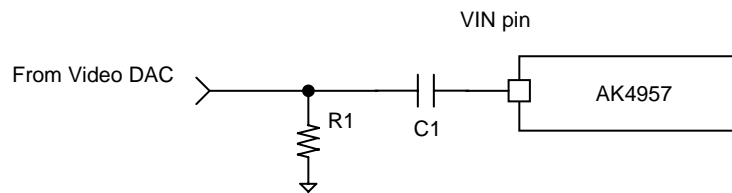


Figure 2. External Resistor of Video Signal Input pin

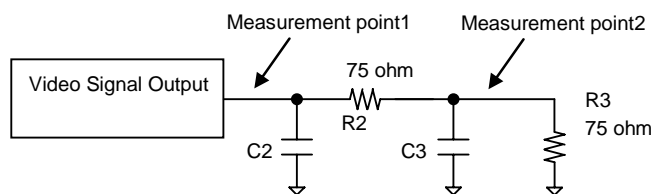


Figure 3. Load Capacitance C2 and C3

Parameter	min	typ	max	Unit
Power Supplies:				
Power Up (PDN pin = "H")				
All Circuit Power-up (Note 19)				
AVDD	-	9.7	14	mA
DVDD +TVDD	-	2.6	4.0	mA
MIC + ADC (Note 20)				
AVDD	-	2.4	-	mA
DVDD +TVDD	-	1.3	-	mA
DAC + Lineout (Note 21)				
AVDD	-	2.1	-	mA
DVDD +TVDD	-	0.5	-	mA
DAC + SPK-Amp (Note 22)				
AVDD	-	2.9	-	mA
DVDD +TVDD	-	0.5	-	mA
Video Block (Note 23)				
AVDD	-	5.3	-	mA
Power Down (PDN pin = "L") (Note 24)				
AVDD+DVDD+TVDD	-	1	5	μA

Note 19. When PMADL=PMADR=PMDAC=PMPFIL=PMLO=PMSPK=PMPLL=MCKO=PMBP=PMMP =PMMICR =PMMICL =M/S =PMV bits = "1", SPK-amp No load, no signals are input to LIN/RIN and MIN pins, black signal is input to the VIN pin, no output from the LOUT/ROUT pin and "0" data input to the SDTI pin in PLL Master Mode (MCKI=13.5MHz). In this case, the output current of the MPWR pin is 0mA. The path settings are, ADCPF = PFSDO bits = "1", PFDAC bit= "0", DACS = DACL bits = "1", and BEEPS = BEEPL bits = "0". MG2-0 bits = "000", HPF = LPF = FIL3 = EQ0 = EQ1~5 = ALC bits = "0", MONO1-0 bits = "00", DVOL7-0 bits = "FFH", and SMUTE bit = "0".

Note 20. When PMADL = PMADR = PMMICL = PMMICLR bits = "1" and no signals are input to the LIN/RIN pin in EXT Slave Mode (PMPLL=M/S=MCKO bits = "0"). The path setting is ADCPF=PFSDO bits = "0".

Note 21. When PMDAC = PMLO = "1", "0" data input to the SDTI pin, and no output from the LOUT/ROUT pin in EXT Slave Mode (PMPLL=M/S=MCKO bits = "0"). The path settings are PFDAC bit = "0", DACL bit = "1", and DACS =BEEPS =BEEPL bits = "0". MONO1-0 bits = "00", DVOL7-0 bits = "FFH", and SMUTE bit = "0".

Note 22. When PMDAC = PMSPK =SPPSN bits = "1", "0" data input to the SDTI pin, and No load at SPK-amp in EXT Slave Mode (PMPLL=M/S=MCKO bits = "0"). The path settings are MONO1-0 bits= "00", DVOL7-0 bits = "FFH", and SMUTE bit = "0".

Note 23. When PMV bit = "1", No-load, and the black signal is input to the VIN pin.

Note 24. All digital input pins are fixed to TVDD or VSS2.

FILTER CHARACTERISTICS

(Ta =25°C; AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V; fs=48kHz)

Parameter	Symbol	min	typ	max	Unit	
ADC Digital Filter (Decimation LPF):						
Passband (Note 25)	±0.16dB	PB	0	-	18.8	kHz
	-0.66dB		-	21.1	-	kHz
	-1.1dB		-	21.7	-	kHz
	-6.9dB		-	24.1	-	kHz
Stopband (Note 25)	SB	28.4	-	-	kHz	
Passband Ripple	PR	-	-	±0.16	dB	
Stopband Attenuation	SA	73	-	-	dB	
Group Delay (Note 26)	GD	-	17	-	1/fs	
Group Delay Distortion	ΔGD	-	0	-	μs	
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response (Note 25)	-3.0dB	FR	-	3.7	-	Hz
	-0.5dB		-	10.9	-	Hz
	-0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 25)	±0.05dB	PB	0	-	21.8	kHz
	-6.0dB		-	24	-	kHz
Stopband (Note 25)	SB	26.2	-	-	kHz	
Passband Ripple	PR	-	-	±0.05	dB	
Stopband Attenuation	SA	54	-	-	dB	
Group Delay (Note 26)	GD	-	22	-	1/fs	
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz	FR	-	±1.0	-	dB	

Note 25. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz. For example, it is 0.454 x fs (ADC) when PB=21.7kHz (@-1.1dB).

Note 26. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (1st order HPF + 1st order LPF + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta =25°C; AVDD = 2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V; fs= 48kHz)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial μP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage (Except I2C pin, TVDD \geq 2.2V)	VIH	70%TVDD	-	-	V
(Except I2C pin, TVDD < 2.2V)		80%TVDD	-	-	V
(I2C pin)	VIH1	70%AVDD	-	-	V
Low-Level Input Voltage (Except I2C pin, TVDD \geq 2.2V)	VIL	-	-	30%TVDD	V
(Except I2C pin, TVDD < 2.2V)		-	-	20%TVDD	V
(I2C pin)	VIL1	-	-	30%AVDD	V
Input Leakage Current	Iin1	-	-	\pm 10	μ A
Audio Interface & Serial μP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = -80 μ A)	VOH	TVDD-0.2	-	-	V
Low-Level Output Voltage (Except SDA pin : Iout = 80 μ A)	VOL1	-	-	0.2	V
(SDA pin, 2.0V \leq TVDD \leq 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V \leq TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	\pm 10	μ A
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=-80 μ A)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80 μ A)	VOL3	-	-	0.4	V

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD = 2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit	
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	fCLK	11.2896	-	27	MHz	
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns	
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns	
MCKO Output Timing						
Frequency	fMCK	0.2352	-	12.288	MHz	
Duty Cycle	dMCK	40	50	60	%	
LRCK Output Timing						
Frequency	fs	8	-	48	kHz	
Duty Cycle	Duty	-	50	-	%	
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle	dBCK	-	50	-	%	
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	fCLK	11.2896	-	27	MHz	
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns	
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns	
MCKO Output Timing						
Frequency	fMCK	0.2352	-	12.288	MHz	
Duty Cycle	dMCK	40	50	60	%	
LRCK Input Timing						
Frequency	fs	8	-	48	kHz	
Duty	Duty	45	-	55	%	
BICK Input Timing						
Period	tBCK	1/(64fs)	-	1/(32fs)	ns	
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns	
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns	

Parameter	Symbol	min	typ	max	Unit	
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency	fs	7.35	-	48	kHz	
Duty	Duty	45	-	55	%	
BICK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	13.6	MHz
	512fs	fCLK	3.7632	-	24.576	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	48	kHz
	1024fs	fs	7.35	-	13	kHz
Duty	Duty	45	-	55	%	
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	24.576	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK “↓” to LRCK Edge (Note 27)	tMBLR	-40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)	tLRD	-70	-	70	ns
BICK “↓” to SDTO	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK “↑” (Note 27)	tLRB	50	-	-	ns
BICK “↑” to LRCK Edge (Note 27)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)	tLRD	-	-	80	ns
BICK “↓” to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN “H” Time	tCSW	150	-	-	ns
CSN Edge to CCLK “↑” (Note 28)	tCSS	50	-	-	ns
CCLK “↑” to CSN Edge (Note 28)	tCSH	50	-	-	ns
CCLK “↓” to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN “↑” to CDTIO (Hi-Z) (at Read Command)(Note 30)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 31)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 27. BICK rising edge must not occur at the same time as LRCK edge.

Note 28. CCLK rising edge must not occur at the same time as CSN edge.

Note 29. I²C-bus is a trademark of NXP B.V.

Note 30. It is the time of 10% potential change of the CDTIO pin when R_L=1kΩ (pull-up or TVDD).

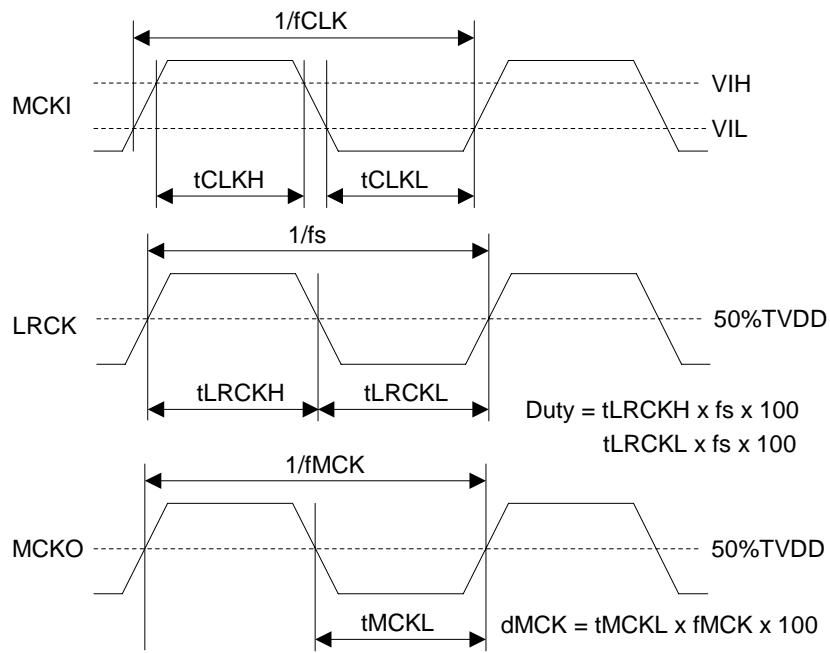
Note 31. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter	Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tDSDS	50	-	-	ns
DMDAT Hold Time	tDSDH	0	-	-	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 32)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 32)	tRPD	-	-	50	ns
PMADL or PMADR “↑” to SDTO valid (Note 33)					
ADRST1-0 bits =“00”	tPDV	-	1059	-	1/fs
ADRST1-0 bits =“01”	tPDV	-	267	-	1/fs
ADRST1-0 bits =“10”	tPDV	-	531	-	1/fs
ADRST1-0 bits =“11”	tPDV	-	135	-	1/fs

Note 32. The AK4957 can be reset by the PDN pin = “L”. The PDN pin must be held “L” for more than 200ns for a certain reset. The AK4957 is not reset by the “L” pulse less than 50ns.

Note 33. This is the count of LRCK “↑” from the PMADL or PMADR bit = “1”.

■ Timing Diagram



Note 34. MCKO is not available at EXT Master mode.
Figure 4. Clock Timing (PLL/EXT Master mode)

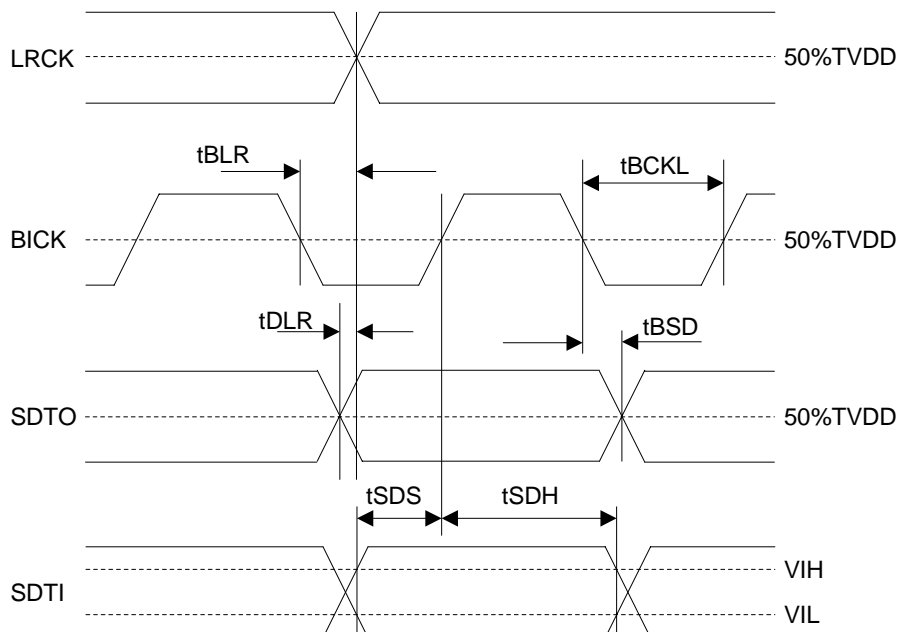


Figure 5. Audio Interface Timing (PLL/EXT Master mode)

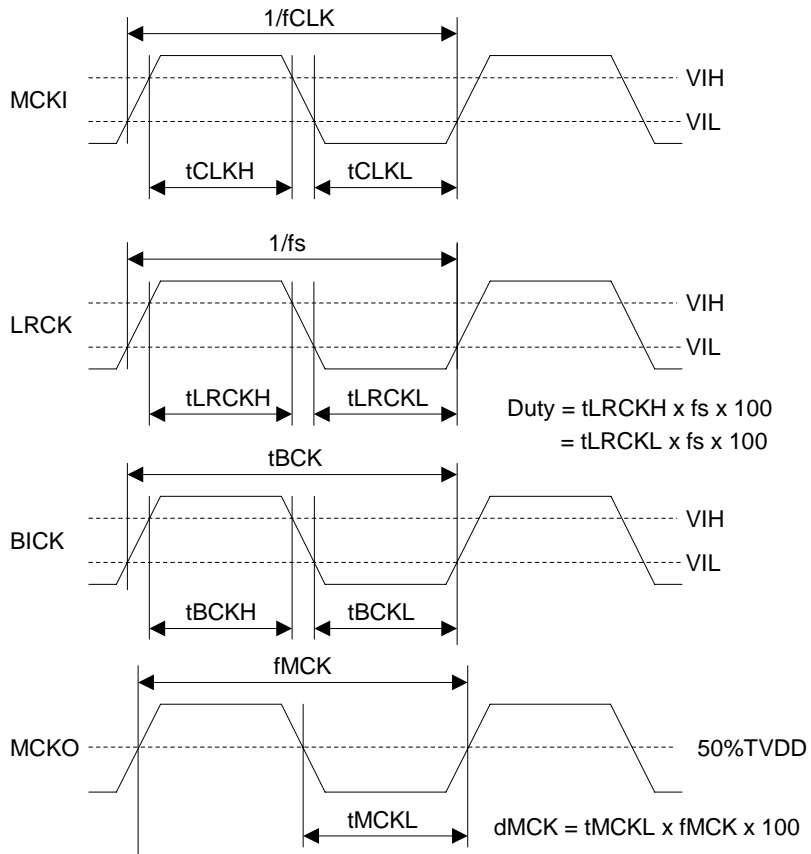


Figure 6. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

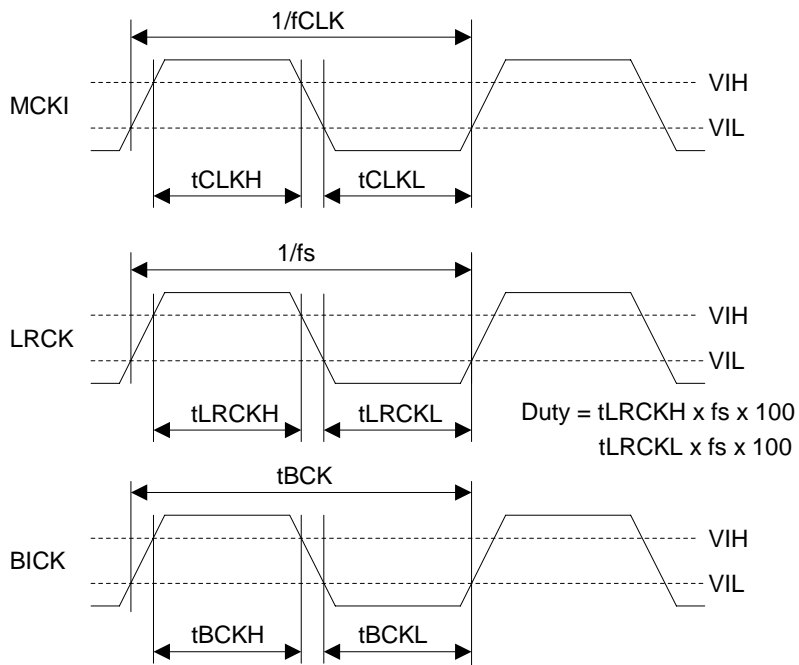


Figure 7. Clock Timing (EXT Slave mode)

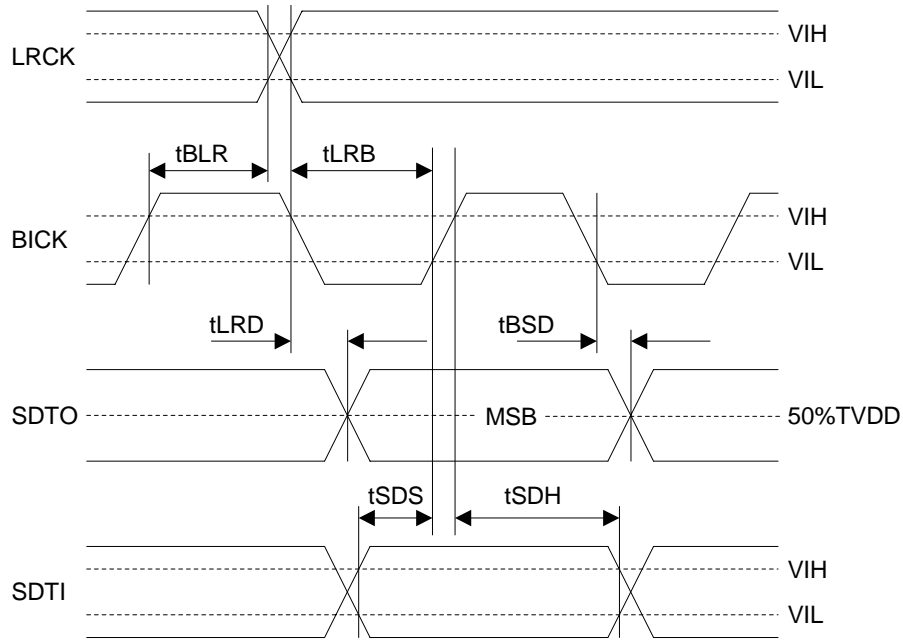


Figure 8. Audio Interface Timing (PLL/EXT Slave mode)

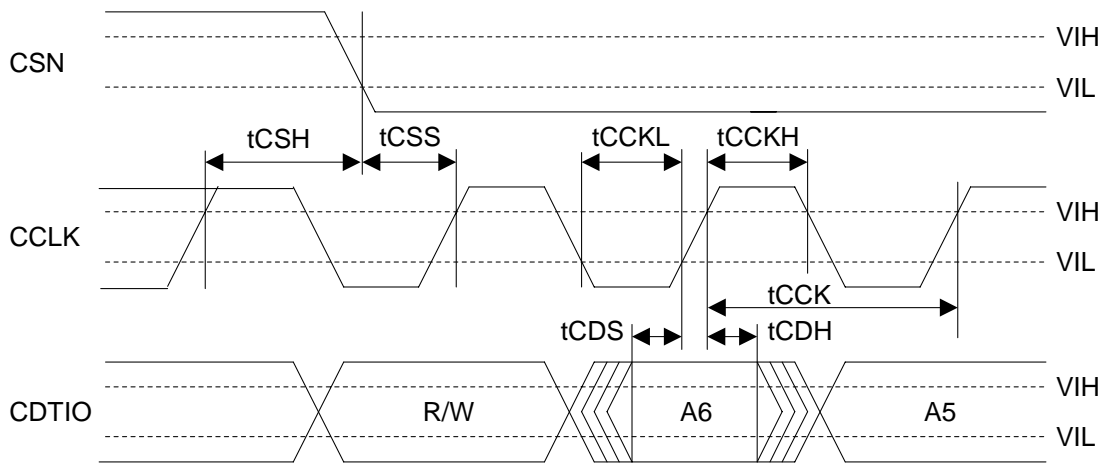


Figure 9. WRITE Command Input Timing

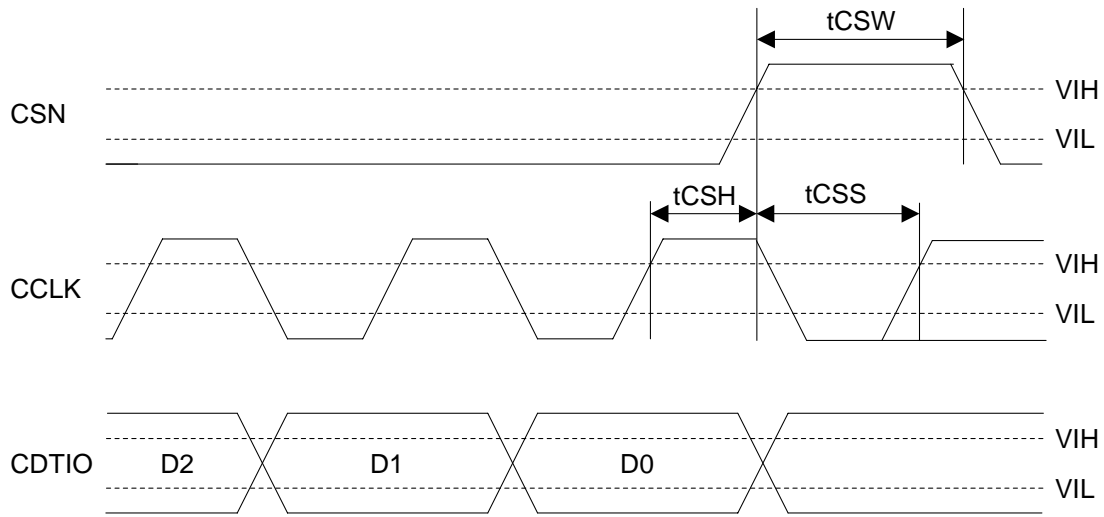


Figure 10. WRITE Data Input Timing

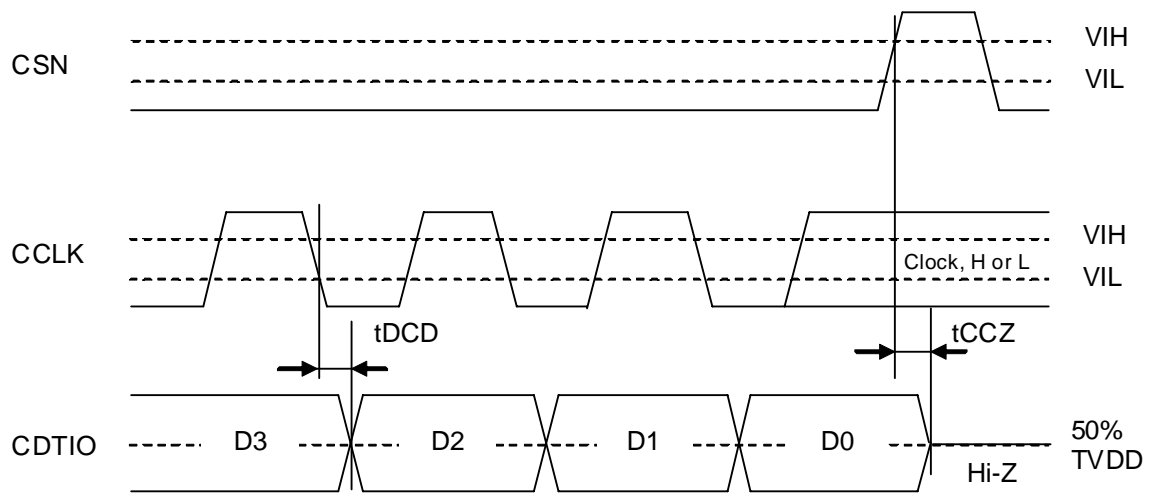


Figure 11. Read Data Output Timing

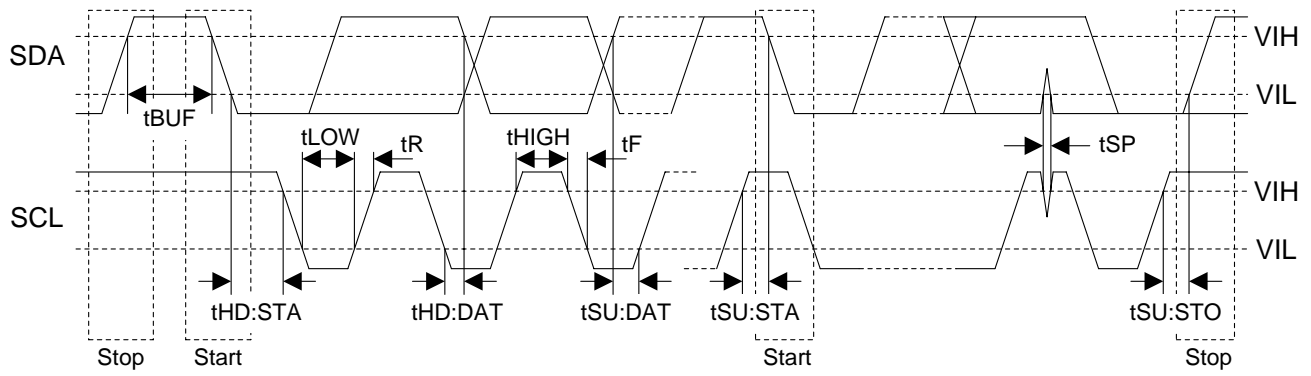
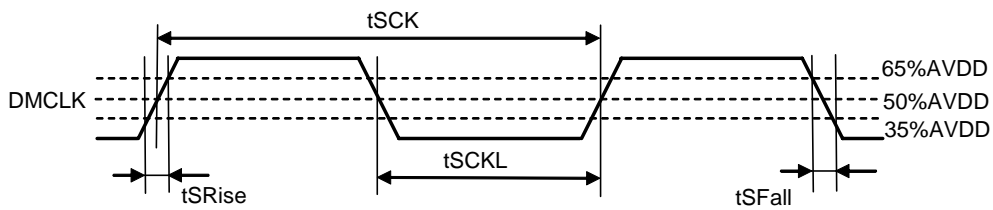


Figure 12. I²C Bus Mode Timing



$$dSCK = 100 \times tSCKL / tSCK$$

Figure 13. DMCLK Clock Timing

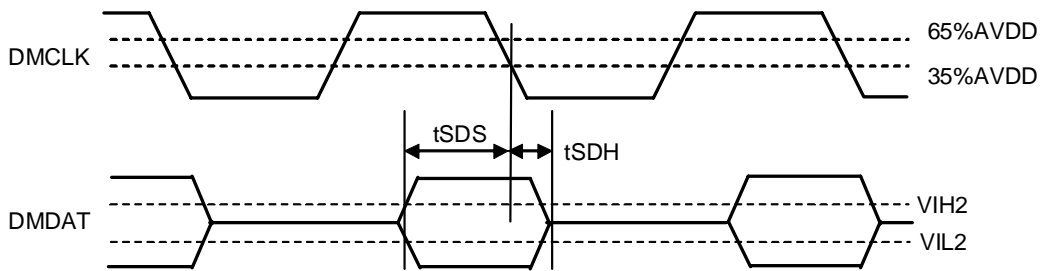


Figure 14. Audio Interface Timing (DCLKP bit = "1")

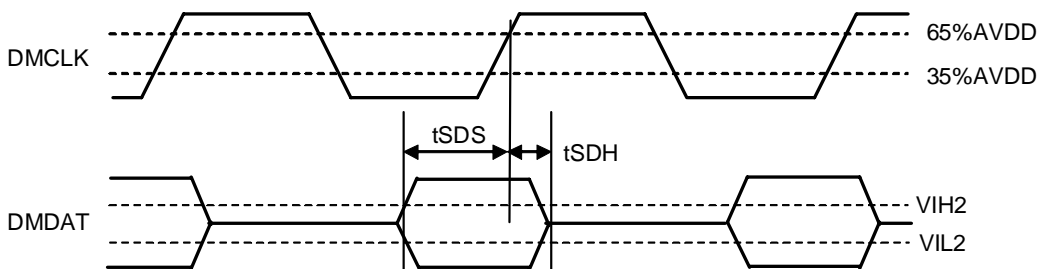


Figure 15. Audio Interface Timing (DCLKP bit = "0")

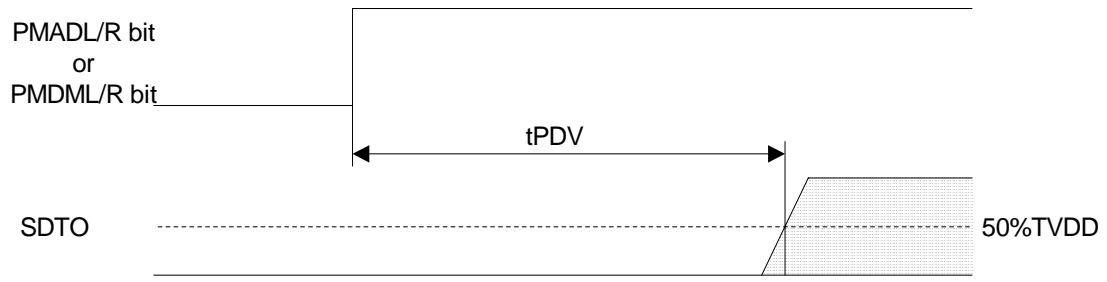


Figure 16. Power Down & Reset Timing 1

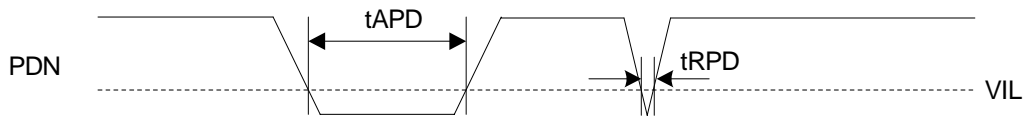


Figure 17. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 35)	1	1	Table 4	Figure 18
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 19
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 20
EXT Slave Mode	0	0	x	Figure 21
EXT Master Mode	0	1	x	Figure 22

Note 35. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO, BICK and LRCK pins.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: BICK pin)	0	L	GND	Input (≥ 32fs)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 36. When M/S bit = "1" and MCKI is input, LRCK and BICK are output even if PMDAC=PMADL= PMADR bits = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4957 is in power-down mode (PDN pin = "L") and when exits reset state, the AK4957 is in slave mode. After exiting reset state, the AK4957 goes to master mode by changing M/S bit to "1".

When the AK4957 is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4957 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode
0	Slave Mode
1	Master Mode

(default)

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4957 is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or the sampling frequency is changed, are shown in [Table 4](#).

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
2	0	0	1	0	BICK pin	32fs	2 ms
3	0	0	1	1	BICK pin	64fs	2 ms
4	0	1	0	0	MCKI pin	11.2896MHz	5 ms
6	0	1	1	0	MCKI pin	12MHz	5 ms
7	0	1	1	1	MCKI pin	24MHz	5 ms
12	1	1	0	0	MCKI pin	13.5MHz	5 ms
13	1	1	0	1	MCKI pin	27MHz	5 ms
Others	Others			N/A			

Table 4. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is “1” (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in [Table 5](#).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency
0	0	0	0	0	8kHz
1	0	0	0	1	12kHz
2	0	0	1	0	16kHz
3	0	0	1	1	24kHz
5	0	1	0	1	11.025kHz
7	0	1	1	1	22.05kHz
10	1	0	1	0	32kHz
11	1	0	1	1	48kHz
15	1	1	1	1	44.1kHz
Others	Others				N/A

Table 5. Setting of Sampling Frequency at PLL2 bit = “1” and PMPLL bit = “1” (Reference Clock = MCKI pin), (N/A: Not Available)

When PLL2 bit is “0” (PLL reference clock input pin is the BICK pin), the sampling frequency is selected by FS3-2 bits. ([Table 6](#)).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz
1	0	1	x	x	12kHz < fs ≤ 24kHz
2	1	0	x	x	24kHz < fs ≤ 48kHz
Others	Others				N/A

Table 6. Setting of Sampling Frequency at PLL2 bit = “0” and PMPLL bit = “1” PLL Slave Mode 2 (PLL Reference Clock: BICK pin), (x: Don’t care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L", and irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

The BICK and LRCK pins do not output irregular frequency clocks such as PLL unlock state by setting PMPLL bit to "0". During PMPLL bit = "0", these pins output the same clocks as EXT Master Mode.

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. The DAC outputs can be muted by setting DACL and DACS bits to "0".

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 9) and switched on and off by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

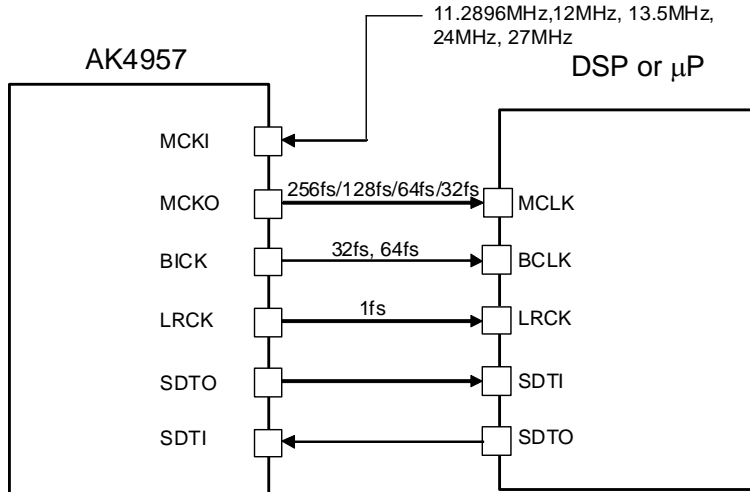


Figure 18. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin
0	0	0	256fs
1	0	1	128fs
2	1	0	64fs
3	1	1	32fs

(default)

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = “1”)

BCKO bit	BICK Output Frequency
0	32fs
1	64fs

(default)

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI or BICK pins. The required clock for the AK4957 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5)

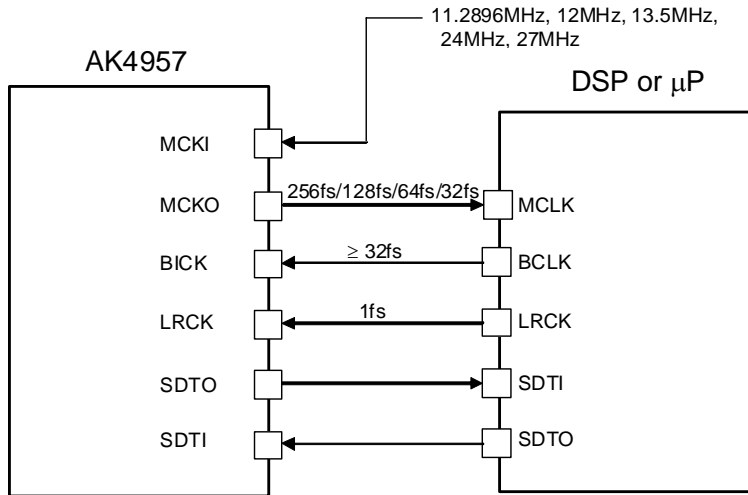


Figure 19. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

The sampling frequency corresponds to a range from 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

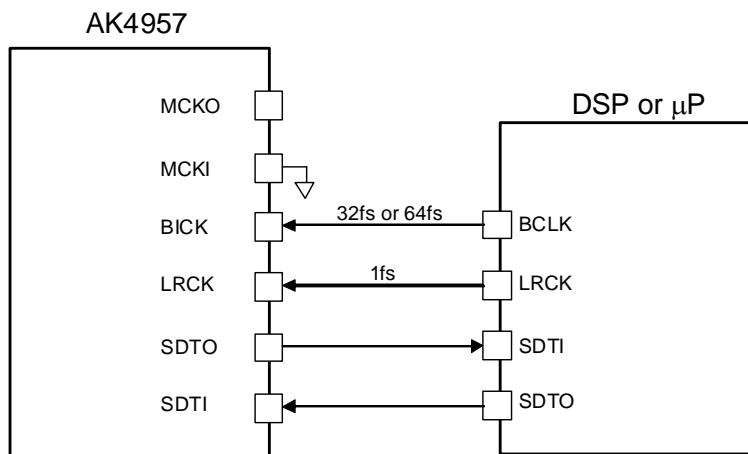


Figure 20. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4957 becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK ($\geq 32fs$). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range
0	x	0	0	256fs	7.35kHz ~ 48kHz
1	x	0	1	1024fs	7.35kHz ~ 13kHz
2	x	1	0	512fs	7.35kHz ~ 26kHz
3	x	1	1	512fs	7.35kHz ~ 48kHz

(x: Don't care)

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode0: 256fs Mode3: 512fs	80dB
Mode2: 512fs	92dB
Mode1: 1024fs	92dB

Table 12. Relationship between MCKI and S/N of LOUT/ROUT pins

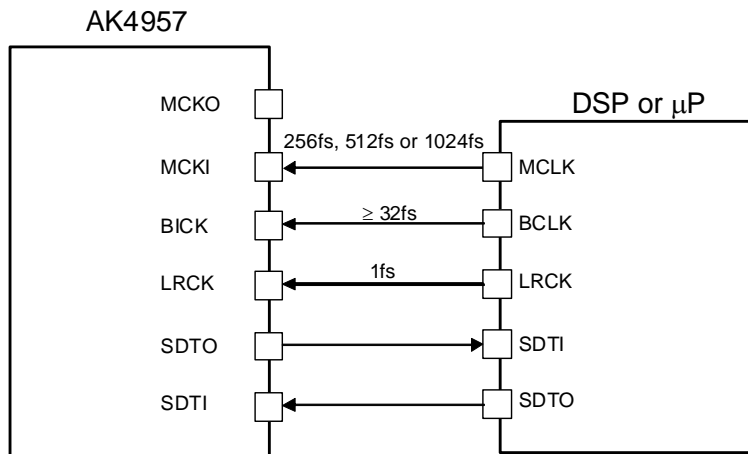


Figure 21. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4957 becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4957 is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 13).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range
0	x	0	0	256fs	7.35kHz ~ 48kHz
1	x	0	1	1024fs	7.35kHz ~ 13kHz
2	x	1	0	512fs	7.35kHz ~ 26kHz
3	x	1	1	512fs	7.35kHz ~ 48kHz

(default)

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”) (x: Don’t care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode0: 256fs Mode3: 512fs	80dB
Mode2: 512fs	92dB
Mode1: 1024fs	92dB

Table 14. Relationship between MCKI and S/N of LOUT/ROUT pins

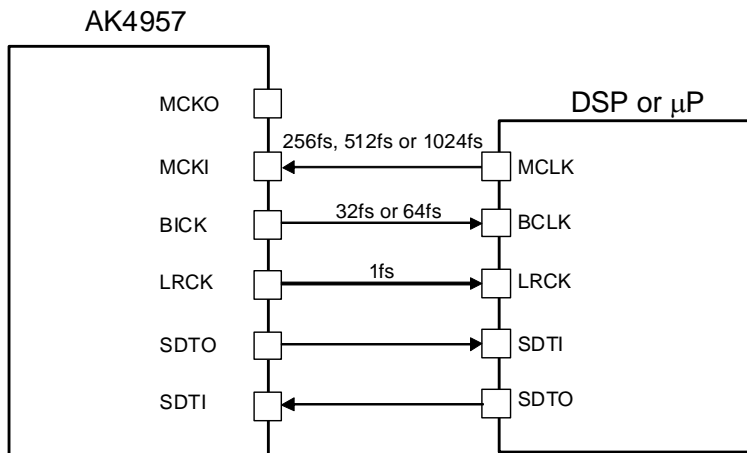


Figure 22. EXT Master Mode

BCKO bit	BICK Output Frequency
0	32fs
1	64fs

(default)

Table 15. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4957 must be reset by bringing the PDN pin = “L”. This reset is released when a dummy command is input after the PDN pin = “H”. This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all “0” to the register address 00H. It is recommended to set the PDN pin to “L” before power up the AK4957.

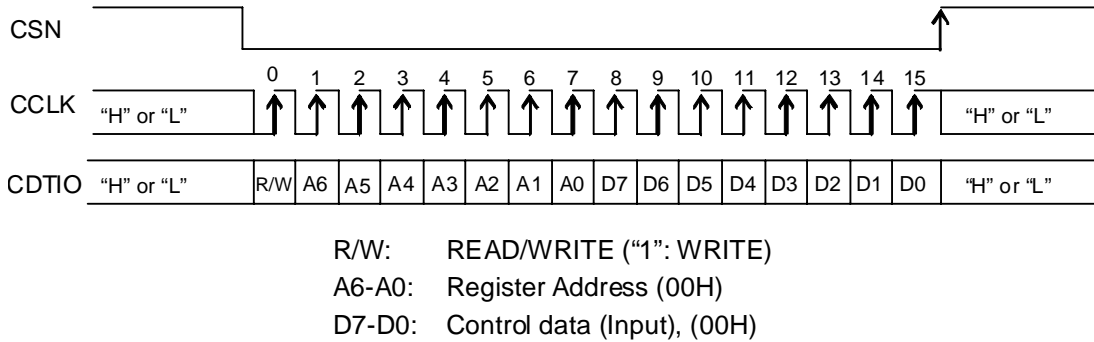


Figure 23. Dummy Command in 3-wire Serial Mode

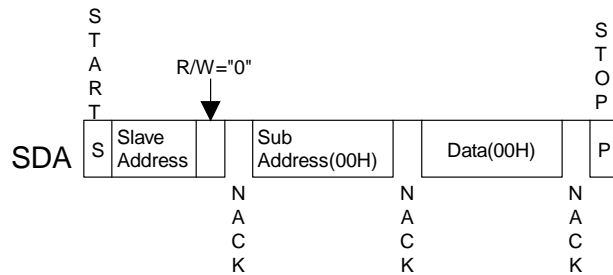


Figure 24. Dummy Command in I²C-bus Mode

The ADC starts an initialization cycle if the one of PMADL or PMADR is set to “1” when both of the PMADL and PMADR bits are “0”. The initialization cycle is set by ADRST1-0 bits (Table 16). During the initialization cycle, the ADC digital data outputs of both channels are forced to “0” in 2’s complement. The ADC output reflects the analog input signal after the initialization cycle is finished. When using a digital microphone, the initialization cycle is the same as ADC’s.

(Note) The initial data of ADC has offset data that depends on microphones and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the first data of ADC outputs.

ADRST1-0 bits	Init Cycle			
	Cycle	fs = 8kHz	fs = 16kHz	fs = 48kHz
00	1059/fs	132.4ms	66.2ms	22ms
01	267/fs	33.4ms	16.7ms	5.6ms
10	531/fs	66.4ms	33.2ms	11.1ms
11	135/fs	16.9ms	8.4ms	2.8ms

Table 16. ADC Initialization Cycle

(default)

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats are supported in both master and slave modes. LRCK and BICK are output from the AK4957 in master mode, but must be input to the AK4957 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 25
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 26
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 27 (default)
3	1	1	I ² S Compatible	I ² S Compatible	=32fs or ≥ 48fs	Figure 28

Table 17. Audio Interface Format

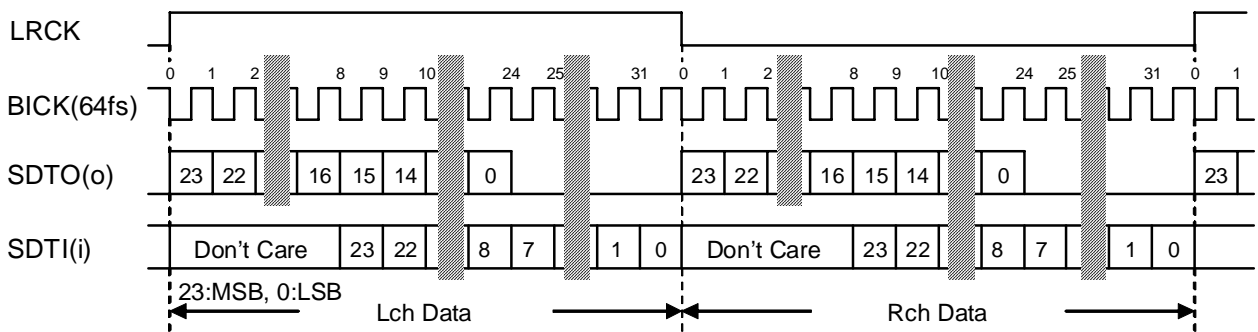


Figure 25. Mode 0 Timing

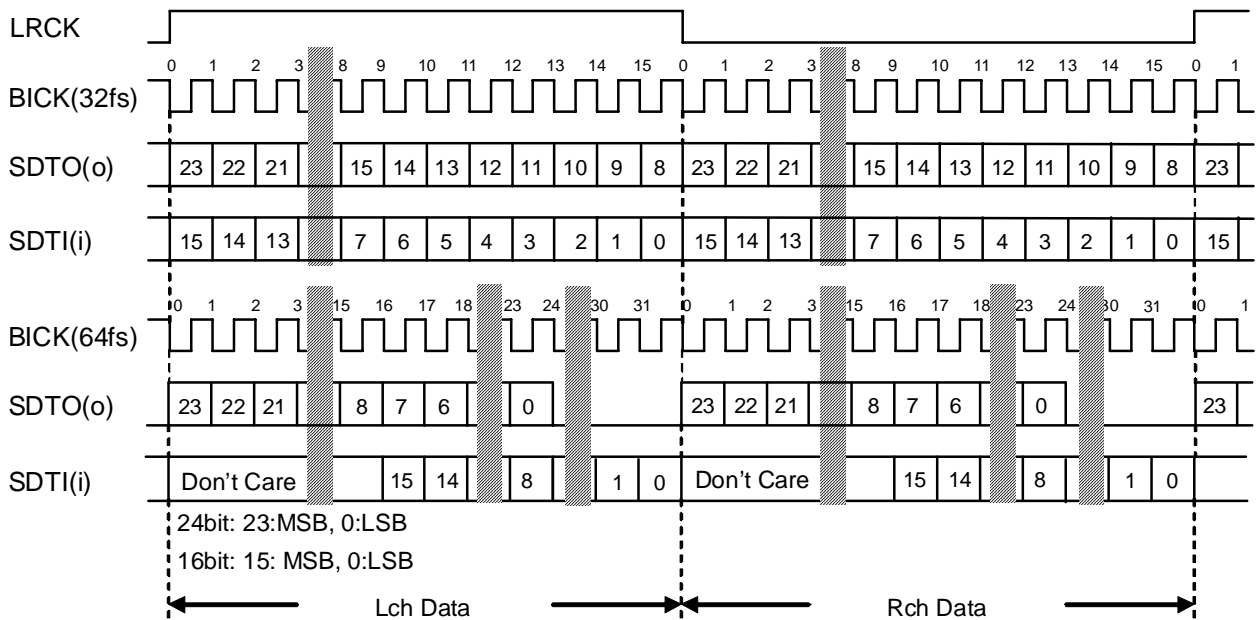


Figure 26. Mode 1 Timing

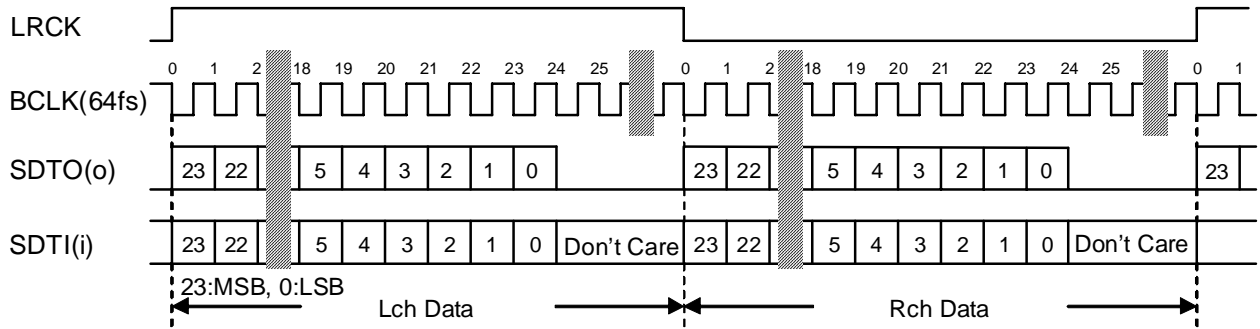


Figure 27. Mode 2 Timing

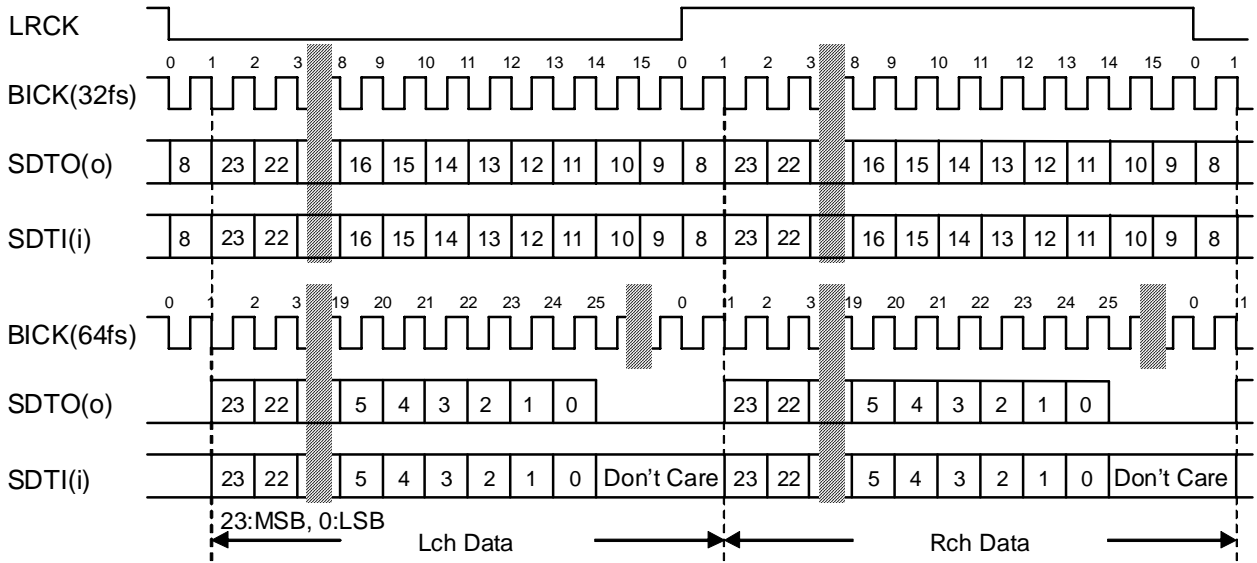


Figure 28. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set “0” at first. When PMDML or PMDMR bit = “1”, PMADL and PMADR bit settings are ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All “0”	All “0”	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 18. Mono/Stereo ADC operation (Analog MIC)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All “0”	All “0”	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Digital MIC)

■ MIC/LINE Input Selector

The AK4957 has an input selector. INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When DMIC bit = “1”, digital microphone input is selected regardless of INL and INR bits.

DMIC bit	INL bit	INR bit	Lch	Rch	
0	0	0	LIN1	RIN1	(default)
	0	1	LIN1	RIN2	
	1	0	LIN2	RIN1	
	1	1	LIN2	RIN2	
1	0	0	Digital Microphone		
	0	1			
	1	0			
	1	1			

Table 20. MIC/Line In Path Select

■ MIC Gain Amplifier

The AK4957 has a gain amplifier for microphone input. It is powered-up by PMMICL/R bit = “1”. The gain of MIC-Amp is selected by the MGAIN2-0 bits (Table 21). The typical input impedance is 33kΩ.

MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0dB	(default)
0	0	1	+8dB	
0	1	0	+14dB	
0	1	1	+16dB	
1	0	0	+18dB	
1	0	1	+21dB	
Others			N/A	

Table 21. Input Gain (N/A: Not available)

■ MIC Power

When PMMP bit = “1”, the MPWR pin supplies the power for microphones. This output voltage is typically 2.4V @MICL bit = “0”, and typically 2.0V @MICL bit = “1”. The load resistance is minimum 0.5kΩ. In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 29).

PMMP bit	MPWR pin
0	Hi-Z
1	Output

(default)

Table 22. MIC Power

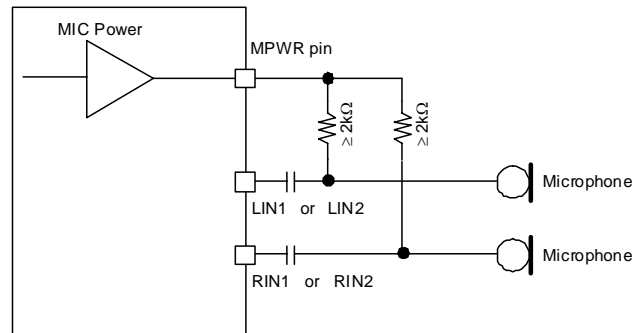


Figure 29. MIC Block Circuit

■ Digital MIC

1. Connection to Digital Microphones

When DMIC bit is set to “1”, the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins, respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 30 and Figure 31 show stereo/mono connection examples. The DMCLK clock is input to a digital microphone from the AK4957. The digital microphone outputs 1bit data, which is generated by $\Delta\Sigma$ Modulator using DMCLK clock, to the DMDAT pin. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). (PMADL/PMADR bits settings do not affect the digital microphone power management. Set PMMP = PMMICL/R bits to “0” when using a digital microphone.) The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4957 is powered down (PDN pin= “L”), the DMCLK and DMDAT pins become floating state. Pull-down resistors must be connected to DMCLK and DMDAT pins externally to avoid this floating state.

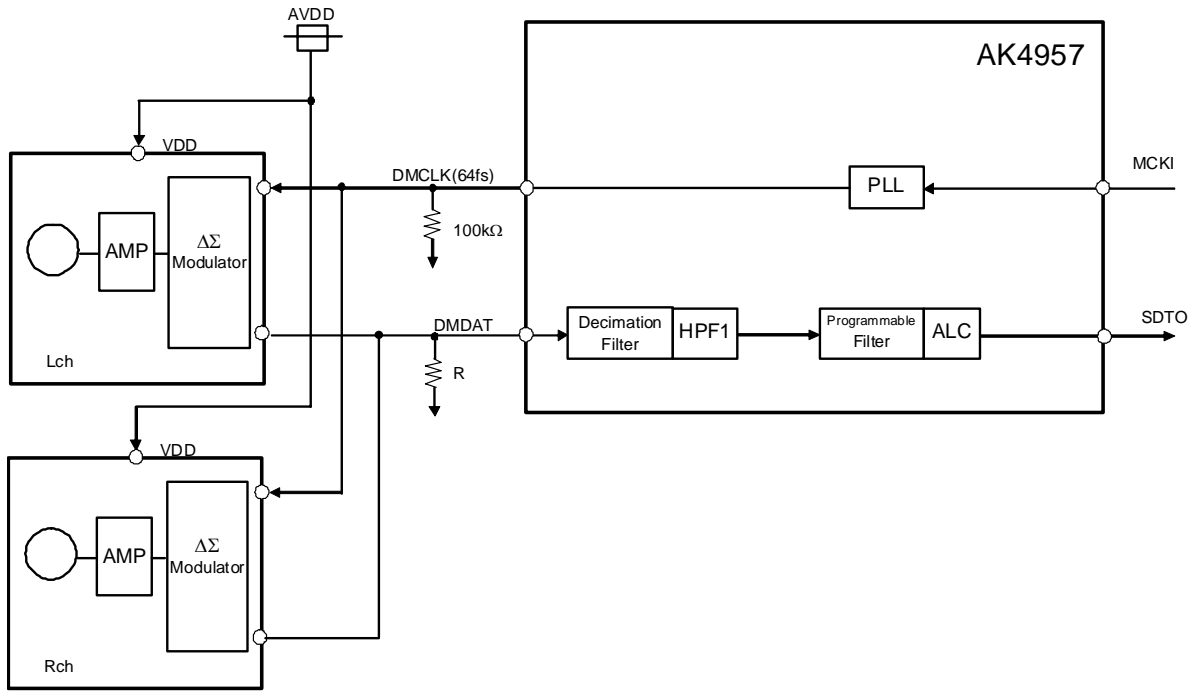


Figure 30. Connection Example of Stereo Digital MIC

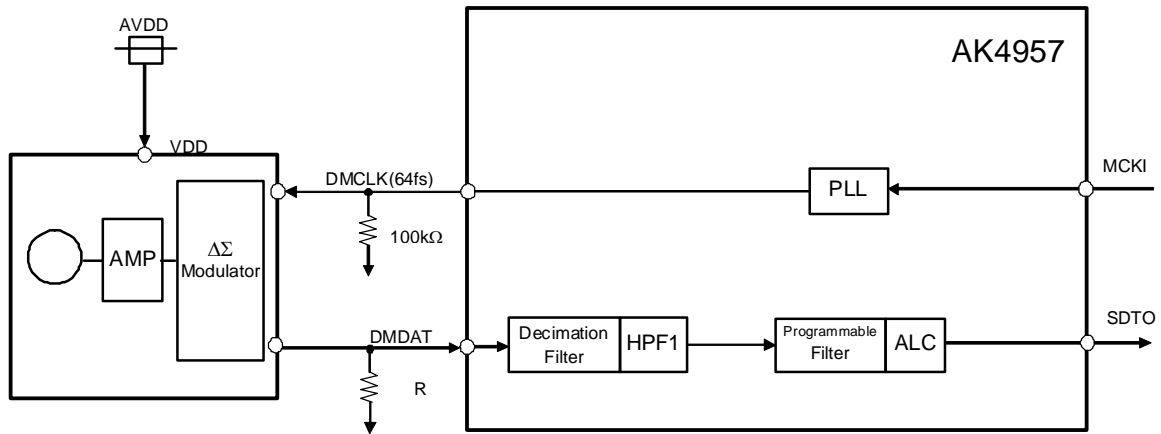


Figure 31. Connection Example of Mono Digital MIC

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = “1”, L channel data is input to the decimation filter if DMCLK = “H”, and R channel data is input if DMCLK = “L”. When DCLKP bit = “0”, R channel data is input to the decimation filter while DMCLK pin= “H”, and L channel data is input while DMCLK pin= “L”. The DMCLK pin only supports 64fs. It outputs “L” when DCLKE bit = “0”, and outputs 64fs when DCLKE bit = “1”. In this case, necessary clocks must be supplied to the AK4957 for ADC operation. The output data through “the Decimation and Digital Filters” is 24bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK pin= “H”	DMCLK pin= “L”
0	Rch	Lch
1	Lch	Rch

(default)

Table 23. Data In/Output Timing with Digital MIC (DCLKP bit = “0”)

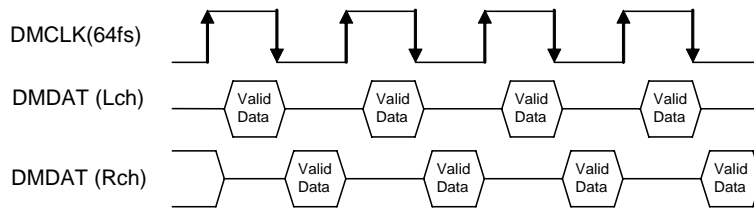


Figure 32. Data In/Output Timing with Digital MIC (DCLKP bit = “1”)

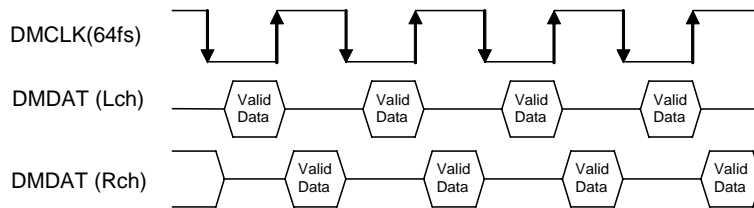
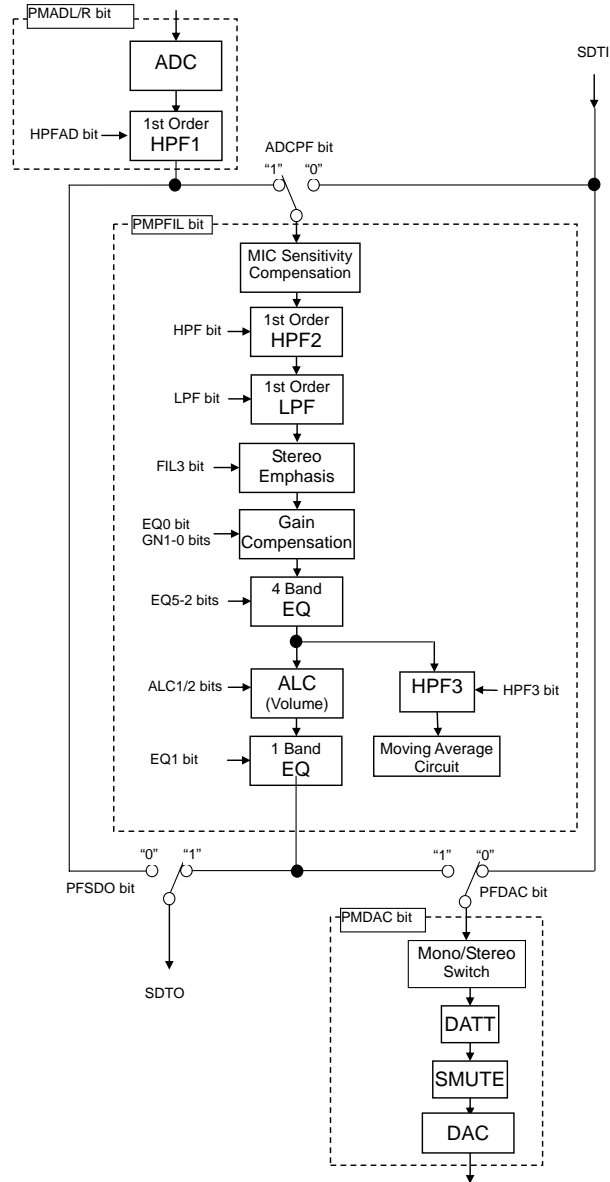


Figure 33. Data In/Output Timing with Digital MIC (DCLKP bit = “0”)

■ Digital Block

The digital block consists of the blocks shown in [Figure 34](#). Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and PFSDO bit. ([Figure 35 ~ Figure 38](#), [Table 24](#))



- (1) ADC: Includes the Digital Filter (LPF) for ADC as shown in “FILTER CHARACTERISTICS”.
- (2) HPF1: High Pass Filter (HPF) for ADC as shown in “FILTER CHARACTERISTICS”.
- (3) MIC Sensitivity Correction: MIC volume control between L and R channels. (See “MIC Sensitivity Correction”)
- (4) HPF2: High Pass Filter. (See “Digital Programmable Filter Circuit”)
- (5) LPF: Low Pass Filter (See “Digital Programmable Filter Circuit”)
- (6) Stereo Emphasis: Stereo emphasis Filter. (See “Digital Programmable Filter Circuit”)
- (7) Gain Compensation: Gain compensation consists of EQ and Gain control. It corrects frequency characteristics after stereo separation emphasis filter. (See “Digital Programmable Filter Circuit”)
- (8) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See “Digital Programmable Filter Circuit”)
- (9) HPF3: The second order HPF for input level reading function.

- (10) ALC (Volume): Digital Volume with ALC Function. (See “Input Digital Volume” and “ALC Operation”)
- (11) 1 Band EQ: Applicable for use as Notch Filter (See “Digital Programmable Filter Circuit”)
- (12) Mono/Stereo Switching: Mono/Stereo lineout outputs select from DAC which described in <Mono Mixing Output> at “Stereo Line Outputs”.
- (13) DVOL: Digital volume for playback path (See “Output Digital Volume2”)
- (14) SMUTE: Soft mute function

Figure 34. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	Figure
Recording Mode 1	1	0	1	Figure 35
Playback Mode 1	0	1	0	Figure 36
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = “0”)	x	0	0	Figure 37
Loopback Mode	1	1	1	Figure 38

Table 24. Recording Playback Mode (x: Don’t care)

When changing those modes, PMPFIL bit must be “0”.

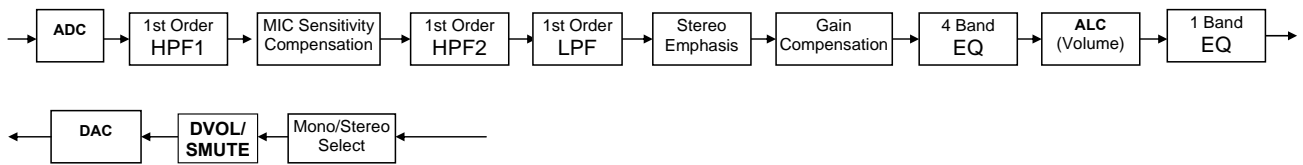


Figure 35. The Path in Recording Mode 1 (default)

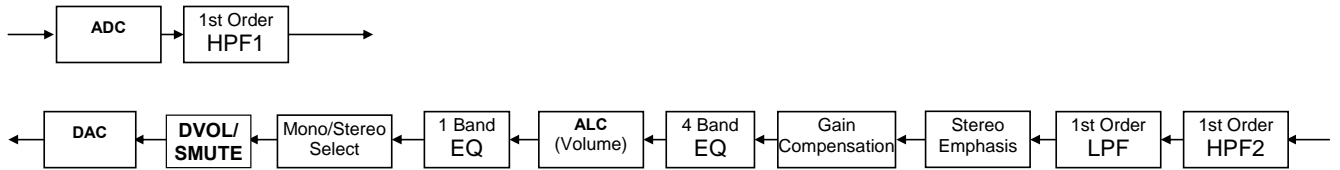


Figure 36. The Path in Playback Mode 1

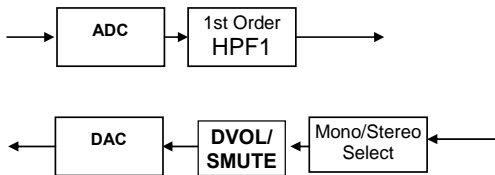


Figure 37. The Path in Recording Mode 2 & Playback Mode 2

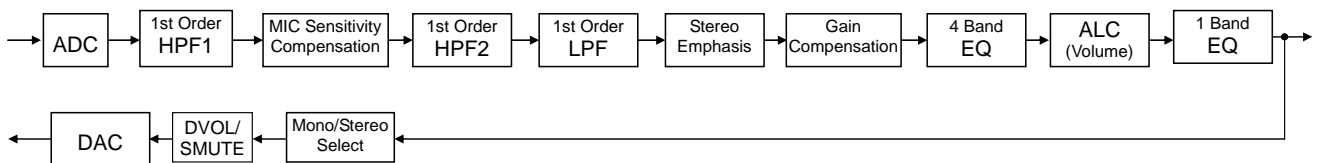


Figure 38. The Path in Loopback Mode

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 25). It is proportional to the sampling frequency (fs) and the default value is 3.7Hz (@fs = 48kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc			(default)
		fs=48kHz	fs=22.05kHz	fs=8kHz	
0	0	3.7Hz	1.7Hz	0.62Hz	
0	1	14.8Hz	6.8Hz	2.47Hz	
1	0	118.4Hz	54.4Hz	19.7Hz	
1	1	236.8Hz	108.8Hz	39.5Hz	

Table 25. HPF1 Cut-off Frequency

■ MIC Sensitivity Correction

The AK4957 has microphone sensitivity correction function controlled by MGL/R4-0 bits.

MGL4-0 bits MGR4-0 bits	GAIN (dB)	Step	(default)
01000	+3	0.375dB	
00111	+2.625		
00110	+2.25		
00101	+1.875		
00100	+1.5		
00011	+1.125		
00010	+0.75		
00001	+0.375		
00000	0		
11111	-0.375		
11110	-0.75		
11101	-1.125		
11100	-1.5		
11011	-1.875		
11010	-2.25		
11001	-2.625		
11000	-3		
Others	N/A		

Table 26. MIC Sensitivity Correction (N/A: Not available)

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or HPF bit = "0". The HPF2 starts operation $4/f_s$ (max) after when HPF bit=PMPFIL bit="1" is set.

f_s : Sampling Frequency

f_c : Cutoff Frequency

Register Setting (Note 37)

HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.

$$f_c / f_s \geq 0.0001 \quad (f_c \text{ min} = 4.8\text{Hz at } 48\text{kHz})$$

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or LPF bit = "0". The LPF starts operation $4/f_s$ (max) after when LPF bit =PMPFIL bit="1" is set.

f_s : Sampling Frequency

f_c : Cutoff Frequency

Register Setting (Note 37)

LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.

$$f_c / f_s \geq 0.05 \quad (f_s \text{ min} = 2400\text{Hz at } 48\text{kHz})$$

(3) Stereo Separation Emphasis Filter (FIL3)

The FIL3 is used to emphasize the stereo separation of stereo microphone recording data and playback data. F3A13-0 bits and F3B13-0 bits set the filter coefficients of the FIL3. When F3AS bit = "0", the FIL3 performs as a High Pass Filter (HPF), and it performs as a Low Pass Filter (LPF) when F3AS bit = "1". FIL3 bit controls ON/OFF of the FIL3. When the stereo separation emphasis filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit or PMPFIL bit is "0". The FIL3 starts operation $4/f_s(\max)$ after when FIL3 bit = PMPFIL bit = "1" is set.

1) In case of setting FIL3 as HPF

f_s : Sampling Frequency

f_c : Cutoff Frequency

K: Gain [dB] ($0\text{dB} \geq K \geq -10\text{dB}$)

Register Setting (Note 37)

FIL3: F3AS bit = "0", F3A[13:0] bits = A, F3B[13:0] bits = B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) In case of setting FIL3 as LPF

f_s : Sampling Frequency

f_c : Cutoff Frequency

K: Gain [dB] ($0\text{dB} \geq K \geq -10\text{dB}$)

Register Setting (Note 37)

FIL3: F3AS bit = "1", F3A[13:0] bits = A, F3B[13:0] bits = B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi f_c / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_c / f_s)}{1 + 1 / \tan(\pi f_c / f_s)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain compensation is used to compensate the frequency response and the gain that is changed by the stereo separation emphasis filter. Gain compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0 bits, E0B13-0 bits and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 27). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". The EQ0 starts operation 4/fs(max) after when EQ0 bit = PMPFIL bit = "1" is set.

- fs: Sampling Frequency
- fc₁: Polar Frequency
- fc₂: Zero-point Frequency
- K: Gain [dB] (Maximum setting is +12dB.)

Register Setting (Note 37)

E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
 (MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2 / fs)}{1 + 1 / \tan(\pi fc_1 / fs)}$$

Transfer Function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

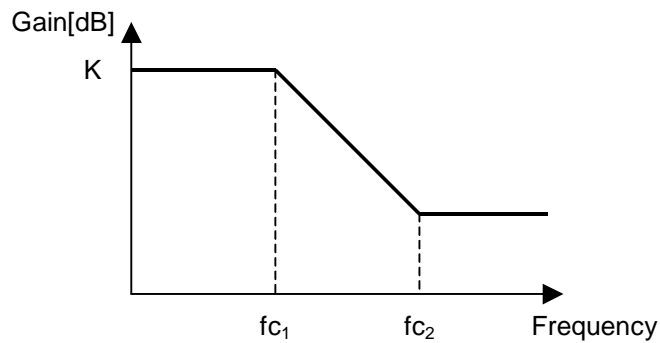


Figure 39. EQ0 Frequency Response

GN1 bit	GN0 bit	Gain
0	0	0dB
0	1	+12dB
1	x	+24dB

(default)

Table 27. Gain Setting (x: Don't care)

(5) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as equalizer or Notch Filter. 4-band equalizers (EQ2~EQ5) are switched ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. EQ1 bit controls ON/OFF switching of the equalizer after ALC (EQ1). When the equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0 bits, E1B15-0 bits and E1C15-0 bits set the coefficient of EQ1. E2A15-0 bits, E2B15-0 bits and E2C15-0 bits set the coefficient of EQ2. E3A15-0 bits, E3B15-0 bits and E3C15-0 bits set the coefficient of EQ3. E4A15-0 bits, E4B15-0 bits and E4C15-0 bits set the coefficient of EQ4. E5A15-0 bits, E5B15-0 bits and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1, 2, 3, 4 or 5) coefficient must be set when EQx bit = "0" or PMPFIL bit = "0". EQx starts operation 4/fs(max) after when EQx = PMPFIL bit = "1" is set.

Each EQ2 ~ 5 blocks have a common gain controller (EQCG) after the equalizer. EQCG7-0 bits control the gain, and EQCT2-0 bits control the gain transition time. EQCG7-0 bits setting is reflected by bringing EQCx bit (x=2~5) to "1". The setting value of EQCG7-0 bits are in common for EQ2~5. EQCG7-0 bits and EQCx bit (x=2~5) can be set during an operation (EQx=PMPFIL bit="1").

fs: Sampling Frequency

fo₁ ~ fo₅: Center Frequency

fb₁ ~ fb₅: Band width where the gain is 3dB different from the center frequency

K₁ ~ K₅: Gain (-1 ≤ K_n < 3)

Register Setting (Note 37)

EQ1: E1A[15:0] bits =A₁, E1B[15:0] bits =B₁, E1C[15:0] bits =C₁

EQ2: E2A[15:0] bits =A₂, E2B[15:0] bits =B₂, E2C[15:0] bits =C₂

EQ3: E3A[15:0] bits =A₃, E3B[15:0] bits =B₃, E3C[15:0] bits =C₃

EQ4: E4A[15:0] bits =A₄, E4B[15:0] bits =B₄, E4C[15:0] bits =C₄

EQ5: E5A[15:0] bits =A₅, E5B[15:0] bits =B₅, E5C[15:0] bits =C₅

(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1 + \tan(\pi fb_n/fs)}, \quad C_n = \frac{1 - \tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer Function

$$H(z) = \{1 + G_2 \times h_2(z) + G_3 \times h_3(z) + G_4 \times h_4(z) + G_5 \times h_5(z)\} \times \{1 + h_1(z)\}$$

(G_{2,3,4,5} = 1 or G)

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.

$$0.003 < fo_n / fs < 0.497$$

When gain of K is set to "-1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 37.

[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
 $X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$

X should be rounded to integer, and then should be translated to binary code (2's complement).
 MSB of each filter coefficient setting register is sine bit.

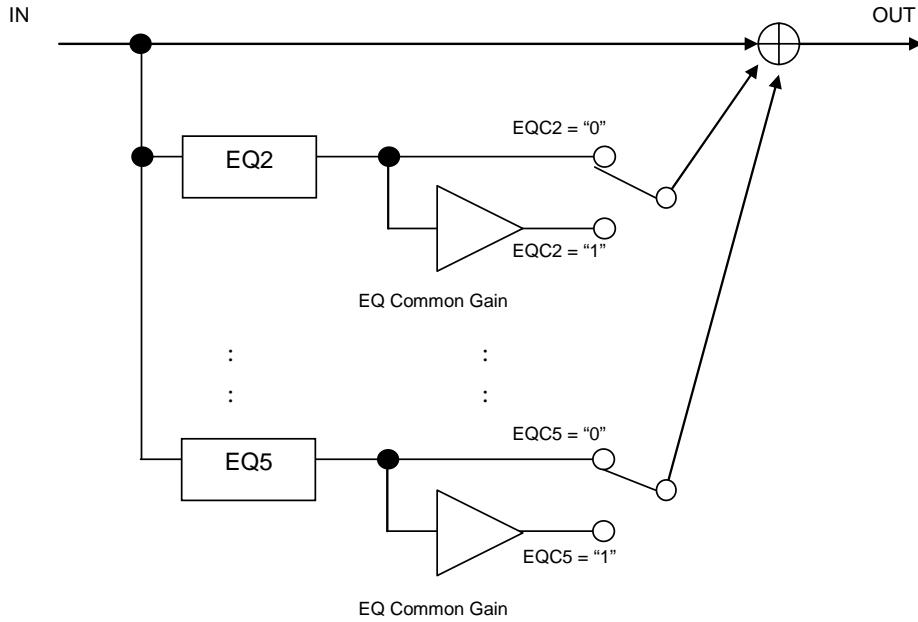


Figure 40 EQ Common Gain (EQC)

EQCG7-0 bits	EATT DATA	EQC Gain [dB]	Formula
FFH	255	0	-
FEH	254	-0.07	$20\log_{10}(\text{EATT DATA}/256)$
FDH	253	-0.1	
:	:	:	
02H	2	-42.14	
01H	1	-48.16	
00H	-	Mute	-

(default)

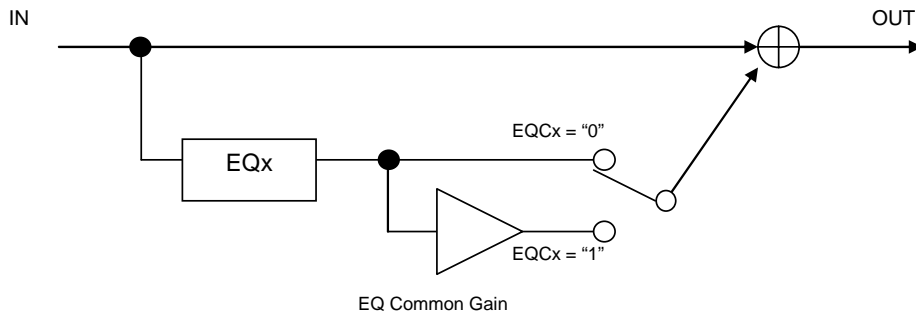
Table 28. EQC Gain Setting

EQCT2-0 bits	Transition Time of EQCG7-0 bits = FFH ~ 00H		
	Setting Value	fs=8kHz	fs=48kHz
000	256/fs	32ms	5.3ms
001	1024/fs	128ms	21.3ms
010	2048/fs	256ms	42.7ms
011	4096/fs	512ms	85.3ms
100	8192/fs	1024ms	170.7ms
101	16384/fs	2048ms	341.3ms
Others	N/A		

Table 29. Transition Time of EQ Common Gain (N/A: Not available)

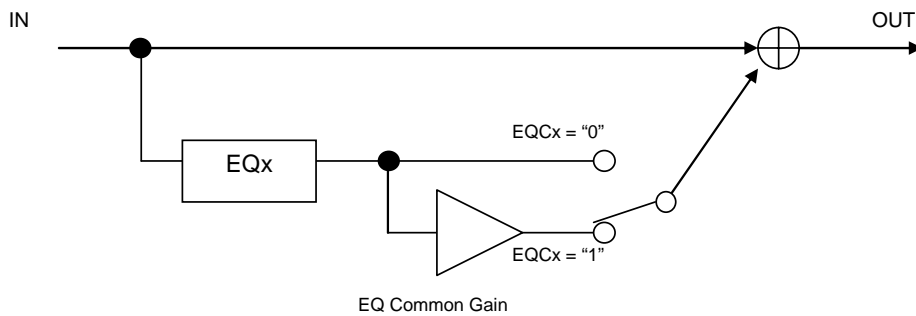
Common Gain Sequence Examples

<When noise is generated>



(1) Set EQCx bit: “1” → “0” (Path Setting). The gain changes immediately by this setting.

<When noise is stopped>



(assuming to continue the sequence from above)

- (2) Set EQCT2-0 bits: “xxx” → “000” (Transition Time)
 - (3) Set EQCG7-0 bits (Gain Setting; should be set to 0dB)
 - (4) Set EQCx bit: “0” → “1” (Path Setting), EQCT2-0 bits Setting (Transition Time: It can be set longer when noise is stopped.) (Note 38)
 - (5) Set EQCG7-0 bits (Gain Setting)
- The gain of EQx is changed after a transition time set by EQCT2-0 bits.

Note 38. When changing a path of EQC2-5 by setting EQC2-5 bits “0” → “1”, the gain should be transitioned to 0dB before the settings. Otherwise, pop noise may occur on the path change.

■ ALC Input Level Read Function

The input level before ALC can be read by INVLO6-0 bits. The input level which is read by this function is bigger output between L and R channels after the signals are averaged by moving average circuit following HPF3. The cutoff frequency of the HPF3 is set by HPF3C2-0 bits. When HPF3 bit = “0”, the audio data passes through the HPF3 block by 0dB gain. Available range of ALC input level reading is from 0 to -95.25dB. It indicates -95.25dB if the read value is less than -95.25dB. ALC input level read should be executed with an interval of 512/fs (min.) after changing HPF3 bit “0” → “1”.

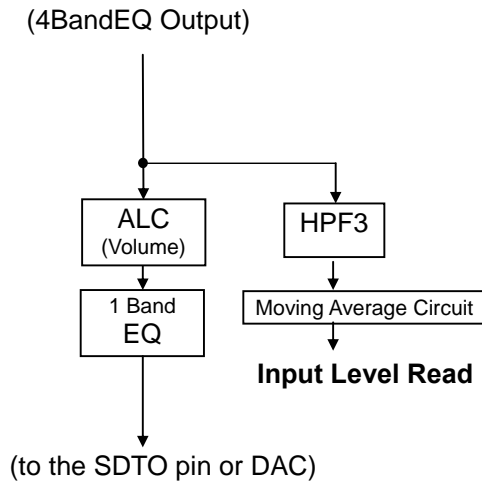


Figure 41. ALC Input Level Read Function

HPF3C2-0 bits	Cutoff Frequency [Hz]		
	fs = 8kHz	fs = 16kHz	fs =48kHz
000	83	167	500
001	167	333	1000
010	250	500	1500
011	333	667	2000
100	500	1000	3000
101	667	1333	4000

(default)

Table 30. HPF3 Cutoff Frequency Setting

INVOL6-0 bits	Input Level [dB]
7FH	-95.25
7EH	-94.5
7DH	-93.75
7CH	-93
:	:
02H	-1.5
01H	-0.75
00H	0

(default)

Table 31. ALC Input Level

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit is “1”, the ALC circuit operates for recording path, and the ALC circuit operates for playback path when ADCPF bit is “0”. ALC1 bit controls ON/OFF of ALC operation at recording path, and ALC2 bit controls ON/OFF of ALC operation at playback path.

Note 39. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.

Note 40. In this section, ALC means ALC1 for recording path, ALC2 for playback path.

Note 41. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 32), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 33). The VOL is then set to the same value for both channels.

When ZELMN bit = “0” (zero cross detection is enabled), the VOL value is changed by ALC limiter operation at the individual zero crossing points of L channel and R channel, or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 34). When ALC output level exceeds full-scale at LFST bit = “1”, VOL values are immediately (Period: 1/fs) changed in 1step(L/R common). When ALC output level is less than full-scale, VOL values are changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = “1” (zero cross detection is disabled), VOL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

After completing the attenuate operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Counter Reset Level	(default)
0	0	ALC Output $\geq -2.5\text{dBFS}$	$-2.5\text{dBFS} > \text{ALC Output} \geq -4.1\text{dBFS}$	
0	1	ALC Output $\geq -4.1\text{dBFS}$	$-4.1\text{dBFS} > \text{ALC Output} \geq -6.0\text{dBFS}$	
1	0	ALC Output $\geq -6.0\text{dBFS}$	$-6.0\text{dBFS} > \text{ALC Output} \geq -8.5\text{dBFS}$	
1	1	ALC Output $\geq -8.5\text{dBFS}$	$-8.5\text{dBFS} > \text{ALC Output} \geq -12\text{dBFS}$	

Table 32. ALC Limiter Detection Level/ Recovery Counter Reset Level

LMAT1 bit	LMAT0 bit	ALC1 Limiter ATT Step				(default)
		ALC1 Output $\geq \text{LMTH}$	ALC1 Output $\geq \text{FS}$	ALC1 Output $\geq \text{FS} + 6\text{dB}$	ALC1 Output $\geq \text{FS} + 12\text{dB}$	
0	0	1	1	1	1	
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 33. ALC Limiter ATT Step

ZTM1 bit	ZTM0 bit	Zero Cross Time Out			(default)	
			8kHz	16kHz		48kHz
0	0	128/fs	16ms	8ms	2.7ms	
0	1	256/fs	32ms	16ms	5.3ms	
1	0	512/fs	64ms	32ms	10.7ms	
1	1	1024/fs	128ms	64ms	21.3ms	

Table 34. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

ALC recovery operation wait for the WTM2-0 bits (Table 35) to be set after completing ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 32) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 36) up to the set reference level (Table 37) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 34). The ALC recovery operation is executed in a period set by WTM2-0 bits. If the setting of ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is executed at a period set by ZTM1-0 bits.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to “01”, VOL is changed to 32H by auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When

“ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

“ALC recovery waiting counter reset level (LMTH1-0) > Output Signal”, the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits (Table 39).

WTM2 bit	WTM1 bit	WTM0 bit	ALC Recovery Operation Waiting Period			(default)
			8kHz	16kHz	48kHz	
0	0	0	128/fs	16ms	8ms	2.7ms
0	0	1	256/fs	32ms	16ms	5.3ms
0	1	0	512/fs	64ms	32ms	10.7ms
0	1	1	1024/fs	128ms	64ms	21.3ms
1	0	0	2048/fs	256ms	128ms	42.7ms
1	0	1	4096/fs	512ms	256ms	85.3ms
1	1	0	8192/fs	1024ms	512ms	170.7ms
1	1	1	16384/fs	2048ms	1024ms	341.3ms

Table 35. ALC Recovery Operation Waiting Period

RGAIN1 bit	RGAIN0 bit	GAIN STEP		(default)
0	0	1 step	0.375dB	
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 36. ALC Recovery Gain Step

IREF7-0 bits	GAIN (dB)	Step
F1H	+36.0	0.375dB (default)
F0H	+35.625	
EFH	+35.25	
:	:	
E1H	+30.0	
:	:	
92H	+0.375	
91H	0.0	
90H	-0.375	
:	:	
2H	-53.625	
1H	-54.0	
0H	MUTE	

Table 37. Reference Level of ALC Recovery Operation for Recoding

OREF5-0 bits	GAIN (dB)	Step
3CH	+36.0	1.5dB (default)
3BH	+34.5	
3AH	+33.0	
:	:	
28H	+6.0	
:	:	
25H	+1.5	
24H	0.0	
23H	-1.5	
:	:	
2H	-51.0	
1H	-52.5	
0H	-54.0	

Table 38. Reference Level of ALC Recovery Operation for Playback

RFST1 bit	RFST0 bit	Recovery Speed
0	0	Double
0	1	Quad
1	0	8times
1	1	16times

Table 39. Fast Recovery Speed Setting (FRN bit = "0")

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is possible to check the current volume by reading the register value of VOL7-0 bits.

VOL7-0 bits	GAIN (dB)
F1H	+36.0
F0H	+35.625
EFH	+35.25
:	:
C5H	+19.5
:	:
92H	+0.375
91H	0.0
90H	-0.375
:	:
2H	-53.625
1H	-54.0
0H	MUTE

Table 40. Value of VOL7-0 bits

4. Example of ALC Setting

Table 41 and Table 42 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	-4.1dBFS	01	-4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
FRN	Fast Recovery mode	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	21.3ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same value or larger value than ZTM1-0 bits	001	32ms	100	42.7ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	01	4 times	01	4 times
ALC1	ALC1 enable	1	Enable	1	Enable

Table 41. Example of the ALC Setting (Recording)

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	-4.1dBFS	01	-4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
FRN	Fast Recovery mode	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	21.3ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same value or larger value than ZTM1-0 bits	001	32ms	100	42.7ms
OREF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
OVL7-0, OVR7-0	Gain of VOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	01	4 times	01	4 times
ALC2	ALC2 enable	1	Enable	1	Enable

Table 42. Example of the ALC Setting (Playback)

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is stopped by ALC1 bit = ALC2 bit= "0". ALC output is "0" data until the AK4957 becomes manual mode after writing "0" to ALC1 and ALC2 bits.

LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN 1-0, IREF7-0, OREF5-0, ZELMN, RFST1-0, LFST, FRN bits

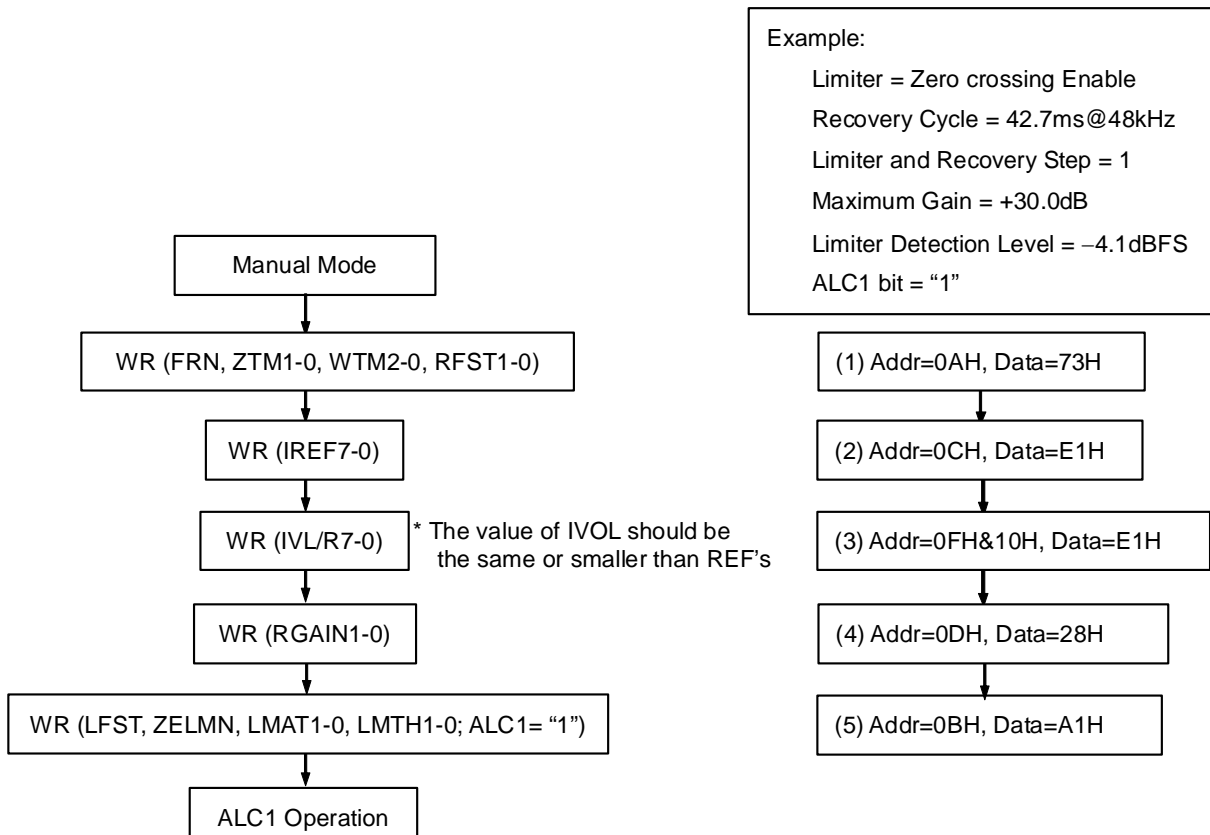


Figure 42. Registers Set-up Sequence at ALC1 Operation (recording path)

6. ALC REF Inflection Point Setting for Recording

The AK4957 can change the slope of REF (input/output characteristics) on an inflection point at recording ALC (ADC side). RF2P2-0 bits control the inflection point and RF2SL2-0 bits control the REF slope that is in the range of when the input volume level is less than the inflection point. (In the following description, the input/output characteristics of REF that is in the range of when the input volume level is over the inflection point (IREF) is described as REF1 and when the input volume level is less than the inflection point is described as REF2.) ALC bit must be “0” when changing RF2P2-0 bits setting. RF2SL2-0 bits can be set regardless of ALC bit setting. RF2P2-0 bits and RF2SL2-0 bits cannot be used when playback (DAC side) or when REF value < 0dB.

When setting REF2SL2-0 bits = “000” → “xxx” (REF1 → REF2), the output volume changes to REF2 value immediately.

When setting REF2SL2-0 bits = “xxx” → “000” (REF2 → REF1), the output volume changes to REF1 value according to the ALC recovery setting.

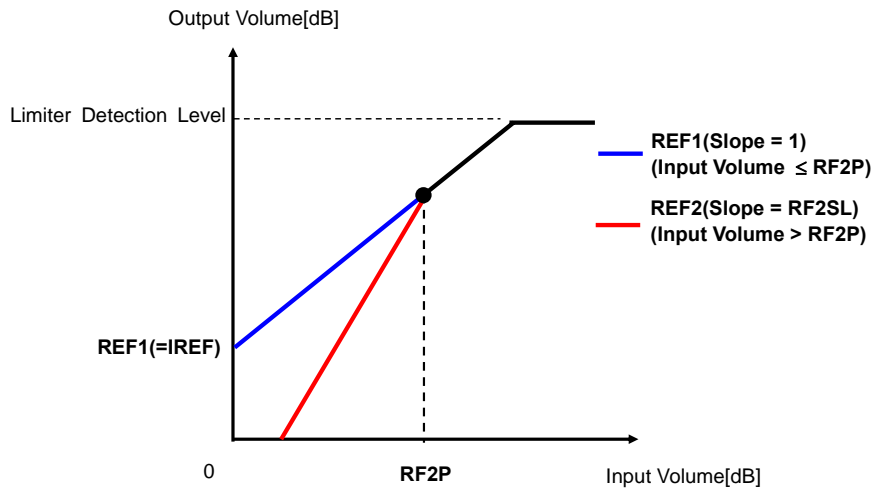


Figure 43. ALC REF Change when Recording

RF2P2-0 bits	RF2P[dB]	Step
000	-33	3dB (default)
001	-36	
010	-39	
011	-42	
100	-45	
101	-48	
110	-51	
111	-54	

Table 43 Inflection Point RF2P Setting

RF2SL2-0 bits	REF2 Slope
000	1.0 (default)
001	1.125
010	1.25
011	1.375
100	1.5
Others	N/A

Table 44 REF2 Inflection Setting (N/A: Not available)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC1 bit is set to “0” while ADCPF bit is “1”. This mode is used in the cases shown below.

1. After exiting reset state, when setting up the registers for ALC operation (ZTM1-0, LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed.
For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 45). The IVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits. Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = “0”. IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = “1”. When changing the volume, zero cross detection is executed on both Lch and Rch independently.

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step
F1H	+36.0	0.375dB (default)
F0H	+35.625	
EFH	+35.25	
:	:	
E2H	+30.375	
E1H	+30.0	
E0H	+29.625	
:	:	
03H	-53.25	
02H	-53.625	
01H	-54	
00H	MUTE	

Table 45. Input Digital Volume Setting

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = “0”, IVOL operation starts with the written values after PMPFIL bit is changed to “1”.

When writing to IVOL7-0 bits continually, take an interval of zero crossing timeout period or more. If not, the zero crossing counters are reset at each time and the volume will not be changed. However, when writing the same register values as the previous time, the zero crossing counters will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC2 bit to “0” when PMPFIL = PMDAC bits = “1” and ADCPF bit is “0”. The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 46). When the OVOLC bit = “1”, the OVL7-0 bits control both L and R channel volume levels. When the OVOLC bit = “0”, the OVL7-0 bits control L channel volume level and the OVR7-0 bits control R channel volume level. When changing the volumes, zero cross detection is executed on both L and R channels independently. The OVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits.

OVL7-0 bits OVR7-0 bits	GAIN [dB]	Step
F1H	+36.0	0.375dB (default)
F0H	+35.625	
EFH	+35.25	
⋮	⋮	
92H	+0.375	
91H	0.0	
90H	-0.375	
⋮	⋮	
2H	-53.625	
1H	-54.0	
0H	MUTE	

Table 46. Output Digital Volume Setting

When writing to the OVL7-0 bits and OVR7-0 bit continuously, the control register should be written in an interval more than zero crossing timeout. If not, the zero crossing counters are reset at each time and the volume will not be changed. However, when writing the same register values as the previous time, the zero crossing counter will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ Output Digital Volume 2

The AK4957 has a digital output volume (256 levels, 0.5dB step, Mute). The volume is included in front of a DAC block. The input data of DAC is changed from +12 to -115dB or MUTE. The DVOL7-0 bits control both Lch and Rch volume levels together. This volume has soft transition function. Therefore no switching noise occurs during the transition. The DVTM bit set the transition time between set values of DVOL7-0 bits (from 00H to FFH) as either 256/fs or 1024/fs (Table 48). When DVTM bit = "0", it takes 1024/fs (=21.3ms@fs=48kHz) from 00H (+12dB) to FFH (MUTE).

DVOL7-0 bits	Gain	Step
00H	+12.0dB	0.5dB (default)
01H	+11.5dB	
02H	+11.0dB	
⋮	⋮	
18H	0dB	
⋮	⋮	
FDH	-114.5dB	
FEH	-115.0dB	
FFH	Mute ($-\infty$)	

Table 47. Output Digital Volume2 Setting

DVTM bit	Transition Time between DVOL7-0 bits = 00H and FFH		
	Setting	fs=8kHz	fs=48kHz
0	1024/fs	128ms	21.3ms
1	256/fs	32ms	5.3ms

Table 48. Transition Time Setting of Output Digital Volume2

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set “1”, the output signal is attenuated by $-\infty$ (“0”) during the cycle set by DVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by DVOL7-0 bits from $-\infty$ during the cycle set by DVTM bit. If the soft mute is cancelled within the cycle set by DVTM bit after starting the operation, the attenuation is discontinued and returned to the level set by DVOL7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transaction.

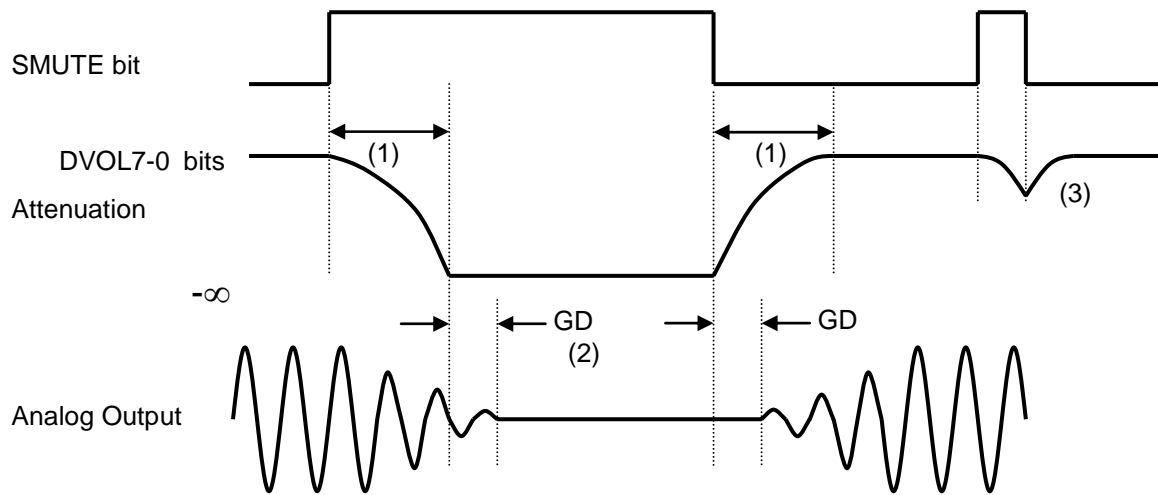


Figure 44. Soft Mute Function

- (1) The input signal is attenuated to $-\infty$ (“0”) in the cycle set by DVTM bit. When ATT DATA = +12dB (00H), $256/f_s = 5.3\text{ms}@ f_s=48\text{kHz}$, DVTM bit= “1”.
- (2) Analog output corresponding to digital input has group delay (GD).
- (3) If soft mute is cancelled before attenuating to $-\infty$, the attenuation is discontinued and returned to the level set by DVOL7-0 bits within the same cycle.

■ BEEP Input

When BEEPS bit is set to “1” during PMBP bit= “1”, the input signal from the MIN pin is output to Speaker-Amp. When BEEPL bit is set to “1”, the input signal from the MIN pin is output to the stereo line output amplifier. An external resistor R_i adjusts the signal level of MIN input when BPM bit = “1”. Table 52 and Table 53 show the typical gain example when $R_i = 66k\Omega$. This gain is in inverse proportion to the R_i value. When BPM bit = “0”, the external resistor R_i is not necessary. BPLVL2-0 bits set the gain of MIN-Amp, and the total gain is defined according to LVCM1-0 and SPKG1-0 bits settings.

BPM bit	BEEP Mode
0	Internal Resistance Mode
1	External Resistance Mode

(default)

Table 49. BEEP Mode Setting

1. MIN-Amp Common Potential

BPVCM bit set the common voltage of MIN input amplifier. (Table 50) When BPVCM bit = “1”, maximum value is AVDD Vpp. Set BEEP GAIN (BPLVL3-0 bits) to keep MIN-Amp output amplitude less than 0.1Vpp.

BPVCM bit	MIN-Amp Common Voltage (typ)
0	1.15V
1	1.65V

(default)

Table 50. Common Potential Setting of MIN-Amp

• Internal Resistance Mode (BPM bits = “0”)

Input BEEP gain is controlled by BPLVL3-0 bits (Table 51). In this case an external resistor R_i is not necessary.

BPLVL3 bit	BPLVL2 bit	BPLVL1 bit	BPLVL0 bit	BEEP Gain
0	0	0	0	0dB
0	0	0	1	-6dB
0	0	1	0	-12dB
0	0	1	1	-18dB
0	1	0	0	-24dB
0	1	0	1	-30dB
0	1	1	0	-33dB
0	1	1	1	-36dB
1	0	0	0	-39dB
1	0	0	1	-42dB
Other	N/A			

(default)

Table 51. BEEP Output Gain Setting when BPM bit = “0” (N/A: Not available)

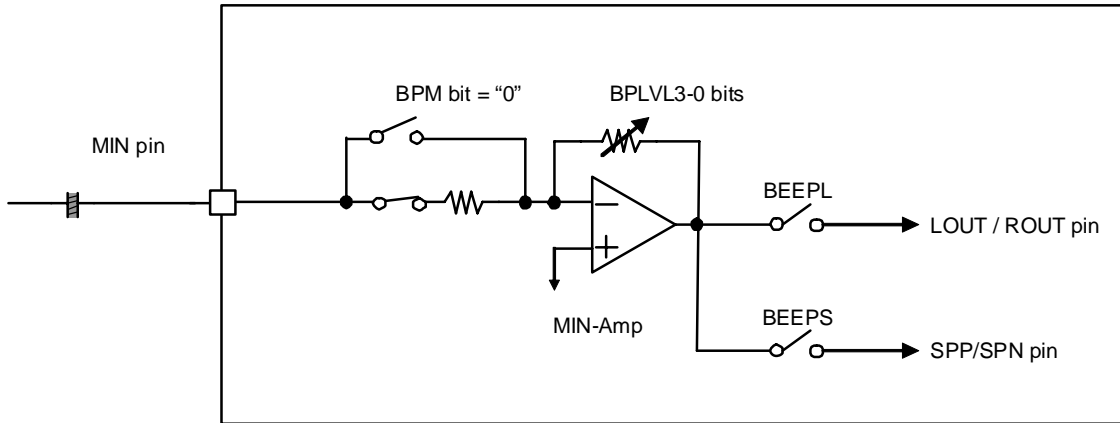


Figure 45. Block Diagram of MIN pin (BPM bit = “0”)

• External Resistance Mode (BPM bit = “1”)

Gain setting of input BEEP signal is controlled by an external resistor R_i . The gain is in inverse proportion to the R_i value. (Figure 46) Gain setting by BPLVL3-0 bits is not available.

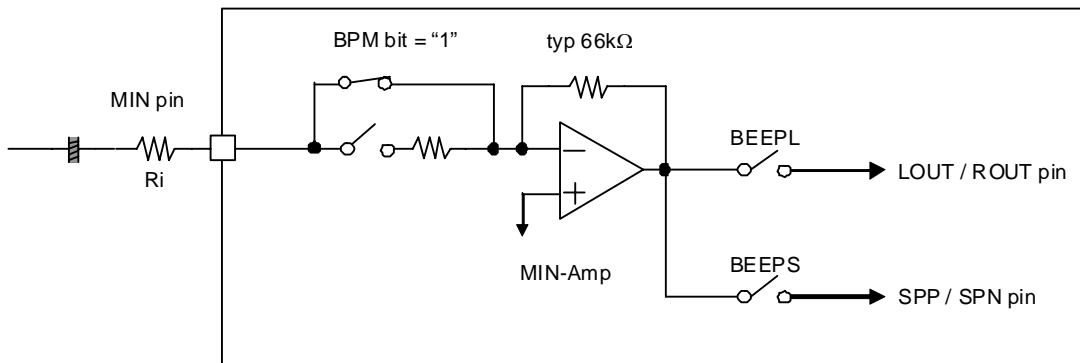


Figure 46. Block Diagram of MIN pin (BPM bit = “1”)

SPKG1-0 bits	MIN → SPP/SPN Gain		(default)
	ALC2 bit = “0”	ALC2 bit = “1”	
00	+6.1dB	+8.1dB	
01	+8.1dB	+10.1dB	
10	+10.1dB	+12.1dB	
11	+12.1dB	+14.1dB	

Table 52. MIN → SPK Output Gain

LVCM1-0 bits	AVDD	MIN → Lineout Gain	Lineout Common Voltage (typ)	(default)
00	2.8 ~ 3.6V	0dB	1.3V	
01	3.0 ~ 3.6V	+2dB	1.5V	
10	2.8 ~ 3.6V	+2dB	1.3V	
11	3.0 ~ 3.6V	+4dB	1.5V	

Table 53. MIN → Lineout Output Gain

■ Stereo Line Output (LOUT, ROUT pin)

When DACL bit is set to “1”, L and R channel signals of DAC are output in single-ended format via LOUT and ROUT pins. When DACL bit is “0”, output signals are muted and LOUT and ROUT pins output common voltage. The load impedance is 10kΩ (min.). When the PMLO bit = LOPS bit = “0”, the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS bit is “1”, stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit when LOPS bit = “1”. In this case, output signal line should be pulled-down to AVSS by 20kΩ after AC coupled as Figure 48. Rise/Fall time is 300ms (max) when C=1μF and R_L=10kΩ. When PMLO bit = “1” and LOPS bit = “0”, stereo line output is in normal operation.

LOVL1-0 bits set the gain of stereo line output.

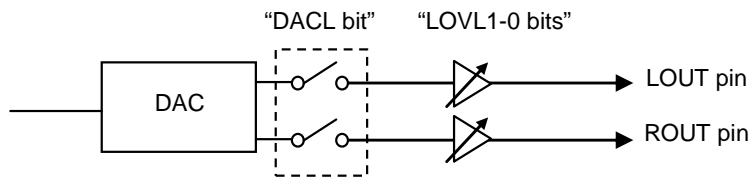


Figure 47. Stereo Line Output

LOPS bit	PMLO bit	Mode	LOUT/ROUT pin
0	0	Power Down	Pull-down to VSS1
	1	Normal Operation	Normal Operation
1	0	Power Save	Fall down to VSS1
	1	Power Save	Rise up to Common Voltage

(default)

Table 54. Stereo Line Output Mode Select

LVCM1-0 bits	AVDD	Gain	Common Voltage (typ)
00	2.8 ~ 3.6V	0dB	1.3V
01	3.0 ~ 3.6V	+2dB	1.5V
10	2.8 ~ 3.6V	+2dB	1.3V
11	3.0 ~ 3.6V	+4dB	1.5V

(default)

Table 55. Stereo Lineout Volume Setting

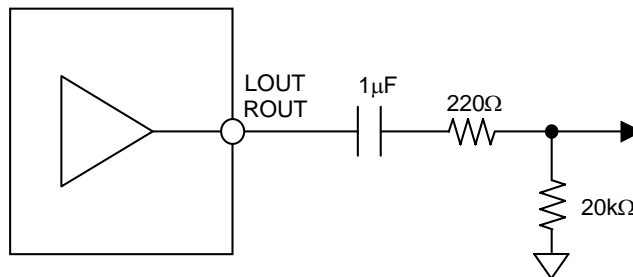


Figure 48. External Circuit for Stereo Line Output (in case of using a Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

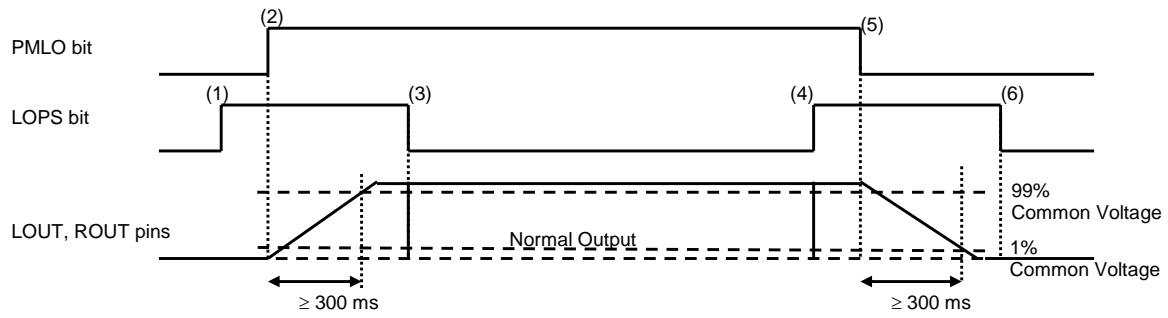


Figure 49. Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

- (1) Set LOPS bit = "1". Stereo line output enters power-save mode.
- (2) Set PMLO bit = "1". Stereo line output exits power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) when $C=1\mu\text{F}$.
- (3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits power-save mode.
Stereo line output is enabled.
- (4) Set LOPS bit = "1". Stereo line output enters power-save mode.
- (5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max 300ms) at $C=1\mu\text{F}$.
- (6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits power-save mode.

< Mono Mixing Output >

Mono mixing outputs are available by setting MONO1-0 bits. Inputted digital data from the SDTI pin can be converted to mono signal $[(L+R)/2]$ and are output via LOUT and ROUR pins. (Figure 34)

MONO1 bit	MONO0 bit	LOUT pin	ROUT pin
0	0	Lch	Rch
0	1	Lch	Lch
1	0	Rch	Rch
1	1	$(Lch+Rch)/2$	$(Lch+Rch)/2$

(default)

Table 56. Output Data Select via LOUT/ROUT pin

■ Speaker Output

The DAC output signal is input to the speaker amplifier as mono signal $[(L+R)/2]$. The speaker amplifier has mono output as it is BLT (Bridged Transless) capable. The gain and output level are set by SPKG1-0 bits. The output level depends on AVDD and SPKG1-0 bits setting.

SPKG1-0 bits	Gain	
	ALC bit = "0"	ALC bit = "1"
00	+6.1dB	+8.1dB
01	+8.1dB	+10.1dB
10	+10.1dB	+12.1dB
11	+12.1dB	+14.1dB

(default)

Table 57. SPK-Amp Gain

SPKG1-0 bits	SPK-Amp Output (DAC Input=0dBFS, AVDD= 3.3V)	
	ALC bit = "0"	ALC bit = "1" (LMTH1-0 bits = "00")
00	3.37Vpp	3.17Vpp
01	4.23Vpp (Note 42)	4.00Vpp
10	5.33Vpp (Note 42)	5.04Vpp (Note 42)
11	6.71Vpp (Note 42)	6.33Vpp (Note 42)

(default)

Note 42. The output level is calculated on the assumption that the signal is not clipped. However, in the actual case, the SPK-Amp output signal is clipped when DAC outputs 0dBFS signal. When SPKG1-0 bits = "10" (ALC bit = "0"), ideal output level is 5.33Vpp. In the actual case, the output level is $1.79V_{rms}@S/(N+D)=typ. 20dB$. The SPK-Amp output level should be kept under 4.0Vpp (AVDD=3.3V) by adjusting digital volume to prevent clipped noise.

Table 58. SPK-Amp Output Level

< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSPK bit. When PMSPK bit is “0”, both SPP and SPN pins are in Hi-Z state. When PMSPK bit is “1” and SPPSN bit is “0”, the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs AVDD/2 voltage.

When the PMSPK bit is “1” after the PDN pin is changed from “L” to “H”, the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to AVDD/2 voltage. Because the SPP and SPN pins rise up in power-save mode, pop noise can be reduced. When the AK4957 is powered-down (PMSPK bit = “0”), pop noise can also be reduced by first entering power-save-mode.

PMSPK bit	SPPSN bit	Mode	SPP pin	SPN pin
0	x	Power-down	Hi-Z	Hi-Z
1	0	Power-save	Hi-Z	AVDD/2
	1	Normal Operation	Normal Operation	Normal Operation

(default)

Table 59 Speaker-Amp Mode Setting (x: Don't care)

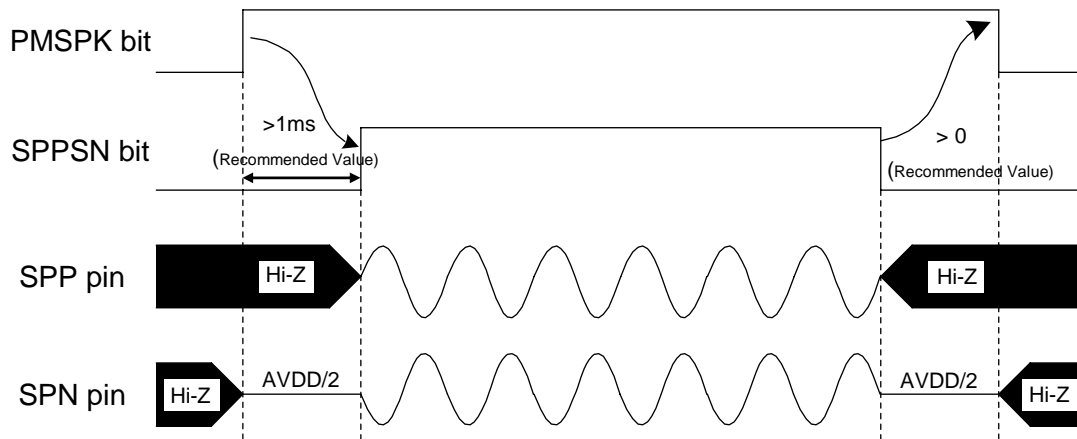


Figure 50. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

When the internal temperature of the device rises up irregularly (e.g. when output pins are shortened), the speaker amplifier is automatically powered down and then THDET bit becomes “1” (thermal shutdown). The thermal shutdown status can be monitored by reading THDET bit. When the thermal shutdown is executed, all blocks except VCOM and LDO blocks are powered-down. These blocks will not return to a normal operation until being reset by the PDN pin. THDET bit becomes “0” by this PDN pin reset.

■ Video Block

The integrated video amplifier has drivability for a load resistance of 150Ω (Figure 51). The AK4957 has a composite input and output. A Low Pass Filter (LPF) and volume are integrated, and VG1-0 bits set the gain (+6/+9/+12/+16.5 dB) (Table 60). The video signal's clamp level is 50mV (typ). The video amplifier power management is controlled by PMV bit. When PMV bit = "0", the VOUT pin outputs 0V. The video inputs must be C-coupled by a 0.047μF capacitor. The video signal source impedance at transmitting side must be in the range of 0.075 ~ 1.6kΩ.

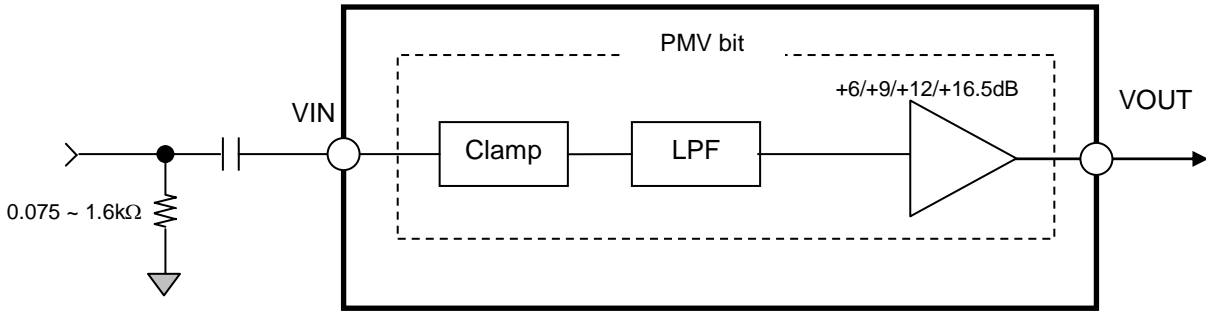


Figure 51. Video Block Diagram

VG1-0 bits	GAIN
00	+6dB
01	+9dB
10	+12dB
11	+16.5dB

(default)

Table 60. Video Signal Gain Setting

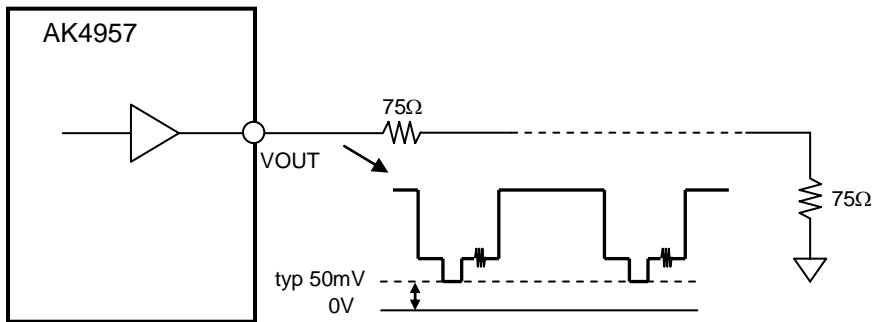


Figure 52. Video Signal Output

■ Regulator Block

The AK4957 integrates a regulator. The 3.3V (typ) power supply voltage from the AVDD pin is converted to 2.3V (typ) by the regulator and supplied to the analog blocks (MIC-Amp, ADC, DAC, MIN, Video-Amp). The regulator is powered up by PMVCM bit = "1", and powered down by PMVCM = "0". Connect a 2.2 μ F (\pm 50%) capacitor to the REGFIL pin to reduce noise on AVDD.

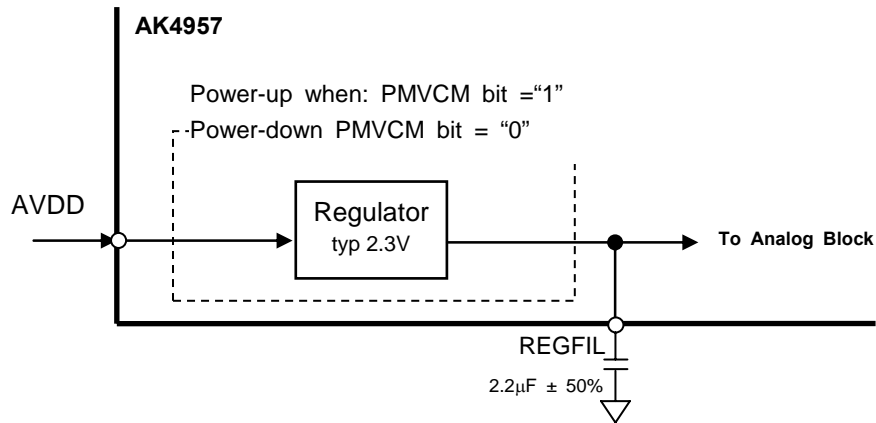


Figure 53 Regulator Block

■ Serial Control Interface

(1) 3-wire Serial Control Mode

1. Data Writing and Reading Modes on Every Address (00H~13H, 15H~50H)

One data is written to (read from) one address.

Internal registers may be written by using 3-wire serial interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control data or Output data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. Data writings become available on the rising edge of CSN. When reading the data, the CDTIO pin changes to output mode at the falling edge of 8th CCLK and outputs data in D7-D0. However this reading function is available only when READ bit = "1". When READ bit = "0", the CDTIO pin stays as Hi-Z even after the falling edge of 8th CCLK. The data output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except when outputting the data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = "L".

Note 43. Data reading is only available on the following addresses; 00 ~ 13H and 15H ~ 50H. When reading the other addresses, the register values are invalid.

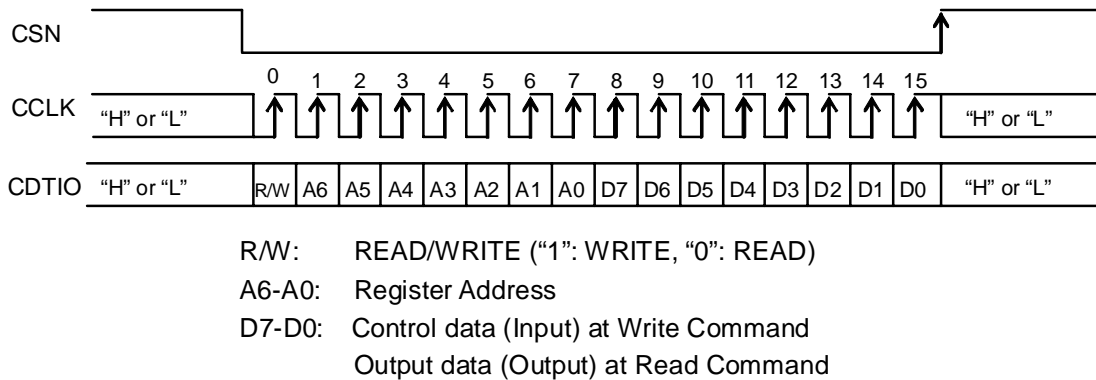


Figure 54. Serial Control Interface Timing 1

2. Continuous Data Writing Mode (00H~13H, 15H~50H)

Address is incremented automatically and data is written continuously. This mode does not support reading. When the written address reaches 50H, it is automatically incremented to 00H. Writing to the address 0EH and 15H are ignored.

In this mode, registers are written by 3-wire serial interface pins (CSN, CCLK and CDTIO). The data on the 3-wire serial interface is 8 bit data, consisting of register address (MSB-first, 7bits) and control or output data (MSB-first, 8xN bits)). The receiving data is latched on a rising edge (“↑”) of CCLK. The first write data becomes effective between the rising edge (“↑”) and the falling edge (“↓”) of 16th CCLK. When the micro processor continues sending CDTIO and CCLK clocks while the CSN pin = “L”, the address counter is incremented automatically and writing data becomes effective between the rising edge (“↑”) and the falling edge (“↓”) of every 8th CCLK. For the last address, writing data becomes effective between the rising edge (“↑”) of 8th CCLK and the rising edge (“↑”) of CSN. The clock speed of CCLK is 5MHz (max). The internal registers are initialized by the PDN pin = “L”.

Even through the writing data does not reach the last address; a write command can be completed when the CSN pin is set to “H”.

Note 44. When CSN “↑” was written before “↑” of 8th CCLK in continuous data writing mode, the previous data writing address becomes valid and the writing address is ignored.

Note 45. After 8bits data in the last address became valid, put the CSN pin “H” to complete the write command. If the CDTIO and CCLK inputs are continued when the CSN pin = “L”, the data in the next address, which is incremented, is over written.

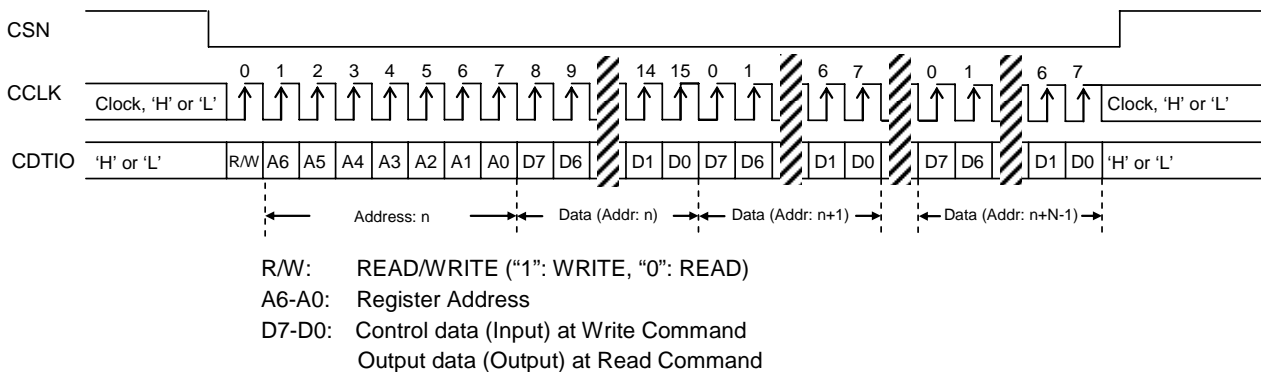


Figure 55. Serial Control Interface Timing 2 (Continuous Writing Mode)

(2) I2C-bus Control Mode (I2C pin = "H")

The AK4957 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to 6V or less voltage. READ bit must be set to "1" before reading data.

(2)-1-1. WRITE Operations

Figure 56 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 62). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 57). If the slave address matches that of the AK4957, the AK4957 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 63). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4957. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 58). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 59). The AK4957 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 62).

The AK4957 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4957 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "50H" prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 64) except for the START and STOP conditions.

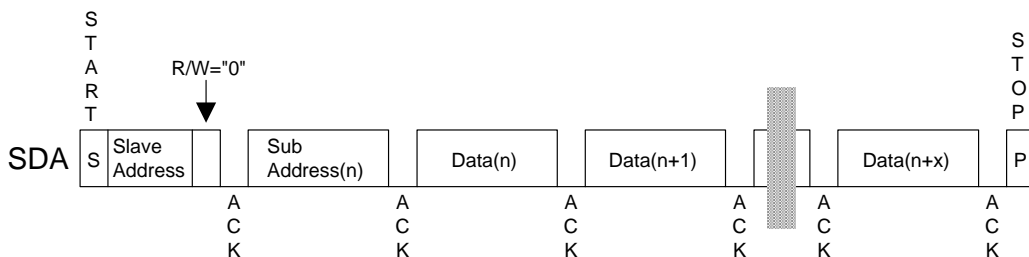


Figure 56. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	1	CAD0	R/W
---	---	---	---	---	---	------	-----

Figure 57. The First Byte

0	A6	A5	A4	A3	A2	A1	A0
---	----	----	----	----	----	----	----

Figure 58. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Figure 59. The Third Byte

(2)-1-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4957. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 50H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

Note 43. Data reading is only available on the following addresses; 00 ~ 13H and 15H ~ 50H. When reading the other addresses, the register values are invalid.

The AK4957 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4957 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4957 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4957 ceases the transmission.

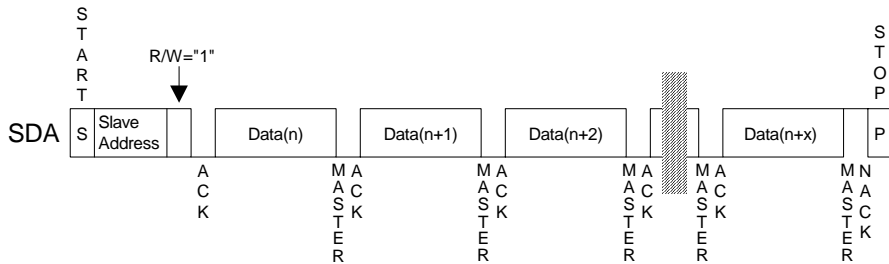


Figure 60. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4957 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4957 ceases the transmission.

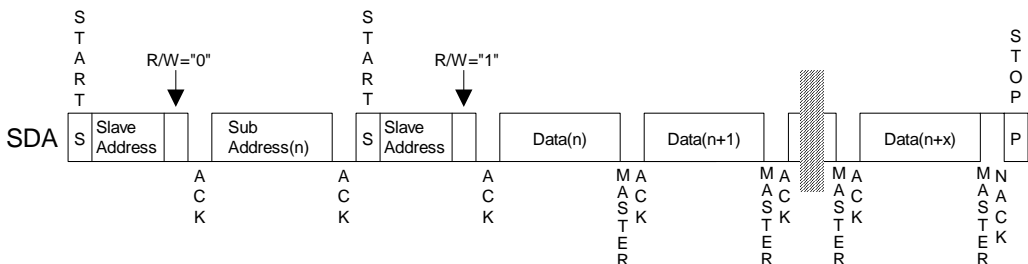


Figure 61. Random Address Read

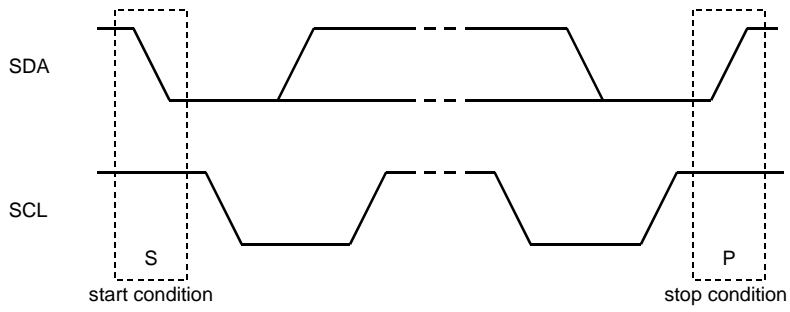


Figure 62. Start Condition and Stop Condition

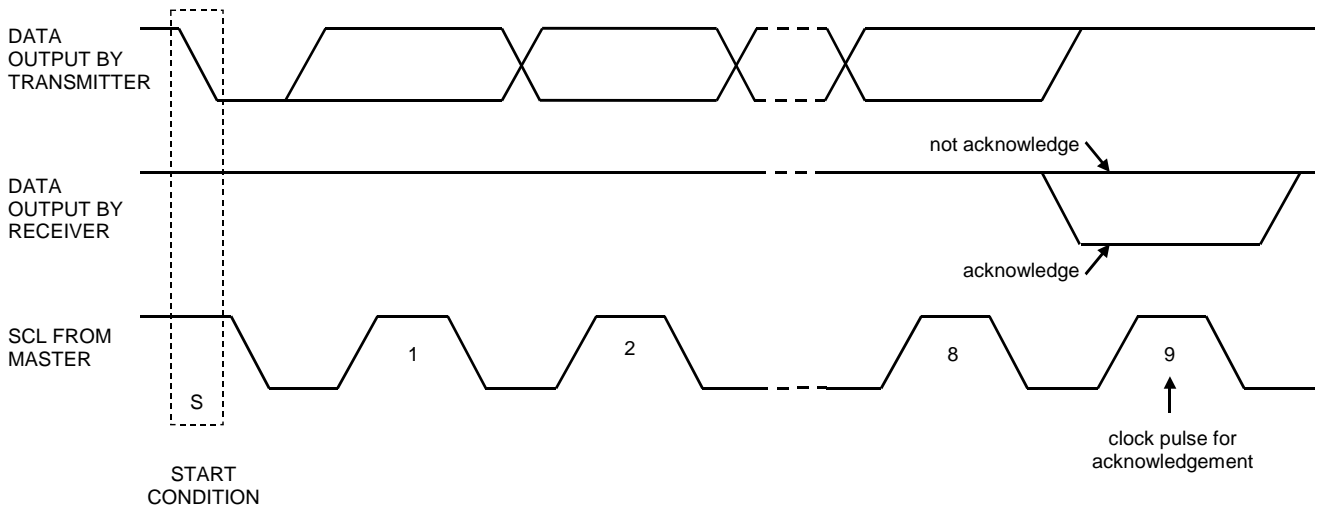


Figure 63. Acknowledge (I²C Bus)

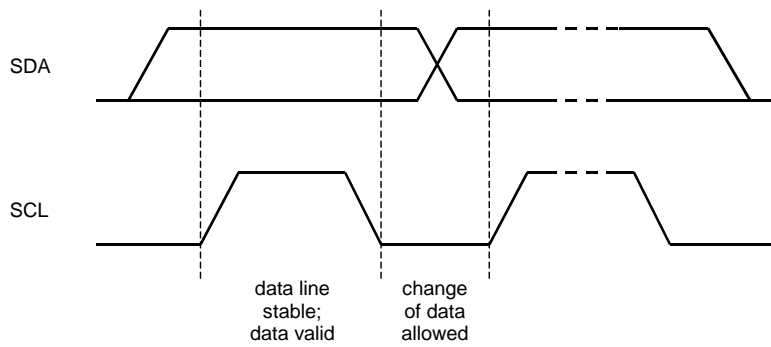


Figure 64. Bit Transfer (I²C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
01H	Power Management 2	PMMICR	PMMICL	0	PMMP	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPPSN	0	0	MICL	0	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	BEEPS	DACS	0	0	INR	INL
04H	Signal Select 3	MONO1	MONO0	LOPS	DACL	BEEPL	0	LVCMI	LVCMI0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
06H	Mode Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
07H	Mode Control 3	READ	THDET	SMUTE	DVOLC	OVOLC	IVOLC	0	0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST0	0	0	0	0	0	DVTM
0AH	ALC Timer Select	FRN	ZTM1	ZTM0	WTM2	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	LMTH1	LMTH0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
0DH	ALC Mode Control 3	RGAIN1	RGAIN0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
13H	Digital Volume2 Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
14H	Reserved	0	0	0	0	0	0	0	0
15H	ALC Input Level	0	INVOL6	INVOL5	INVOL4	INVOL3	INVOL2	INVOL1	INVOL0
16H	REF2 Setting	0	RF2SL2	RF2SL1	RF2SL0	0	RF2P2	RF2P1	RF2P0
17H	Lch MIC Gain Setting	0	0	0	MGL4	MGL3	MGL2	MGL1	MGL0
18H	Rch MIC Gain Setting	0	0	0	MGR4	MGR3	MGR2	MGR1	MGR0
19H	BEEP Volume Control		BPVCM	0	BPM	BPLVL3	BPLVL2	BPLVL1	BPLVL0
1AH	Video Control	0	0	0	0	VG1	VG0	0	PMV
1BH	HPF Filter Control	0	HPF3C2	HPF3C1	HPF3C0	0	HPFC1	HPFC0	HPFAD
1CH	Digital Filter Select 1	HPF3	0	LPF	HPF	EQ0	GN1	GN0	FIL3
1DH	Digital Filter Mode	0	0	0	0	0	PFDAC	ADCPF	PFSDO
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Digital EQ Select	EQCT2	EQCT1	EQCT0	EQC5	EQC4	EQC3	EQC2	0
32H	Digital EQ Setting	EQCG7	EQCG6	EQCG5	EQCG4	EQCG3	EQCG2	EQCG1	EQCG0
33H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
34H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
35H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
36H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
37H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
38H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
39H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
3AH	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3BH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3CH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3DH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3EH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3FH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
40H	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
41H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
42H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
43H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
44H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
45H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
46H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
47H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
48H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
49H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
4AH	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4BH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4CH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4DH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4EH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4FH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
50H	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 46. PDN pin = "L" resets the registers to their default values.

Note 47. The bits defined as 0 must contain a "0" value.

Note 48. Address 0EH and 15H are a read only register. Writing access to 0EH and 15H are ignored and does not effect the operation.

■ Register Definitions

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMADL: ADC Lch Power Management

0: Power-down (default)

1: Power-up

When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle (1059/fs=21.3ms @48kHz, ADRST1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMADR: ADC Rch Power Management

0: Power down (default)

1: Power up

When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle (1059/fs=21.3ms @48kHz, ADRST1-0 bits = “00”) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management

0: Power-down (default)

1: Power-up

PMLO: Stereo Line Output Power Management

0: Power-down (default)

1: Power-up

PMSPK: Speaker-Amp Power Management

0: Power-down (default)

1: Power-up

PMBP: BEEP Input Power Management

0: Power-down (default)

1: Power-up

PMVCM: VCOM and Regulator (2.3V) Power Management

0: Power down (default)

1: Power up

PMPFIL: Programmable Filter Block Power Management

0: Power down (default)

1: Power up

The AK4957 can be powered-down by writing “0” to the address “00H” and PMPLL, PMMICL/R, PMMP, PMDML/R, DMPE, PMV and MCKO bits. In this case, register values are maintained.

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
01H	Power Management 2	PMMICR	PMMICL	0	PMMP	M/S	0	MCKO	PMPLL
	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMPLL: PLL Power Management

0: EXT Mode and Power down (default)

1: PLL Mode and Power up

MCKO: Master Clock Output Enable

0: Disable: MCKO pin = "L" (default)

1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select

0: Slave Mode (default)

1: Master Mode

PMMP: Microphone Power Management

0: Power down (default)

1: Power up

PMMICL: Microphone Amplifier Lch Power Management

0: Power down (default)

1: Power up

PMMICR: Microphone Amplifier Rch Power Management

0: Power down (default)

1: Power up

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
02H	Signal Select 1	SPPSN	0	0	MICL	0	MGAIN2	MGAIN1	MGAIN0
	R/W	R/W	R	R	R/W	R	R/W	R/W	R/W
	Default	0	0	0	0	0	1	0	0

MGAIN2-0: MIC-Amp Gain Control ([Table 21](#))

Default: "100"(+18dB)

MICL: MIC Power Output Voltage Select

0: typ 2.4 V (default)

1: typ 2.0V

SPPSN: Speaker-Amp Power-Save Mode

0: Power Save Mode (default)

1: Normal Operation

When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs AVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	BEEPS	DACS	0	0	INR	INL
	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
	Default	0	0	0	0	0	0	0	0

INL: ADC Lch Input Source Select

- 0: LIN1 pin (default)
- 1: LIN2 pin

INR: ADC Rch Input Source Select

- 0: RIN1 pin (default)
- 1: RIN2 pin

DACS: Signal Switch Control from DAC to Speaker-Amp

- 0: OFF (default)
- 1: ON

When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Signal Switch Control from the MIN pin to Speaker-Amp

- 0: OFF (default)
- 1: ON

SPKG1-0: Speaker-Amp Output Gain Select ([Table 57](#))

Default: "00" (+6.1dB @ ALC2 bit = "0", +8.1dB @ ALC2 bit = "1")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	MONO1	MONO0	LOPS	DACL	BEEPL	0	LVCM1	LVCM0
	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
	Default	0	0	0	0	0	0	0	1

LVCM1-0: Stereo Line Output Gain and Common Voltage Setting ([Table 55](#))

Default: "01" (+2dB)

BEEPL: Signal Switch Control from the MIN pin to Lineout

- 0: OFF (default)
- 1: ON

DACL: DAC Output Signal to Stereo Line Amp Control

- 0: OFF (default)
- 1: ON

When PMLO bit = "1", this bit setting is enabled. LOUT and ROUT pins output VSS1 when PMLO bit = "0".

LOPS: Stereo Line Output Power Save

- 0: Normal Operation (default)
- 1: Power Save Mode

MONO1-0: LOUT/ROUT Output Signal Mode Select ([Table 56](#))

Default: "00" (LOUT pin = Lch, ROUT pin = Rch)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
	Default	1	1	0	0	0	0	1	0

DEM1-0: Audio Interface Format (Table 17)

Default: "10" (MSB justified)

BCKO: Master Mode BICK Output Frequency Setting (Table 15)

Default: "0"(32fs)

PLL3-0: PLL Reference Clock Select (Table 4)

Default: "1100" (MCKI = 13.5MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency (Table 5, Table 6)

PS1-0: MCKO Frequency Setting (Table 9)

Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	READ	THDET	SMUTE	0	OVOLC	IVOLC	0	0
	R/W	R/W	R	R/W	R	R/W	R/W	R	R
	Default	0	0	0	0	1	1	0	0

IVOLC: IVOL Control

0: Independent

1: Dependent (default)

When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits.

OVOLC: Output Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume levels, while register values of OVL7-0 bits are not written to OVR7-0 bits.

SMUTE: Soft Mute Control

0: Normal Operation (default)

1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection

0: Thermal Shutdown Off (default)

1: Thermal Shutdown ON

READ: Read Function Enable

0: Disable (default)

1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
	R/W	R	R	R/W	R/W	R/W	R	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select

0: Analog Microphone (default)

1: Digital Microphone

DCLKP: Data Latching Edge Select

0: Lch data is latched on the DMCLK rising edge (“↑”). (default)

1: Lch data is latched on the DMCLK falling edge (“↓”).

DCLKE: DMCLK pin Output Clock Control

0: “L” Output (default)

1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 20)

Default: “00”

ADC digital block is powered-down by PMDML = PMDMR bits = “0” when selecting a digital microphone input (DMIC bit = “1”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	0	0	0	0	0	DVTM
	R/W	R/W	R/W	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

DVTM: Digital Volume Soft Transition Time Setting (Table 48)

Default: “0” (1024/fs)

This transition time is for when DVOL7-0 bits are changed from 00H to FFH.

ADRST1-0: ADC Initial Cycle Setting (Table 16)

Default: “00” (1059/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	FRN	ZTM1	ZTM0	WTM2	WTM1	WTM0	RFST1	RFST0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	1

RFST1-0: ALC First Recovery Speed (Table 39)

Default: “01” (Quad Speed)

WTM2-0: ALC Recovery Waiting Period (Table 35)

Default: “000” (128/fs).

A period of recovery operation when any limiter operation does not occur during ALC operation

ZTM1-0: ALC Zero Cross Timeout Setting (Table 34)

Default: “00” (128/fs).

In case of the μ P WRITE operation or ALC recovery operation, the volume is changed at zero crossing or timeout.

FRN: ALC First Recovery Function Enable

0: Enable (default)

1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	LMTH1	LMTH0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level ([Table 32](#))

Default: "00"

LMAT1-0: ALC Limiter ATT Step ([Table 33](#))

Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation

0: Enable (default)

1: Disable

ALC1: ALC Enable for Recording

0: Recording ALC Disable (default)

1: Recording ALC Enable

ALC2: ALC Enable for Playback

0: Playback ALC Disable (default)

1: Playback ALC Enable

LFST: ALC Limiter operation when the output level exceed FS(Full-scale) level.

0: The volume is changed at zero crossing or zero crossing time out. (default)

1: When output of ALC is larger than FS, OVOL value is changed immediately (1/fs).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	1	1	0	0	0	0	1

IREF7-0: Reference Value of ALC Recovery Operation (Recording). 0.375dB step, 242 Level ([Table 37](#))

Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Mode Control 3	RGAIN1	RGAIN0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	1	0	1	0	0	0

OREF7-0: Reference Value of ALC Recovery Operation (Playback). 0.375dB step, 242 Level ([Table 38](#))

Default: "28H" (+6.0dB)

RGAIN1-0: ALC Recovery GAIN Step ([Table 36](#))

Default: "00" (0.375dB step)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	R/W	R	R	R	R	R	R	R	R
	Default	1	0	0	1	0	0	0	1

VOL7-0: Current ALC volume value, 0.375dB step, 242 Level, Read operation only (Table 40)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume, 0.375dB step, 242 Level (Table 45)
Default: "E1H" (+30dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume (Table 46)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	0

DVOL7-0: Output Digital Volume 2 (Table 47)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	ALC Input Level	0	INVOL6	INVOL5	INVOL4	INVOL3	INVOL2	INVOL1	INVOL0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

INVOL6-0: ALC Input Level Read Function (Table 31)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	ALC REF2 Setting	0	RF2SL2	RF2SL1	RF2SL0	0	RF2P2	RF2P1	RF2P0
	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	0

RF2P2-0: ALC Input Level Inflection Point (Table 43)

Default: "010" (-39dB)

RF2SL2-0: ALC REF2 Slope Setting (Table 44)

Default: "000" (Slope = 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	Lch MIC Gain Setting	0	0	0	MGL4	MGL3	MGL2	MGL1	MGL0
	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

MGL4-0 bits: Lch Mic Sensitivity Correction (Table 26)

Default: "00H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Rch MIC Gain Setting	0	0	0	MGR4	MGR3	MGR2	MGR1	MGR0
	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

MGR4-0 bits: Rch Mic Sensitivity Correction (Table 26)

Default: "00H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	BEEP Control	0	BPVCM	0	BPM	BPLVL3	BPLVL2	BPLVL1	BPLVL0
	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

BPLVL3-0: BEEP Output Level Setting (Table 51)

Default: "0000" (0dB)

BPM: BEEP Mode Setting (Table 49)

0: Internal Resistance Mode (default)

1: External Resistance Mode

BPVCM: Common Voltage Setting of MIN Input Amplifier (Table 50)

0: 1.15V (default)

1: 1.65V

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Video Control	0	0	0	0	VG1	VG0	0	PMV
	R/W	R	R	R	R	R/W	R/W	R	R/W
	Default	0	0	0	0	0	0	0	0

PMV: Composite Video Block Power Management

0: Power down (default)

1: Power up

VG1-0: Video Amplifier Gain Select ([Table 60](#))

Default: "00" (6dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	HPF Filter Control	0	HPF3C2	HPF3C1	HPF3C0	0	HPFC1	HPFC0	HPFAD
	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	1

HPFAD: HPF1 Control of ADC

0: OFF

1: ON (default)

When HPFAD bit is "1", the settings of HPFC1-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).

When PMADL bit = "1" or PMADR bit = "1", set HPFAD bit to "1".

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) ([Table 25](#))

Default: "00" (3.7Hz @ fs = 48kHz)

HPF3C2-0: HPF3 (Before ALC Input Volume Read) Cutoff Frequency Setting ([Table 30](#))

Default: "000" (500Hz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Digital Filter Select 1	HPF3	0	LPF	HPF	EQ0	GN1	GN0	FIL3
	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

FIL3: Stereo Emphasis Filter Control

0: OFF (default)

1: ON

When FIL3 bit = "1", settings of F3A13-0 and F3B13-0 bits are enabled.

GN1-0: Gain Block Gain Setting ([Table 27](#))

Default: "00" (0dB)

EQ0: Gain Correction Filter (EQ0) Control

0: OFF (default)

1: ON

When EQ0 bit = "1", settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit = "0", the audio data passes this block by 0dB gain.

HPF: HPF2 Coefficient Setting Enable

0: OFF (default)

1: ON

When HPF bit is "1", settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is "0", the audio data passes this block by 0dB gain.

LPF: LPF Coefficient Setting Enable

0: OFF (default)

1: ON

When LPF bit is "1", settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is "0", the audio data passes this block by 0dB gain.

HPF3: HPF3 (Before ALC Input Level Read) Control

0: OFF (default)

1: ON

HPF3C2-0 bits setting is valid when HPF3 bit = "1". The data passes the HPF3 block by 0dB gain when HPF3 bit = "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Control	0	0	0	0	0	PFDAC	ADCPF	PFSDO
	R/W	R	R	R	R	R	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select

0: ADC (+ 1st HPF) Output

1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select

0: SDTI

1: ADC Output (default)

PFDAC: DAC Input Signal Select

0: SDTI (default)

1: Programmable Filter / ALC Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)

Default: F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F

$f_c = 150\text{Hz}@f_s=48\text{kHz}$

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)

Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: Stereo Emphasis FIL3 Coefficient (14bit x 2)
 Default: "0000H"

F3AS: Stereo Emphasis FIL3 Select
 0: HPF (default)
 1: LPF

E0A15-0, E0B13-0, E0C15-C0: Gain Compensation Filter Coefficient (16bit x 2 + 14bit x 1)
 Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ1 bit = "1", settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit = "0", the audio data passes this block by 0dB gain.

EQ2: Equalizer 2 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ2 bit = "1", settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit = "0", the audio data passes this block by 0dB gain.

EQ3: Equalizer 3 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ3 bit = "1", settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit = "0", the audio data passes this block by 0dB gain.

EQ4: Equalizer 4 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ4 bit = "1", settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit = "0", the audio data passes this block by 0dB gain.

EQ5: Equalizer 5 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ5 bit = "1", settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit = "0", the audio data passes this block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
31H	EQ Common Gain Setting1	EQCT2	EQCT1	EQCT0	0	EQC5	EQC4	EQC3	EQC2
	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

EQC2: Equalizer 2 Common Gain Selector

0: Disable (default)

1: Enable

When EQC2 bit = "1", the common gain setting (EQCG) is reflected.

EQC3: Equalizer 3 Common Gain Selector

0: Disable (default)

1: Enable

When EQC3 bit = "1", the common gain setting (EQCG) is reflected.

EQC4: Equalizer 4 Common Gain Selector

0: Disable (default)

1: Enable

When EQC4 bit = "1", the common gain setting (EQCG) is reflected.

EQC5: Equalizer 5 Common Gain Selector

0: Disable (default)

1: Enable

When EQC5 bit = "1", the common gain setting (EQCG) is reflected.

EQCT2-0: EQ Common Gain Transition Time ([Table 29](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	EQ Common Gain Setting2	EQCG7	EQCG6	EQCG5	EQCG4	EQCG3	EQCG2	EQCG1	EQCG0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

EQCG7-0: EQ Common Gain Setting ([Table 28](#))

Default: 00H (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
33H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
34H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
35H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
36H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
37H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
38H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
39H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
3AH	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3BH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3CH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3DH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3EH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3FH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
40H	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
41H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
42H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
43H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
44H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
45H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
46H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
47H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
48H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
49H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
4AH	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4BH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4CH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4DH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4EH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4FH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
50H	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
Default		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: "0000H"

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: "0000H"

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: "0000H"

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: "0000H"

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: "0000H"

SYSTEM DESIGN

Figure 65 shows the system connection diagram. An evaluation board (AKD4957) is available for fast evaluation as well as suggestions for peripheral circuitry.

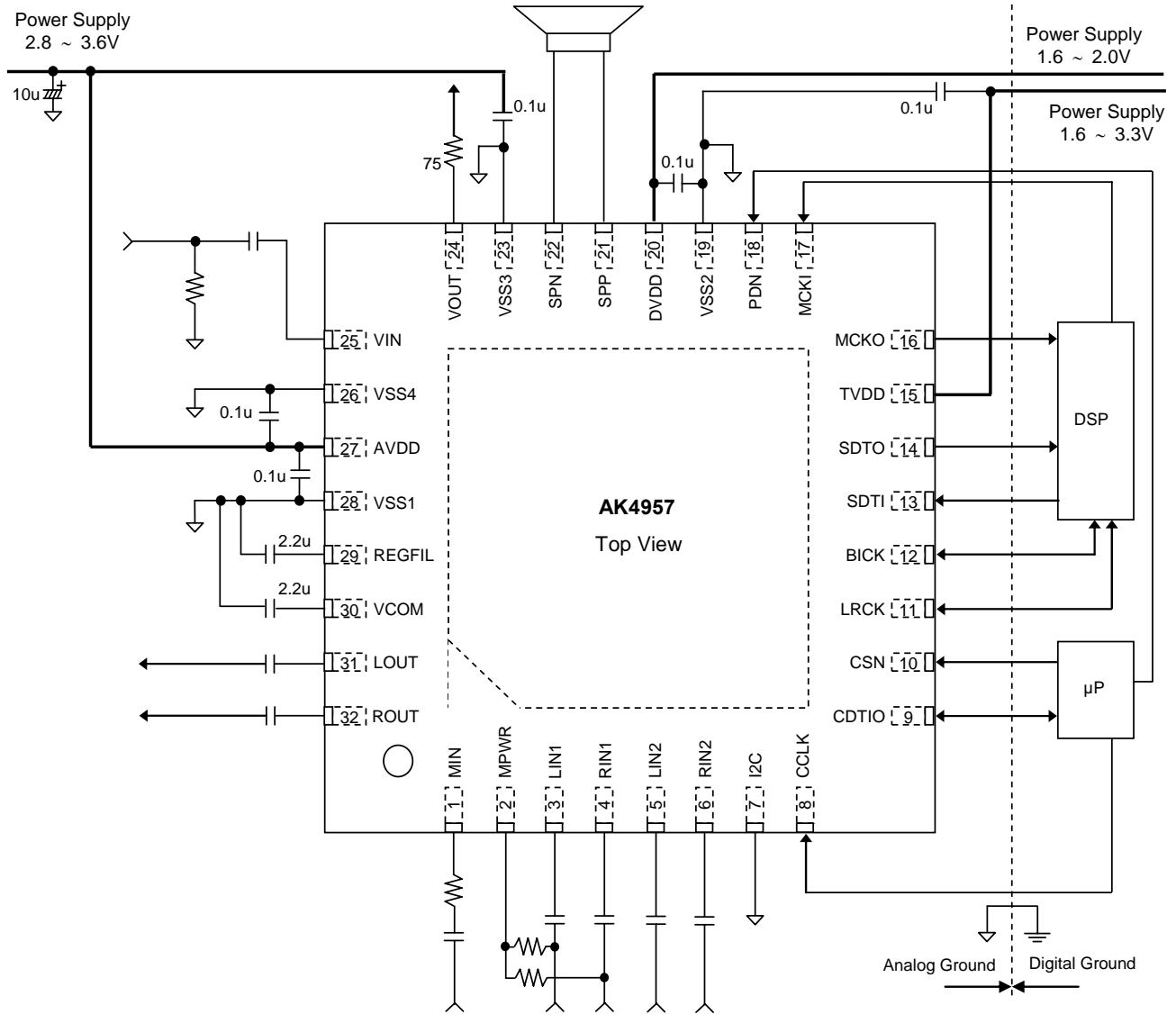


Figure 65. System Connection Diagram
 (3-wire Serial Mode: I2C pin = "L", MIN pin External Resistance Mode: BPM bit = "0")

Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4957 must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4957 is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up or pull-down resistor around 100kΩ must be connected to LRCK and BICK pins of the AK4957.

1. Grounding and Power Supply Decoupling

The AK4957 requires careful attention to power supply and grounding arrangements. If AVDD, DVDD and TVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2, VSS3 and VSS4 of the AK4957 must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4957 as possible, with the small value ceramic capacitor being the nearest.

2. Internal Regulated Voltage Power Supply

REGFIL is a power supply of the analog circuit (typ. 2.3V). A 2.2 μ F \pm 50% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4957. No load current may be drawn from the REGFIL pin. All digital signals, especially clocks, should be kept away from the REGFIL pin in order to avoid unwanted coupling into the AK4957.

3. Reference Voltage

VCOM is a signal ground of this chip. A 2.2 μ F \pm 50% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4957. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4957.

4. Analog Inputs

The Mic and Line inputs supports single-ended. The input signal range scales with nominally at typ. 2.07V_{pp} (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.15V). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $f_c = 1/(2\pi RC)$.

5. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit data). The common voltage of stereo lineout is typically 1.0V_{rms} (AVDD=3.3V) centered on 1.5V (typ) (@LVCM0 bit = "1"). The speaker outputs are centered on AVDD/2 (typ).

CONTROL SEQUENCE

■ Clock Set Up

When ADC, DAC or Programmable Filter is powered-up, the clocks must be supplied.

1. PLL Master Mode

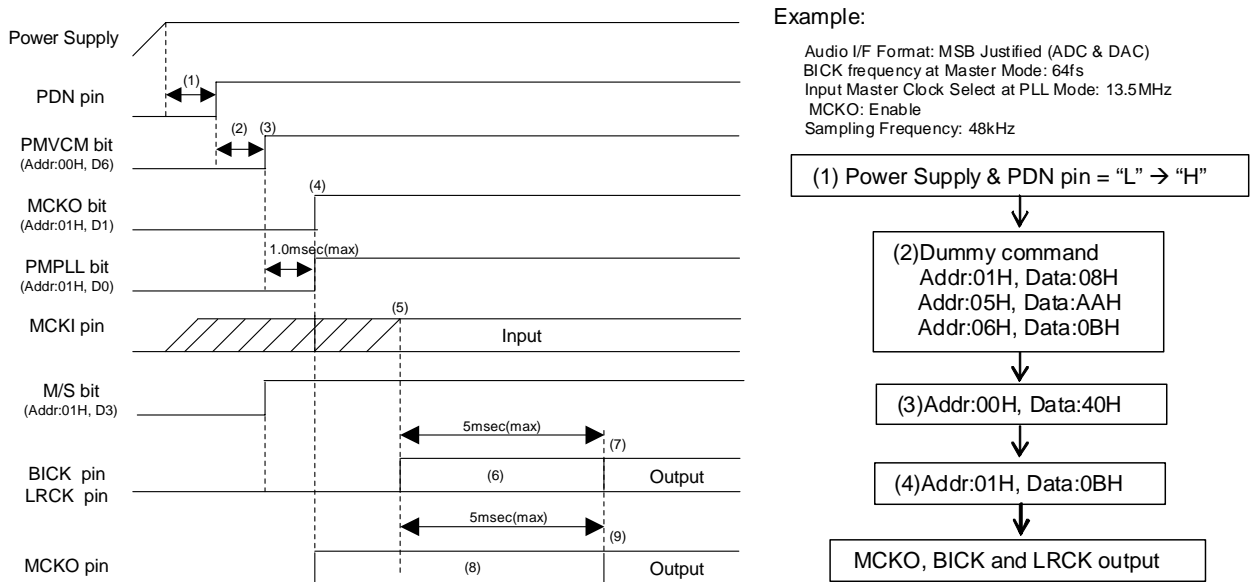


Figure 66. Clock Set Up Sequence (1)

<Example>

- (1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4957.
- (2) After Dummy Command input, M/S, DIF1-0, BCKO, PLL3-0, FS3-0 and PS1-0 bits must be set during this period.
- (3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.
- (4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"
- (5) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 5ms (max)
- (6) BICK pin outputs "H" and LRCK pin outputs "L" during this period.
- (7) The AK4957 starts to output the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.
- (8) An invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".
- (9) A normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (BICK pin)

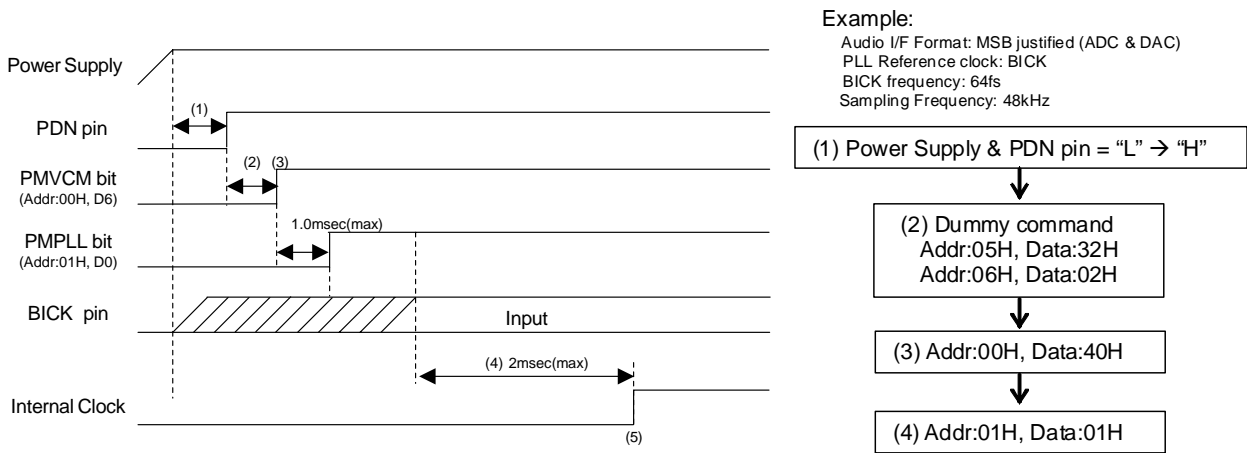


Figure 67. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up: PDN pin "L" → "H"
 "L" time of 200ns or more is needed to reset the AK4957.
- (2) After Dummy Command input, DIF1-0, PLL3-0, and FS3-0 bits must be set during this period.
- (3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
 VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock.
- (5) Normal operation starts after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

Example:

Audio I/F Format: MSB justified (ADC & DAC)
 Input Master Clock Select at PLL Mode: 13.5MHz
 MCKO: Enable
 Sampling Frequency: 48kHz

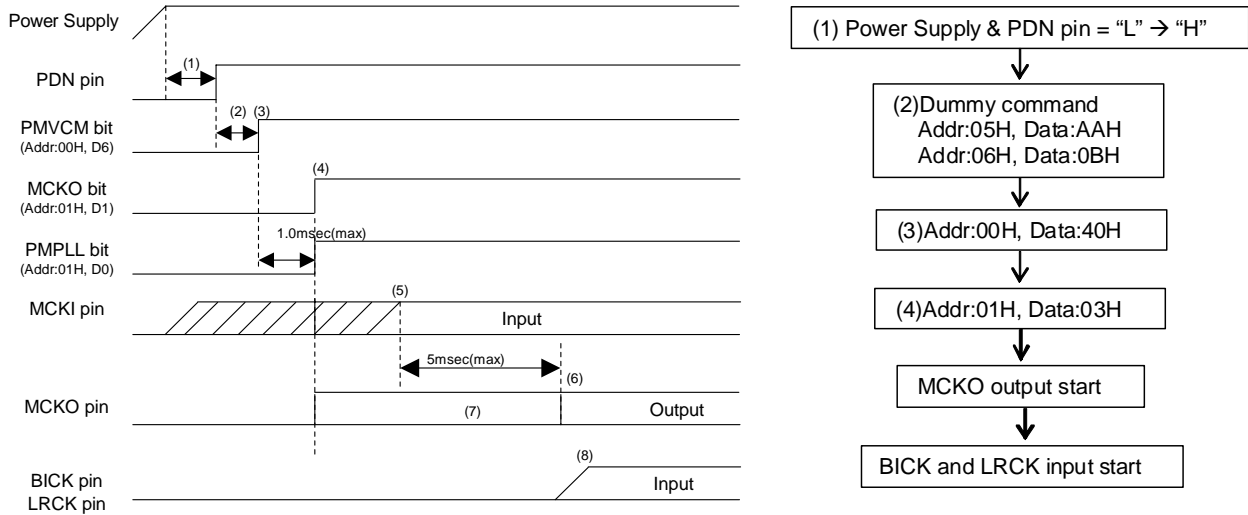


Figure 68. Clock Set Up Sequence (3)

<Example>

- (1) After Power Up: PDN pin "L" → "H"
 "L" time of 200ns or more is needed to reset the AK4957.
- (2) After Dummy Command input, DIF1-0, PLL3-0, FS3-0 and PS1-0 bits must be set during this period.
- (3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
 VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.
- (4) Enable MCKO output: MCKO bit = "1"
- (5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
 PLL lock time is 5ms (max).
- (6) A normal clock is output from MCKO after PLL is locked.
- (7) An invalid frequency is output from MCKO during this period.
- (8) BICK and LRCK clocks must be synchronized with MCKO clock.

4. EXT Slave Mode

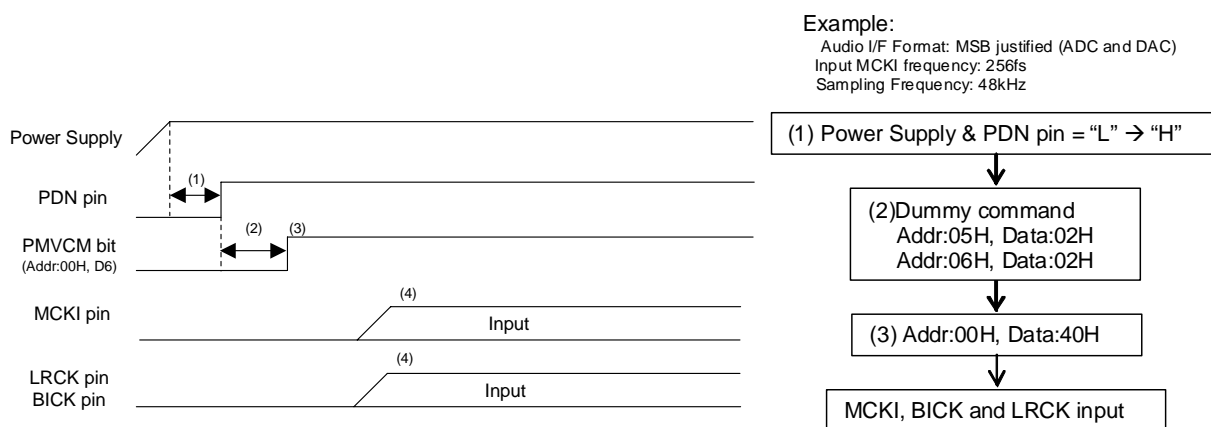


Figure 69. Clock Set Up Sequence (4)

<Example>

- (1) After Power Up: PDN pin "L" → "H"
 "L" time of 200ns or more is needed to reset the AK4957.
- (2) After Dummy Command input, DIF1-0 and FS3-0 bits must be set during this period.
- (3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
 VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.
- (4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

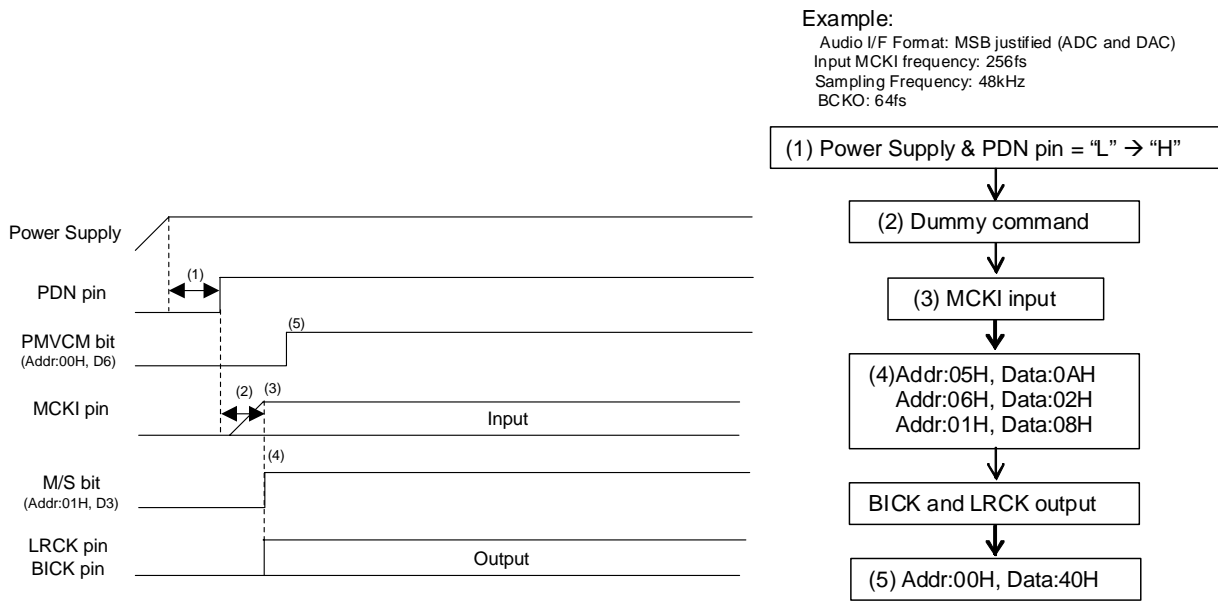


Figure 70. Clock Set Up Sequence (5)

<Example>

- (1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4957.
- (2) Dummy Command must be input during this period.
- (3) MCKI is supplied.
- (4) After DIF1-0, BCKO and FS3-0 bits are set. M/S bit should be set to "1". Then LRCK and BICK are output.
- (5) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 2.0ms (max) when both capacitances of an external capacitor for the VCOM and REGFIL pins are 2.2μF ±50% each.

■ MIC Input Recording (Stereo)

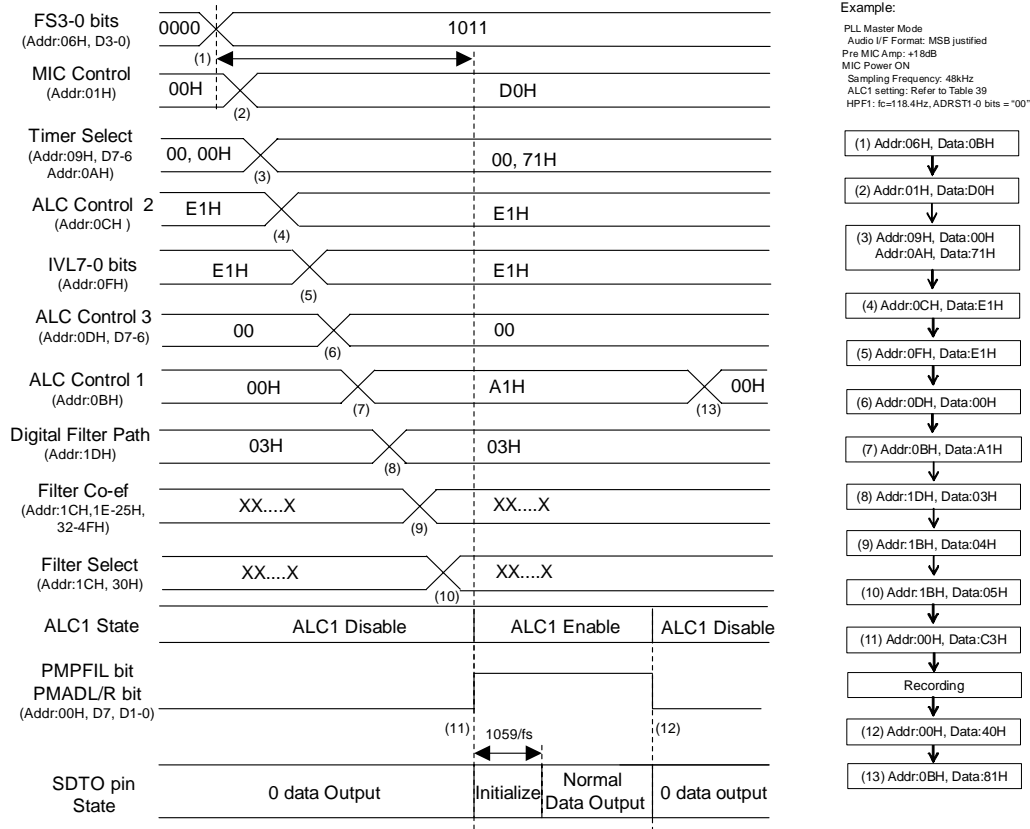


Figure 71. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs= 48kHz. For changing the parameter of ALC, please refer to Table 39. At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). When the AK4957 is in PLL mode, MIC, ADC and Programmable Filter of (11) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up MIC Amp and MIC Power. (Addr = 01H)
- (3) Set up ALC1 Timer, ADRST1-0 bits (Addr = 09H, 0AH)
- (4) Set up IREF value at ALC1 (Addr = 0CH)
- (5) Set up IVOL value at ALC1 operation start (Addr = 0FH)
- (6) Set up RGAIN1-0 bits (Addr = 0DH)
- (7) Set up LMTH1-0, LMAT1-0, ZELMN, ALC1 and LFST bits (Addr = 0BH)
- (8) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = “1” (Addr = 1DH)
- (9) Set up Coefficient Programmable Filter (Addr: 1CH, 1EH ~ 25H, 32H ~ 4FH)
- (10) Programmable Filter ON/OFF Setting
- (11) Power Up ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = “0” → “1”
 The initialization cycle time of ADC is 1059/fs=22ms @ fs=48kHz, ADRST1-0 bit = “00”. ADC outputs “0” data during the initialization cycle. After the ALC1 bit is set to “1”, the ALC1 operation starts from IVOL value of (5).
- (12) Power Down ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = “1” → “0”
- (13) ALC Disable: ALC1 bit = “1” → “0”

■ Digital MIC Input Recording (Stereo)

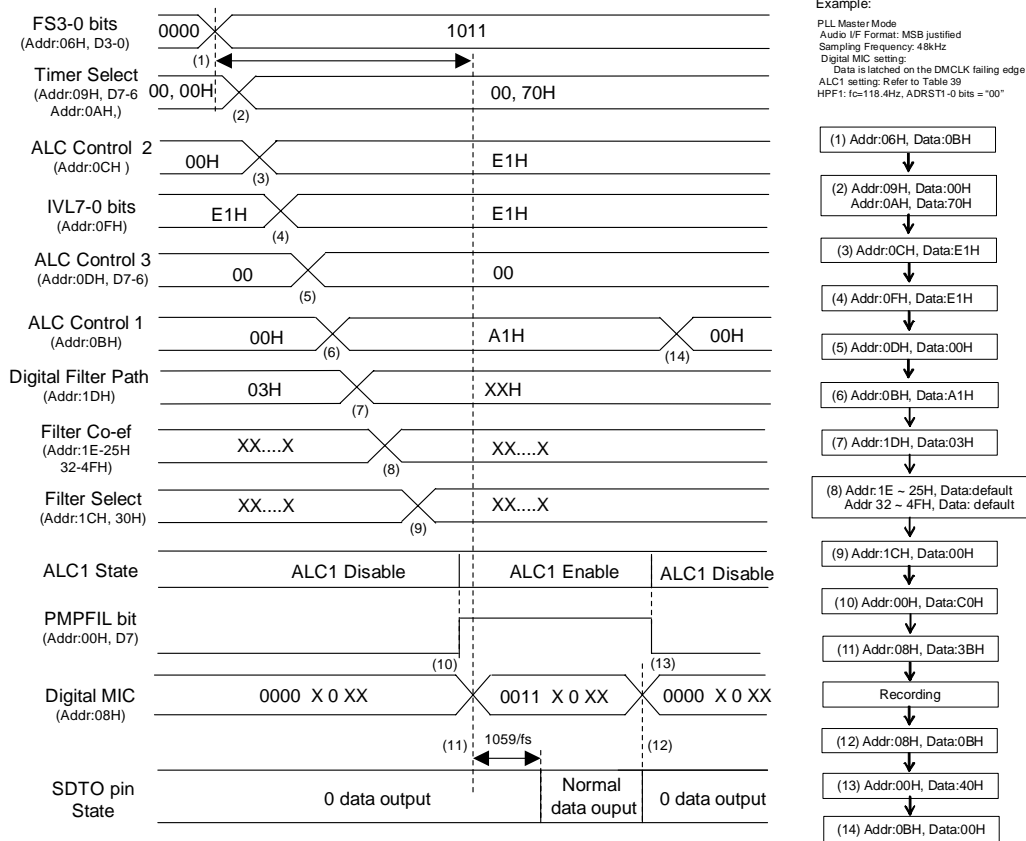


Figure 72. Digital MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=48kHz. For changing the parameter of ALC, please refer to Table 39. At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). When the AK4957 is PLL mode, Digital MIC of (11) and Programmable Filter of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up ALC1 Timer and ADRST1-0 bits (Addr = 09H, 0AH)
- (3) Set up IREF value for ALC1 (Addr = 0CH)
- (4) Set up IVOL value at ALC1 operation start (Addr = 0FH)
- (5) Set up RGAIN1-0 bits (Addr = 0DH)
- (6) Set up LMTH1-0, LMAT1-0, ZELMN, ALC1 and LFST bits (Addr = 0BH)
- (7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = “1” (Addr = 1DH)
- (8) Set up Coefficient of Programmable Filter (Addr: 1EH ~ 25H, 32H ~ 4FH)
- (9) Set up Programmable Filter ON/OFF
- (10) Power Up Programmable Filter: PMPFIL bit = “0” → “1”
- (11) Set Up & Power Up Digital MIC: PMDMR = PMDML bits = “0” → “1”
 The initialization cycle time of ADC is 1059/fs=22ms@ fs=48kHz, ADRST1-0 bit = “00”. ADC outputs “0” data during initialization cycle. After the ALC1 bit is set to “1”, the ALC1 operation starts from IVOL value of (4).
- (12) Power Down Digital MIC: PMDMR = PMDML bits = “1” → “0”
- (13) Power Down Programmable Filter: PMPFIL bit = “1” → “0”
- (14) ALC1 Disable: ALC1 bit = “1” → “0”

■ Speaker-Amp Output

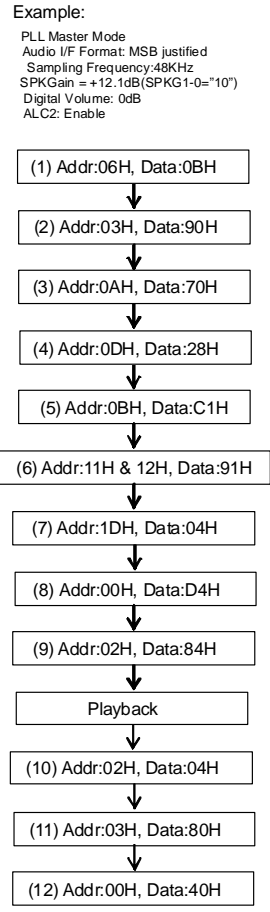
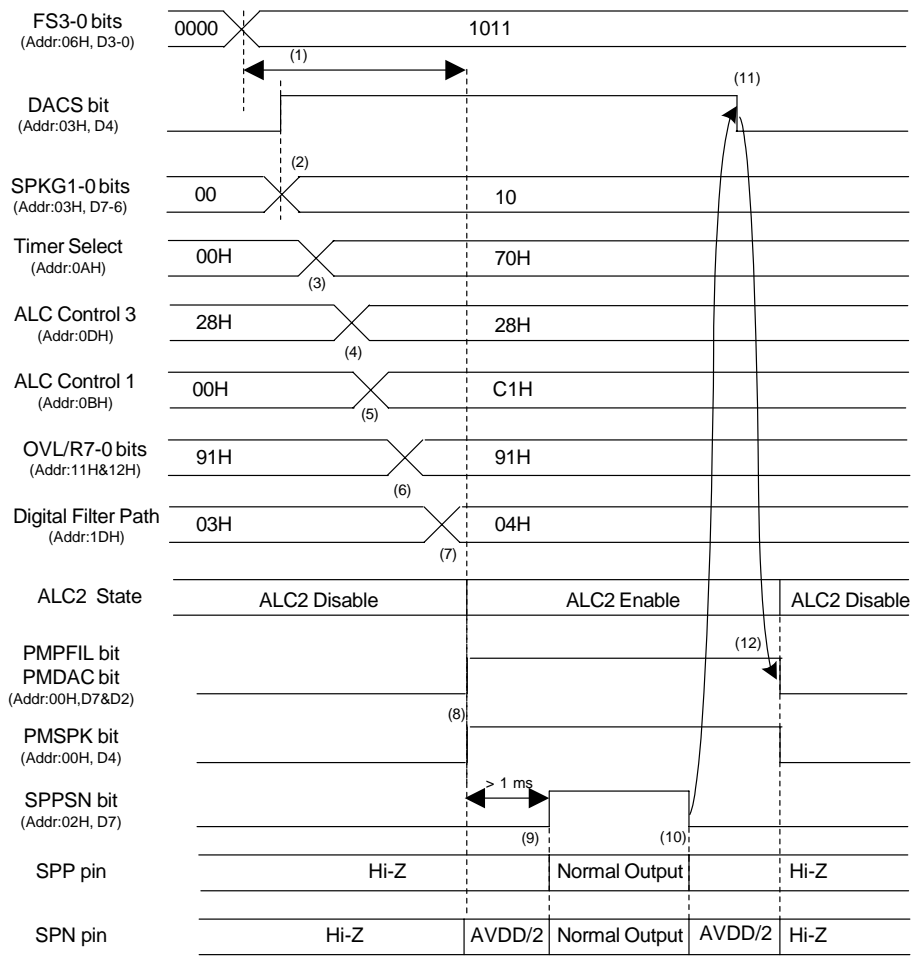


Figure 73. Speaker-Amp Output Sequence

<Example>

At first, clocks must be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). When the AK4957 is in PLL mode, DAC and Speaker-Amp of (9) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up the path of DAC → SPK-Amp: DACS bit = “0” → “1”,
 SPK-Amp gain setting: SPKG1-0 bits = “00” → “01”
- (3) Set up Timer Select for ALC2 (Addr = 0AH)
- (4) Set up OREF value of ALC2 and RGAIN1-0 bits (Addr = 0DH)
- (5) Set up LMTH1-0, LMAT1-0, ZELMIN, ALC2, LFST bits (Addr = 0BH)
- (6) Set up the output digital volume. (Addr = 11H, 12H)
 Set up OVOL value at ALC2 operation start. When OVOLC bit is “1” (default), OVL7-0 bits set the volume of both channels. When ALC2 bit is “0”, it could be digital volume control.
- (7) Set up Programmable Filter Path (PFDAC, ADCPF, PFSDO bits) (Addr = 1DH)
- (8) Power up DAC, Programmable Filter and Speaker Amp: PMDAC = PMPFIL = PMSPK bits = “0” → “1”
- (9) Exit the power-save mode of Speaker-Amp: SPPSN bit = “0” → “1”
- (10) Enter Speaker-Amp Power Save Mode: SPPSN bit = “1” → “0”
- (11) Disable the path of DAC → SPK-Amp: DACS bit = “1” → “0”
- (12) Power down DAC, Programmable Filter and speaker: PMDAC = PMPFIL = PMSPK bits = “1” → “0”

■ Beep Signal Output from Speaker-Amp

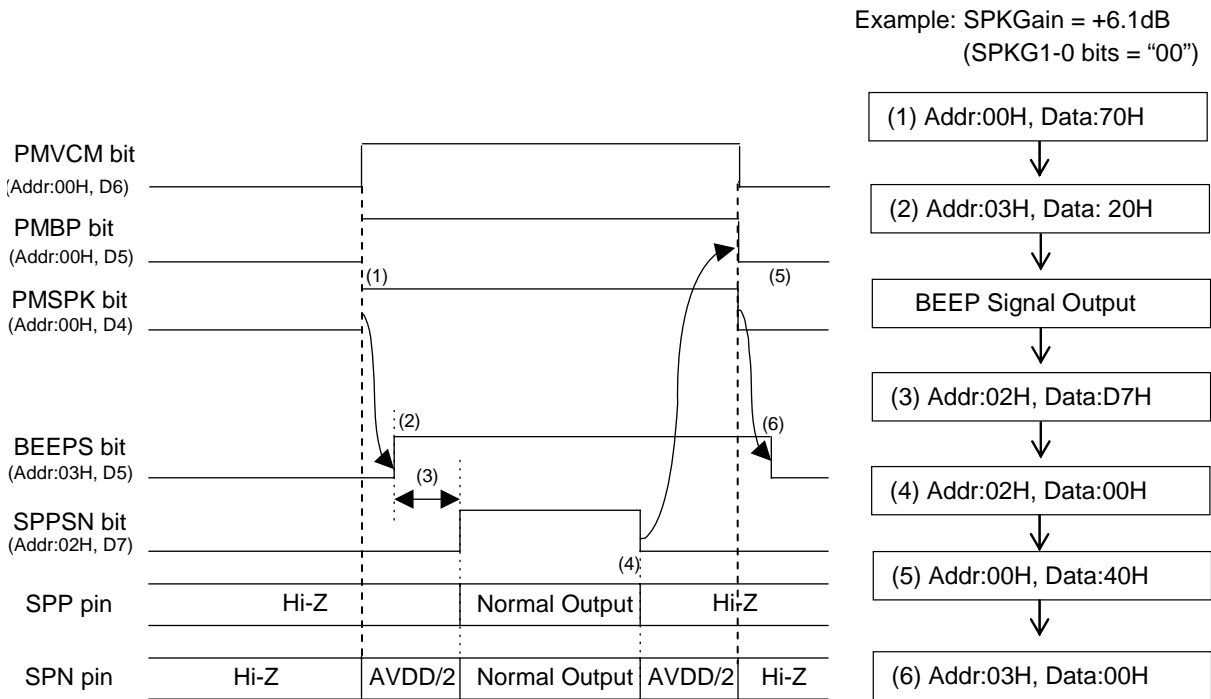


Figure 74. "MIN-Amp → Speaker-Amp" Output Sequence

<Example>

Clock input is not necessary when the AK4957 is operating only on the path of "MIN-Amp" → "SPK-Amp".

- (1) Power up VCOM, MIN-Amp and Speaker: PMVCM = PMBP = PMSPK bits = "0" → "1"
- (2) Set up the path of MIN → SPK-Amp: BEEPS bit = "0" → "1"
- (3) Exit the power save mode of Speaker-Amp: SPPSN bit = "0" → "1"
 Period (3) should be set according to the time constant of a capacitor and a resistor that are connected to the MIN pin. Pop noise may occur if the SPK-Amp output is enabled before the MIN-Amp input is stabilized.
 e.g. R=66kΩ, C=0.1μF: Recommended Wait Time 5τ = 33ms or more
- (4) Enter Speaker-Amp Power-save mode: SPPSN bit = "1" → "0"
- (5) Power Down MIN-Amp and Speaker: PMBP = PMSPK bits = "1" → "0"
- (6) Disable the path of MIN → SPK-Amp: BEEPS bit = "1" → "0"

■ Stereo Line Output

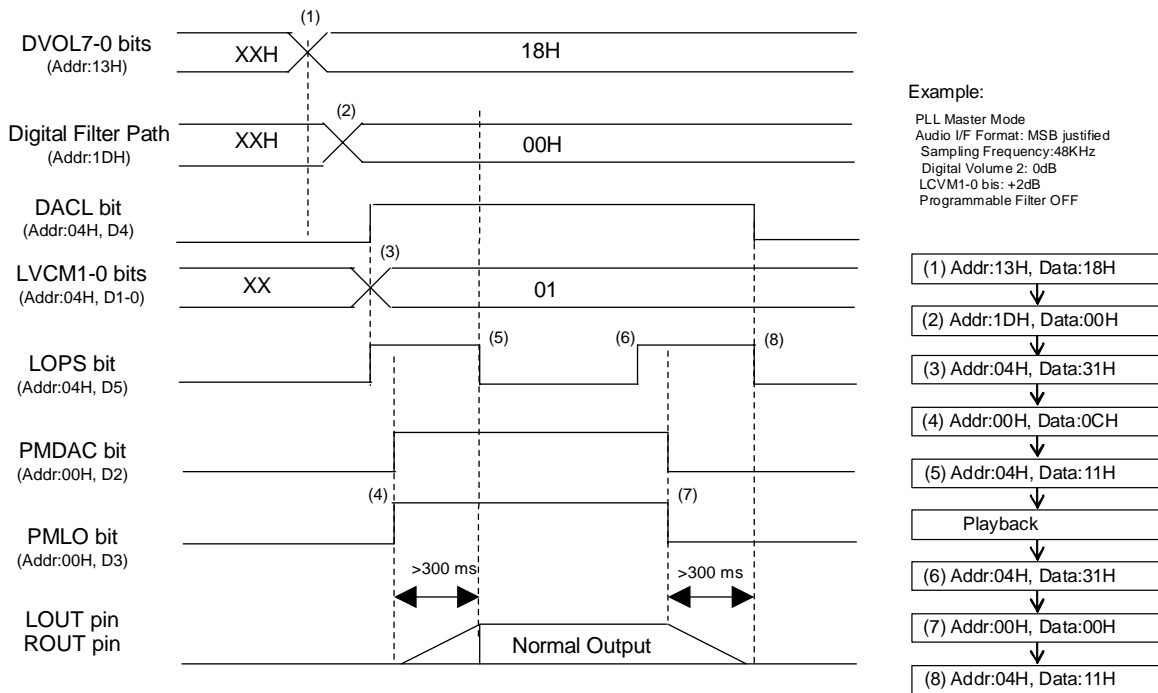


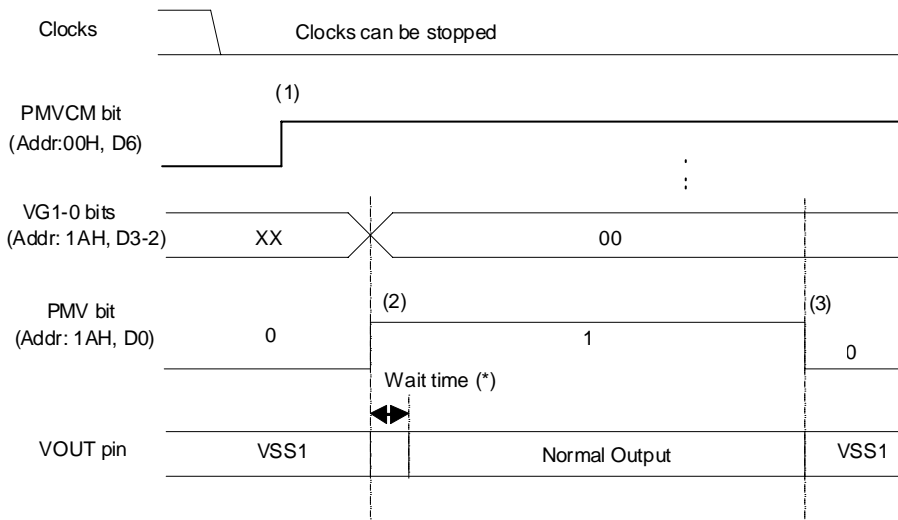
Figure 75. Stereo Lineout Sequence

<Example>

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up output digital volume 2. (Addr = 13H)
- (2) Set up Programmable Filter Path (PFDAC, ADCPF, PFSDO bits). (Addr = 1DH)
- (3) Set up the path of “DAC → Stereo Line-Amp”: DACL bit = “0” → “1” (Addr = 04H)
 Stereo Line Output Amplifier Setting: LVCM1-0 bits = “xx” → “01”
 Set the stereo line amplifier to power save mode: LOPS bit = “0” → “1”
- (4) Power up Stereo Line-Amp: PMDAC = PMLO bits = “0” → “1” (Addr = 00H)
 LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to “1”. Rise time to 99% VCOM voltage is 300ms (max.) when C = 1μF and R_L=10kΩ.
- (5) Exit power-save mode of Stereo Line-Amp: LOPS bit = “1” → “0” (Addr = 04H)
 LOPS bit should be set to “0” after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to “0”.
- (6) Enter power save mode of Stereo Line-Amp: LOPS bit = “0” → “1” (Addr = 04H)
- (7) Power down DAC and Stereo Line-Amp: PMDAC = PMLO bits = “1” → “0” (Addr = 00H)
 LOUT and ROUT pins fall down to 1% of the VCOM voltage. Fall time is 300ms (max.) at C = 1μF and R_L=10kΩ.
- (8) Disable the path of “DAC → Stereo Line-Amp”: DACL bit = “1” → “0” (Addr = 04H)
 Exit power-save mode of the Stereo Line-Amp: LOPS bit = “1” → “0”
 LOPS bit should be set to “0” after LOUT and ROUT pins fall down.

■ Video Input/Output



Example:

Audio Function :No use
Video Gain = +6dB

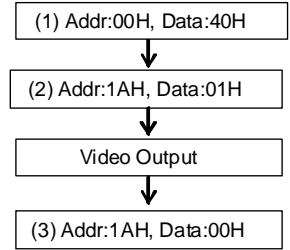


Figure 76. Video Output Sequence

<Example>

When only the video block is in operation, the clocks are not needed.

(1) Power up VCOM: PMVCM bit = “0” → “1”

(2) Set up Video Gain (VG1-0 bits)

Video Amp Power Up: PMV bit = “0” → “1”

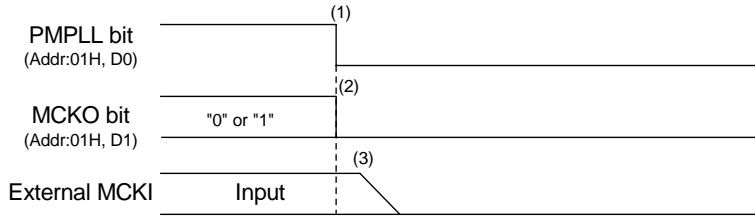
(*) Wait time is the time until the video clamp circuit output is stabled. It depends on the value of a DC-cut capacitor for the VIN pin. The wait time is 50ms (max.) when the DC-cut capacitor of the VIN pin input is 0.047μF. (It is a rising time without a DC offset)

(3) Video Amp Power Down: PMV bit = “0” → “1”

The VOUT pin output is stopped and becomes 0V.

■ Stop of Clock

1. PLL Master Mode



Example:

Audio I/F Format: MSB justified (ADC & DAC)
 BICK frequency at Master Mode: 64fs
 Input Master Clock Select at PLL Mode: 12.288MHz

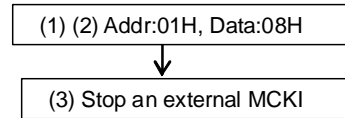
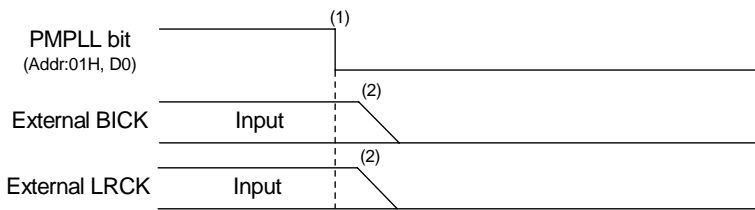


Figure 77. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop MCKO clock: MCKO bit = "1" → "0"
- (3) Stop an external master clock.

2. PLL Slave Mode (BICK pin)



Example

Audio I/F Format : MSB justified (ADC & DAC)
 PLL Reference clock: BICK
 BICK frequency: 64fs

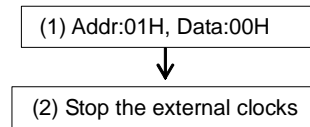


Figure 78. Clock Stopping Sequence (2)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop an external master clock.

3. PLL Slave Mode (MCKI pin)

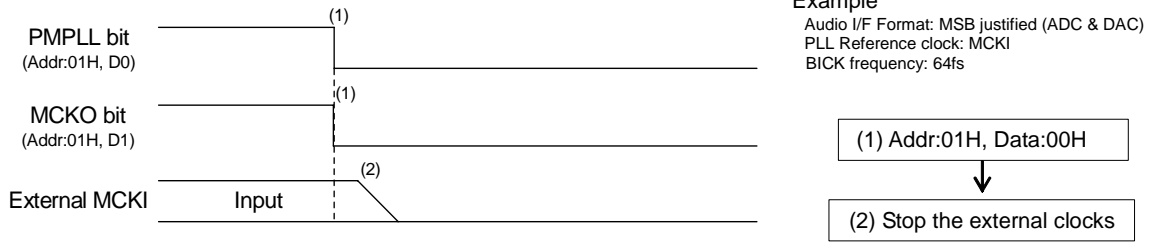


Figure 79. Clock Stopping Sequence (3)

<Example>

- (1) Power down PLL: PMPLL bit = “1” → “0”
 Stop MCKO output: MCKO bit = “1” → “0”
- (2) Stop the external master clock

4. EXT Slave Mode

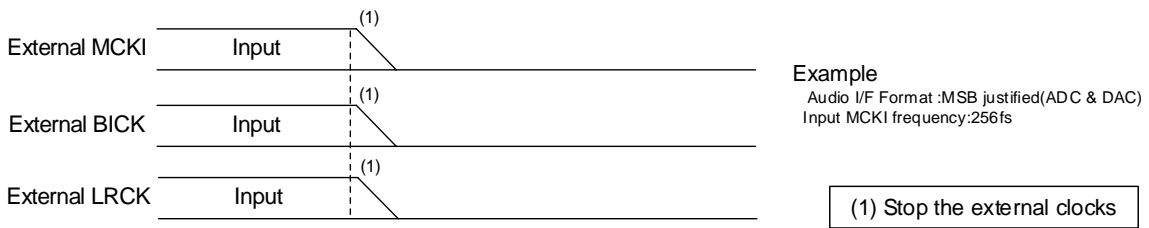


Figure 80. Clock Stopping Sequence (4)

<Example>

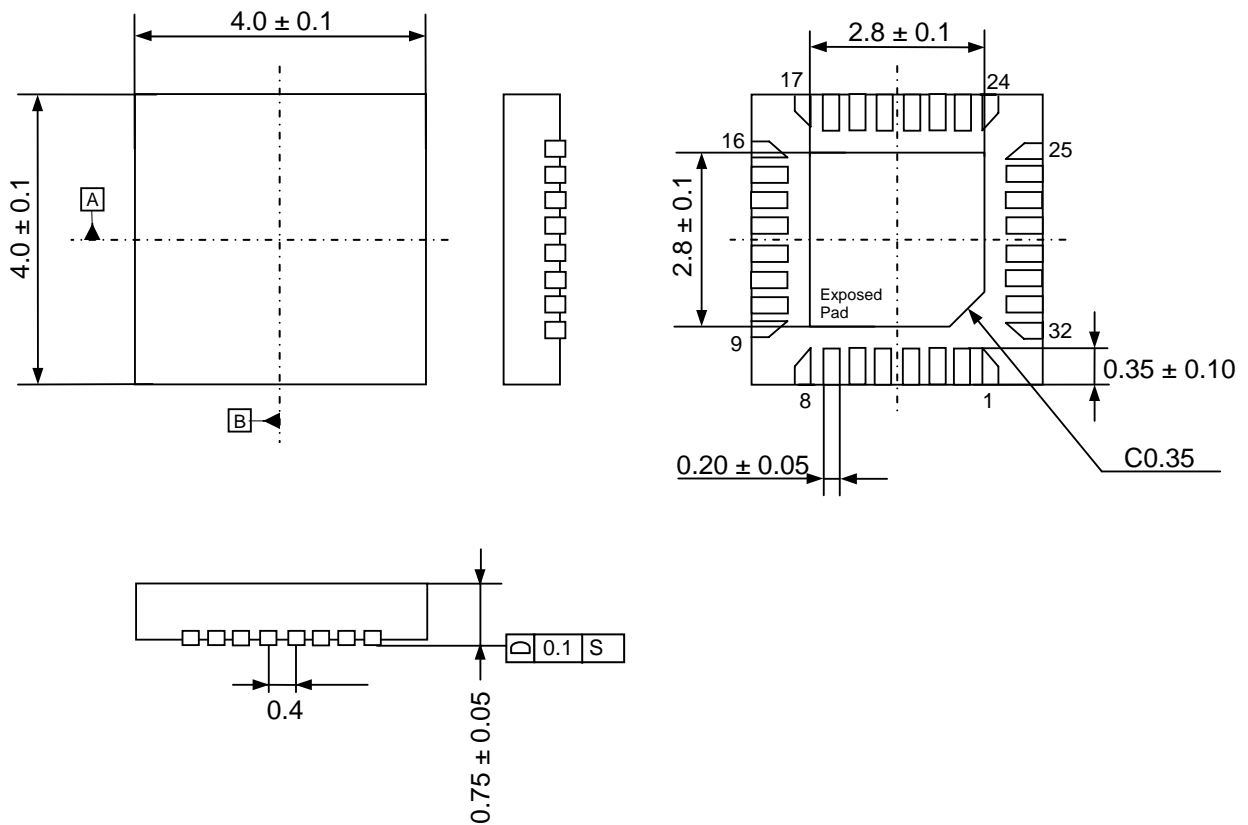
- (1) Stop the external MCKI, BICK and LRCK clocks.

■ Power Down

Power supply current cannot be shut down by stopping clocks and setting PMVCM bit = “0”. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = “L”. When the PDN pin = “L”, all registers are initialized.

PACKAGE

32pin QFN (Unit: mm)

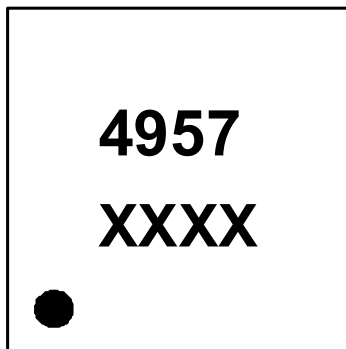


Note: The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

MARKING



1

XXXX: Date code (4 digit)
Pin #1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/06/11	00	First Edition		

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