AsahiKASEI
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AK4675

Stereo CODEC with MIC/RCV/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4675 is a stereo CODEC with a built-in Microphone-Amplifier, Receiver-Amplifier, cap-less Headphone-Amplifier and stereo audio class-D Speaker-Amplifier. The AK4675 features dual PCM I/F in addition to audio I/F that allows easy interfacing in mobile phone designs with Bluetooth I/F. The Speaker-Amplifier includes ALC (Automatic Level Control) circuit what is able to stabilize each output sound levels. The AK4675 is available in an 83pin BGA, utilizing less board space than competitive offerings.

FEATURES

1. Recording Function (Stereo CODEC)
- **4 Stereo Input Selector x 2ch**
- **4 Stereo Inputs (Single-ended) or 2 Stereo Input (Full-differential)**
- **MIC Amplifier: +30dB ~ –12dB, 3dB step**
- **Digital ALC (Automatic Level Control): +36dB ~ –54dB, 0.375dB Step, Mute**
- **Wind-noise Reduction Filter**
- **Stereo Separation Emphasis**
- **5-band Programmable Notch Filter**
- **Audio Interface Format: 16bit MSB justified, I^2S, DSP Mode**

2. Playback Function (Stereo CODEC)
- **Digital Volume (+12dB ~ –115.0dB, 0.5dB Step, Mute)**
- **Digital ALC (Automatic Level Control): +36dB ~ –54dB, 0.375dB Step, Mute**
- **Stereo Separation Emphasis**
- **5-band EQ**
- **Stereo Line Output**
- **Mono Receiver-Amp**
  - **BTL Output**
  - **Output Power: 30mW@32Ω (AVDD=3.3V)**
- **Stereo Cap-less Headphone Amplifier**
  - **Mono / Stereo Mode**
  - **Output Power: 64mW x 2ch @ 16Ω, SVDDA=3.3V, THD+N = –40dB**
  - **THD+N: -58dB @ 16Ω, Po=30mW, SVDDA=3.3V**
  - **Output Noise Level: 24μVrms**
  - **Outputs Volume: +12dB to –50dB, 2dB Step**
  - **Pop Noise Free at Power-ON/OFF and Mute**
- **Class-D Speaker Amplifier**
  - **BTL output**
  - **Output Power: 1.6W @ 8Ω, SVDDA=5.0V**
    0.8W @ 8Ω, SVDDA=3.6V
  - **THD+N: –65dB @8Ω, Po=0.25W, SVDDA=3.6V**
  - **Output Noise Level: 71μVrms**
  - **ALC (Automatic Level Control) Circuit**
  - **Pop Noise Free at Power-ON/OFF and Mute**
  - **External filter-less**
  - **Short Protection circuit**
- **Thermal Shutdown / Short protection circuit**
- **Analog Mixing: 4 Stereo Input**
- **Audio Interface Format: 16bit MSB justified, 16bit LSB justified, 16-24bit I^2S, DSP Mode**

3. Dual PCM I/F for Baseband & Bluetooth Interface

- **Sample Rate Converter (Up sample: up to x6: Down sample: down to x1/6)**
- **Sample Rate: 8kHz**
- **Digital Volume**
- **Audio Interface Format:**
  - **16bit Linear, 8bit A-law, 8bit μ-law**
  - **Short/Long Frame, I^2S, MSB justified**

4. 10bit SAR ADC
- **3 Input Selectors**

5. Power Management

6. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz, 27MHz (MCKI pin)**
  1fs (LRCK pin)
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Sampling Rate: 256fs, 384fs, 512fs, 768fs or 1024fs (MCKI pin)**

7. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs

8. Sampling Rate (Stereo CODEC):
- **PLL Slave Mode (LRCK pin): 8kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 8kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Master/Slave Mode:**
  8kHz ~ 48kHz (256fs, 384fs), 8kHz ~ 26kHz (512fs, 768fs),
  8kHz ~ 13kHz (1024fs)

9. μP I/F: I^2C Bus (Ver 1.0, 400kHz High Speed Mode)

10. Master/Slave mode

11. Ta = –30 ~ 85°C

12. Power Supply:
- **Analog1: 2.2 ~ 3.6V**
- **Analog2: 2.6 ~ 3.6V**
- **Digital I/F: 1.6 ~ 3.6V**
- **Speaker Amp: 3.0 ~ 5.5V**

13. Package: 83pin BGA (5.5mm x 5.5mm, 0.5mm pitch)

■ Block Diagram (CODEC Block)

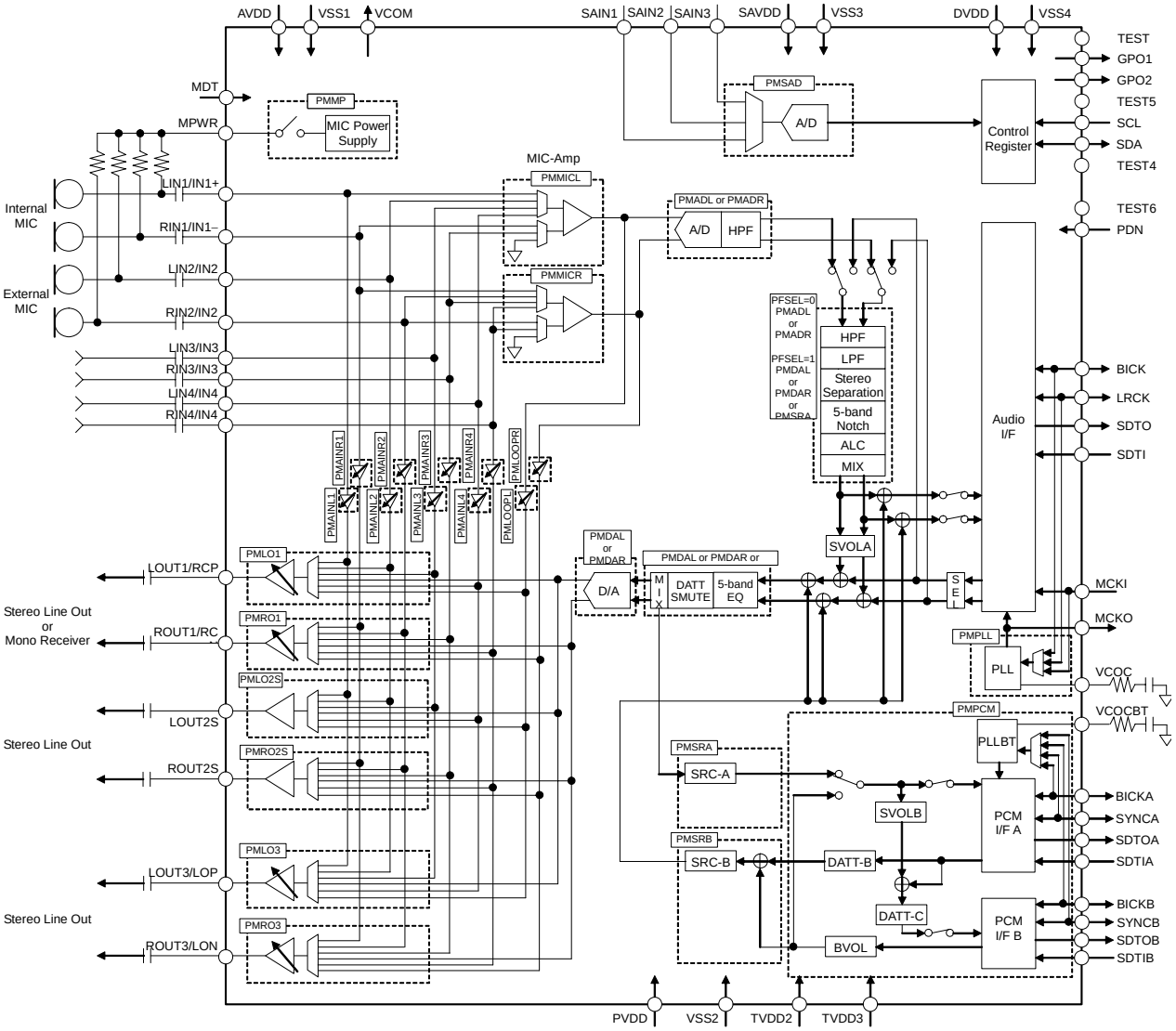


Figure 1. Block Diagram (CODEC Block)

■ Block Diagram (HP/SPK-Amp Block)

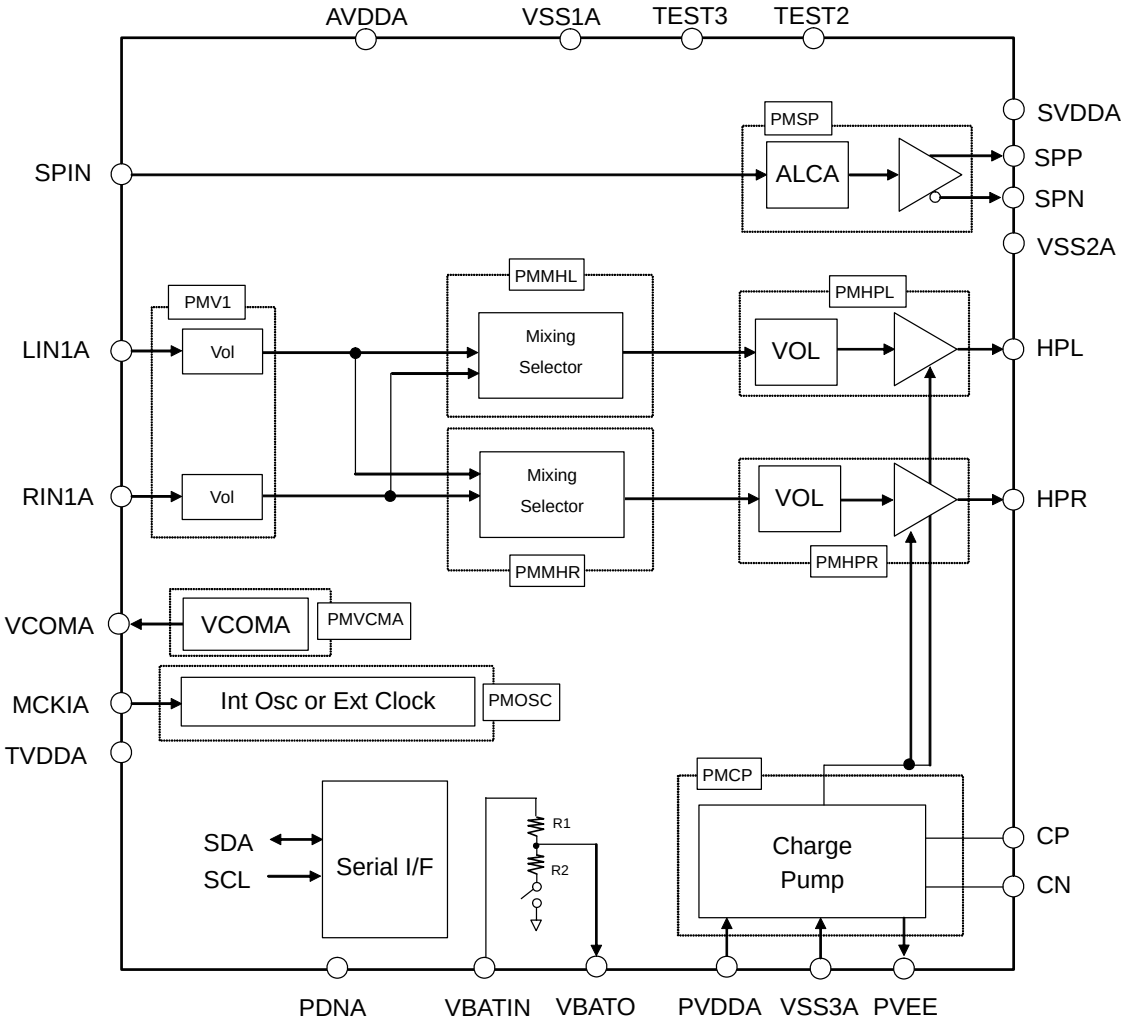
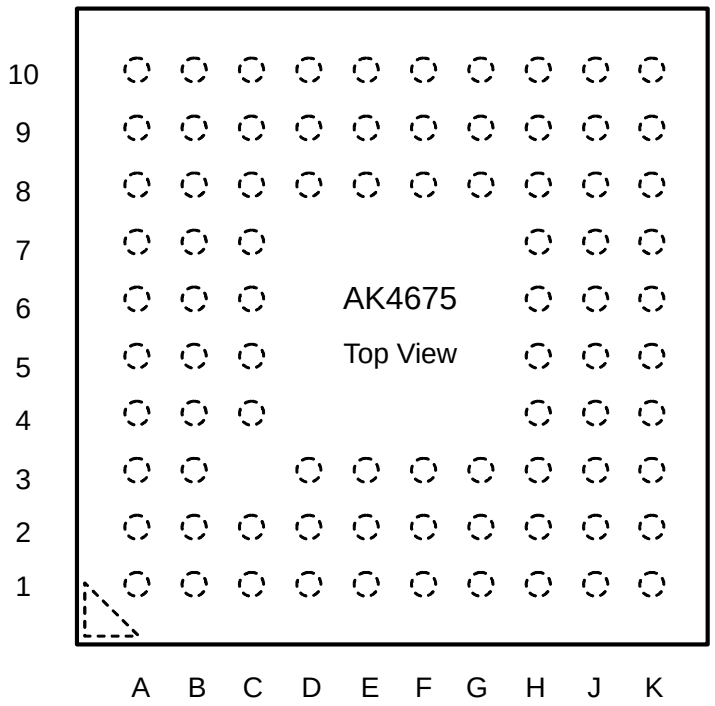


Figure 2. Block Diagram (HP/SPK-Amp Block)

■ Ordering Guide

AK4675EG	–30 ~ +85°C	83pin BGA (0.5mm pitch)
AKD4675	Evaluation board for AK4675	

■ Pin Layout



10	TEST	HPR	VCOM	VCOC	HPL	PVDDA	VSS3A	CP	SDTIA	GPO2
9	AVDD	ROUT1 /RCN	VBATO	VCOCBT	PVEE	SDTOA	SYNCA	CN	PDNA	BICKA
8	VSS1	ROUT3 /LON	VCOMA	RIN4 /IN4–	PVDD	VSS2	TVDD2	TVDDA	VSS4	MCKIA
7	VBATIN	LOUT3 /LOP	LIN3 /IN3+	Top View				TEST6	DVDD	SDA
6	LOUT1 /RCP	LIN4 /IN4+	RIN1A					MCKO	NC	SCL
5	RIN3 /IN3–	RIN2 /IN2–	SAIN2					MCKI	TEST5	BICK
4	LIN2 /IN2+	SAIN3	SAIN1					LRCK	PDN	VSS1A
3	LIN1 /IN1+	RIN1 /IN1–		SAVDD	SDTOB	SDTO	BICKB	NC	TEST3	AVDDA
2	LIN1A	MPWR	ROUT2S	NC	VSS3	SPN	SYNCB	SDTIB	TEST4	SPIN
1	MDT	LOUT2S	NC	SVDDA	VSS2A	TVDD3	SPP	TEST2	SDTI	GPO1
	A	B	C	D	E	F	G	H	J	K

PIN/FUNCTION

No.	Pin Name	I/O	Function
A1	MDT	I	MIC Detection Pin (Internal pull down by typ. 500kΩ)
B2	MPWR	O	MIC Power Supply Pin
B4	SAIN3	I	10bit SAR ADC Analog Input 3 Pin
C5	SAIN2	I	10bit SAR ADC Analog Input 2 Pin
C4	SAIN1	I	10bit SAR ADC Analog Input 1 Pin
D3	SAVDD	-	10bit SAR ADC Power Supply Pin 2.2V ~ 3.6V
E2	VSS3	-	Ground 3 Pin for CODEC
F1	TVDD3	-	Digital I/O Power Supply 3 Pin for CODEC 1.6V ~ 3.6V
E3	SDTOB	O	Serial Data Output B Pin
G2	SYNCB	I/O	Sync Signal B Pin
G3	BICKB	I/O	Serial Data Clock B Pin
H2	SDTIB	I	Serial Data Input B Pin
J1	SDTI	I	Audio Serial Data Input Pin
K1	GPO1	O	General Purpose Output 1 Pin
J2	TEST4	O	TEST Pin This pin must be open.
F3	SDTO	O	Audio Serial Data Output Pin
J4	PDN	I	CODEC Power-Down Mode Pin "H": Power-up "L": Power-down, reset and initializes the control registers for CODEC. "L" time of 150ns or more after power-up is needed to reset the AK4675.
H4	LRCK	I/O	Input / Output Channel Clock Pin
H5	MCKI	I	External Master Clock Input Pin
H6	MCKO	O	Master Clock Output Pin
H7	TEST6	I	Test Pin Connect to DVDD.
K5	BICK	I/O	Audio Serial Data Clock Pin
J5	TEST5	I	TEST Pin This pin must be connected to VSS4.
K6	SCL	I	Control Data Clock Input Pin
J8	VSS4	-	Ground 4 Pin for CODEC
J7	DVDD	-	Digital Power Supply Pin for CODEC 1.6V ~ 3.6V
K7	SDA	I/O	Control Data Input/Output Pin
K10	GPO2	O	General Purpose Output 2 Pin

No.	Pin Name	I/O	Function
J10	SDTIA	I	Serial Data Input A Pin
K9	BICKA	I/O	Serial Data Clock A Pin
G9	SYNCA	I/O	Sync Signal A Pin
F9	SDTOA	O	Serial Data Output A Pin
G8	TVDD2	-	Digital I/O Power Supply 2 Pin for CODEC 1.6V ~ 3.6V
F8	VSS2	-	Ground 2 Pin for CODEC
E8	PVDD	-	PLLBT Power Supply Pin 2.2V ~ 3.6V
D9	VCOCBT	O	Output Pin for Loop Filter of PLLBT Circuit This pin must be connected to VSS2 pin with one resistor and capacitor in series.
D10	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 pin with one resistor and capacitor in series.
C10	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs and DAC outputs.
A10	TEST	-	Test Pin This pin must be open.
A9	AVDD	-	Analog Power Supply Pin for CODEC 2.2V ~ 3.6V
A8	VSS1	-	Ground 1 Pin for CODEC
B9	ROUT1	O	Rch Stereo Line Output 1 Pin (RCV bit = "0": Stereo Line Output)
	RCN	O	Receiver-Amp Negative Output Pin (RCV bit = "1": Receiver Output)
A6	LOUT1	O	Lch Stereo Line Output 1 Pin (RCV bit = "0": Stereo Line Output)
	RCP	O	Receiver-Amp Positive Output Pin (RCV bit = "1": Receiver Output)
B8	ROUT3	O	Rch Stereo Line Output 3 Pin (LODIF bit = "0": Single-ended Stereo Output)
	LON	O	Negative Line Output Pin (LODIF bit = "1": Full-differential Mono Output)
B7	LOUT3	O	Lch Stereo Line Output 3 Pin (LODIF bit = "0": Single-ended Stereo Output)
	LOP	O	Positive Line Output Pin (LODIF bit = "1": Full-differential Mono Output)
D8	RIN4	I	Rch Analog Input 4 Pin (MDIF4 bit = "0": Single-ended Input)
	IN4−	I	Negative Line Input 4 Pin (MDIF4 bit = "1": Full-differential Input)
B6	LIN4	I	Lch Analog Input 4 Pin (MDIF4 bit = "0": Single-ended Input)
	IN4+	I	Positive Line Input 4 Pin (MDIF4 bit = "1": Full-differential Input)
A5	RIN3	I	Rch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input)
	IN3−	I	Negative Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input)
C7	LIN3	I	Lch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input)
	IN3+	I	Positive Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input)
B5	RIN2	I	Rch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input)
	IN2−	I	Negative Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input)
A4	LIN2	I	Lch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input)
	IN2+	I	Positive Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input)
B3	RIN1	I	Rch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input)
	IN1−	I	Negative Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input)
A3	LIN1	I	Lch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input)
	IN1+	I	Positive Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input)
C2	ROUT2S	O	Rch Stereo Line Output 2 Pin
B1	LOUT2S	O	Lch Stereo Line Output 2 Pin

No.	Pin Name	I/O	Function
H1	TEST2	-	Test 2 Pin This pin must be open.
H3	NC	-	No Connect Pin No internal bonding. This pin must be opened or connected to the ground.
K3	AVDDA	-	HP/SPK-Amp Analog Power Supply Pin 2.6V ~ 3.6V
K4	VSS1A	-	HP/SPK-Amp Ground 1 Pin
H8	TVDDA	-	HP/SPK-Amp Digital Interface Power Supply Pin 1.6V ~ 3.6V This pin must be connected to DVDD.
J6	NC	-	No Connect Pin No internal bonding. This pin must be opened or connected to the ground.
K8	MCKIA	I	HP/SPK-Amp External Clock Input Pin (Internal Pull-down pin to VSS1A: typ. 100kΩ)
J9	PDNA	I	HP/SPK-Amp Power-Down Mode Pin "H": Power-up "L": Power-down, reset and initializes the control registers for HP/SPK-Amp. "L" time of 150ns or more after power-up is needed to reset the AK4675.
H10	CP	O	Positive Charge Pump Capacitor Terminal Pin
H9	CN	I	Negative Charge Pump Capacitor Terminal Pin
F10	PVDDA	-	Charge Pump Circuit Positive Power Supply Pin 2.6V ~ 3.6V
G10	VSS3A	-	HP/SPK-Amp Ground 3 Pin
E9	PVEE	O	Charge Pump Circuit Negative Voltage Output Pin
E10	HPL	O	Lch Headphone-Amp Output Pin
B10	HPR	O	Rch Headphone-Amp Output Pin
A7	VBATIN	I	Battery Monitor Input Pin
C9	VBATO	O	Battery Monitor Output Pin
C8	VCOMA	O	HP/SPK-Amp Analog Common Voltage Output Pin
C6	RIN1A	I	Rch HP-Amp Input Pin
A2	LIN1A	I	Lch HP-Amp Input Pin
D2	NC	-	No Connect Pin No internal bonding. This pin must be opened or connected to the ground.
C1	NC	-	No Connect Pin No internal bonding. This pin must be opened or connected to the ground.
D1	SVDDA	-	Speaker-Amp Power Supply Pin 3.0V ~ 5.5V
E1	VSS2A	-	HP/SPK-Amp Ground 2 Pin
G1	SPP	O	Positive Speaker-Amp Output Pin
F2	SPN	O	Negative Speaker-Amp Output Pin
J3	TEST3	-	TEST Pin This pin must be open.
K2	SPIN	I	Speaker-Amp Input Pin

Note 1. All input pins except analog input pins (MDT, LIN1/IN1+, RIN1/IN1−, LIN2/IN2+, RIN2/IN2−, LIN3/IN3+, RIN3/IN3−, LIN4/IN4+, RIN4/IN4−, SAIN1, SAIN2, SAIN3, LIN1A, RIN1A, SPIN, VBATIN) must not be left floating. I/O pins except the SDA pin (LRCK, BICK, SYNCA, BICKA, SYNCB, BICK) must be processed appropriately as shown in "Master Mode/Slave Mode" and "PCM I/F Master Mode/Slave Mode". The PDA pin should be pulled-up externally and connected to (DVDD+0.3)V or less.

■ Handling of Unused Pins

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, MDT, VCOC, ROUT3/LON, LOUT3/LOP, ROUT2S, LOUT2S, ROUT1/RCN, LOUT1/RCP, RIN4/IN4−, LIN4/IN4+, RIN3/IN3−, LIN3/IN3+, RIN2/IN2−, LIN2/IN2+, RIN1/IN1−, LIN1/IN1+, VCOCBT, SAIN1, SAIN2, SAIN3, HPL, HPR, SPIN, SPP, SPN, LIN1A, RIN1A, VBATIN, VBATO, TEST2	These pins msut be open.
Digital	MCKO, SDTOA, SDTOB, GPO1, GPO2, BICKA, SYNCA, BICKB, SYNCB	These pins must be open.
	MCKI, , SDTIA, SDTIB	These pins must be connected to VSS4.
	MCKIA	These pins must be connected to VSS1A.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=VSS1A=VSS2A=VSS3A=0V; Note 2, Note 3)

Parameter		Symbol	Min	max	Units
Power Supplies: (Note 4)	CODEC Analog	AVDD	–0.3	4.0	V
	PLLBT	PVDD	–0.3	4.0	V
	10bit SAR ADC	SAVDD	–0.3	4.0	V
	CODEC Digital	DVDD	–0.3	4.0	V
	CODEC Digital I/O 2	TVDD2	–0.3	4.0	V
	CODEC Digital I/O 3	TVDD3	–0.3	4.0	V
	HP/SPK-Amp Analog	AVDDA	–0.3	6.0	V
	HP/SPK-Amp Digital I/F	TVDDA	–0.3	6.0	V
	Speaker-Amp & Headphone-Amp	SVDDA	–0.3	6.0	V
	Charge Pump	PVDDA	–0.3	4.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage 1 (Note 5)		VINA1	–0.3	AVDD+0.3	V
Analog Input Voltage 2 (Note 6)		VINA2	–0.3	SAVDD+0.3	V
Analog Input Voltage 3 (Note 7)		VINA3	–0.3	(AVDDA+0.3) or 6.0	V
Analog Input Voltage 4 (Note 8)		VINA4	–0.3	6.0	V
Digital Input Voltage 1 (Note 9)		VIND1	–0.3	DVDD+0.3	V
Digital Input Voltage 2 (Note 10)		VIND2	–0.3	TVDD2+0.3	V
Digital Input Voltage 3 (Note 11)		VIND3	–0.3	TVDD3+0.3	V
Digital Input Voltage 4 (Note 12)		VIND4	–0.3	(TVDDA+0.3) or 6.0	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 13)	Ta=85°C (Note 14)	Pd1	-	0.91	W
	Ta=70°C (Note 15)	Pd2	-	1.18	W

Note 2. All voltages with respect to ground.

Note 3. VSS1, VSS2, VSS3, VSS4, VSS1A, VSS2A and VSS3A must be connected to the same analog ground plane.

Note 4. TVDDA should be connected to DVDD.

Note 5. RIN4/IN4–, LIN4/IN4+, RIN3/IN3–, LIN3/IN3+, RIN2/IN2–, LIN2/IN2+, RIN1/IN1–, LIN1/IN1+ pins

Note 6. SAIN1, SAIN2, SAIN3 pins

Note 7. LIN1A, RIN1A, SPIN pins. The maximum value is smaller value between (AVDDA+0.3)V and 6.0V.

Note 8. VBATIN pin

Note 9. PDN, SCL, SDA, SDTI, LRCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

Note 10. BICKA, SYNCA, SDTIA pins

Note 11. BICKB, SYNCB, SDTIB pins

Note 12. PDNA, MCKIA pins. The maximum value is smaller value between (AVDDA+0.3)V and 6.0V.

Note 13. In case that the PCB wiring density is 300%. This power is the AK4675 internal dissipation that does not include power of externally connected speaker and headphone.

Note 14. When Ta=85°C, the HP-Amp power must be under 30mW@16Ω and SPK-Amp power must be 1.0W@8Ω.

Note 15. When Ta=70°C, the HP-Amp power must be under 30mW@16Ω and SPK-Amp power must be 1.6W@8Ω.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=VSS1A=VSS2A=VSS3A=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 16)	CODEC Analog	AVDD	2.2	3.3	3.6	V
	PLLBT	PVDD	2.2	3.3	3.6	V
	10bit SAR ADC	SAVDD	2.2	3.3	3.6	V
	CODEC Digital	DVDD	1.6	3.3	3.6	V
	CODEC Digital I/O 2	TVDD2	1.6	3.3	3.6	V
	CODEC Digital I/O 3	TVDD3	1.6	3.3	3.6	V
	HP/SPK-Amp Analog	AVDDA	2.6	3.3	3.6	V
	HP/SPK-Amp Digital I/F	TVDDA	1.6	3.3	3.6	V
	Speaker-Amp & Headphone-Amp	SVDDA	3.0	3.6	5.5	V
	Charge Pump	PVDDA	2.6	3.3	3.6	V
	Difference 1	AVDD–PVDD	–0.1	0	+0.1	V
	Difference 2	PVDDA–AVDDA	–0.3	0	+0.3	V
	Difference 3	SVDDA–AVDDA	–0.3	-	-	V
	Difference 4	DVDD–TVDDA	–0.3	0	+0.3	V

Note 2. All voltages with respect to ground.

Note 16. TVDDA must be connected to DVDD. The power-up sequence between AVDD, PVDD, SAVDD, DVDD, TVDD2, TVDD3, AVDDA, TVDDA, SVDDA and PVDDA is not critical. However, the PDN and PDNA pin must be held to “L” until all power supply pins are supplied. After all power supplies are filled, PDN and PDNA pins should be set to “H”.

* The AK4675 supports the following two cases of partial power ON/OFF. In these cases, PDNA pin should be “L” and all power management bits (PMVCM, PMMP, PMMICL, PMMICR, PMADL, PMADR, PMDAL, PMDAR, PMPLL, PMLOOPL, PMLOOPR, PMAINL1, PMAINR1, PMAINL2, PMAINR2, PMAINL3, PMAINR3, PMAINL4, PMAINR4, PMLO1, PMRO1, PMLO2S, PMRO2S, PMLO3, PMRO3, PMSRA, PMSRB, PMPCM, and PMSAD) should be OFF or PDN and PDNA pins should be “L”.
  1. DVDD=TVDDA=SVDDA=ON, AVDD=PVDD=SAVDD=TVDD2=TVDD3=AVDDA=PVDDA=OFF
  2. DVDD=TVDDA=ON, AVDD=PVDD=SAVDD=TVDD2=TVDD3=AVDDA=PVDDA=SVDDA=OFF

When the power state is changed from OFF to ON in the above cases, the PDN and PDNA pins should be set to “H” after all power supply pins are supplied.

When DVDD and TVDDA are powered OFF, AVDD, PVDD, SAVDD, TVDD2, TVDD3, AVDDA, TVDDA, SVDDA or PVDDA must be powered OFF. When only DVDD and TVDDA are OFF, leak current of 10mA to 100mA may occur.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=AVDDA=PVDDA=TVDDA=3.3V, SVDDA=3.6V; VSS1=VSS2=VSS3=VSS4=VSS1A=VSS2A=VSS3A=0V; Signal Frequency=1kHz; 16bit Data; fs=44.1kHz, BICK=64fs, LP bit = "0"; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins; PMAINL1/R1/L2/R2/L3/R3/L4/R4 bits = "0"					
Input Resistance					
MGNL/R0 bit = "0"		28	42	56	kΩ
MGNL/R0 bit = "1"		20	30	40	kΩ
Gain (Note 17)					
Max (MGNL/R3-0 bits = "FH")		-	+30	-	dB
Min (MGNL/R3-0 bits = "1H")		-	–12	-	dB
MIC Power Supply: MPWR pin					
Output Voltage (Note 18)		2.47	2.64	2.81	V
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
MIC Detection: MDT pin					
Comparator Voltage Level (Note 19)		0.165		0.247	mV
Internal pull down Resistance		250	500	750	kΩ
Stereo ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins → Stereo ADC → IVOL, IVOL=0dB, ALC=OFF					
Resolution		-	-	16	Bits
Input Voltage (Note 20)	(Note 21)	0.150	0.176	0.203	Vpp
	(Note 22)	1.68	1.98	2.28	Vpp
S/(N+D) (–1dBFS)	(Note 21)	72	82	-	dB
	(Note 22)	-	87	-	dB
D-Range (–60dBFS, A-weighted)	(Note 21)	75	86	-	dB
	(Note 22)	-	95	-	dB
S/N (A-weighted)	(Note 21)	75	86	-	dB
	(Note 22)	-	95	-	dB
Interchannel Isolation	(Note 21)	75	90	-	dB
	(Note 22)	-	100	-	dB
Interchannel Gain Mismatch	(Note 21)	-	0.1	0.8	dB
	(Note 22)	-	0.1	0.8	dB

Note 17. In case of full-differential input, MGAIN=0dB (min) and AVDD=2.4V (min).
Note 18. Output voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ).
Note 19. Comparator Voltage Level is proportional to AVDD voltage. Vth = 0.05 x AVDD(min), 0.075 x AVDD(max).
Note 20. Input voltage is proportional to AVDD voltage. Vin = 0.053 x AVDD (typ)@MGNL3-0=MGNR3-0 bits = "CH" (+21dB), Vin = 0.6 x AVDD(typ)@MGNL3-0=MGNR3-0 bits = "5H" (0dB).
Note 21. MGNL3-0=MGNR3-0 bits = "CH" (+21dB).
Note 22. MGNL3-0=MGNR3-0 bits = "5H" (0dB).

Parameter	min	typ	max	Units
Stereo DAC Characteristics:				
Resolution	-	-	16	Bits
Stereo Line Output Characteristics: Stereo DAC → LOUT1/ROUT1/LOUT3/ROUT3 pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L1VL=L3VL=0dB, RCV bit = "0", R_L=10kΩ; unless otherwise specified.				
Output Voltage (Note 23)	1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)	75	85	-	dB
S/N (A-weighted)	82	92	-	dB
Interchannel Isolation	85	100	-	dB
Interchannel Gain Mismatch	-	0.1	0.5	dB
Load Resistance	10	-	-	kΩ
Load Capacitance	-	-	30	pF
Stereo Line Output Characteristics: Stereo DAC → LOUT2S/ROUT2S pins, ALC=OFF, IVOL=0dB, OVOL=0dB, R_L=25kΩ; unless otherwise specified.				
Output Voltage (Note 23)	1.78	1.98	2.18	Vpp
S/(N+D) (0dBFS)	72	85	-	dB
S/N (A-weighted)	82	92	-	dB
Interchannel Isolation	85	100	-	dB
Interchannel Gain Mismatch	-	0.1	0.5	dB
Load Resistance	25	-	-	kΩ
Load Capacitance	-	-	30	pF
Mono Receiver-Amp Output Characteristics: Stereo DAC → RCP/RCN pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L1VL=0dB, RCV bit = "1", R_L=32Ω, BTL; unless otherwise specified.				
Output Voltage (Note 24)				
−6dBFS, R_L=32Ω (Po=15mW)	1.57	1.96	2.35	Vpp
−3dBFS, R_L=32Ω (Po=30mW)	-	2.77	-	Vpp
S/(N+D)				
−6dBFS, R_L=32Ω (Po=15mW)	40	60	-	dB
−3dBFS, R_L=32Ω (Po=30mW)	-	20	-	dB
S/N (A-weighted)	82	92	-	dB
Load Resistance	32	-	-	Ω
Load Capacitance	-	-	30	pF

Note 23. The Output voltage is proportional to the AVDD voltage. Vout = 0.6 x AVDD (typ).
Note 24. The Output voltage is proportional to the AVDD voltage. Vout = (RCP) – (RCN) = 0.59 x AVDD (typ)@−6dBFS.
Note 25. VSS1 load capacitance to output pins.

Parameter	min	typ	max	Units
Mono Line Output Characteristics: Stereo DAC → LOP/LON pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L3VL=0dB, LODIF bit = "1", R_L=10kΩ for each pin (Full-differential)				
Output Voltage (Note 26)	3.52	3.96	4.36	Vpp
S/(N+D) (0dBFS)	75	85	-	dB
S/N (A-weighted)	85	95	-	dB
Load Resistance (LOP/LON pins, respectively)	10	-	-	kΩ
Load Capacitance (LOP/LON pins, respectively)	-	-	30	pF
Single-ended Line Input: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins; (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")				
Maximum Input Voltage (Note 28)	-	1.98	-	Vpp
Gain				
Input→LOUT1/ROUT1/LOUT2S/ROUT2S/LOUT3/ROUT3 (LODIF=RCV bits = "0")				
	–1	0	+1	dB
Input → RCP/RCN/LOP/LON (LODIF=RCV bits = "1")				
	-	+6	-	dB
Full-differential Line Input: IN1+/–, IN2+/–, IN3+/–, IN4+/– pins; (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")				
Maximum Input Voltage (Note 29)	-	1.98	-	Vpp
Gain				
Input→LOUT1/ROUT1/LOUT2S/ROUT2S/LOUT3/ROUT3 (LODIF=RCV bits = "0")				
	–1	0	+1	dB
Input → RCP/RCN/LOP/LON (LODIF=RCV bits = "1", Note 30)				
	-	+6	-	dB

Note 26. The Output voltage is proportional to the AVDD voltage. Vout = (LOP) – (LON) = 1.2 x AVDD (typ).
Note 27. VSS1 load capacitance to output pins.
Note 28. The Maximum Input voltage is proportional to the AVDD voltage. Vin = 0.6 x AVDD (typ).
Note 29. The Maximum Input voltage is proportional to the AVDD voltage. Vin = (IN4+) – (IN4–) = 0.6 x AVDD (typ).
Note 30. Vout = (RCP) – (RCN) at RCV bit = "1", Vout = (LOP) – (LON) at LODIF bit = "1".

ANALOG CHARACTERISTICS (HP/SPK-Amp)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=AVDDA=PVDDA=TVDDA=3.3V, SVDDA=3.6V; VSS1=VSS2=VSS3=VSS4=VSS1A=VSS2A=VSS3A=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Headphone-Amp: R_L =16Ω; Speaker-Amp: R_L =8Ω + 10μH; Charge Pump Circuit External Capacitance: C1=C2= 2.2μF (Figure 3); unless otherwise specified)

Parameter	min	typ	max	Units
LIN1A, RIN1A pins				
Input Resistance	25	50	110	kΩ
Input Analog Volume: L1V3-0, R1V3-0 bits				
Step Size	1	2	3	dB
Gain Control Range	–20	-	+10	dB
Headphone-Amp: (LIN1A/RIN1A → HPL/HPR pins), HPGA = 0dB				
Output Power (THD+N=1%) SVDDA=3.3V	-	64	-	mW
THD+N 0.7Vrms Single-ended Input, Po = 30mW	-	-58	-	dB
Output Noise (A-weighted)	-	24	40	μVrms
Interchannel Gain Mismatch	-	0.2	0.8	dB
Load Resistance	16	-	-	Ω
Load Capacitance	-	-	300	pF
Output Voltage: 0.7Vrms at single-ended Input	0.62	0.69	0.76	Vrms
PSRR				
217Hz (Note 31)	-	70	-	dB
1kHz (Note 31)	-	70	-	dB
217Hz (Note 32)	-	100	-	dB
1kHz (Note 32)	-	80	-	dB
Interchannel Isolation	60	80	-	dB
Headphone Analog Volume 1 (HPGA4-0 bits)				
Step Size	0.5	2	3.5	dB
Gain Control Range	–50	-	+12	dB
SPIN pins				
Input Resistance	15	26	36	kΩ
Speaker Analog Volume: SPGA5-0 bits				
Step Size	0.1	0.5	0.9	dB
Gain Control Range	–12	-	+19.5	dB
Class-D Speaker-Amp: SPIN → SPP/SPN; ALC = OFF, Input Volume=SPGA=0dB, BTL				
Output Power (THD+N=10%)				
SVDDA=5.0V	-	1.6	-	W
SVDDA=3.6V	-	0.8	-	W
Output Level (Note 33)				
SVDDA = 5.0V, Input Level = 0.85Vrms	-	2.7	-	Vrms
SVDDA = 3.6V, Input Level = 0.64Vrms	-	2.0	-	Vrms
SVDDA = 3.6V, Input Level = 0.46Vrms	1.33	1.48	1.63	Vrms
THD+N: Po=0.25W, Input Level=0.46Vrms(Note 33)	-	-65	-40	dB
Output Noise (A-weighted)	-	71	150	μVrms
Load Resistance	8	-	-	Ω
Load Capacitance (Note 34)	-	-	300	pF
PSRR				
217Hz (Note 35)	-	60	-	dB
1kHz (Note 35)	-	50	-	dB
217Hz (Note 36)	-	50	-	dB
1kHz (Note 36)	-	50	-	dB
Switching Frequency	150	250	400	kHz
Short Protection Current (Note 37)		40	120	mA
Start-Up Time	18	30	48	ms

Note 31. PSR is applied to AVDDA and PVDDA with 100mVpp. This is the value of convoluting sinusoidal voltage of 100mVpp.
Note 32. PSR is applied to SVDDA with 0.89Vpp. This is the value of convoluting sinusoidal voltage of 100mVpp.
Note 33. When the input data is single-ended.
Note 34. VSS1 load capacitance to output pins. For differential signals, the load capacitance will be twice as big as this value.
Note 35. PSR is applied to AVDDA with 100mVpp. This is the value of convoluting sinusoidal voltage of 100mVpp.
Note 36. PSR is applied to SVDDA with 100mVpp. This is the value of convoluting sinusoidal voltage of 100mVpp.
Note 37. The average current between SVDDA and VSS2A, when the SPP pin and SPN pin are shorted and 1kHz, 0.85Vrms sine wave is input at Single-ended mode.

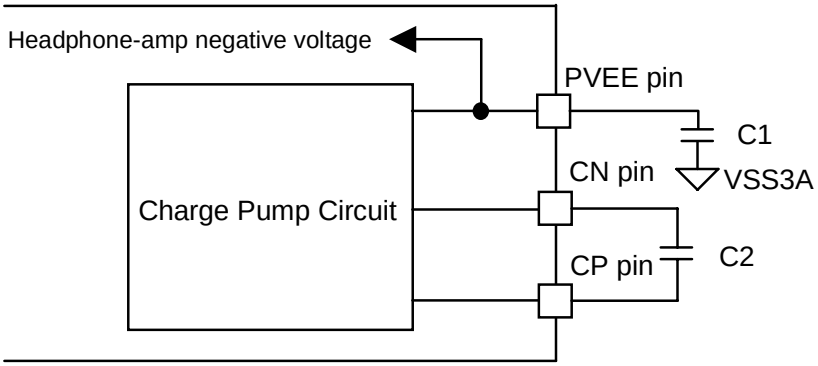


Figure 3. Charge Pump Circuit External Capacitor

Parameter	min	typ	max	Units
Battery Monitor: (BATCPU bit = "1")				
Input Resistance (VBATIN pin)	5	10	-	kΩ
Attenuation (VBATO / VBATIN) (Note 38)	0.245	0.25	0.255	-

Note 38. When input 4.4V to the VBATIN pin.

ANALOG CHARACTERISTICS (Power Supply Current)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=AVDDA=PVDDA=TVDDA=3.3V, SVDDA=3.6V; VSS1=VSS2=VSS3=VSS4=VSS1A=VSS2A=VSS3A=0V;
Signal Frequency=1kHz; 16bit Data; fs=44.1kHz, BICK=64fs, LP bit = "0"; Measurement frequency=20Hz ~ 20kHz;
Headphone-Amp: R_L=16Ω; Speaker-Amp: R_L=8Ω + 10μH; Charge Pump Circuit External Capacitance: C1=C2=2.2μF (Figure 3); unless otherwise specified)

Parameter		min	typ	max	Units
Power Supplies:					
CODEC Block Power Up (PDN pin = "H", All Circuits Power-up)					
AVDD+PVDD+DVDD +TVDD2+TVDD3+SAVDD	(Note 39)	-	20	-	mA
	(Note 40)	-	21	30	mA
	(Note 41)	-	8	12	mA
HP/SPK-Amp Block Power Up (PDNA pin = "H", All Circuits Power-up)					
AVDDA+TVDDA:	ALL ON (Note 42)	-	4.0	6.5	mA
	HP-Amp ON (Note 43)	-	2.0	-	mA
	SPK-Amp ON (Note 44)	-	2.8	-	mA
PVDDA (No Output) HP-Amp ON		-	1.3	3.2	mA
SVDDA (No Output): HP-Amp ON		-	2.0	4.0	mA
SPK-Amp ON			1.0	4.0	mA
Power Down (PDN=PDNA pins = "L") (Note 45)					
AVDD+PVDD+DVDD+TVDD2+TVDD3+SAVD D+ AVDDA+PVDDA+SVDDA+TVDDA		-	1	60	μA

Note 39. EXT Slave Mode and LP bit = "0", fs=44.1kHz, PMMICL = PMMICR = PMADL = PMADR = PMDAL = PMDAR = PMLO1 = PMRO1 = PMLO2S = PMRO2S = PMLO3 = PMRO3 =PMSAD = PMVCM bits = "1", PMPLL = MCKO = PMMP = M/S = PMSRA = PMSRB = PMPCM bits = "0".
AVDD=12.1mA (typ), PVDD=0mA (typ), DVDD=5.6mA (typ), TVDD2=0mA (typ), TVDD3=0mA (typ), SAVDD=0.8mA (typ).

Note 40. PLL Master Mode and LP bit = "0", fs=44.1kHz, PMADL = PMMICL= PMMICR= PMADR = PMDAL = PMDAR = PMLO1 = PMRO1 = PMLO2S = PMRO2S = PMLO3 = PMRO3 =PMSAD = PMVCM = PMPLL = M/S = PMMP bits = "1", MCKO = PMSRA = PMSRB = PMPCM bits = "0", MCKI=11.2896MHz.
AVDD=TBDmA (typ), PVDD=TBDmA (typ), DVDD=TBDmA (typ), TVDD2=TBDmA (typ), TVDD3=TBDmA (typ), SAVDD=TBDmA (typ).

Note 41. EXT Slave Mode and LP bit = "1", fs=8kHz, PMVCM = PMMP = PMMICL = PMADL = PMDAL = RCV = PMLO1 = PMRO1 = PMSRA = PMSRB = PMPCM = "1".
AVDD=3.2mA (typ), PVDD=0.8mA (typ), DVDD=2.7mA (typ), TVDD2=0mA (typ), TVDD3=0mA (typ), SAVDD=0mA (typ).

Note 42. Headphone-Amp & Speaker-Amp are powered-up.
(PMVCMA=PMOSC=PMCP=PMHPL=PMHPR=PMMHL=PMMHR=PMSPK=PMV1 bits= "1")

Note 43. Headphone-Amp is powered-up.
(PMVCMA=PMOSC=PMCP=PMHPL=PMHPR=PMMHL=PMMHR=PMV1 bits= "1", PMSPK bits= "0")

Note 44. Speaker-Amp is powered-up
(PMVCMA=PMOSC=PMCP=PMSPK bits= "1", PMHPL=PMHPR=PMMHL=PMMHR=PMV1 bits= "0")

Note 45. All digital input pins are fixed to each supply pin (DVDD, TVDD2 or TVDD3) or VSS4.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=3.3V; VSS1=VSS2=VSS3=VSS4=0V;
Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics (Down Sampling: SRC-A): SDTI → SRC-A → SDTOA/SDTOB					
Resolution		-	-	16	Bits
Input Sample Rate (Note 47)	FSI (fs)	8	-	48	kHz
Output Sample Rate (Note 47)	FSO (fs2)	-	8	-	kHz
THD+N (Input = 1kHz, −1dBFS, Note 46) FSO/FSI = 8kHz/44.1kHz		-	-94	-	dB
Dynamic Range (Input = 1kHz, −60dBFS, Note 46) FSO/FSI = 8kHz/44.1kHz		-	97	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6	-	1	-
SRC Characteristics (Up Sampling: SRC-B): SDTIA/SDTIB → SRC-B → SDTO					
Resolution		-	-	16	Bits
Input Sample Rate (Note 47)	FSI (fs2)	-	8	-	kHz
Output Sample Rate (Note 47)	FSO (fs)	8	-	48	kHz
THD+N (Input = 1kHz, −1dBFS, Note 46) FSO/FSI = 44.1kHz/8kHz		-	-95	-	dB
Dynamic Range (Input = 1kHz, −60dBFS, Note 46) FSO/FSI = 44.1kHz/8kHz		-	100	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1	-	6	-

Note 46. Measured by Audio Precision System Two Cascade.
Note 47. “fs” is the sampling frequency for Stereo CODEC. “fs2” is for PCM I/F.

ANALOG CHARACTERISTICS (10bit SAR ADC)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=3.3V; VSS1=VSS2=VSS3=VSS4=0V; unless otherwise specified)

Parameter	min	typ	max	Units
10bit SAR ADC Characteristics				
Resolution	-	10	-	Bits
No Missing Codes	9	10	-	Bits
Integral Linearity Error	-	-	±2	LSB
DNL	-	±1	-	LSB
Analog Input Voltage Range	0	-	SAVDD	V
Offset Error	-	-	±3	LSB
Gain Error	-	-	±2	LSB
Accuracy (Note 48)	-	-	±1	%

Note 48. Accuracy is the difference between the output code when 1.1V is input to SAIN1, SAIN2 or SAIN3 pin and the "ideal" code at 1.1V.

FILTER CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=PVDD=SAVDD=2.2 ~ 3.6V; DVDD=TVDD2=TVDD3=1.6 ~ 3.6V; fs=44.1kHz; Programmable Filter=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 49)	±0.16dB	PB	0	-	17.3	kHz
	−0.66dB		-	19.4	-	kHz
	−1.1dB		-	19.9	-	kHz
	−6.9dB		-	22.1	-	kHz
Stopband		SB	25.9	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 50)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
DAC Digital Filter (LPF):						
Passband (Note 49)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 50)		GD	-	19	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.4	-	dB

Note 49. The passband and stopband frequencies scale with fs (system sampling rate).
For example, DAC is PB=0.454 x fs (@−0.7dB). Each response refers to that of 1kHz.

Note 50. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC.
For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal.

FILTER CHARACTERISTICS (SRC)

(Ta=25°C; AVDD=PVDD=SAVDD=2.2 ~ 3.6V; DVDD=TVDD2=TVDD3=1.6 ~ 3.6V; fs2=8kHz; Programmable Filter=OFF)

Parameter		Symbol	min	typ	max	Units
Down Sampling (SRC-A): fs=8kHz						
Passband	±0.15dB	PB	0	-	3.0	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	5	-	ms
Down Sampling (SRC-A): fs=11.025kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	4	-	ms
Down Sampling (SRC-A): fs=12kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	4	-	ms
Down Sampling (SRC-A): fs=16kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=22.05kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=24kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms

Note 51. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Down Sampling (SRC-A): fs=32kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=44.1kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=48kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 51)		GD	-	3	-	ms

Note 51. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Up Sampling (SRC-B): fs=8kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=11.025kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=12kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=16kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=22.05kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=24kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms

Note 51. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Up Sampling (SRC-B): fs=32kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=44.1kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=48kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 51)		GD	-	2	-	ms

Note 51. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

DC CHARACTERISTICS (CODEC, SRC)

(Ta=25°C; AVDD=PVDD=SAVDD=2.2 ~ 3.6V; DVDD=TVDD2=TVDD3=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage 1	2.2V≤DVDD≤3.6V	VIH1	70%DVDD	-	-	V
(Note 52)	1.6V≤DVDD<2.2V	VIH1	80%DVDD	-	-	V
Low-Level Input Voltage 1	2.2V≤DVDD≤3.6V	VIL1	-	-	30%DVDD	V
(Note 52)	1.6V≤DVDD<2.2V	VIL1	-	-	20%DVDD	V
High-Level Input Voltage 2	2.2V≤TVDD2≤3.6V	VIH2	70%TVDD2	-	-	V
(Note 53)	1.6V≤TVDD2<2.2V	VIH2	80%TVDD2	-	-	V
Low-Level Input Voltage 2	2.2V≤TVDD2≤3.6V	VIL2	-	-	30%TVDD2	V
(Note 53)	1.6V≤TVDD2<2.2V	VIL2	-	-	20%TVDD2	V
High-Level Input Voltage 3	2.2V≤TVDD3≤3.6V	VIH3	70%TVDD3	-	-	V
(Note 54)	1.6V≤TVDD3<2.2V	VIH3	80%TVDD3	-	-	V
Low-Level Input Voltage 3	2.2V≤TVDD3≤3.6V	VIL3	-	-	30%TVDD3	V
(Note 54)	1.6V≤TVDD3<2.2V	VIL3	-	-	20%TVDD3	V
High-Level Output Voltage						
(Note 55, Iout=−200μA)		VOH1	DVDD−0.2	-	-	V
(Note 56, Iout=−200μA)		VOH2	TVDD2−0.2	-	-	V
(Note 57, Iout=−200μA)		VOH3	TVDD3−0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL1	-	-	0.2	V
(SDA pin, 2.0V≤DVDD≤3.6V: Iout=3mA)		VOL2	-	-	0.4	V
(SDA pin, 1.6V≤DVDD<2.0V: Iout=3mA)		VOL2	-	-	20%DVDD	V
Input Leakage Current						
(Note 58)		Iind	-	-	±2	μA
(Note 59)		Iina	-	-	±2	μA

Note 52. TEST5, SCL, SDA, TEST3, PDN, BICK, LRCK, SDTI, MCKI pins.
Note 53. BICKA, SYNCA, SDTIA pins.
Note 54. BICKB, SYNCB, SDTIB pins.
Note 55. MCKO, BICK, LRCK, SDTO, GPO1, GPO2 pins.
Note 56. BICKA, SYNCA, SDTOA pins.
Note 57. BICKB, SYNCB, SDTOB pins.
Note 58. SYNCB, BICKB, SDTIB, SDTI, LRCK, MCKI, BICK, SCL, SDA, SDTIA, BICKA, SYNCA pins. I/O pins (SYNCB, BICKB, LRCK, BICK, SDA, BICKA, SYNCA) are at the time of Input state.
Note 59. SAIN1, SAIN2, SAIN3 pins.

DC CHARACTERISTICS (HP/SPK-Amp)

(Ta= 25°C; AVDDA=PVDDA=2.6 ~ 3.6V; SVDDA=2.6 ~ 5.5V, TVDDA=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(2.2V≤TVDDA≤3.6V)	VIH4	70%TVDDA	-	-	V
(Note 60)	(1.6V≤TVDDA<2.2V)	VIH4	80%TVDDA	-	-	V
Low-Level Input Voltage	(2.2V≤TVDDA≤3.6V)	VIL4	-	-	30%TVDDA	V
(Note 60)	(1.6V≤TVDDA<2.2V)	VIL4	-	-	20%TVDDA	V
Input Leakage Current (Note 61)		Iin	-	-	±10	μA

Note 60. PDNA, MCKIA pins.
Note 61. Except the MCKIA pin. The MCKIA pin has internal pulled-down device, nominally 100kΩ.

SWITCHING CHARACTERISTICS (CODEC, SRC)

(Ta=25°C; AVDD=PVDD=SAVDD=2.2 ~ 3.6V; DVDD=TVDD2=TVDD3=1.6 ~ 3.6V; C_L=20pF (except SDA pin) or 400pF (SDA pin); unless otherwise specified)

Parameter		Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz		dMCK	40	50	60	%
256fs at fs=32kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	8	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	8	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	8	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	8	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = “0010”	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	13.312	MHz
	768fs	fCLK	6.144	-	19.968	MHz
	1024fs	fCLK	8.192	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs/384fs	fs	8	-	48	kHz
	512fs/768fs	fs	8	-	26	kHz
	1024fs	fs	8	-	13	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	13.312	MHz
	768fs	fCLK	6.144	-	19.968	MHz
	1024fs	fCLK	8.192	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	8	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
	BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BICK "↑" (Note 62)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BICK "↓" (Note 63)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
BICK "↑" to SDTO (BCKP bit = "0")	tBSD	–70	-	70	ns
BICK "↓" to SDTO (BCKP bit = "1")	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK "↑" to BICK "↑" (Note 62)	tLRB	0.4 x tBCK	-	-	ns
LRCK "↑" to BICK "↓" (Note 63)	tLRB	0.4 x tBCK	-	-	ns
BCLK "↑" to LRCK "↑" (Note 62)	tBLR	0.4 x tBCK	-	-	ns
BICK "↓" to LRCK "↑" (Note 63)	tBLR	0.4 x tBCK	-	-	ns
BICK "↑" to SDTO (BCKP bit = "0")	tBSD	-	-	80	ns
BICK "↓" to SDTO (BCKP bit = "1")	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Audio Interface Timing (Right/Left justified & I^2S)					
Master Mode					
BICK "↓" to LRCK Edge (Note 64)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 64)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 64)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 62. MSBS, BCKP bits = "00" or "11".
Note 63. MSBS, BCKP bits = "01" or "10".
Note 64. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKA, SYNCA, SDTIA, SDTOA pins; Slave Mode):					
SYNCA Timing					
Frequency	fs2	-	8	-	kHz
Serial Interface Timing at Short/long Frame Sync					
BICKA Frequency	fBCK2	128	-	2048	kHz
BICKA Period	tBCK2	488	-	-	ns
BICKA Pulse Width Low	tBCKL2	200	-	-	ns
Pulse Width High	tBCKH2	200	-	-	ns
SYNCA Edge to BICKA "↑" (Note 65)	tSYB2	50	-	-	ns
SYNCA Edge to BICKA "↓" (Note 66)	tSYB2	50	-	-	ns
BICKA "↑" to SYNCA Edge (Note 65)	tBSY2	50	-	-	ns
BICKA "↓" to SYNCA Edge (Note 66)	tBSY2	50	-	-	ns
SYNCA to SDTOA (MSB) (Except Short Frame)	tSYD2	-	-	80	ns
BICKA "↑" to SDTOA (BCKPA bit = "0")	tBSD2	-	-	80	ns
BICKA "↓" to SDTOA (BCKPA bit = "1")	tBSD2	-	-	80	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Pulse Width Low	tSYL2	0.8 x tBCK2	-	-	ns
Pulse Width High	tSYH2	0.8 x tBCK2	-	-	ns
Serial Interface Timing at MSB justified and I^2S					
BICKA Frequency	fBCK2	256	-	2048	kHz
BICKA Period	tBCK2	488	-	-	ns
BICKA Pulse Width Low	tBCKL2	200	-	-	ns
Pulse Width High	tBCKH2	200	-	-	ns
SYNCA Edge to BICKA "↑"	tSYB2	50	-	-	ns
BICKA "↑" to SYNCA Edge	tBSY2	50	-	-	ns
SYNCA to SDTOA (MSB) (Except I^2S mode)	tSYD2	-	-	80	ns
BICKA "↓" to SDTOA	tBSD2	-	-	80	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDH2	50	-	-	ns
SYNCA Duty Cycle	dSYC2	45	50	55	%

Note 65. MSBSA, BCKPA bits = "00" or "11".
Note 66. MSBSA, BCKPA bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKA, SYNCA, SDTIA, SDTOA pins; Master Mode):					
SYNCA Timing					
Frequency	fs2	-	8	-	kHz
BICKA Timing					
Period (BCKO2 bit = "0")	tBCK2	-	1/(16fs2)	-	kHz
(BCKO2 bit = "1")	tBCK2	-	1/(32fs2)	-	kHz
Duty Cycle	dBCK2	-	50	-	%
Serial Interface Timing at Short/long Frame Sync					
SYNCA Edge to BICKA "↑" (Note 65)	tSYB2	0.5 x tBCK2 – 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
SYNCA Edge to BICKA "↓" (Note 66)	tSYB2	0.5 x tBCK2 – 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
BICKA "↑" to SDTOA (BCKPA bit = "0")	tBSD2	–70	-	70	ns
BICKA "↓" to SDTOA (BCKPA bit = "1")	tBSD2	–70	-	70	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Pulse Width High	tSYH2	-	tBCK2	-	ns
Serial Interface Timing at MSB justified and I^2S					
BICKA "↓" to SYNCA Edge	tBSY2	–40	-	40	ns
SYNCA to SDTOA (MSB) (Except I^2S mode)	tSYD2	–70	-	70	ns
BICKA "↓" to SDTOA	tBSD2	–70	-	70	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDH2	50	-	-	ns
SYNCA Duty Cycle	dSYC2	-	50	-	%

Note 65. MSBSA, BCKPA bits = "00" or "11".
Note 66. MSBSA, BCKPA bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKB, SYNCB, SDTIB, SDTOB pins; Slave Mode):					
SYNCB Timing					
Frequency	fs2	-	8	-	kHz
Serial Interface Timing at Short/long Frame Sync					
BICKB Frequency	fBCK3	128	-	2048	kHz
BICKB Period	tBCK3	488	-	-	ns
BICKB Pulse Width Low	tBCKL3	200	-	-	ns
Pulse Width High	tBCKH3	200	-	-	ns
SYNCB Edge to BICKB "↑" (Note 67)	tSYB3	50	-	-	ns
SYNCB Edge to BICKB "↓" (Note 68)	tSYB3	50	-	-	ns
BICKB "↑" to SYNCB Edge (Note 67)	tBSY3	50	-	-	ns
BICKB "↓" to SYNCB Edge (Note 68)	tBSY3	50	-	-	ns
SYNCB to SDTOB (MSB) (Except Short Frame)	tSYD3	-	-	80	ns
BICKB "↑" to SDTOB (BCKPB bit = "0")	tBSD3	-	-	80	ns
BICKB "↓" to SDTOB (BCKPB bit = "1")	tBSD3	-	-	80	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Pulse Width Low	tSYL3	0.8 x tBCK2	-	-	ns
Pulse Width High	tSYH3	0.8 x tBCK2	-	-	ns
Serial Interface Timing at MSB justified and I^2S					
BICKB Frequency	fBCK3	256	-	2048	kHz
BICKB Period	tBCK3	488	-	-	ns
BICKB Pulse Width Low	tBCKL3	200	-	-	ns
Pulse Width High	tBCKH3	200	-	-	ns
SYNCB Edge to BICKB "↑"	tSYB3	50	-	-	ns
BICKB "↑" to SYNCB Edge	tBSY3	50	-	-	ns
SYNCB to SDTOB (MSB) (Except I^2S mode)	tSYD3	-	-	80	ns
BICKB "↓" to SDTOB	tBSD3	-	-	80	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDH3	50	-	-	ns
SYNCB Duty Cycle	dSYC3	45	50	55	%

Note 67. MSBSB, BCKPB bits = "00" or "11".
Note 68. MSBSB, BCKPB bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKB, SYNCB, SDTIB, SDTOB pins; Master Mode):					
SYNCB Timing					
Frequency	fs2	-	8	-	kHz
BICKB Timing					
Period (BCKO2 bit = "0")	tBCK2	-	1/(16fs2)	-	kHz
(BCKO2 bit = "1")	tBCK2	-	1/(32fs2)	-	kHz
Duty Cycle	dBCK2	-	50	-	%
Serial Interface Timing at Short/long Frame Sync					
SYNCB Edge to BICKB "↑" (Note 67)	tSYB3	0.5 x tBCK2 – 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
SYNCB Edge to BICKB "↓" (Note 68)	tSYB3	0.5 x tBCK2 – 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
BICKB "↑" to SDTOB (BCKPB bit = "0")	tBSD3	–70	-	70	ns
BICKB "↓" to SDTOB (BCKPB bit = "1")	tBSD3	–70	-	70	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Pulse Width High	tSYH3	-	tBCK2	-	ns
Serial Interface Timing at MSB justified and I^2S					
BICKB "↓" to SYNCB Edge	tBSY3	–40	-	40	ns
SYNCB to SDTOB (MSB) (Except I^2S mode)	tSYD3	–70	-	70	ns
BICKB "↓" to SDTOB	tBSD3	–70	-	70	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDH3	50	-	-	ns
SYNCB Duty Cycle	dSYC3	-	50	-	%

Note 67. MSBSB, BCKPB bits = "00" or "11".
Note 68. MSBSB, BCKPB bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 69)					
SCL Clock Frequency (Note 70)	fSCL	30	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 71)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 72)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 73)	tPDV	-	1059	-	1/fs
PMSRA "↑" to SDTOA valid (Note 74)	tPDV2	-	21	-	1/fs2
PMSRB "↑" to SDTO valid (Note 75)	tPDV3	-	135	-	1/fs

Note 69. I^2C is a registered trademark of Philips Semiconductors.

Note 70. In case that SAR ADC data is read out via I^2C bus, SCL should be input corresponding 2 byte data including ACK (Figure 110).

Note 71. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 72. CODEC & SRC blocks of the AK4675 can be reset by bringing PDN pin = "L" to "H" only upon power up

Note 73. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1" when PMSRB bit = "0".

Note 74. The signal path is SDTI → SRC-A → SDTOA and PLLBT is locked.

Note 75. The signal path is SDTIA → SRC-B → SDTO.

SWITCHING CHARACTERISTICS (HP/SPK-Amp)

(Ta= 25°C; AVDDA=PVDDA=2.6 ~ 3.6V; SVDDA=2.6 ~ 5.5V; TVDDA=1.6 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
MCKIA Input Timing (OSCN bit = "1")					
Frequency	fCLK	2.048	-	3.072	MHz
Pulse Width Low	fCLKL	0.4/fCLK	-	-	ns
Pulse Width High	fCLKH	0.4/fCLK	-	-	ns
Power-down & Reset Timing					
PDNA Pulse Width (Note 76)	tPD	150	-	-	ns

Note 76. HP/SPK-Amp blocks can be reset by power up of the AK4675 when the PDNA pin = "L".

■ Timing Diagram (CODEC, SRC)

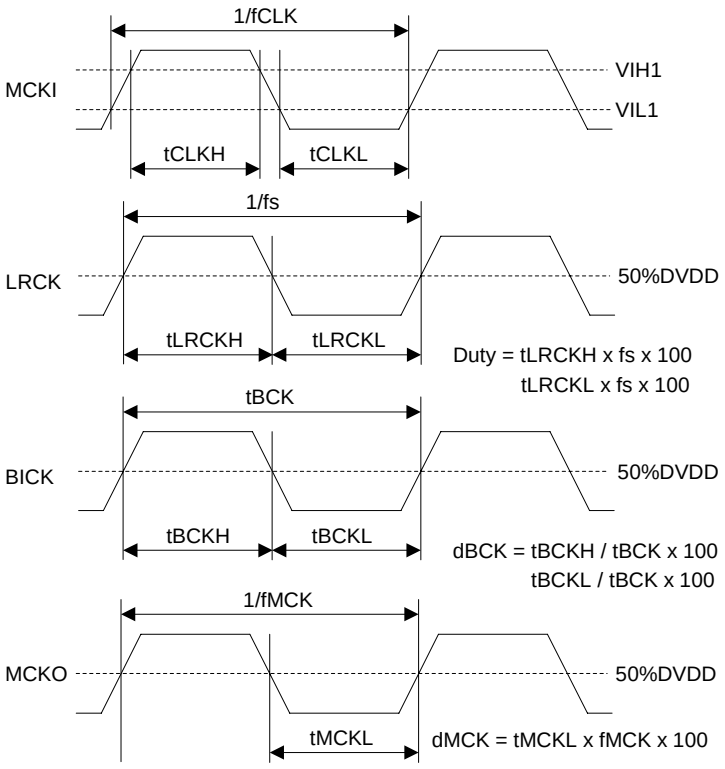


Figure 4. Clock Timing (PLL/EXT Master mode)
Note 77. MCKO is not available at EXT Master mode.

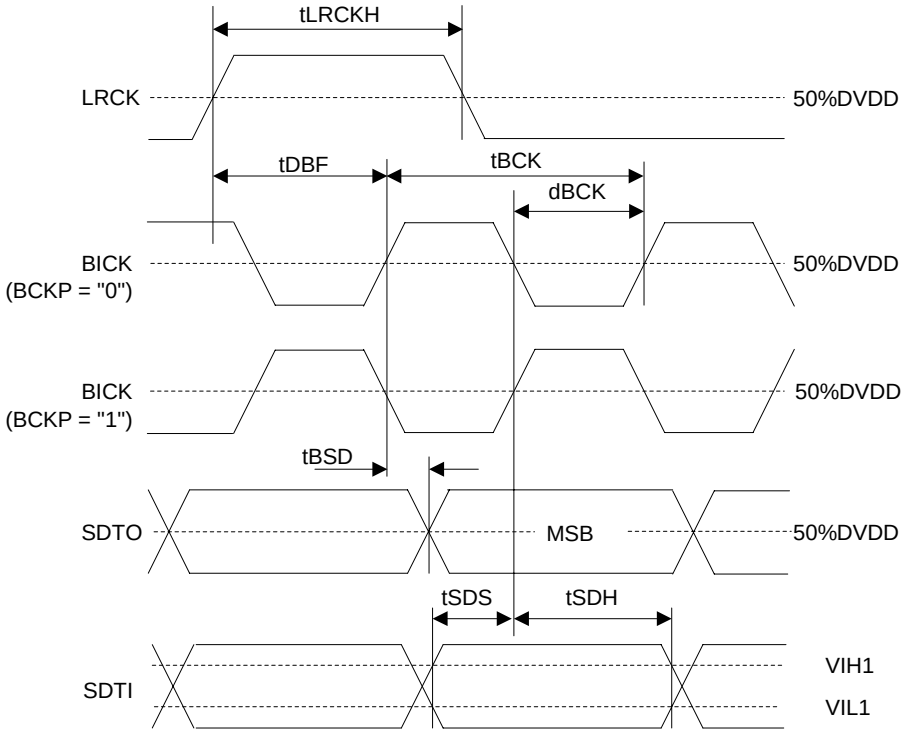


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “0”)

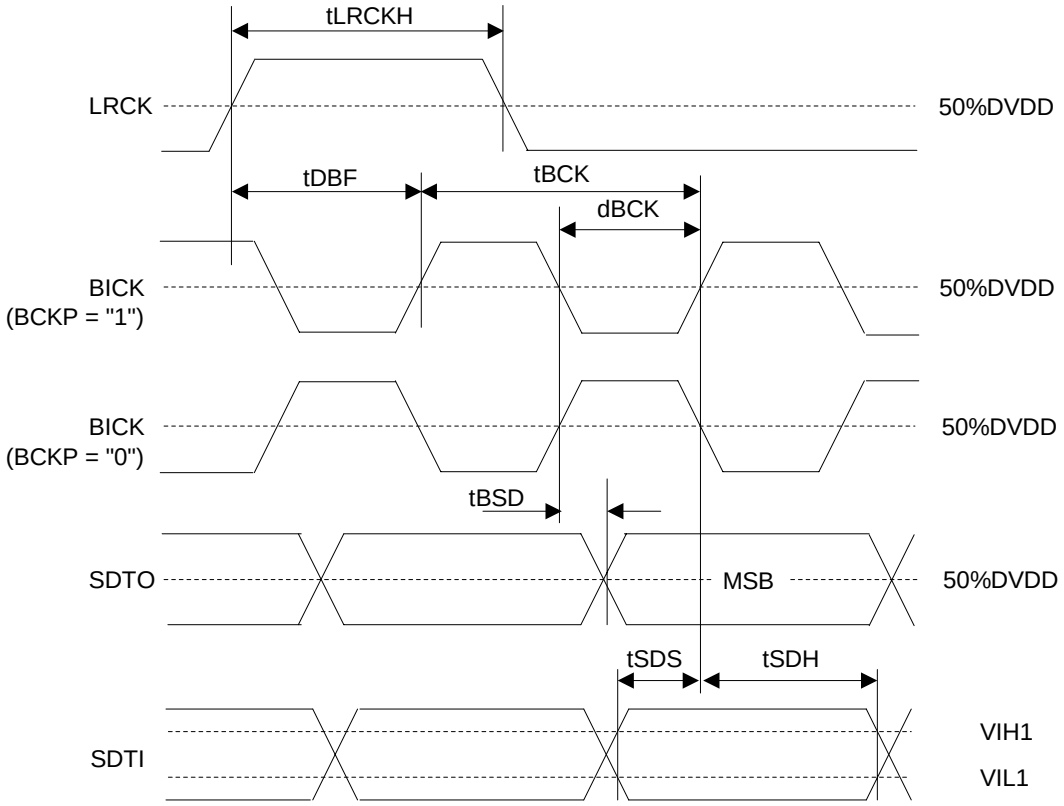


Figure 6. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

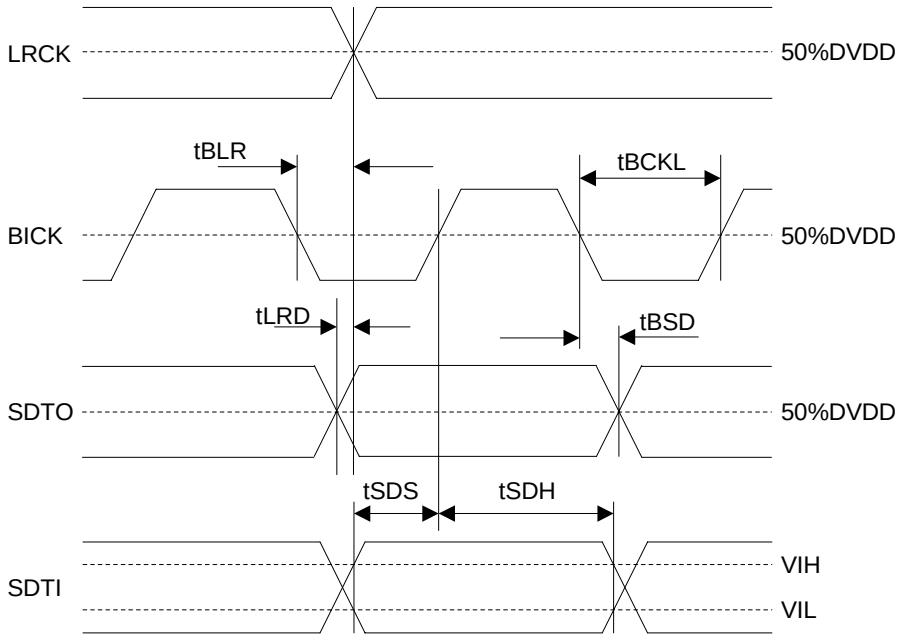


Figure 7. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

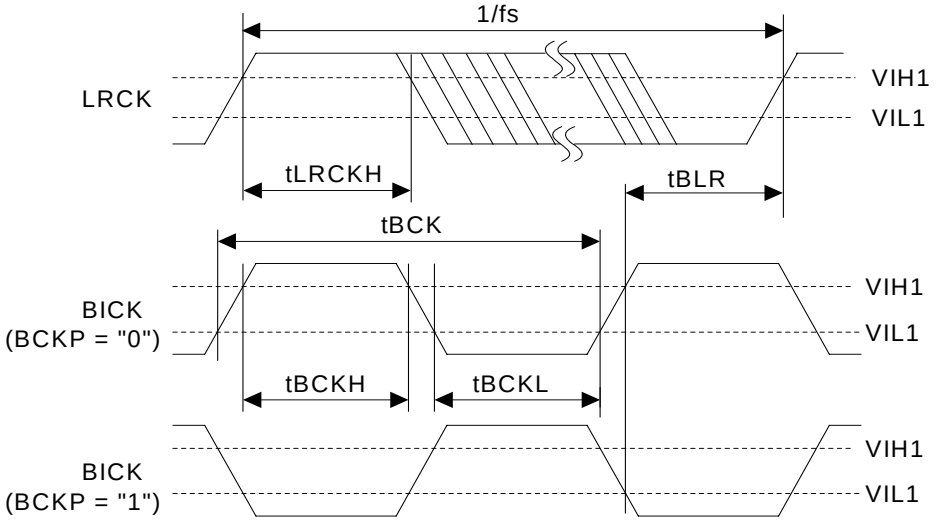


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “0”)

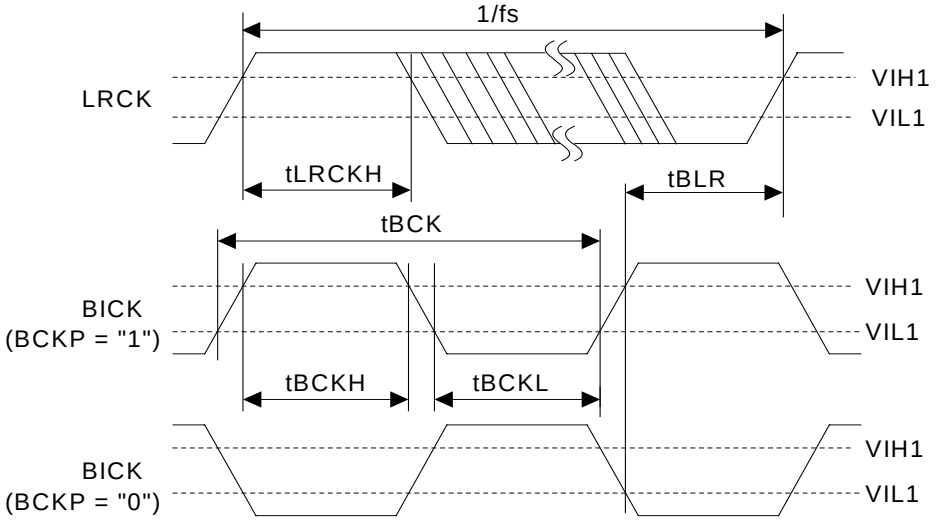


Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = “1”)

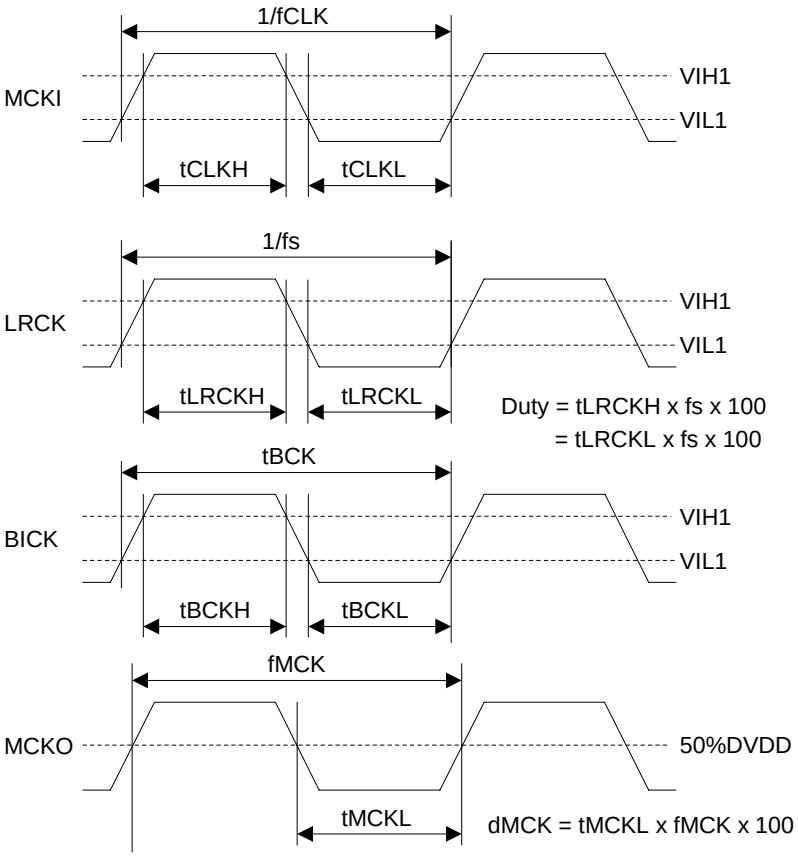


Figure 10. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin, Except DSP mode)

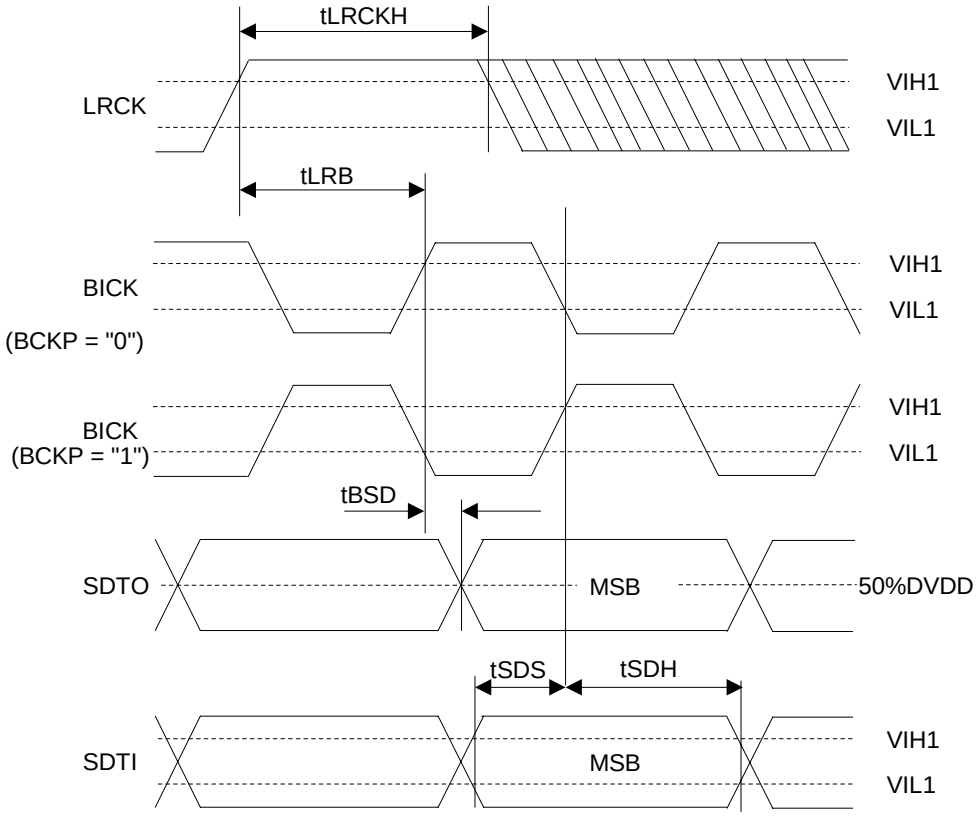


Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = “0”)

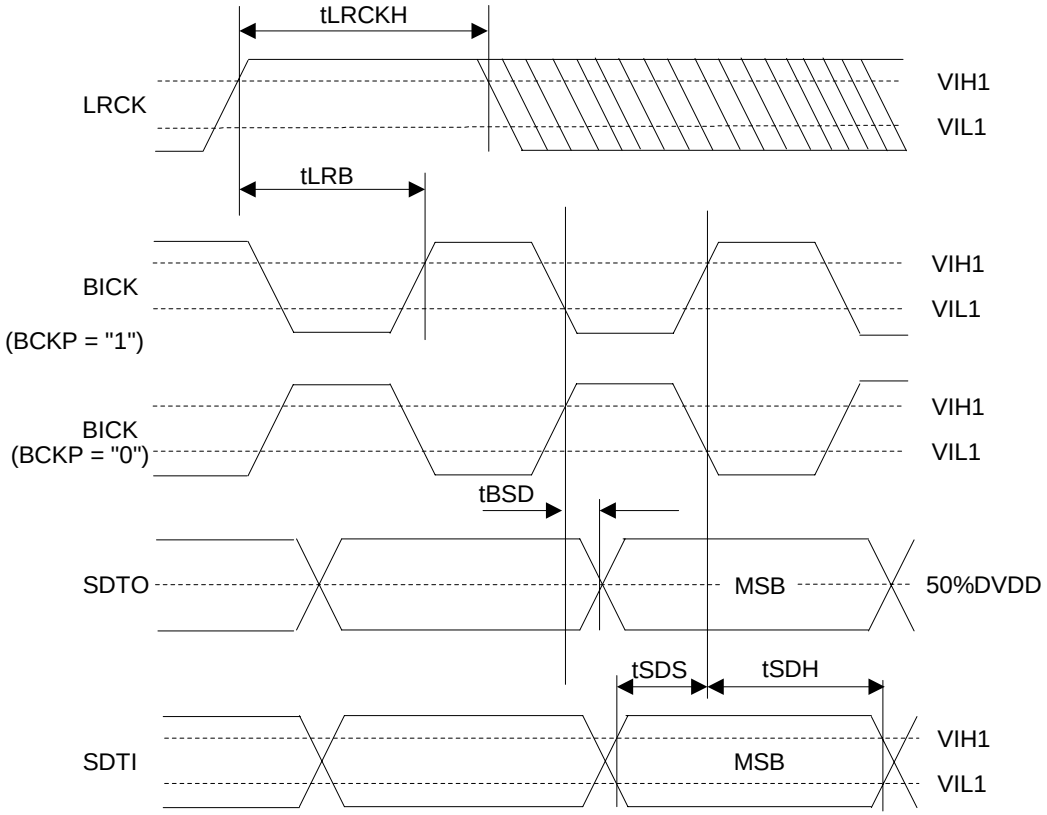


Figure 12. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = "1")

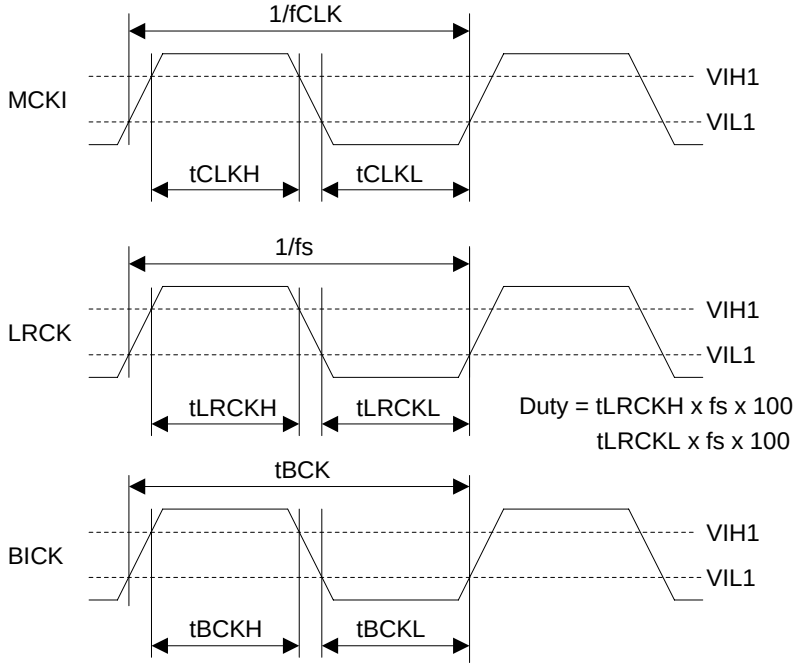


Figure 13. Clock Timing (EXT Slave mode)

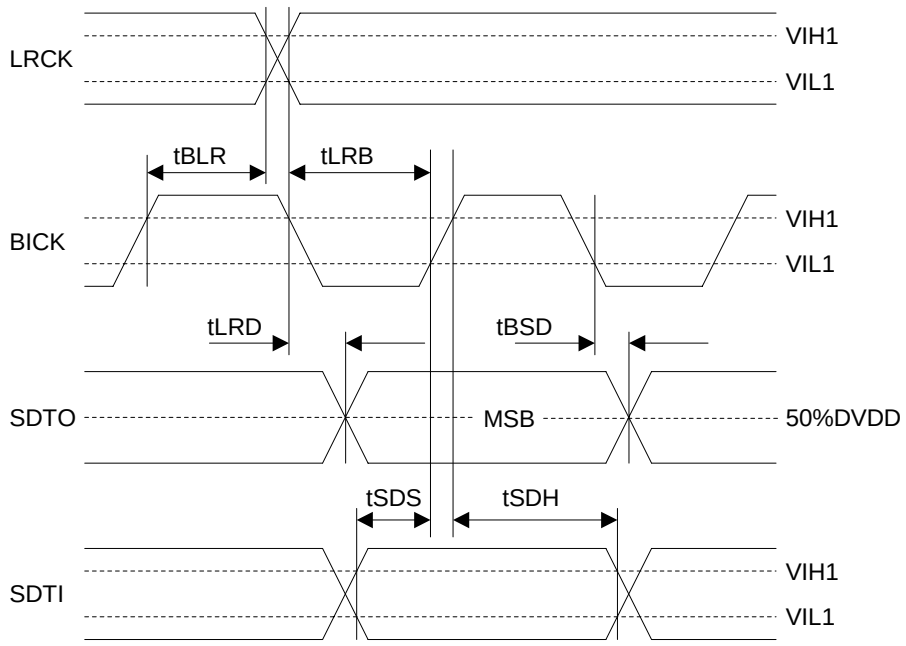


Figure 14. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

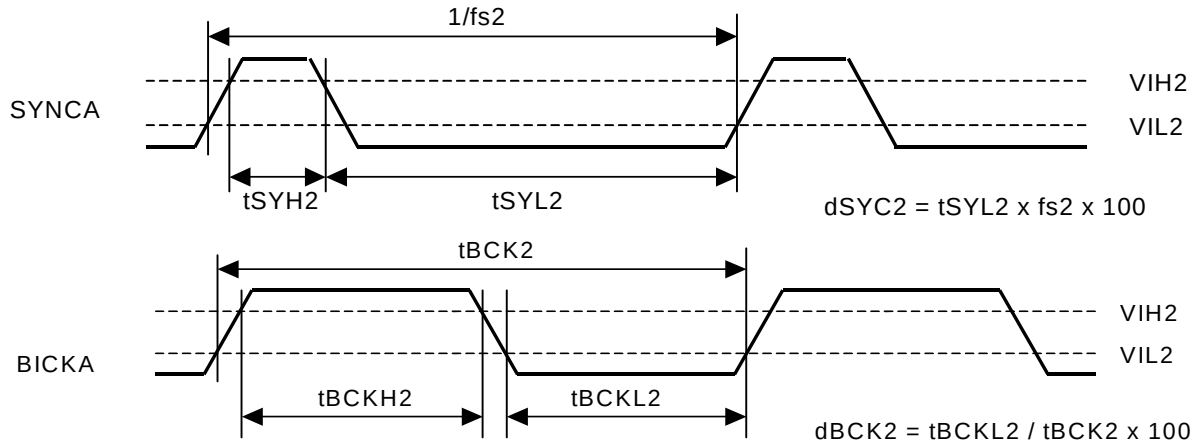


Figure 15. Clock Timing of PCM I/F A (SYNCA, BICKA)

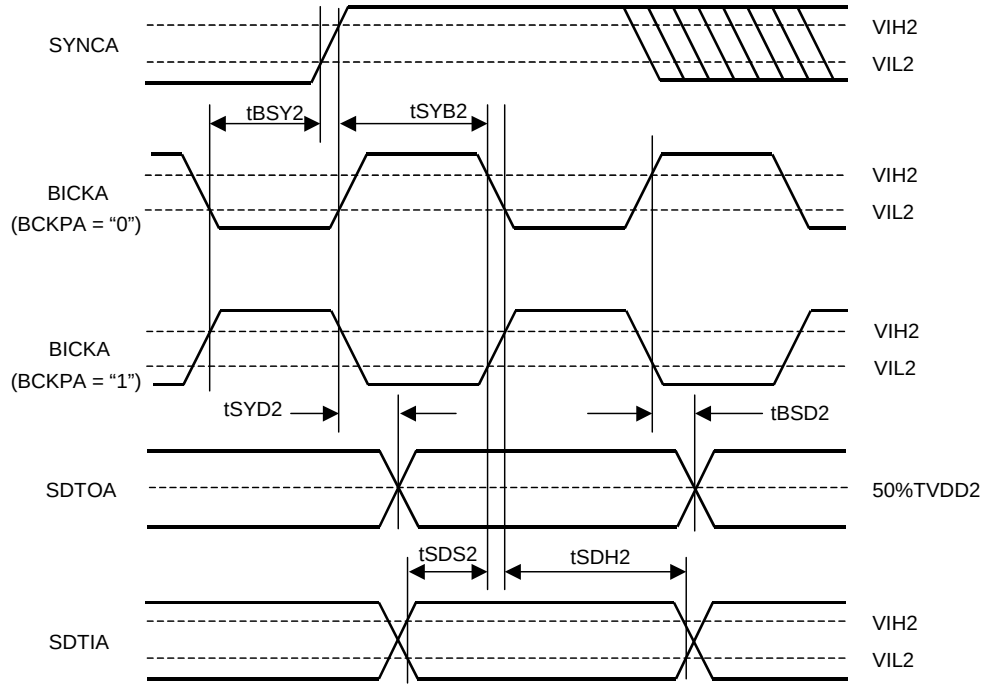


Figure 16. PCM I/F A Timing at short and long frame sync (SYNCA, BICKA, SDTOA, SDTIA)

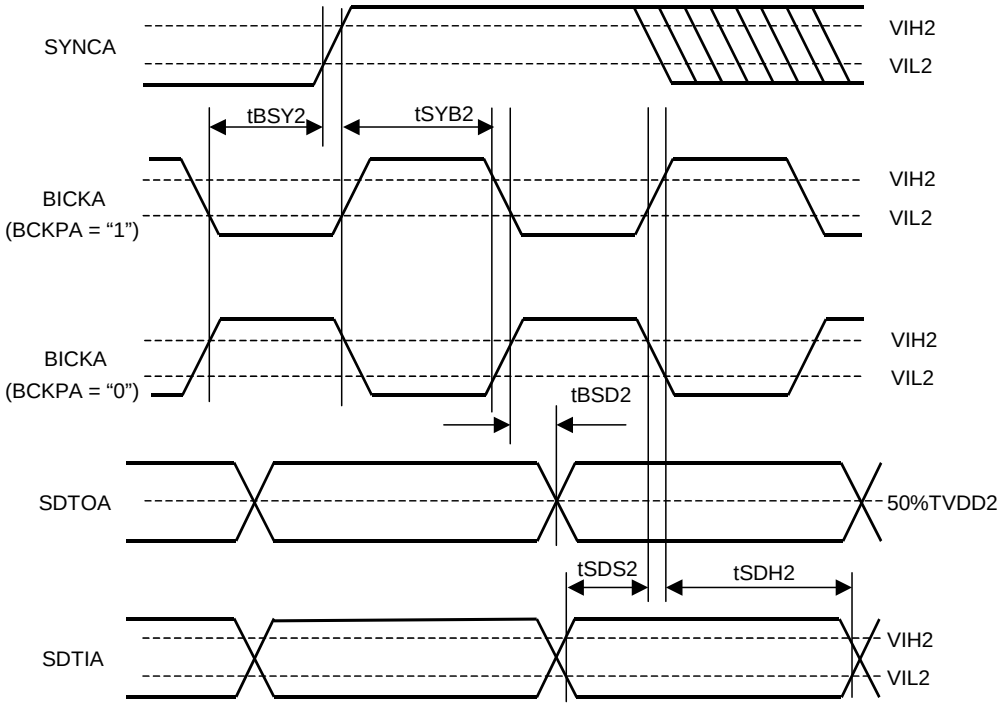


Figure 17. PCM I/F B Timing at MSB justified and I^2S (SYNCA, BICKA, SDTOA, SDTIA)

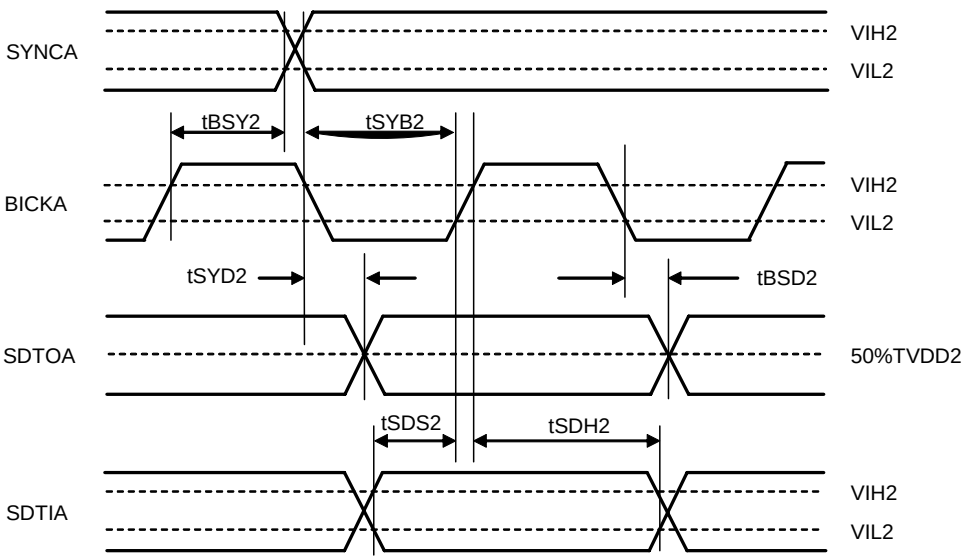


Figure 18. PCM I/F A Timing at MSB justified and I^2S (Slave mode)

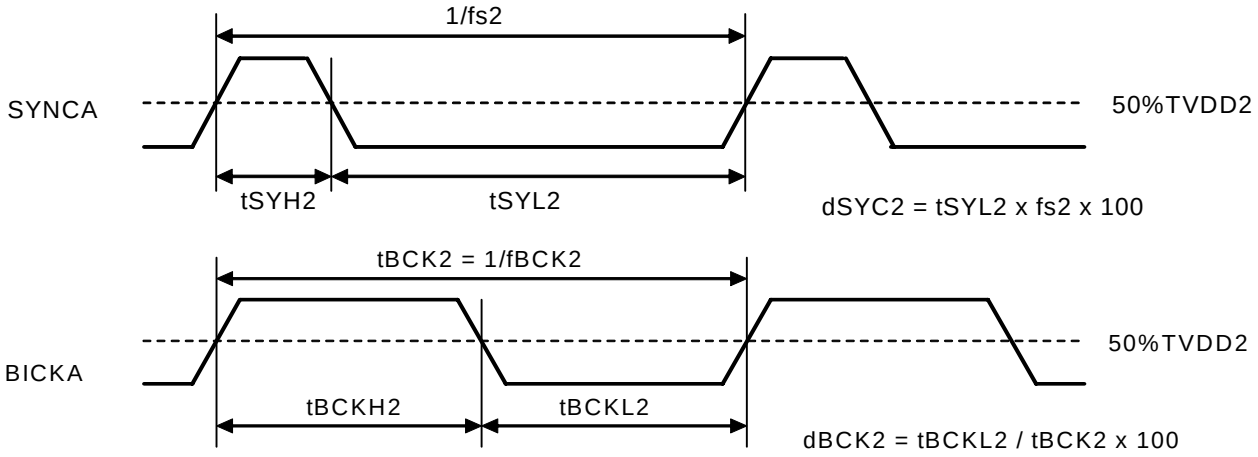


Figure 19. Clock Timing of PCM I/F A (Master mode)

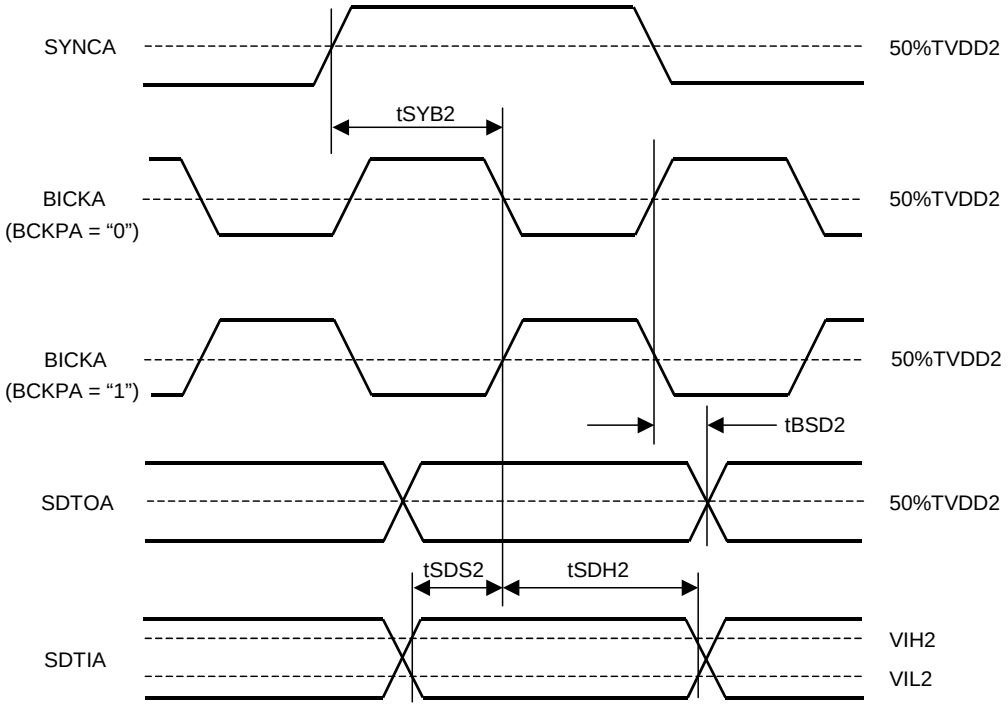


Figure 20. PCM I/F A Timing at short and long frame sync (Master mode; MSBSA = "0")

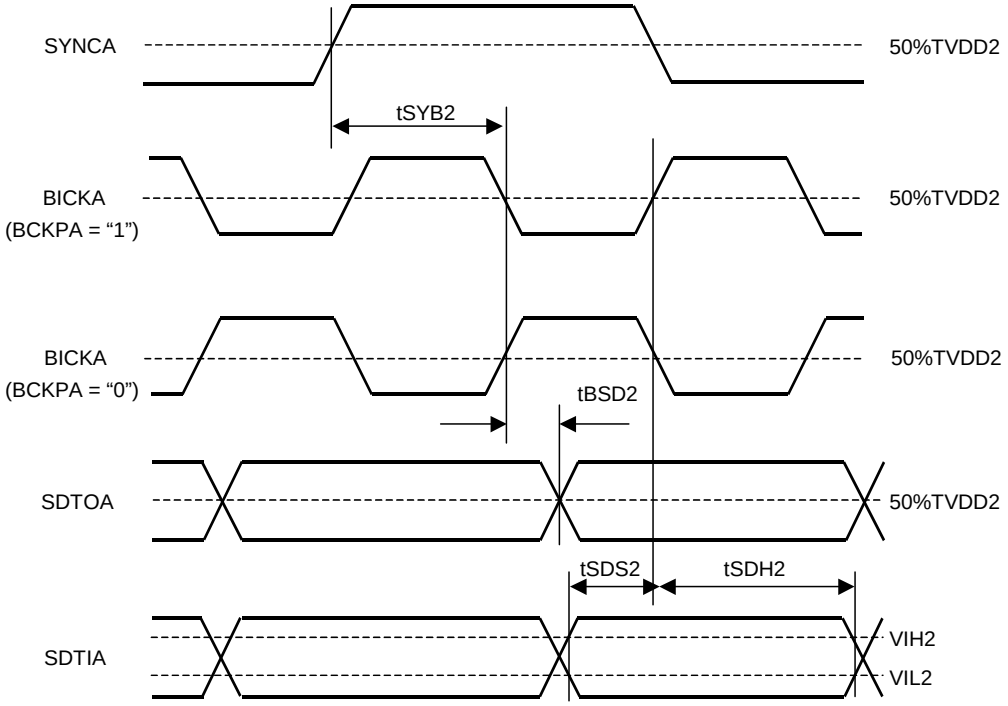


Figure 21. PCM I/F A Timing at short and long frame sync (Master mode; MSBSA = "1")

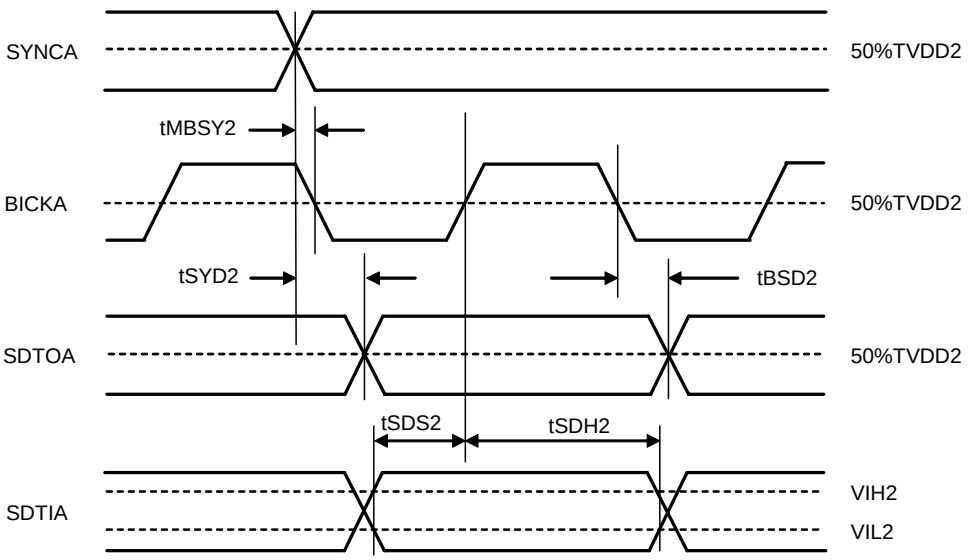


Figure 22. PCM I/F A Timing at MSB justified and I^2S (Master mode)

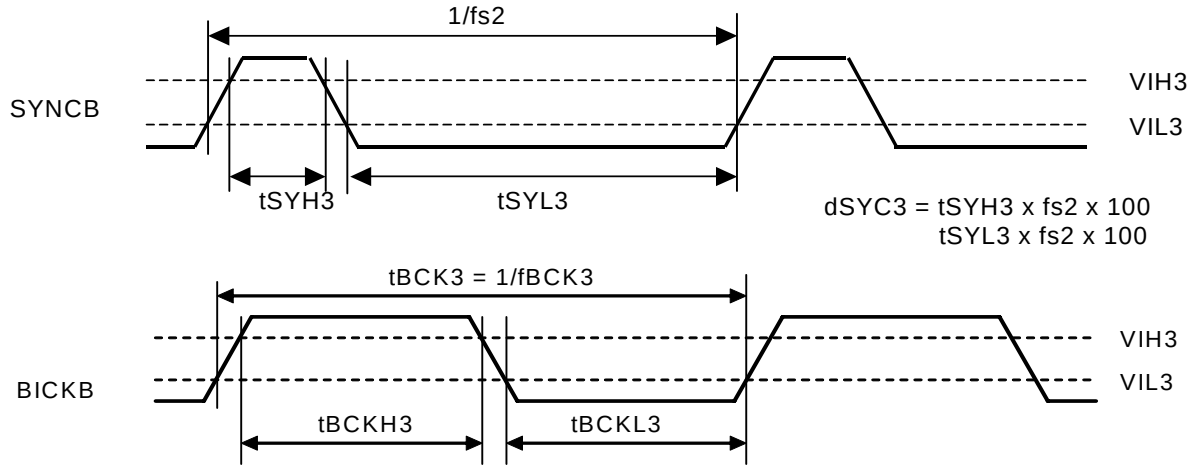


Figure 23. Clock Timing of PCM I/F B (Slave mode)

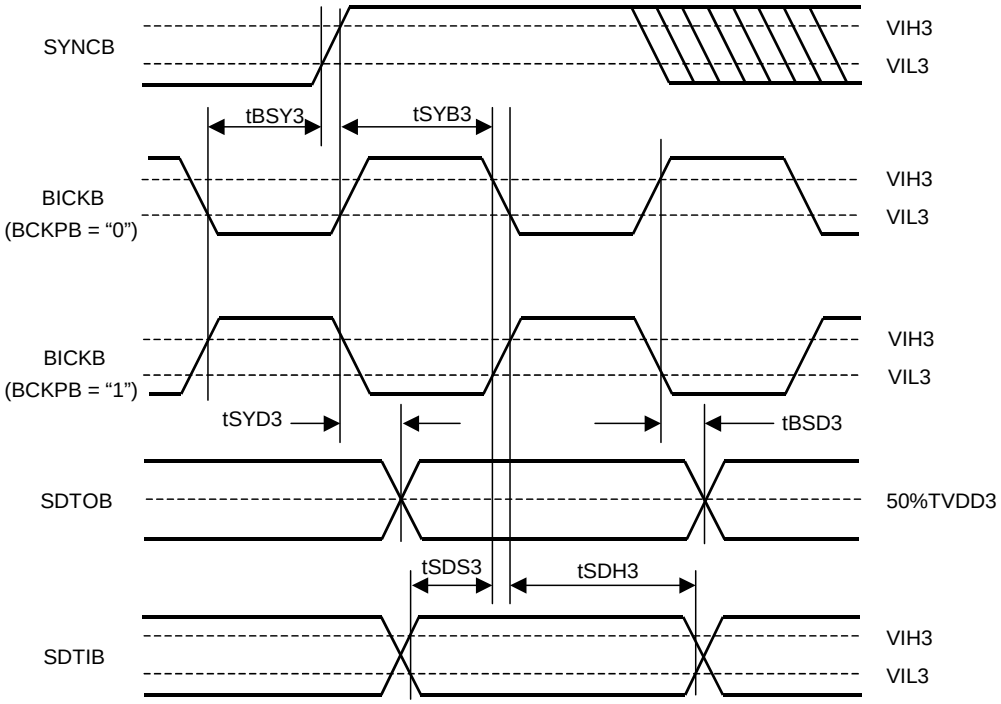


Figure 24. PCM I/F B Timing at short and long frame sync (Slave mode; MSBSB = "0")

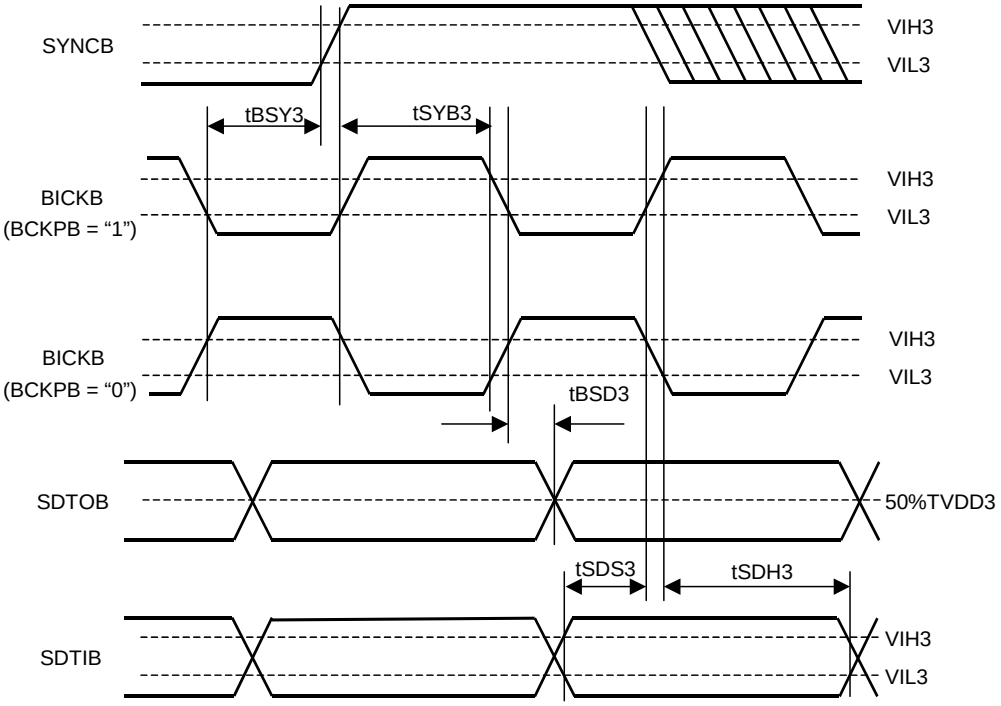


Figure 25. PCM I/F B Timing at MSB justified and I^2S (Slave mode; MSBSB = "1")

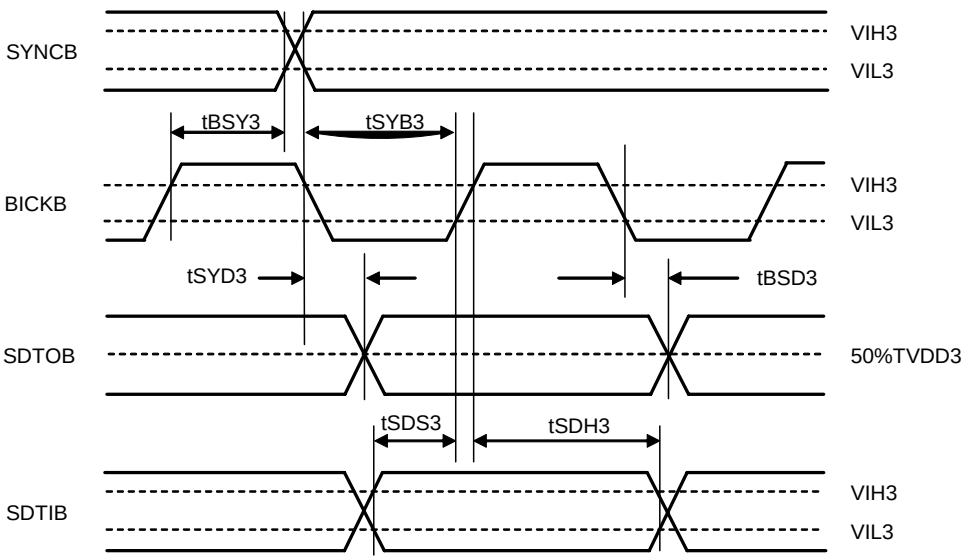


Figure 26. PCM I/F B Timing at MSB justified and I^2S (Slave mode)

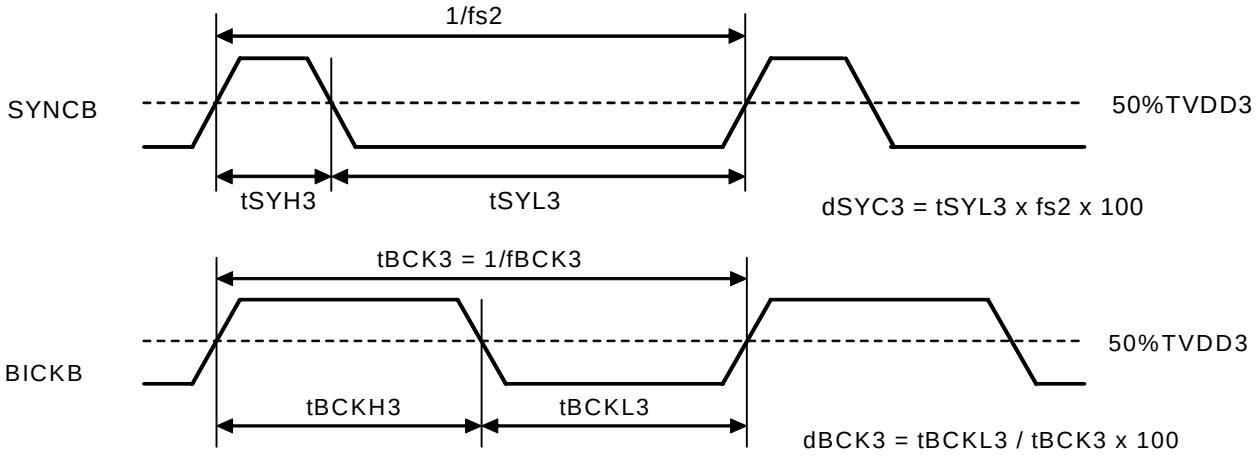


Figure 27. Clock Timing of PCM I/F B (Master mode)

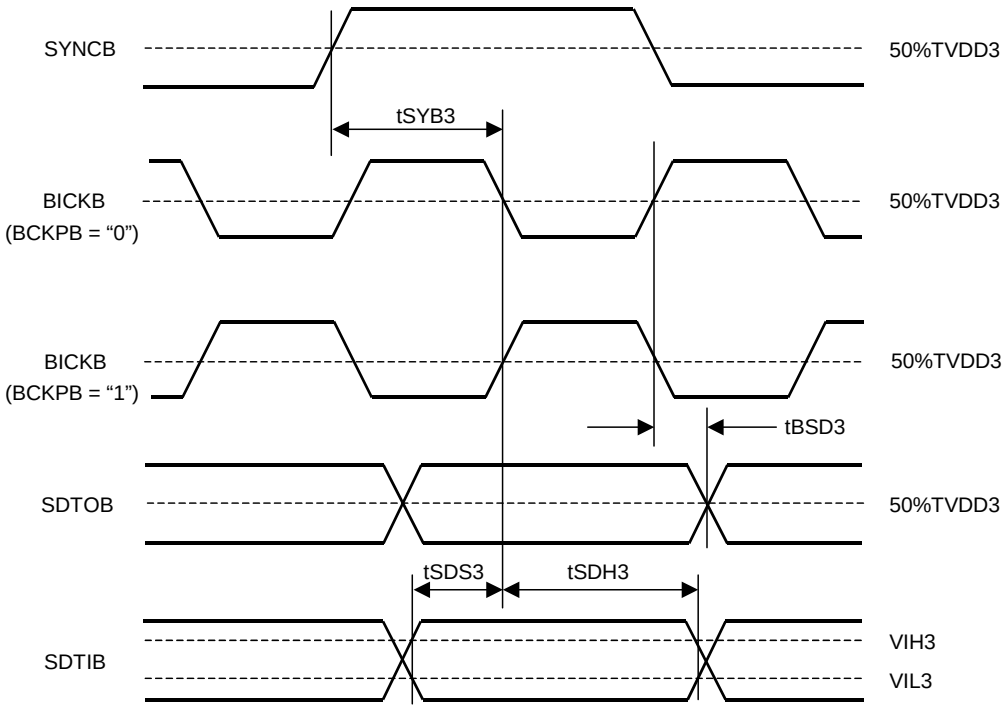


Figure 28. PCM I/F B Timing at short and long frame sync (Master mode; MSBSB = "0")

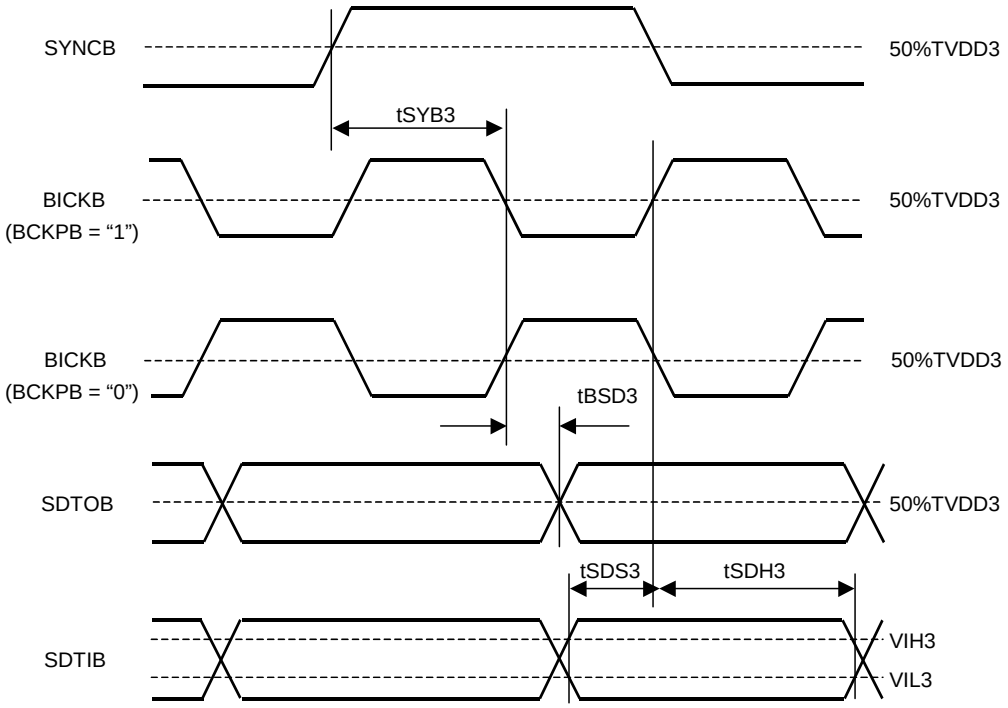


Figure 29. PCM I/F B Timing at short and long frame sync (Master mode; MSBSB = "1")

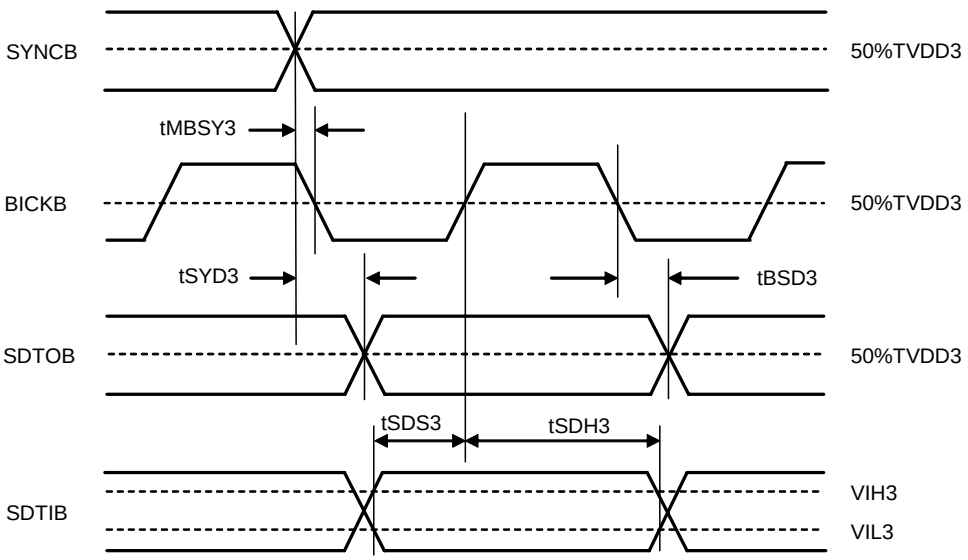


Figure 30. PCM I/F B Timing at MSB justified and I^{2}S (Master mode)

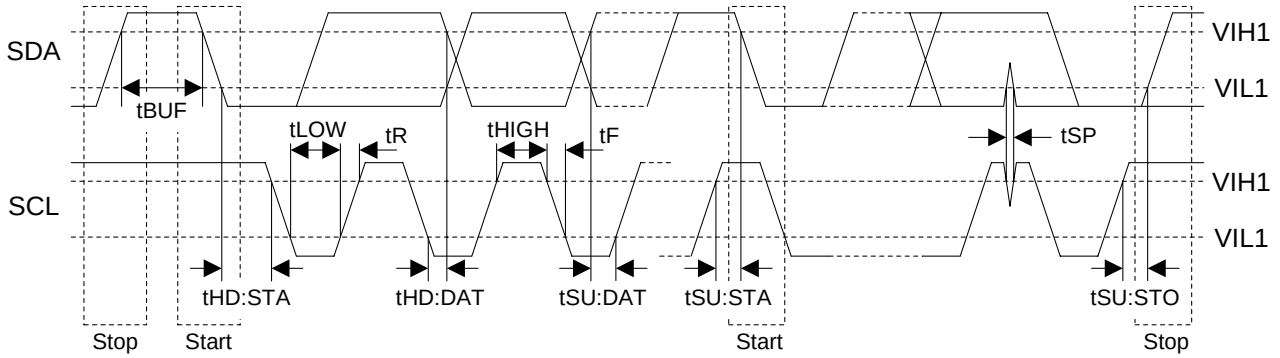


Figure 31. I^{2}C Bus Mode Timing

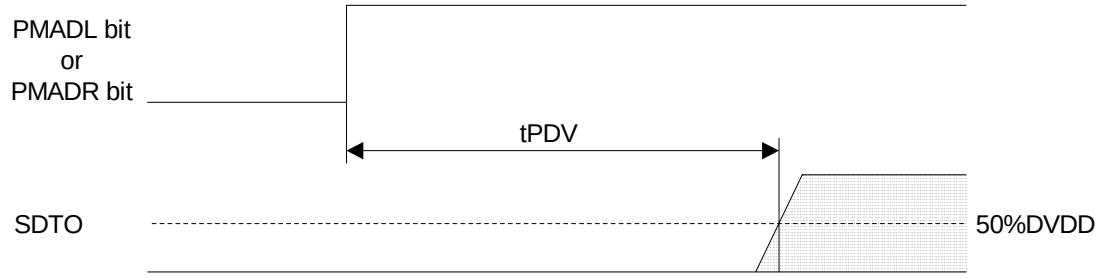


Figure 32. Power Down & Reset Timing 1

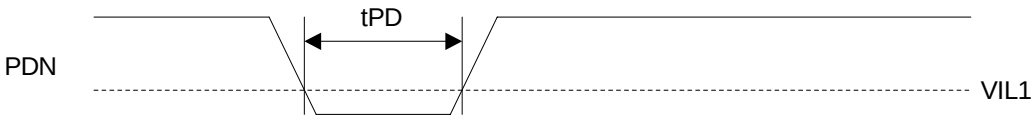


Figure 33. Power Down & Reset Timing 2

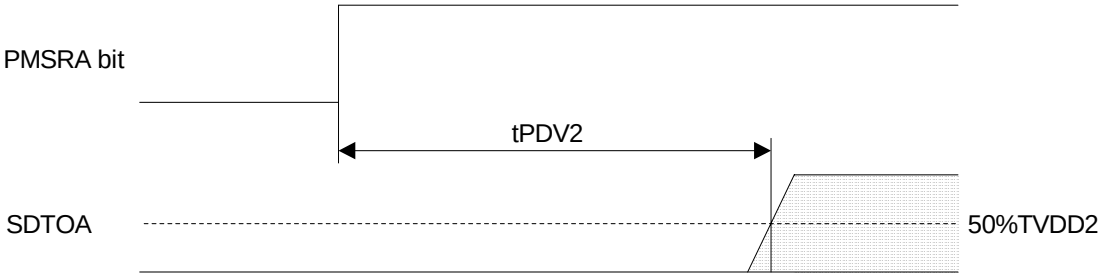


Figure 34. Power Down & Reset Timing 3

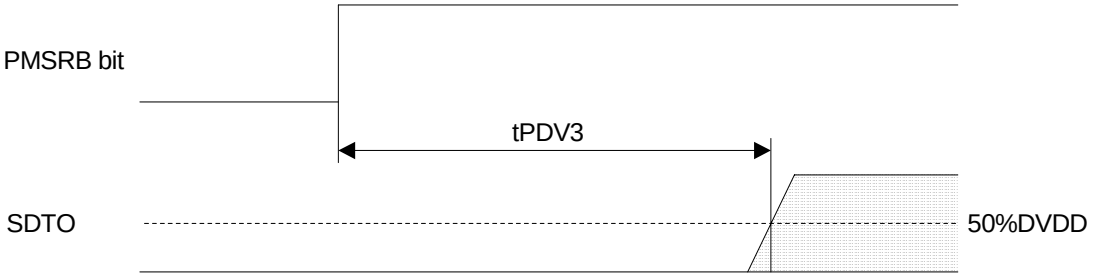


Figure 35. Power Down & Reset Timing 4

■ Timing Diagram (HP/SPK-Amp)

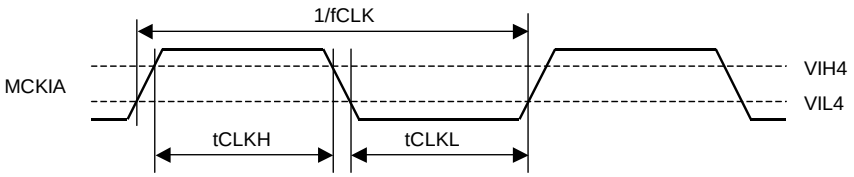


Figure 36. MCKIA Input Timing

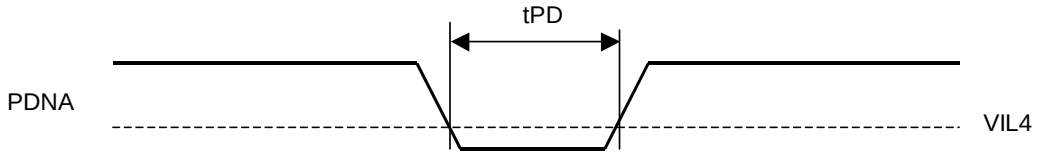


Figure 37. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock (Audio I/F)

There are the following five clock modes to interface with external devices. (Table 1 and Table 2.)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 78)	1	1	See Table 4	Figure 38
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 39
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	See Table 4	Figure 40 Figure 41
EXT Slave Mode	0	0	x	Figure 42
EXT Master Mode	0	1	x	Figure 43

Note 78. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	"L"	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	"L"	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	"L"	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	0	"L"	Selected by FS1-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	"L"	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4675 is power-down mode (PDN pin = "L") and exits reset state, the AK4675 is in slave mode. After exiting reset state, the AK4675 goes to master mode by changing M/S bit = "1".

When the AK4675 is in master mode, LRCK and BICK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK4675 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = "1")

When PMPLL bit is "1", an integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, when the AK4675 is supplied stable clock after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency is changed. When AIN3 bit = "1", the PLL is not available.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	10n	40ms	(default)
7	0	1	1	1	MCKI pin	24MHz	10k	10n	40ms	
8	1	0	0	0	MCKI pin	19.2MHz	10k	4.7n	40ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
14	1	1	1	0	MCKI pin	13MHz	10k	220n	60ms	
15	1	1	1	1	MCKI pin	26MHz	10k	220n	60ms	
Others	Others				N/A					

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
5	0	1	0	1	11.025kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
15	1	1	1	1	44.1kHz	(default)
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = MCKI pin)

When PLL reference clock input is LRCK or BICK pin, the sampling frequency is selected by FS3-2 bits (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	Don't care	Don't care	8kHz ≤ fs ≤ 12kHz	
1	0	1	Don't care	Don't care	12kHz < fs ≤ 24kHz	
2	1	Don't care	Don't care	Don't care	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins go to "L" and irregular frequency clock is output from the MCKO pins at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin goes to "L". (Table 7)

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 9	See Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL, DACR, DACH and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

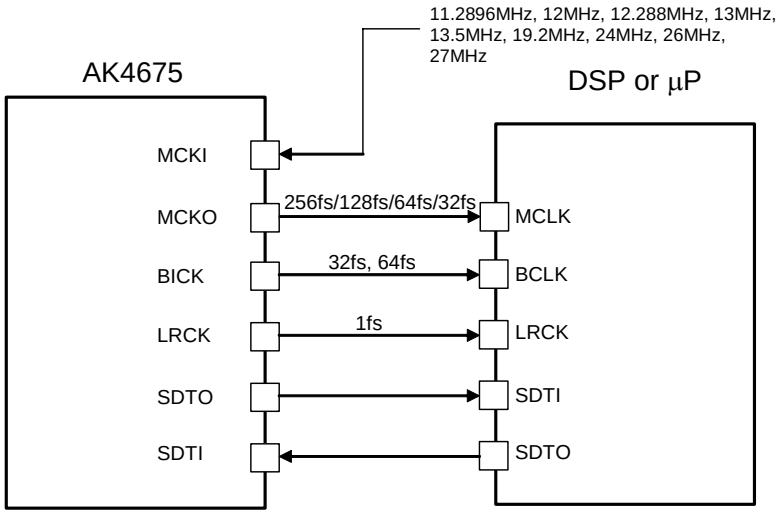


Figure 38. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Frequency (PLL mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock to the AK4675 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

In case that the CODEC is used without Audio I/F (like phone call), the CODEC can be operated by MCKI only. In this case, BICK and LRCK can be stopped.

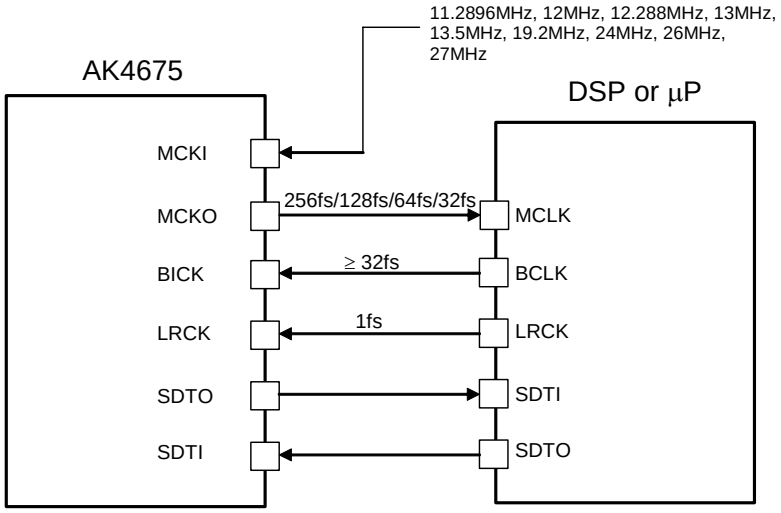


Figure 39. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits. (Table 6)

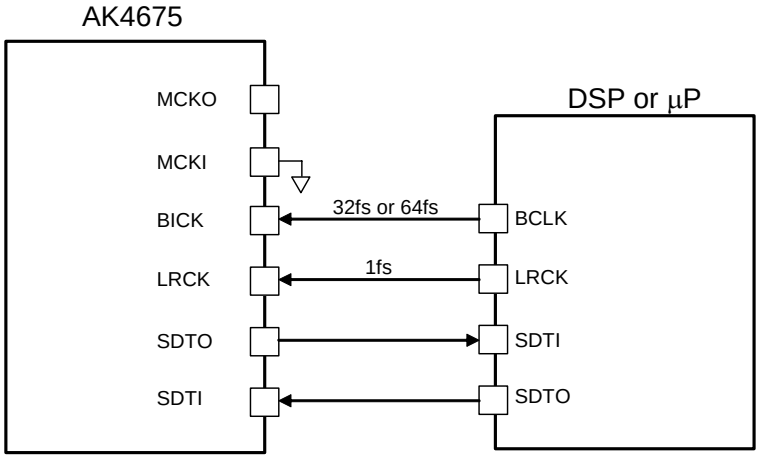


Figure 40. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

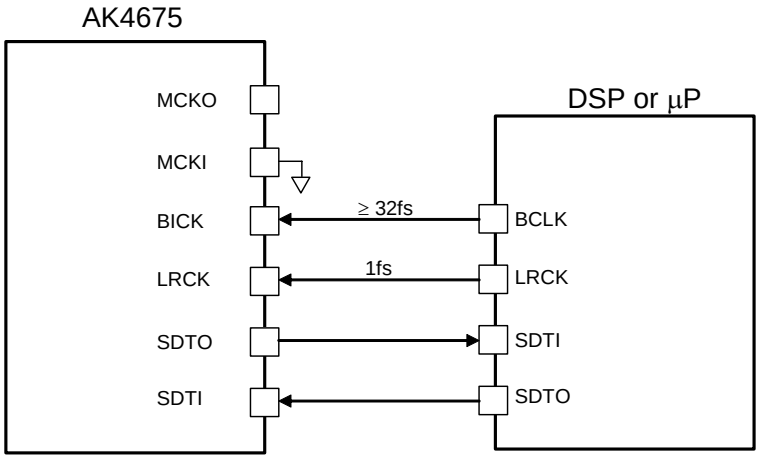


Figure 41. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1", PMDAL bit = "1" or PMDAR bit = "1"). If MCKI is not provided, the AK4675 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4675 becomes EXT mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 384fs, 512fs, 768fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

In case that the CODEC is used without Audio I/F (like phone call), the CODEC can be operated by MCKI only. In this case, BICK and LRCK can be stopped.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	0	256fs	8kHz ~ 48kHz	
1	x	0	0	1	1024fs	8kHz ~ 13kHz	
4	x	1	0	0	384fs	8kHz ~ 48kHz	
5	x	1	0	1	768fs	8kHz ~ 26kHz	
6	x	1	1	0	512fs	8kHz ~ 26kHz	
7	x	1	1	1	256fs	8kHz ~ 48kHz	(default)
Others	Others				N/A	N/A	

(N/A: Not available, x: Don't care)

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 12. Relationship between MCKI and S/N of LOUT1/ROUT1 pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1", PMDAL bit = "1" or PMDAR bit = "1"). If these clocks are not provided, the AK4675 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = "0").

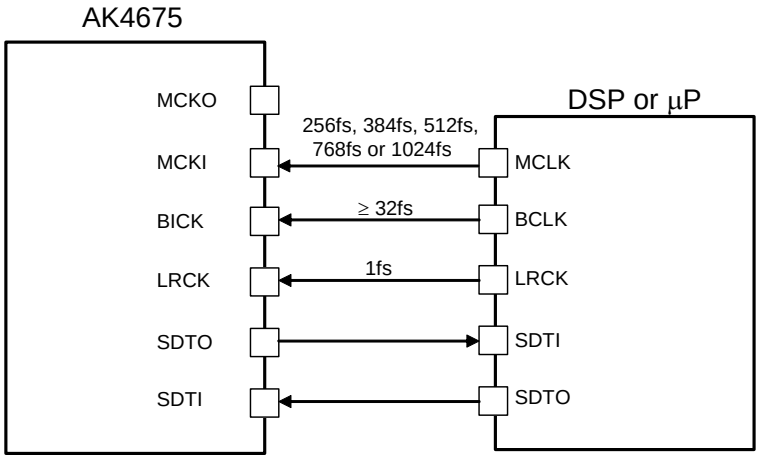


Figure 42. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4675 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 384fs, 512fs, 768fs or 1024fs). The input frequency of MCKI is selected by FS2-0 bits (Table 13).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	0	256fs	8kHz ~ 48kHz	
1	x	0	0	1	1024fs	8kHz ~ 13kHz	
4	x	1	0	0	384fs	8kHz ~ 48kHz	
5	x	1	0	1	768fs	8kHz ~ 26kHz	
6	x	1	1	0	512fs	8kHz ~ 26kHz	
7	x	1	1	1	256fs	8kHz ~ 48kHz	(default)
Others	Others				N/A	N/A	

(N/A: Not available, x: Don't care)

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through the LOUT/ROUT pins at fs=8kHz is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 14. Relationship between MCKI and S/N of LOUT1/ROUT1 pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1", PMDAL bit = "0" or PMDAR bit = "1"). If MCKI is not provided, the AK4675 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = "0").

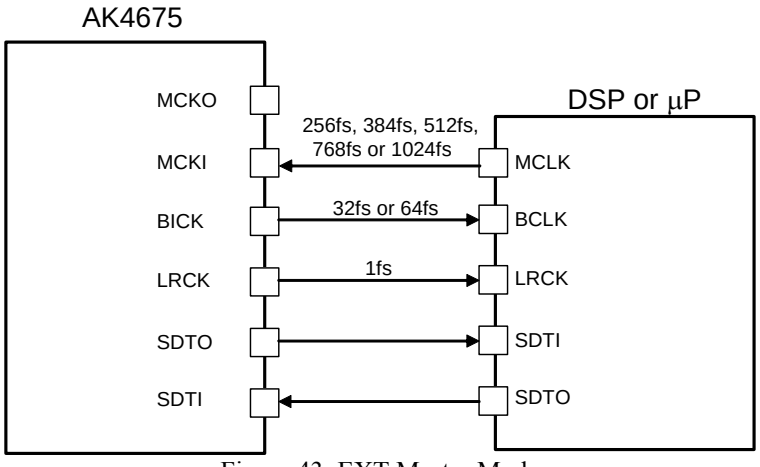


Figure 43. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 15. BICK Output Frequency at Master Mode

■ System Reset

The PDNA pin must keep “L” until all power supply pins are supplied, and must be set to “H”. After exiting reset (PDNA pin: “L” → “H”), all blocks of HP/SPK-Amp blocks (Input Volume, VCOMA, Oscillator, Mixer, Headphone-Amp, Speaker-Amp and charge pump circuit) switch to the power-down state. The contents of the control register are maintained until this reset by the PDNA pin.

Upon power-up, CODEC & SRC blocks of the AK4675 must be reset by bringing the PDN pin = “L”. This ensures that all internal registers of CODEC & SRC blocks reset to their initial values.

The ADC enters initialization cycle when the PMADL or PMADR bit is changed from “0” to “1” if PMDAL and PMDAR bits are “0”. The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During initialization cycle, the ADC digital data outputs of both channels are forced to a 2’s complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When PMDAL or PMDAR is “1”, the ADC does not require an initialization cycle.

■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits (Table 16). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4675 in master mode, but must be input to the AK4675 in slave mode.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	DSP Mode	DSP Mode	≥ 32fs	Table 17	
1	0	1	MSB justified	LSB justified	≥ 32fs	Figure 48	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 49	(default)
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 50	

Table 16. Audio Interface Format

In modes 1-3, the SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑").

In Modes 0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 17).

DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure	
0	0	0	0	MSB of SDTO is output by the rising edge ("↑") of the first BICK after the rising edge ("↑") of LRCK. MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB.	Figure 44	(default)
		0	1	MSB of SDTO is output by the falling edge ("↓") of the first BICK after the rising edge ("↑") of LRCK. MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB.	Figure 45	
		1	0	MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BICK after the rising edge ("↑") of LRCK. MSB of SDTI is latched by the falling edge ("↓") of the BICK just after the output timing of SDTO's MSB.	Figure 46	
		1	1	MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BICK after the rising edge ("↑") of LRCK. MSB of SDTI is latched by the rising edge ("↑") of the BICK just after the output timing of SDTO's MSB.	Figure 47	

Table 17. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

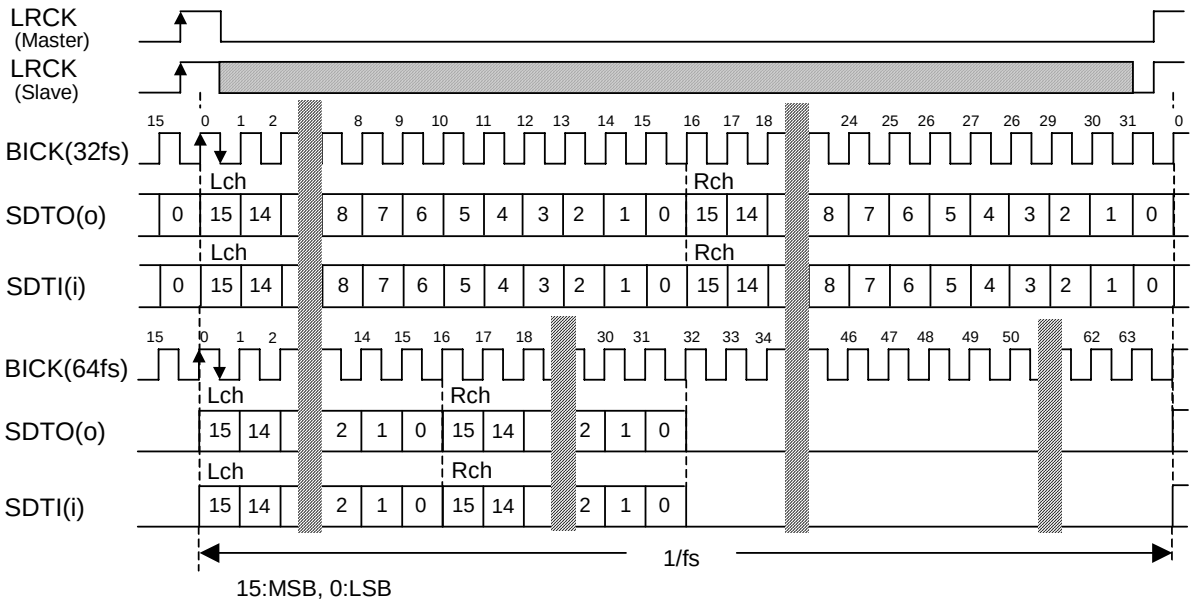


Figure 44. Mode 0 Timing (BCKP = "0", MSBS = "0")

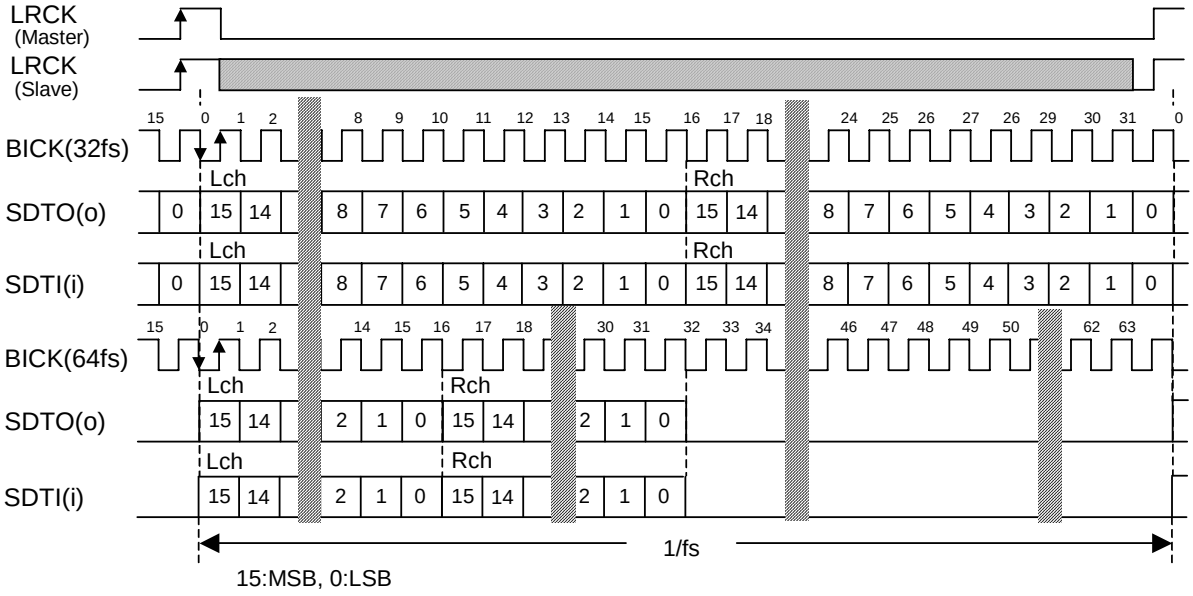


Figure 45. Mode 0 Timing (BCKP = "1", MSBS = "0")

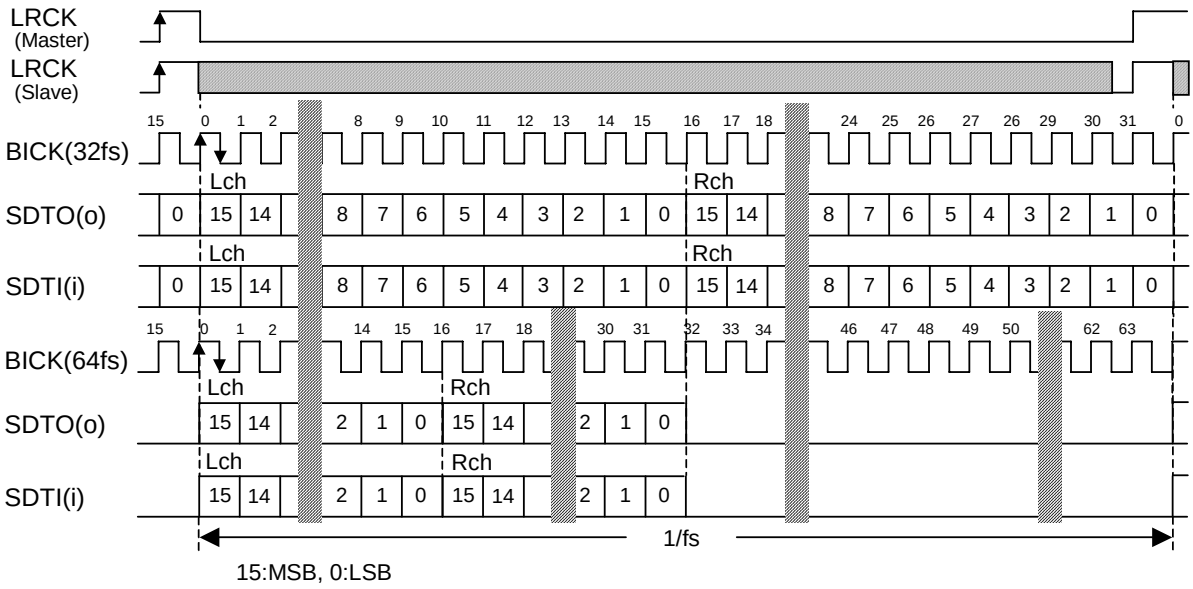


Figure 46. Mode 0 Timing (BCKP = "0", MSBS = "1")

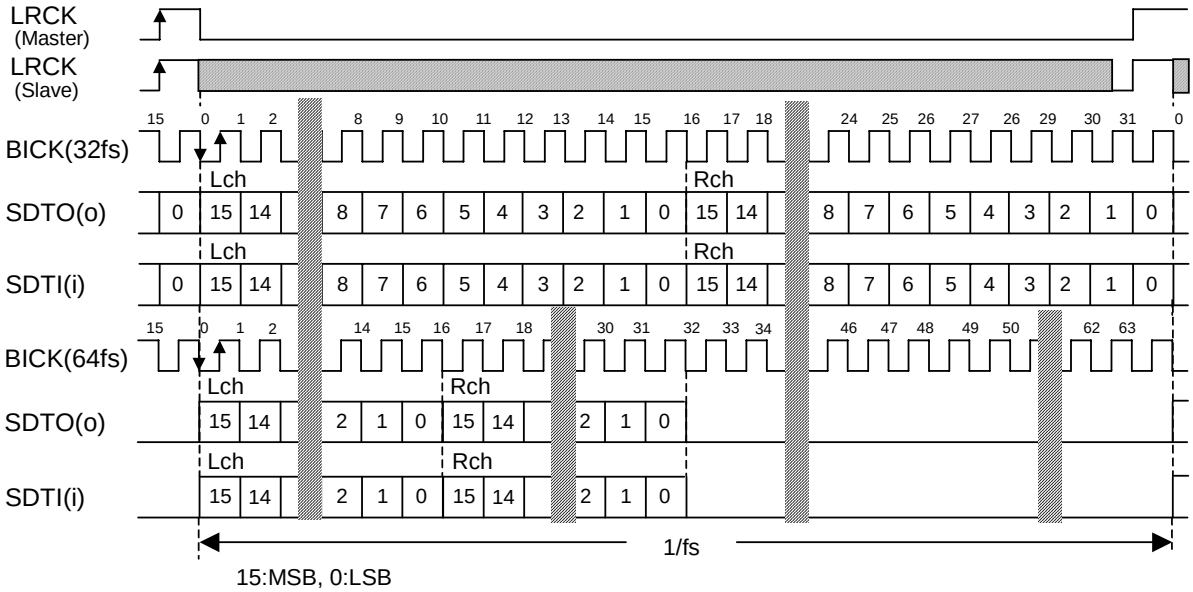


Figure 47. Mode 0 Timing (BCKP = "1", MSBS = "1")

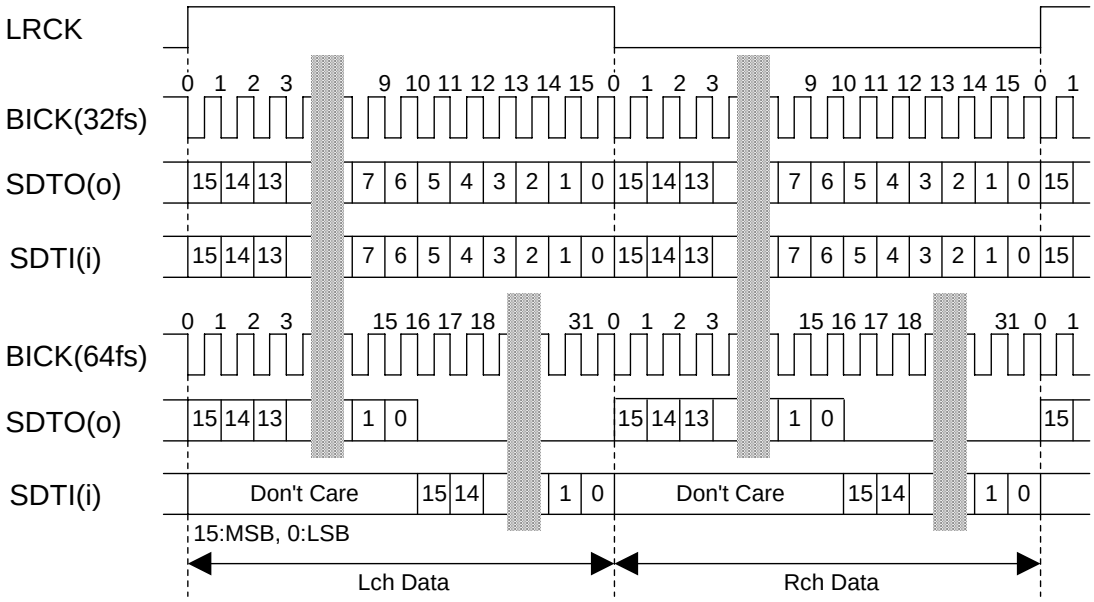


Figure 48. Mode 1 Timing

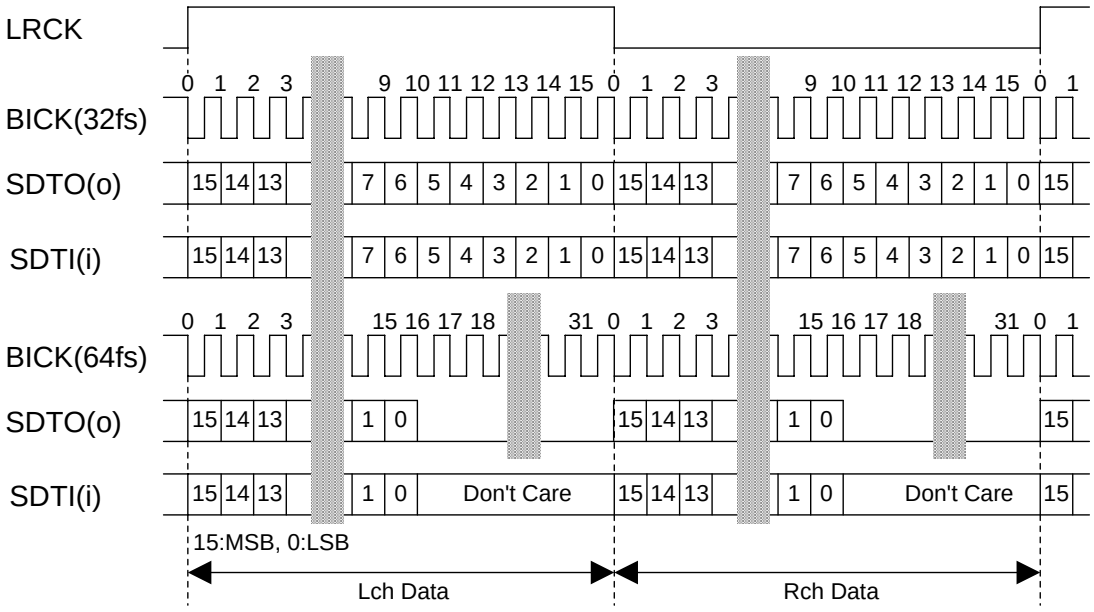


Figure 49. Mode 2 Timing

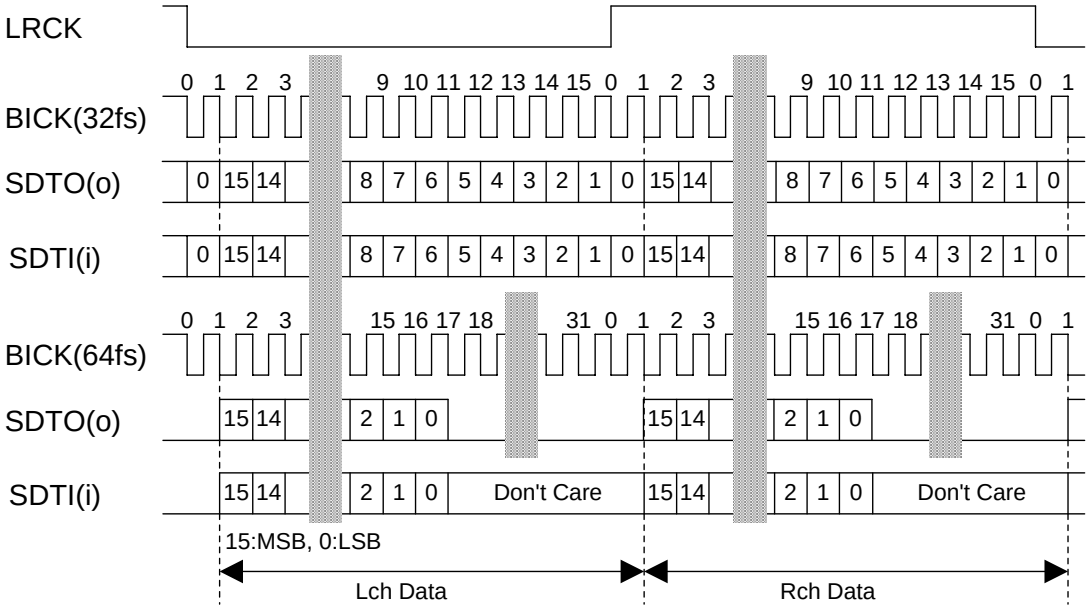


Figure 50. Mode 3 Timing

■ MIC/LINE Input Selector

The AK4675 has input selector. When MDIF1, MDIF2, MDIF3 and MDIF4 bits are "0", INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3/LIN4 and RIN1/RIN2/RIN3/RIN4, respectively. When MDIF1, MDIF2, MDIF3 and MDIF4 bits are "1", LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 pins become IN1+/–, IN2+/–, IN3+/– and IN4+/– pins, respectively. In this case, full-differential input is available (Figure 52).

MDIF1	MDIF2	MDIF3	MDIF4	INL1	INL0	INR1	INR0	Lch	Rch	
0	0	0	0	0	0	0	0	LIN1	RIN1	(default)
0	0	0	0	0	0	0	1	LIN1	RIN2	
0	0	0	0	0	0	1	0	LIN1	RIN3	
0	0	0	0	0	0	1	1	LIN1	RIN4	
0	0	0	0	0	1	0	0	LIN2	RIN1	
0	0	0	0	0	1	0	1	LIN2	RIN2	
0	0	0	0	0	1	1	0	LIN2	RIN3	
0	0	0	0	0	1	1	1	LIN2	RIN4	
0	0	0	0	1	0	0	0	LIN3	RIN1	
0	0	0	0	1	0	0	1	LIN3	RIN2	
0	0	0	0	1	0	1	0	LIN3	RIN3	
0	0	0	0	1	0	1	1	LIN3	RIN4	
0	0	0	0	1	1	0	0	LIN4	RIN1	
0	0	0	0	1	1	0	1	LIN4	RIN2	
0	0	0	0	1	1	1	0	LIN4	RIN3	
0	0	0	0	1	1	1	1	LIN4	RIN4	
0	0	0	1	0	0	1	1	LIN1	IN4+/–	
0	0	0	1	0	1	1	1	LIN2	IN4+/–	
0	0	0	1	1	0	1	1	LIN3	IN4+/–	
0	0	1	0	1	0	0	0	IN3+/–	RIN1	
0	0	1	0	1	0	0	1	IN3+/–	RIN2	
0	0	1	0	1	0	1	1	IN3+/–	RIN4	
0	0	1	1	1	0	1	1	IN3+/–	IN4+/–	
0	1	0	0	0	0	0	1	LIN1	IN2+/–	
0	1	0	0	1	0	0	1	LIN3	IN2+/–	
0	1	0	0	1	1	0	1	LIN4	IN2+/–	
0	1	1	0	1	0	0	1	IN3+/–	IN2+/–	
1	0	0	0	0	0	0	1	IN1+/–	RIN2	
1	0	0	0	0	0	1	0	IN1+/–	RIN3	
1	0	0	0	0	0	1	1	IN1+/–	RIN4	
1	0	0	1	0	0	1	1	IN1+/–	IN4+/–	
1	1	0	0	0	0	0	1	IN1+/–	IN2+/–	
Others								N/A		

Table 18. MIC-Amp Input Signal

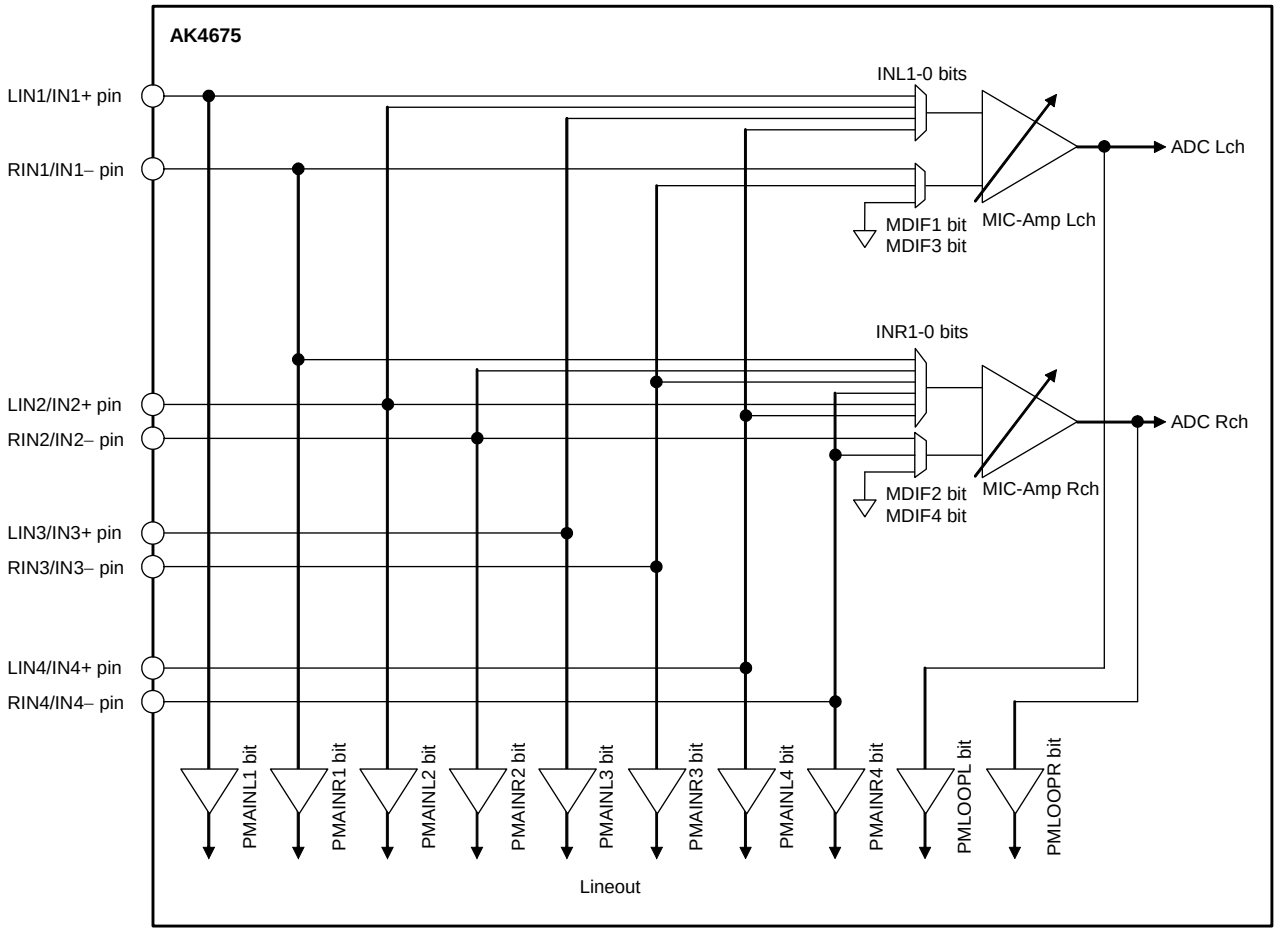


Figure 51. Mic/Line Input Selector

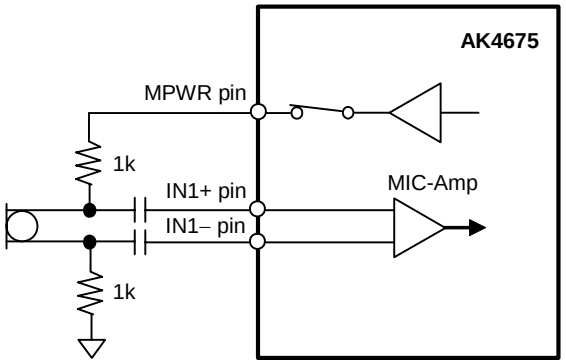


Figure 52. Connection Example for Full-differential Mic Input (MDIF1/2/3/4 bits = "1")

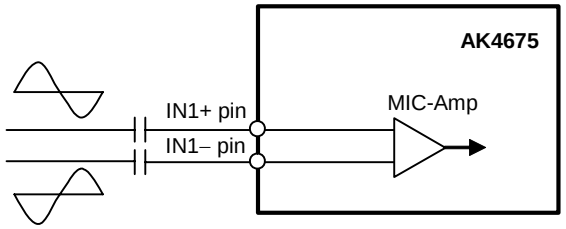


Figure 53. Connection Example for Full-differential Mic Input (MDIF1/2/3/4 bits = "1")

■ MIC Gain Amplifier

The AK4675 has a gain amplifier for microphone input. The gain of MIC-Amp Lch and Rch is independently selected by the MGNL3-0 and MGNR3-0 bits (Table 19). The typical input impedance is 42kΩ(typ)@MGNL/R0 bits = "0" or 30kΩ(typ)@MGNL/R0 bits = "1".

Mode	MGNL3 MGNR3	MGNL2 MGNR2	MGNL1 MGNR1	MGNL0 MGNR0	Input Gain	Input Resistance	
0	0	0	0	0	N/A	N/A	
1	0	0	0	1	–12dB	30kΩ	
2	0	0	1	0	–9dB	42kΩ	
3	0	0	1	1	–6dB	30kΩ	
4	0	1	0	0	–3dB	42kΩ	
5	0	1	0	1	0dB	30kΩ	(default)
6	0	1	1	0	+3dB	42kΩ	
7	0	1	1	1	+6dB	30kΩ	
8	1	0	0	0	+9dB	42kΩ	
9	1	0	0	1	+12dB	30kΩ	
10	1	0	1	0	+15dB	42kΩ	
11	1	0	1	1	+18dB	30kΩ	
12	1	1	0	0	+21dB	42kΩ	
13	1	1	0	1	+24dB	30kΩ	
14	1	1	1	0	+27dB	42kΩ	
15	1	1	1	1	+30dB	30kΩ	

Table 19. Mic Input Gain

■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 0.8 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 54).

PMMP bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 20. MIC Power

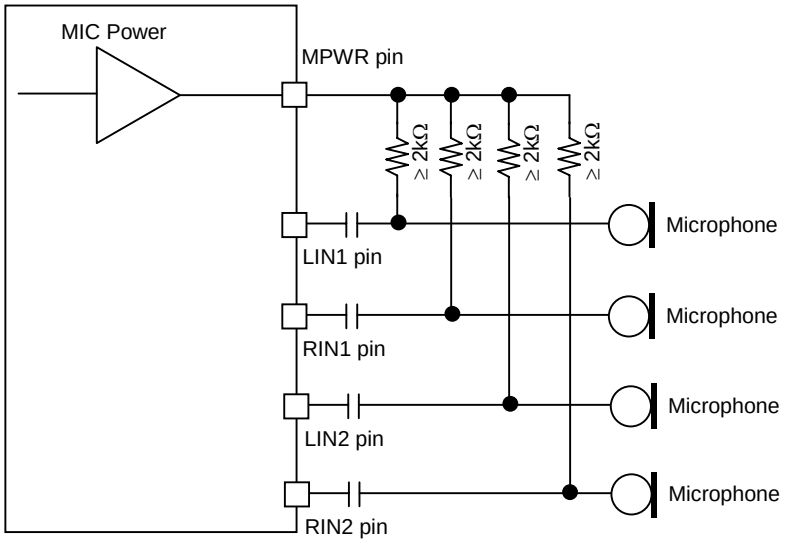


Figure 54. MIC Block Circuit

■ MIC Detection

The AK4675 has a detect function of microphone inputs.

The followings show the example of external microphone detection sequence:

(1) PMMP bit should be set to "1" after CPU detects the jack insertion of microphone or headphone.
(2) The MPWR pin drives external microphone.
(3) The GPO2 pin (at GPOM2 bit = "1") and DTMIC bit are set as Table 21. In case of Headset (with Mic), the input voltage of the MDT pin is higher than 0.075 x AVDD because of the relationship between the bias resistance at the MPWR pin (typ. 2.2kΩ) and the microphone impedance. In case of Headphone (No Mic), the input voltage of the MDT pin is 0V because the pin of headphone jack is connected to the MDT pin is assigned as ground.

Input Level of MDT pin	GPO2 pin	DTMIC bit	Result
≥ 0.075 x AVDD	H	1	Mic (Headset)
< 0.050 x AVDD	L	0	No Mic (Headphone)

Table 21. Microphone Detection Result

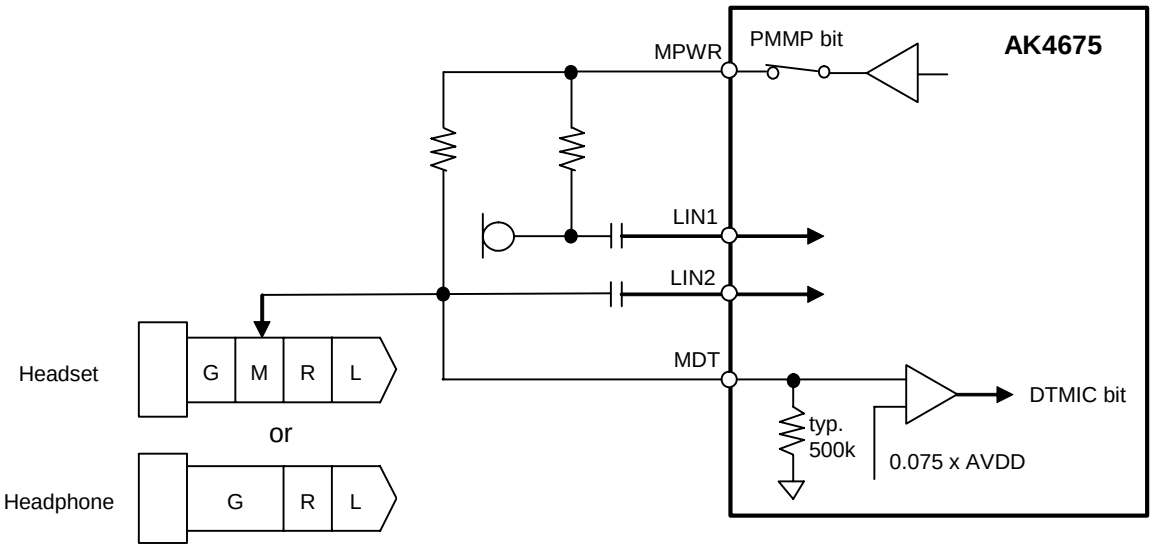


Figure 55. Microphone Power Supply and Mic Detection

■ Digital Block

Digital block is composed as Figure 56. Each block can be powered-down by power management bit (PMADL, PMADR, PMDAL, PMDAR, PMSRA, PMSRB and PMPCM bits). When blocks from HPF to MIX are powered-down, both MIX and SVOLA blocks should not be selected by SDOL/R bits and PFMXL/R bits.

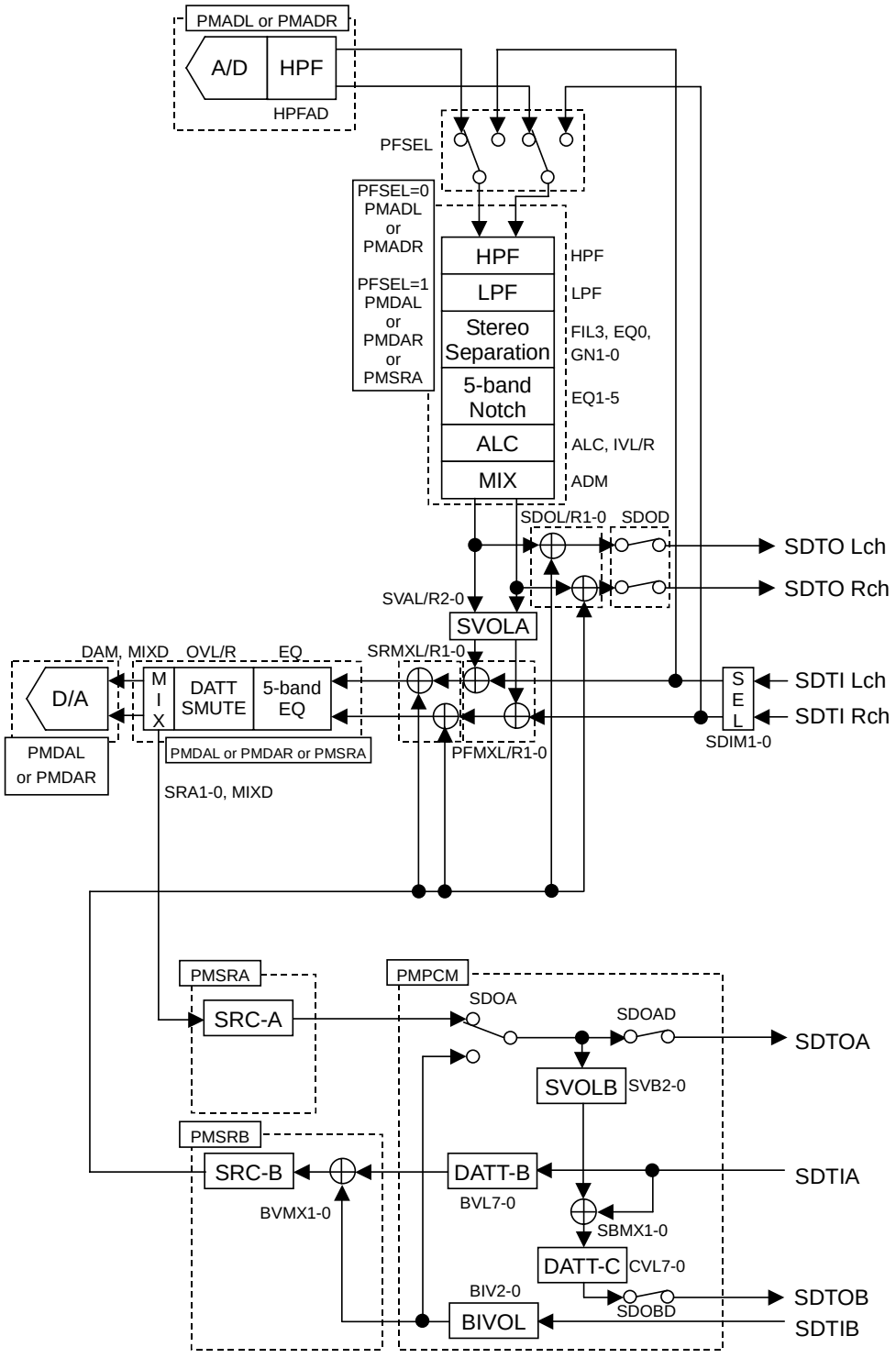


Figure 56. Path Select of Digital Block

(1) ADC: Include the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) DAC: Include the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(3) HPF: High Pass Filter. Applicable to use as Wind-Noise Reduction Filter. (See "Digital Programmable Filter".)
(4) LPF: Low Pass Filter (See "Digital Programmable Filter".)
(5) Stereo Separation: Stereo Separation Emphasis Filter & Gain Comparison. (See "Digital Programmable Filter".) Gain Comparison is composed with EQ0 and Gain blocks. This block adjusts the frequency response after Stereo Separation Emphasis.
(6) 5-Band Notch: Applicable to use as Equalizer or Notch Filter. (See "Digital Programmable Filter".)
(7) ALC: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC Operation".)
(8) SVOLA: Side Tone Volume at Internal MIC/SPK or External Headset Phone Call. (See "Side Tone Volume (SVOLA)".)
(9) 5-Band EQ: Equalizer for playback path. (See "5-band Equalizer".)
(10) DATT: Digital Volume for playback path. (See "Digital Output Volume".)
(11) SMUTE: Soft mute. (See "Soft Mute".)
(12) DATT-B: Digital Volume for Recording of Received Voice. (See "Digital Volume for Recording of Received Voice")
(13) DATT-C: Digital Volume of Received Voice. (See "Digital Volume of Received Voice")
(14) SVOLA: Side Tone Volume at B/T Headset Phone Call. (See "Side Tone Volume for B/T Phone Call".)

Mode	PMADL	PMADR	PMDAL	PMDAR	PFSEL	Figure
Recording Mode	1	1	0	0	0	Figure 57
	1	0	0	0	0	
	0	1	0	0	0	
Recording & Playback Mode	1	1	1	1	0	Figure 58
	1	0	1	1	0	
	0	1	1	1	0	
Playback Mode	0	0	1	1	1	Figure 59

Table 22. Recode/Playback Mode

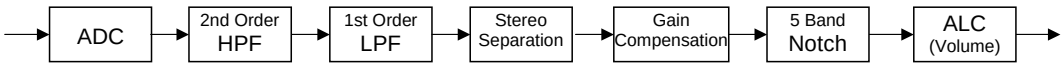


Figure 57. Path at Recording Mode

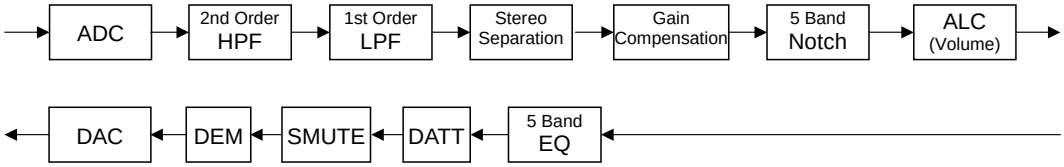


Figure 58. Path at Recording & Playback Mode

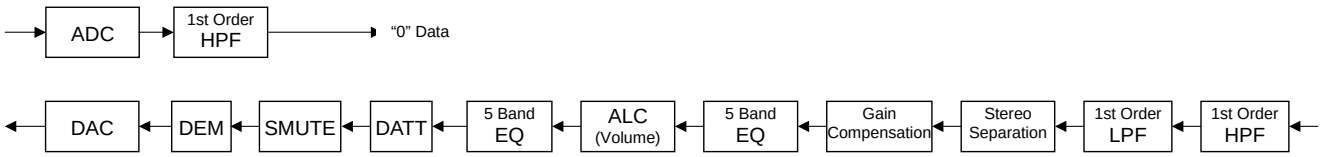


Figure 59. Path at Playback Mode

■ Digital Programmable Filter

(1) High Pass Filter (HPF)

Normally, this HPF is used for a Wind-Noise Reduction Filter. This is composed with 2 steps of 1st order HPF. The coefficient of both HPF is the same and set by F1A13-0 bits and F1B13-0 bits. HPFAD bit controls ON/OFF of the 1st step HPF and HPF bit controls ON/OFF of the 2nd step HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when HPFAD=HPF bits = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 79)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when LPF bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 79)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo mic recording data or playback data. F3A13-0 and F3B13-0 bits set the filter coefficient of FIL3. FIL3 becomes High Pass Filter (HPF) at F3AS bit = "0", and Low Pass Filter (LPF) at F3AS bit = "1". FIL3 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit = "0" or PMADL = PMADR = PMDAL = PMDAR bits = "0".

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 79)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 79)
FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed with Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0, E0B13-0 and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 23). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 79)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

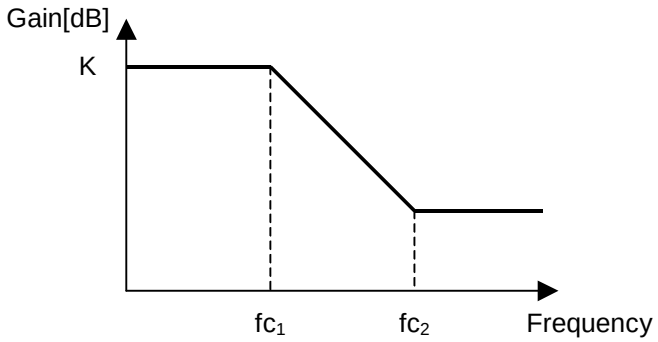


Figure 60. EQ0 Frequency Response

GN1	GN0	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 23. Gain select of gain block (x: Don't care)

(5) 5-band Notch

This block can be used as Equalizer or Notch Filter. 5-band Equalizer (EQ1, EQ2, EQ3, EQ4 and EQ5) is ON/OFF independently by EQ1, EQ2, EQ3, EQ4 and EQ5 bits. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient should be set when EQx bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency
$fo_1 \sim fo_5$: Center frequency
$fb_1 \sim fb_5$: Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: Gain ($-1 \le K_n \le 3$)

Register setting (Note 79)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = 1 + h_1(z) + h_2(z) + h_3(z) + h_4(z) + h_5(z)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency should be set as below.
$fo_n / fs < 0.497$

Note 79. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is done by ALC block when ALC bit is "1". ALC circuit operates at playback path for Playback mode and operates at recording path for Recording mode as shown in Table 22.

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 24), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 25).

When ZELMN bit = "0" (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout periods of both ALC limiter and recovery operation (Table 26). IVL and IVR values are attenuated 1 step immediately (period: 1/fs) by ALC limiter operation when output level is over FS (Digital Full Scale). When output level is not over FS, the IVL and IVR values are changed at the individual zero crossing points of Lch and Rch or at the zero crossing timeout.

When ZELMN bit = "1" (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 24) or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limier Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 24. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1	LMAT0	ALC Limiter ATT Step				
		ALC Output ≥ LMTH	ALC Output ≥ FS	ALC Output ≥ FS + 6dB	ALC Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 25. ALC Limiter ATT Step (x: Don't care)

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 26. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

ALC recovery operation waits for the WTM2-0 bits (Table 27) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 24) during the wait time, ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 28) up to the set reference level (Table 29) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 26). Then the IVL and IVR are set to the same value for both channels. ALC recovery operation is executed at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed. If ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is executed at a period set by ZTM1-0 bits.

For example, when the current IVL and IVR values are 30H and RGAIN1-0 bits are set to "01", IVL and IVR values are changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVL and IVR values exceed the reference level (REF7-0 bits), the IVL and IVR values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 30).

WTM2	WTM1	WTM0		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 27. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 28. ALC Recovery GAIN Step

REF7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
2H	–53.625		
1H	–54.0		
0H	MUTE		

Table 29. Reference Level at ALC Recovery Operation

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	4 times	(default)
0	1	8 times	
1	0	16times	
1	1	N/A	

Table 30. Fast Recovery Speed Setting (N/A: Not available)

3. Example of ALC Operation

Table 31 and Table 32 show the examples of the ALC setting for mic recording and playback, respectively.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period * ZTM1-0 bits should be equal to or shorter than WTM2-0 bits.	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period	001	32ms	100	46.4ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC	ALC enable	1	Enable	1	Enable

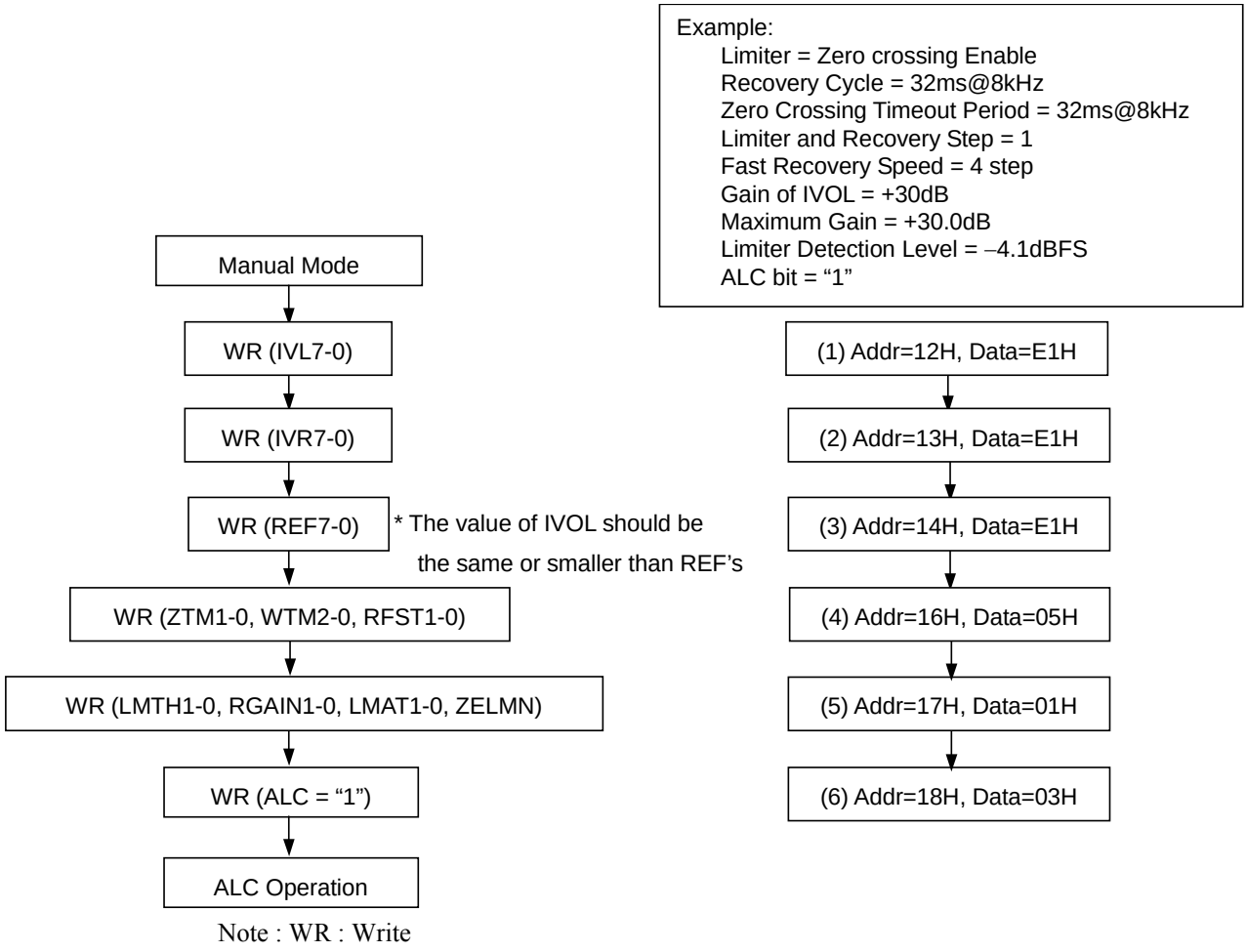
Table 31. Example of the ALC setting (Recording Path)

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same data as ZTM1-0 bits	001	32ms	100	46.4ms
REF7-0	Maximum gain at recovery operation	A1H	+6dB	A1H	+6dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC	ALC enable	1	Enable	1	Enable

Table 32. Example of the ALC setting (Playback Path)

The following registers should not be changed during ALC operation. These bits should be changed after ALC operation is finished by ALC bit = "0".

Each bit of LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN and RFST1-0.



Note : WR : Write

Figure 61. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example, in the case that the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 33). When IVOLC bit is "0", IVL7-0 and IVR7-0 bits control Lch and Rch volume values independently. When IVOLC bit is "1", IVL7-0 bits controls both channels. The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to "1".

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 33. Input Digital Volume Setting

■ Side Tone Volume (SVOLA)

The AK4675 has the channel independent side tone volume (5 levels, 6dB step). The volume can be set by the SVAL/R2-0 bits. The volume is included at mixing path from ALC to 5-band EQ. The output data of ALC is changed from 0 to –24dB.

SVAL/R2-0	Gain	
0H	0dB	(default)
1H	–6dB	
2H	–12dB	
3H	–18dB	
4H	–24dB	
Others	N/A	

Table 34. Side Tone Volume A Code Table (N/A: Not available)

■ 5-Band Equalizer

The AK4675 has 5-Band Equalizer before DAC of Stereo CODEC.

The center frequencies and cut/boost amount are the followings.

- Center frequency: 100Hz, 250Hz, 1kHz, 3.5kHz, 10kHz (Note 80, Note 81, Note 82)
- Cut/Boost amount: –10.5dB ~ +12dB, 1.5dB step

Note 80: These are the frequencies when the sampling frequency is 44.1kHz. These frequencies are proportional to the sampling frequency.
Note 81: 100Hz is not center frequency but the frequency component lower than 100Hz is controlled.
Note 82: 10kHz is not center frequency but the frequency component higher than 10kHz is controlled.

EQ bit controls ON/OFF of this Equalizer and these Boost amount are set by EQA3-0, EQB3-0, EQC3-0, EQD3-0 and EQE3-0 bits, respectively, as shown in Table 35.

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz

EQx3-0	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	(default)
:	:	
DH	–7.5dB	
EH	–9.0dB	
FH	–10.5dB	

Table 35. Boost amount of 5-Band Equalizer

■ Digital Output Volume

The AK4675 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the OVL7-0 and OVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –115dB or MUTE. When the OVOLC bit = "1", the OVL7-0 bits control both Lch and Rch attenuation levels. When the OVOLC bit = "0", the OVL7-0 bits control Lch level and OVR7-0 bits control Rch level. This volume has a soft transition function. The OVTM bit sets the transition time between set values of OVL/R7-0 bits as either 1061/fs or 256/fs (Table 37). When OVTM bit = "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=24ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

OVL/R7-0	Gain	Step	
00H	+12.0dB	0.5dB	
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		(default)
:	:		
FDH	–114.5dB		
FEH	–115.0dB		
FFH	MUTE (–∞)		

Table 36. Digital Volume Code Table

OVTM bit	Transition time between DVL/R7-0 bits = 00H and FFH			
	Setting	fs=8kHz	fs=44.1kHz	
0	1061/fs	133ms	24ms	(default)
1	256/fs	32ms	6ms	

Table 37. Transition Time Setting of Digital Output Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by –∞ ("0") during the cycle set by the OVTM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by the OVL/R7-0 bits during the cycle set of the OVTM bit. If the soft mute is cancelled within the cycle set by the OVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the OVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 62).

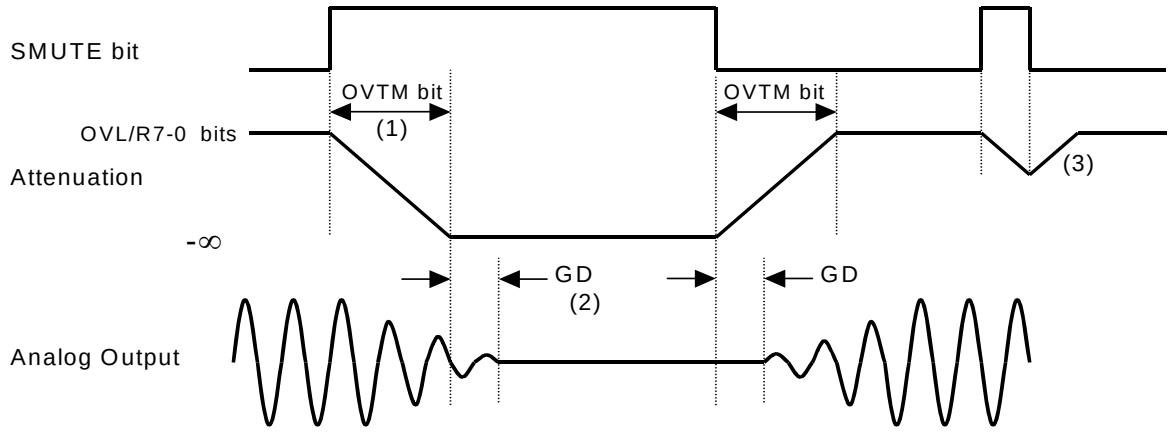


Figure 62. Soft Mute Function

(1) The output signal is attenuated until –∞ ("0") by the cycle set by the OVTM bit.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled within the cycle set by the OVTM bit, the attenuation is discounted and returned to the value set by the OVL/R7-0 bits.

■ Digital Volume Control for Recording of Received Voice (DATT-B)

The AK4675 has a digital output volume control (DATT-B: 256 levels, 0.5dB step, Mute) for recording of received voice. The volume can be set by the BVL7-0 bits. The volume is included in front of an SRC-B block. The input data of SRC-B is changed from +12 to –115dB or MUTE. This volume has a soft transition function. The transition time between set values of BVL7-0 bits is 256/fs2. It takes 256/fs2 (=32ms@fs2=8kHz) from 00H (+12dB) to FFH (MUTE).

BVL7-0	Gain	Step	
00H	+12.0dB	0.5dB	
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		(default)
:	:		
FDH	–114.5dB		
FEH	–115.0dB		
FFH	MUTE (–∞)		

Table 38. Digital Volume B Code Table

■ Digital Volume Control for Received Voice (DATT-C)

The AK4675 has a digital output volume control (DATT-C: 256 levels, 0.5dB step, Mute) for received voice. The volume can be set by the CVL7-0 bits. The volume is included in front of SDTOB output. The input data of SRC-C is changed from +12 to –115dB or MUTE. This volume has a soft transition function. The transition time between set values of CVL7-0 bits is 256/fs2. It takes 256/fs2 (=32ms@fs2=8kHz) from 00H (+12dB) to FFH (MUTE).

CVL7-0	Gain	Step	
00H	+12.0dB	0.5dB	
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		(default)
:	:		
FDH	–114.5dB		
FEH	–115.0dB		
FFH	MUTE (–∞)		

Table 39. Digital Volume C Code Table

■ Side Tone Volume Control for B/T Phone Call (SVOLB)

The AK4675 has a side tone volume control (5 levels, 6dB step) for B/T phone call. The volume can be set by the SVL2-0 bits. The volume is included at mixing path from SRC-A to DATT-C. The output data of SRC-A is changed from 0 to –24dB.

SVB2-0	Gain	
0H	0dB	(default)
1H	–6dB	
2H	–12dB	
3H	–18dB	
4H	–24dB	
Others	N/A	

Table 40. Side Tone Volume B Code Table (N/A: Not available)

■ Digital Volume Control for B/T MIC Input (BIVOL)

The AK4675 has a digital volume control (5 levels, 6dB step) for B/T mic input. The volume can be set by the BIV2-0 bits. The volume is included at SDTIB input. The input data is changed from 0 to –24dB.

BIV2-0	Gain	
0H	0dB	(default)
1H	–6dB	
2H	–12dB	
3H	–18dB	
4H	–24dB	
Others	N/A	

Table 41. B/T Mic Volume Code Table (N/A: Not available)

■ Path & Mixing Setting of Digital Block (Figure 56.)

PMADL and PMADR bits set both ADC power management and output data selection. In case of mono operation, the same data is output to both channel slots.

PMADL	PMADR	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 42. ADC Mono/Stereo Select

PFSEL bit select the input data of programmable filter.

PFSEL	Programmable Filter Input	
0	ADC Output (selected by Table 42.)	(default)
1	SDTI Input (selected by Table 48)	

Table 43. Programmable Filter Input Signal Select

When ADM bit is "1", ALC output data is output to both channels of SDTO and SVOLA as (L+R)/2, respectively.

ADM	Lch	Rch	
0	L	R	(default)
1	(L+R)/2	(L+R)/2	

Table 44. ALC Output Mono Mixing

SDOL1-0 and SDOR1-0 bits set the data mixing for each channel of SDTO from the data selected by Table 44 and SRC-B output data.

SDOL1	SDOL0	SDTO Lch	
0	0	Lch Signal selected by Table 44	(default)
0	1	SRC-B	
1	0	(Lch Signal selected by Table 44) + (SRC-B)	
1	1	N/A	

Table 45. SDTO Lch Output Mixing (N/A: Not available)

SDOR1	SDOR0	SDTO Rch	
0	0	Rch Signal selected by Table 44	(default)
0	1	SRC-B	
1	0	(Rch Signal selected by Table 44) + (SRC-B)	
1	1	N/A	

Table 46. SDTO Rch Output Mixing (N/A: Not available)

When SDOD bit is "1", SDTO output data can be disabled (fixed to "L"). Input data of SVOLA is not disabled.

SDOD	SDTO	
0	Enable (Output)	(default)
1	Disable ("L")	

Table 47. SDTO Disable

SDIM1-0 bits select stereo or mono of SDTI input data. In case of mono mode, the same data is input to both channels.

SDIM1	SDIM0	Lch	Rch	
0	0	L	R	(default)
0	1	L	L	
1	0	R	R	
1	1	N/A		

Table 48. SDTI Stereo/Mono Select (N/A: Not available)

PFMXL1-0 and PFMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by Table 48 and SVOLA output data.

PFMXL1	PFMXL0	5-band EQ Lch Input	
0	0	Lch Signal selected by Table 48	(default)
0	1	SVOLA Lch	
1	0	(Lch Signal selected by Table 48) + (SVOLA Lch)	
1	1	N/A	

Table 49. 5-band EQ Lch Input Mixing 1 (N/A: Not available)

PFMXR1	PFMXR0	5-band EQ Rch Input	
0	0	Rch Signal selected by Table 48	(default)
0	1	SVOLA Rch	
1	0	(Rch Signal selected by Table 48) + (SVOLA Rch)	
1	1	N/A	

Table 50. 5-band EQ Rch Input Mixing 1 (N/A: Not available)

SRMXL1-0 and SRMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by Table 49/Table 50 and SVOLA output data.

SRMXL1	SRMXL0	5-band EQ Lch Input	
0	0	Signal selected by Table 49	(default)
0	1	SRC-B	
1	0	(Signal selected by Table 49) + (SRC-B)	
1	1	N/A	

Table 51. 5-band EQ Lch Input Mixing 2 (N/A: Not available)

SRMXR1	SRMXR0	5-band EQ Rch Input	
0	0	Signal selected by Table 50	(default)
0	1	SRC-B	
1	0	(Signal selected by Table 50) + (SRC-B)	
1	1	N/A	

Table 52. 5-band EQ Rch Input Mixing 2 (N/A: Not available)

DAM and MIXD bits set the data mixing for DAC input.

DAM	MIXD	Lch	Rch	
0	x	L	R	(default)
1	0	L+R	L+R	
1	1	(L+R)/2	(L+R)/2	

Table 53. DAC Mono Mixing (x: Don't care)

SRA1-0 and MIXD bits set the data mixing for SRC-A input.

SRA1	SRA0	MIXD	SRC-A	
0	0	x	L	(default)
0	1	x	R	
1	0	0	L+R	
1	0	1	(L+R)/2	
1	1	x	N/A	

Table 54. SRC-A Input Mixing (x: Don't care, N/A: Not available)

SDOA bit selects the output data of SDTOA.

SDOA	SDTOA	
0	SRC-A	(default)
1	SDTIB	

Table 55. SDTOA Output Select

When SDOAD bit is "1", SDTOA output data can be disabled (fixed to "L"). Input data of SVOLB is not disabled.

SDOAD	SDTOA	
0	Enable (Output)	(default)
1	Disable ("L")	

Table 56. SDTOA Disable

SBMX1-0 bits set the data mixing from SDTIA input and SVOLB output. The mixed data is output to SDTOB via DATT-C.

SBMX1	SBMX0	DATT-C Input	
0	0	SDTIA	(default)
0	1	SVOLB	
1	0	(SDTIA) + (SVOLB)	
1	1	N/A	

Table 57. SDTOB Mixing (N/A: Not available)

When SDOBD bit is "1", SDTOB output data can be disabled (fixed to "L").

SDOBD	SDTOB	
0	Enable (Output)	(default)
1	Disable ("L")	

Table 58. SDTOB Disable

BVMX1-0 bits set the data mixing for SRC-B from SDTIA input (DATT-B output) and SDTIB input (BIVOL output).

BVMX1	BVMX0	SRC-B Input	
0	0	SDTIA	(default)
0	1	SDTIB	
1	0	(SDTIA) + (SDTIB)	
1	1	N/A	

Table 59. SRC-B Input Mixing (N/A: Not available)

■ Analog Mixing: Single-ended Input (LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins)

AK4675 supports analog mixing function from each line input to each line output (Figure 63).

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is "1". When PMAINL1=PMAINR1=PMAINL2=PMAINR2=PMAINL3=PMAINR3=PMAINL4=PMAINR4=PMMICL=PMMICR bits = "1", the input resistance of LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins becomes 25kΩ (typ) at MGNL/R0 bits = "0" and 20kΩ (typ) at MGNL/R0 bits = "1", respectively.

L1G1-0, L2G1-0, L3G1-0, L4G1-0 and LPG1-0 bits adjust the gain for each path (Table 60, Table 61, Table 62, Table 63, Table 64).

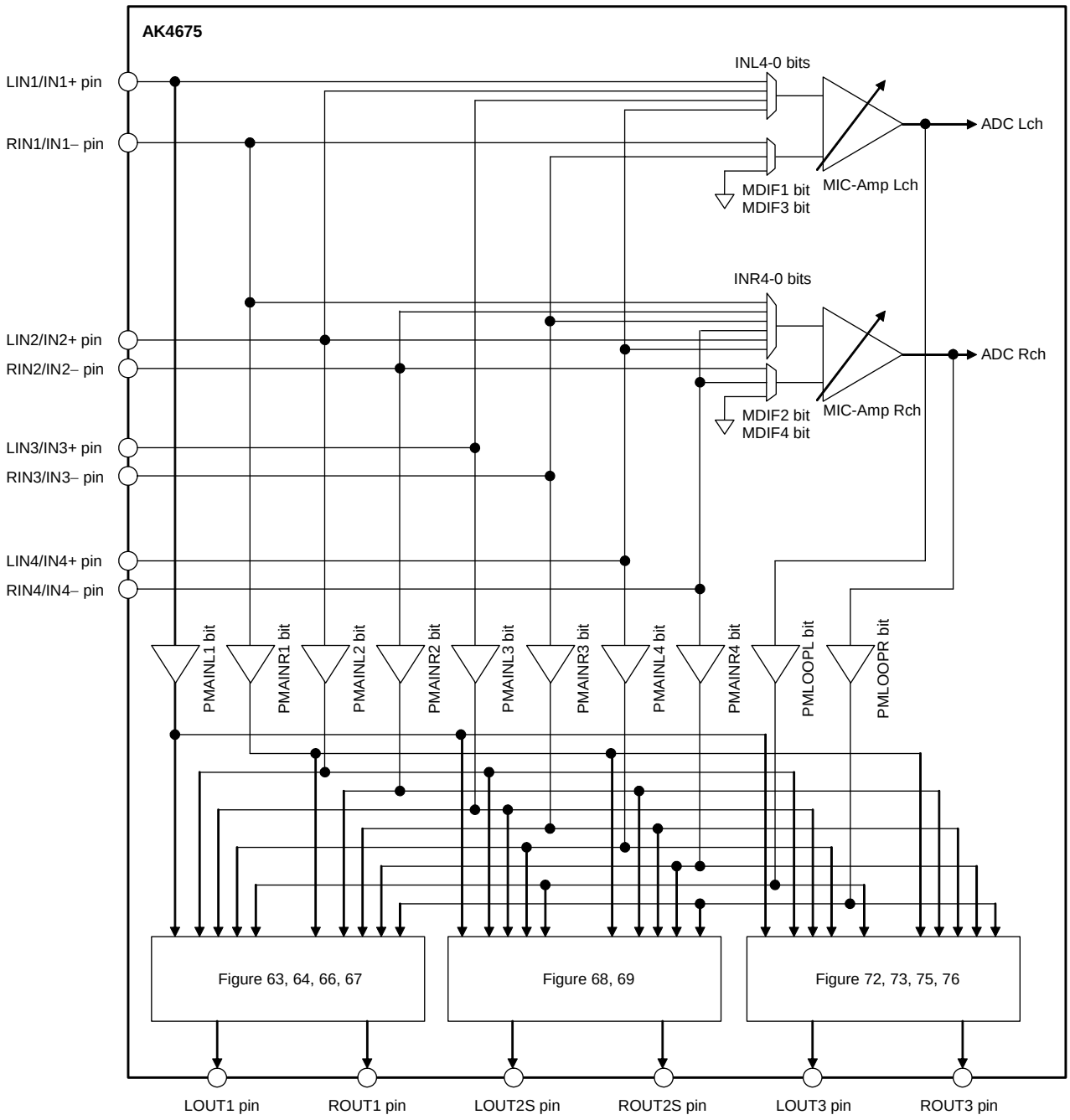


Figure 63. Analog Mixing Circuit

L1G1 bit	L1G0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	–6dB	
1	1	N/A	

Table 60. LIN1/RIN1 (or IN1+/–) Mixing Gain (typ) (N/A: Not available)

L2G1 bit	L2G0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	–6dB	
1	1	N/A	

Table 61. LIN2/RIN2 (or IN2+/–) Mixing Gain (typ) (N/A: Not available)

L3G1 bit	L3G0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	–6dB	
1	1	N/A	

Table 62. LIN3/RIN3 (or IN3+/–) Mixing Gain (typ) (N/A: Not available)

L4G1 bit	L4G0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	–6dB	
1	1	N/A	

Table 63. LIN4/RIN4 (or IN4+/–) Mixing Gain (typ) (N/A: Not available)

LPG1 bit	LPG0 bit	Gain	
0	0	0dB	(default)
0	1	+6dB	
1	0	–6dB	
1	1	N/A	

Table 64. MIC-Amp Mixing Gain (typ) (N/A: Not available)

■ Analog Mixing: Full-differential Input (IN1+/IN1–/IN2+/IN2–/IN3+/IN3–/IN4+/IN4– pins)

When MDIF1, MDIF2, MDIF3 and MDIF4 bits are "1", LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 pins become IN1+/–, IN2+/–, IN3+/– and IN4+/– pins, respectively, and analog mixing is available.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is "1". When PMAINL1=PMAINR1=PMAINL2=PMAINR2=PMAINL3=PMAINR3=PMAINL4=PMAINR4=PMMICL=PMMICR bits = "1", the input resistance of IN1+/–, IN2+/–, IN3+/– and IN4+/– pins becomes 25kΩ (typ) at MGNL/R0 bits = "0" and 20kΩ (typ) at MGNL/R0 bits = "1", respectively.

L1G1-0, L2G1-0, L3G1-0, L4G1-0 and LPG1-0 bits adjust the gain for each path (Table 60, Table 61, Table 62, Table 63, Table 64).

■ Stereo Line Output (LOUT1/ROUT1 pins)

When DACL and DACR bits are "1", Lch/Rch signal of DAC is output from the LOUT1/ROUT1 pins which is single-ended. When DACL and DACR bits are "0", output signal is muted and LOUT1/ROUT1 pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO1=PMRO1=LOPS1 bits = "0", LOUT1/ROUT1 enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS1 bit is "1", LOUT1/ROUT1 enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO1 and PMRO1 bits at LOPS1 bit = "1". In this case, output signal line should be pulled-down to VSS1 by 20kΩ after AC coupled as Figure 64. Rise/Fall time is 300ms(max) at C=1μF and AVDD=3.3V. When PMLO1=PMRO1 bits = "1" and LOPS1 bit = "0", LOUT1/ROUT1 is in normal operation.

L1VL2-0 bits control the volume of LOUT1/ROUT1.
When LOM bit = "1", DAC output signal is output to LOUT1 and ROUT1 pins as (L+R) mono signal.
When LOOPM bit = "1", the MIC-Amp signal is output to LOUT1 and ROUT1 pins as (L+R) mono signal.

LOPS1	PMLO1	Mode	LOUT1 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 65. Stereo Line Output Mode Select (LOUT1)

LOPS1	PMRO1	Mode	ROUT1 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 66. Stereo Line Output Mode Select (ROUT1)

L1VL2-0	Attenuation	
6H	+6dB	
5H	0dB	(default)
4H	−6dB	
3H	−12dB	
2H	−18dB	
1H	−24dB	
0H	MUTE	

Table 67. Stereo Line Output Volume Setting

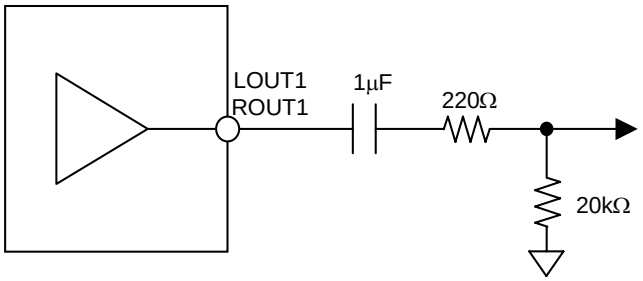


Figure 64. External Circuit for Stereo Line Output (in case of using Pop Noise Reduction Circuit)

<Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

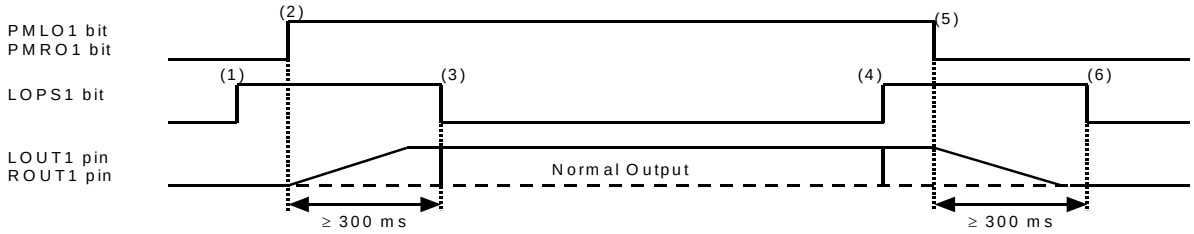


Figure 65. Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)

(1) Set LOPS1 bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO1=PMRO1 bits = "1". Stereo line output exits the power-down mode.
LOUT1 and ROUT1 pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(3) Set LOPS1 bit = "0" after LOUT1 and ROUT1 pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS1 bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO1=PMRO1 bits = "0". Stereo line output enters power-down mode.
LOUT1 and ROUT1 pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(6) Set LOPS1 bit = "0" after LOUT1 and ROUT1 pins fall down. Stereo line output exits the power-save mode.

<Analog Mixing Circuit for LOUT1/ROUT1>

DACL, DACR, LOM, LINL1, RINR1, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, LOOPL, LOOPR and LOOPM bits control each path switch.

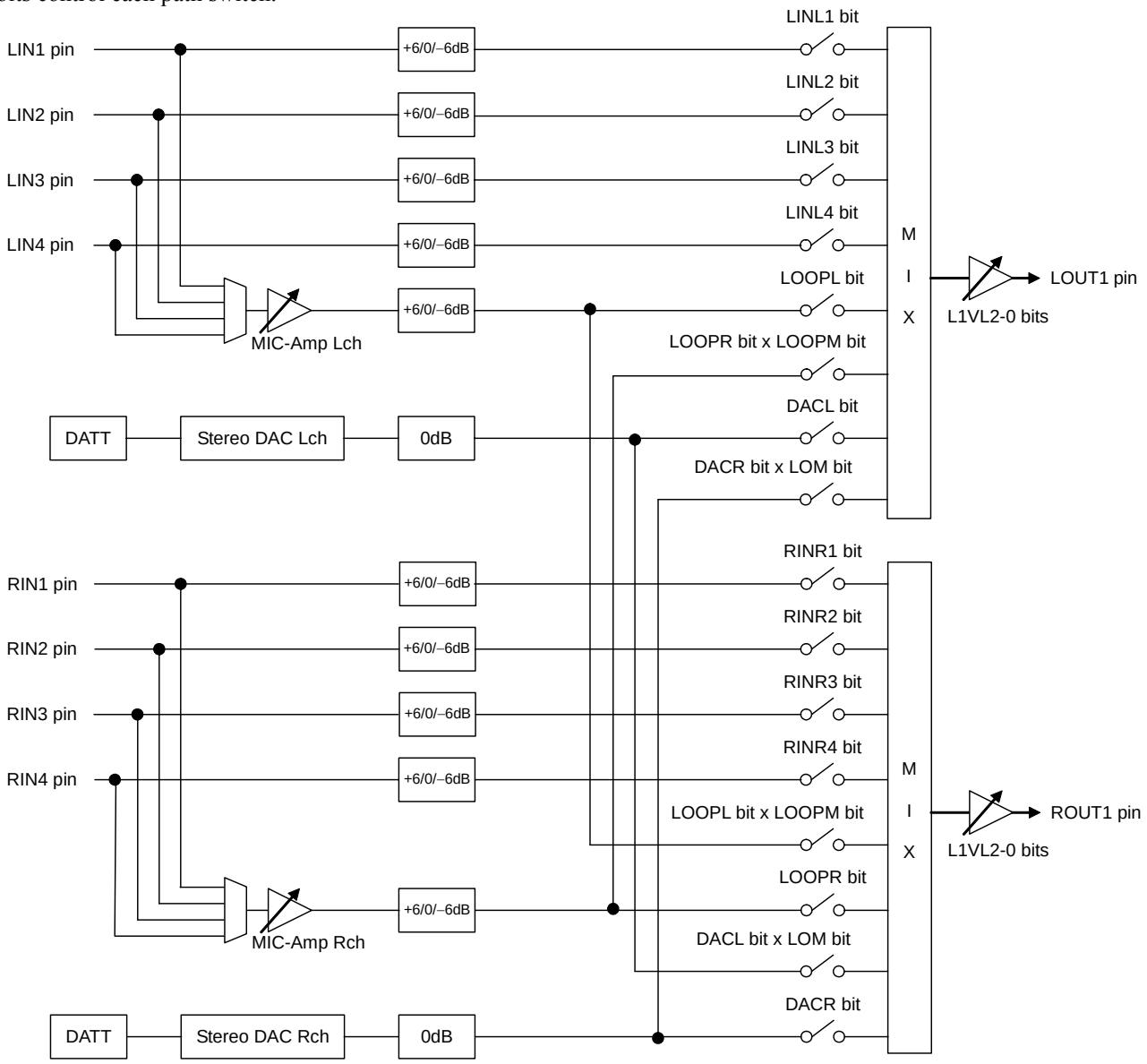


Figure 66. LOUT1/ROUT1 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

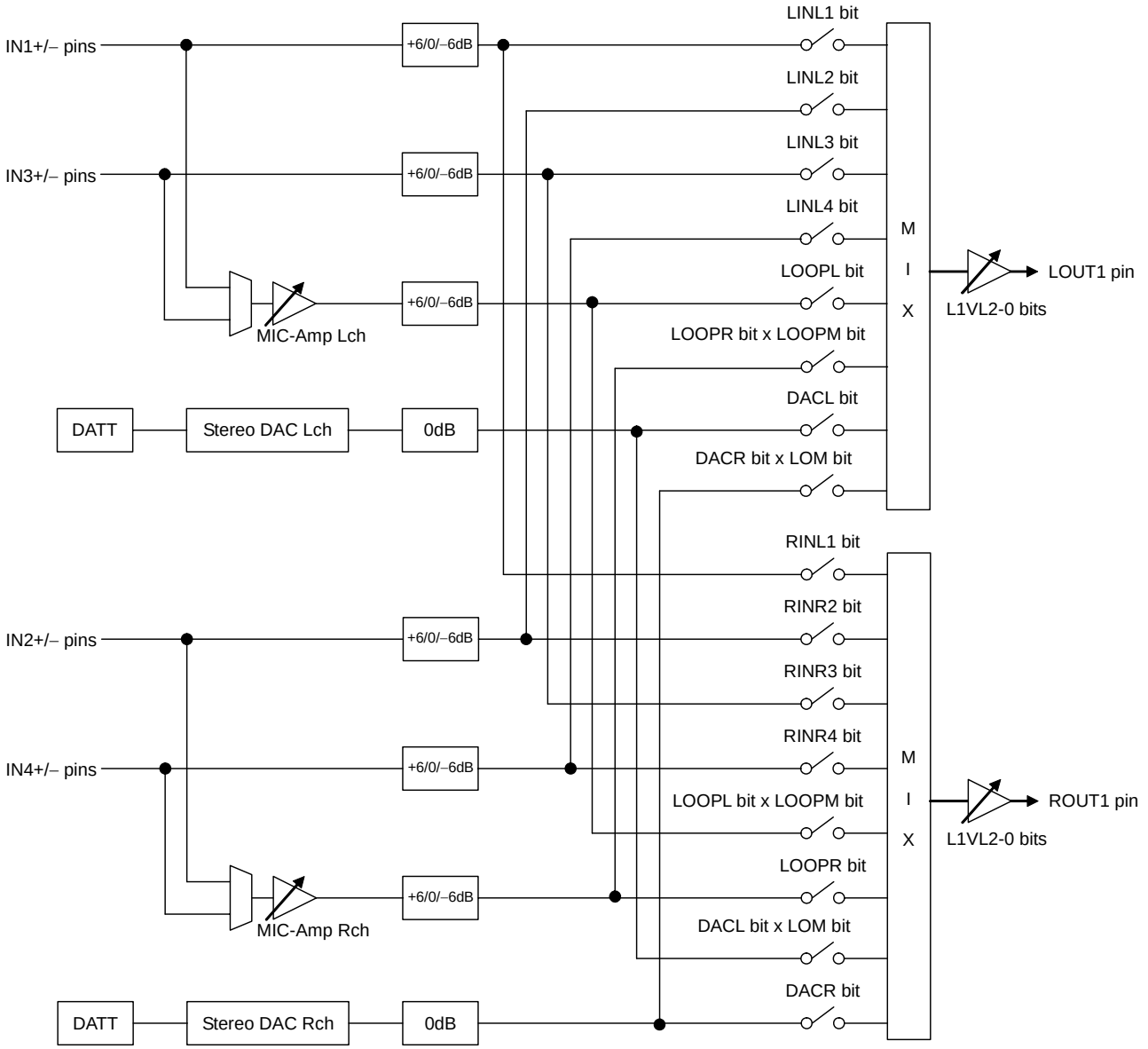


Figure 67. LOUT1/ROUT1 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Receiver-Amp (RCP/RCN pins)

When RCV bit = "1", LOUT1/ROUT1 pins become RCP/RCN pins, respectively. Lch/Rch signal of DAC or LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the RCP/RCN pins which is BTL as (L+R) signal. The load impedance is 32Ω (min). When the PMLO1 = PMRO1 bits = "0", the mono receiver output enters power-down mode and the output is Hi-Z. When the PMLO1 = PMRO1 bits = "1" and LOPS1 bit = "1", mono receiver output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO1 and PMRO1 bits at LOPS1 bit = "0". When PMLO1 = PMRO1 bits = "1" and LOPS1 bit = "0", mono receiver output enters in normal operation. L1VL3-0 bits control the volume of mono receiver output.

L1VL2-0	Attenuation	
6H	+12dB	
5H	+6dB	(default)
4H	0dB	
3H	−6dB	
2H	−12dB	
1H	−18dB	
0H	MUTE	

Table 68. Mono Receiver Output Volume Setting

PMLO1/RO1	LOPS1	Mode	RCP	RCN	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	1	Power-save	Hi-Z	VCOM	
	0	Normal Operation	Normal Operation	Normal Operation	

Table 69. Receiver-Amp Mode Setting (x: Don't care)

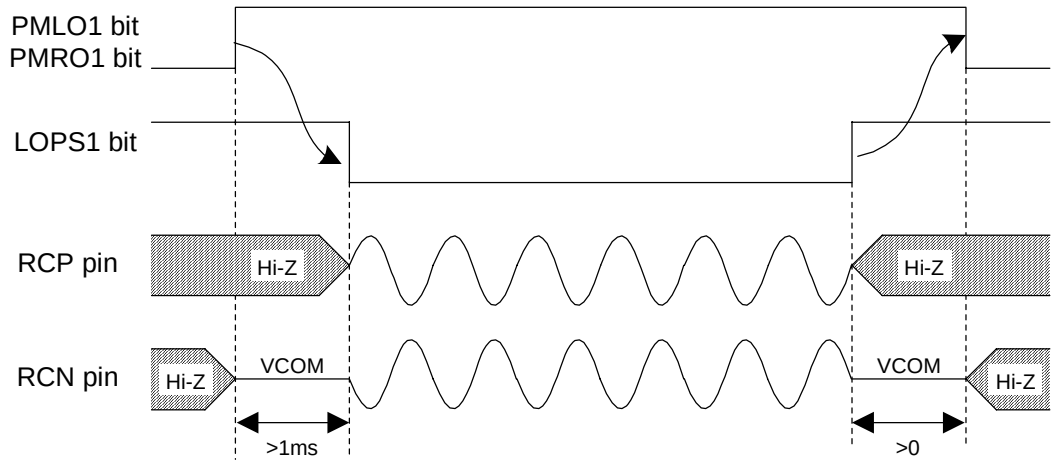


Figure 68. Power-up/Power-down Timing for Receiver-Amp

<Analog Mixing Circuit for Receiver Output>

DACL, DACR, LINL1, RINR1, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, LOOPL and LOOPR bits control each path switch.
When MDIF1/2/3/4 bits = "1", RINR1/2/3/4 bits should be "0".

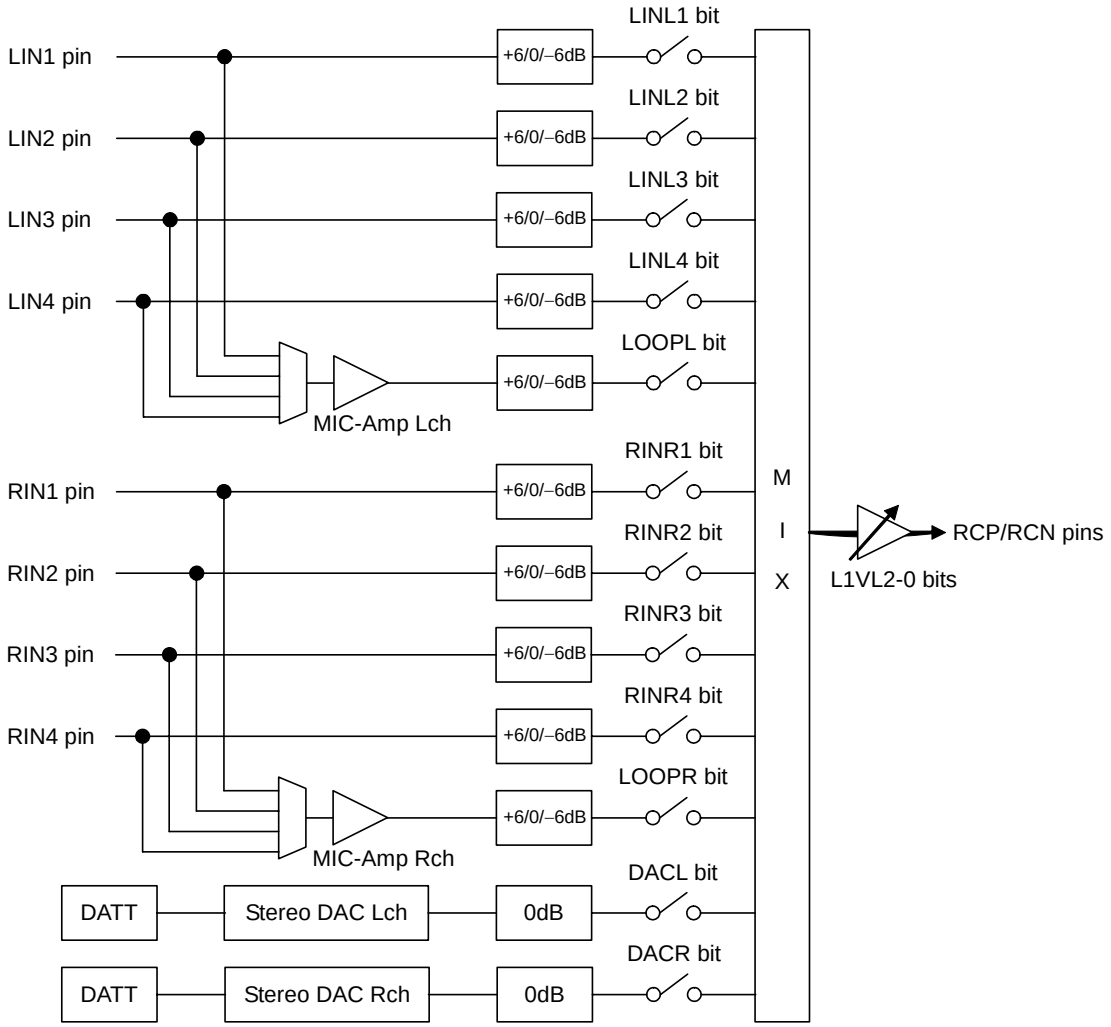


Figure 69. Receiver Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

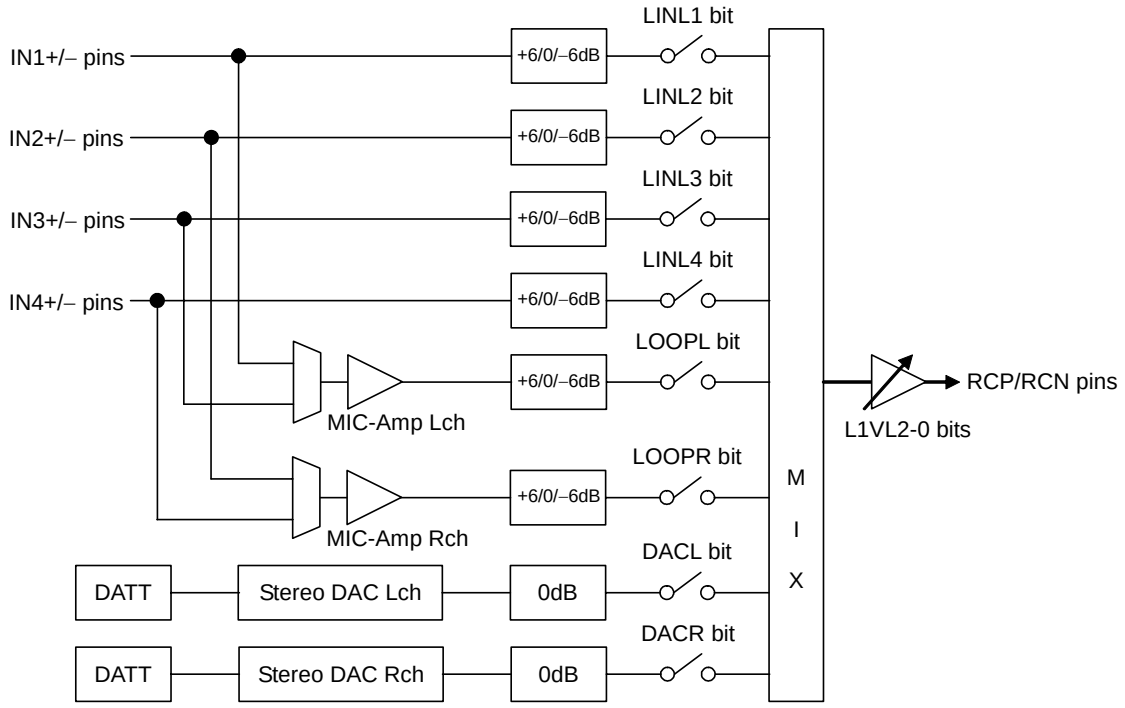


Figure 70. Receiver Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Stereo Line Output 2 (LOUT2S/ROUT2S pins)

Power supply voltage for the LOUT2S/ROUT2S is supplied from the AVDD pin and centered on the 0.5 x AVDD (typ) voltage. The load resistance is 25kΩ (min).

When LOM2 bit = "1", DAC output signal is output to LOUT2S and ROUT2S pins as (L+R) mono signal.
When LOOPM2 bit = "1", the MIC-Amp signal is output to LOUT2S and ROUT2S pins as (L+R) mono signal.

When PMLO2S and PMRO2S bits are "0", the LOUT2S/ROUT2S is powered-down, and the outputs (LOUT2S and ROUT2S pins) go to "L" (VSS1).

<Analog Mixing Circuit for LOUT2S/ROUT2S>

DACHL, DACHR, LOM2, LINH1, RINH1, LINH2, RINH2, LINH3, RINH3, LINH4, RINH4, LOOPHL, LOOPHR and LOOPM2 bits control each path switch.

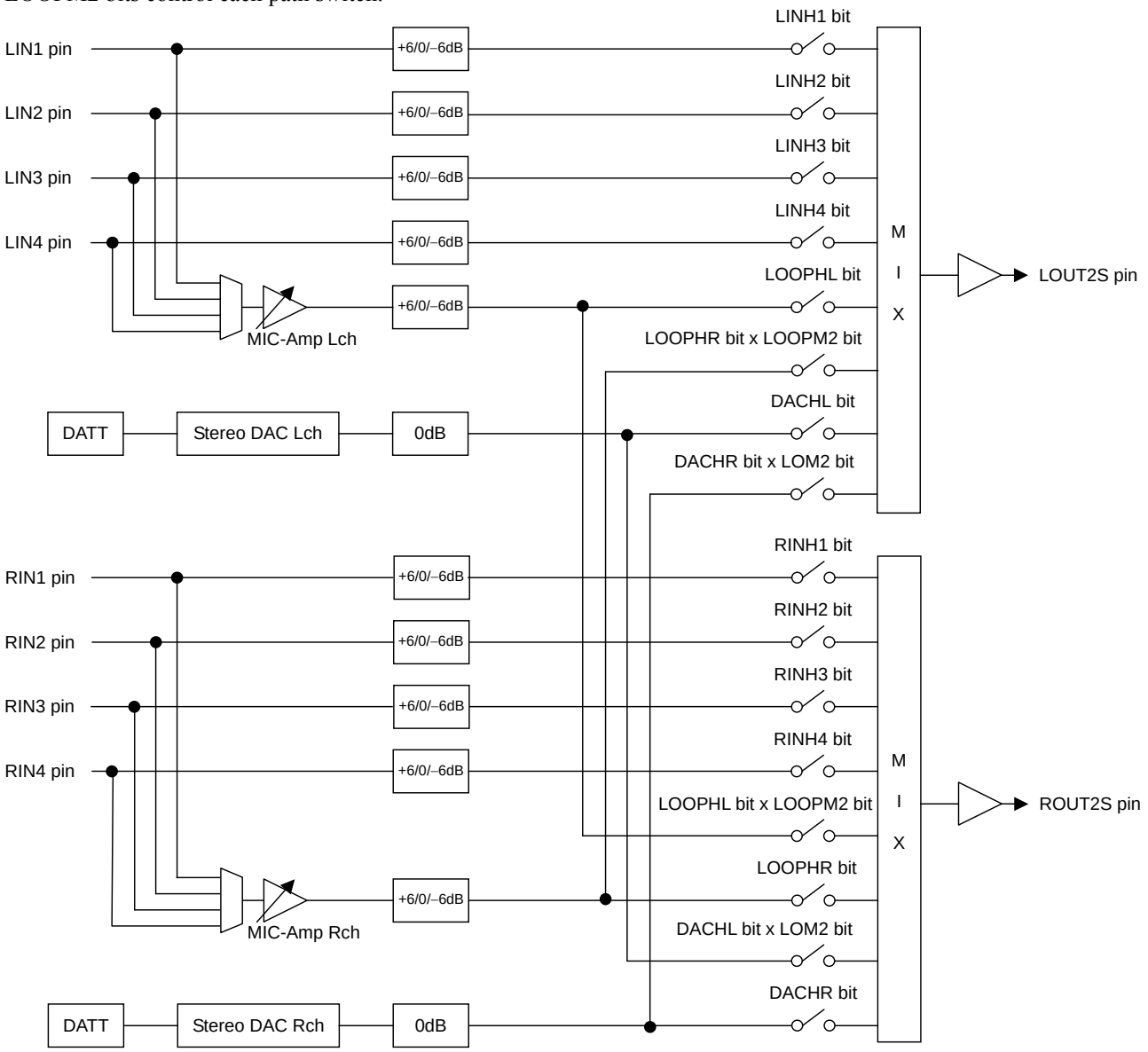


Figure 71. LOUT2S/ROUT2S Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

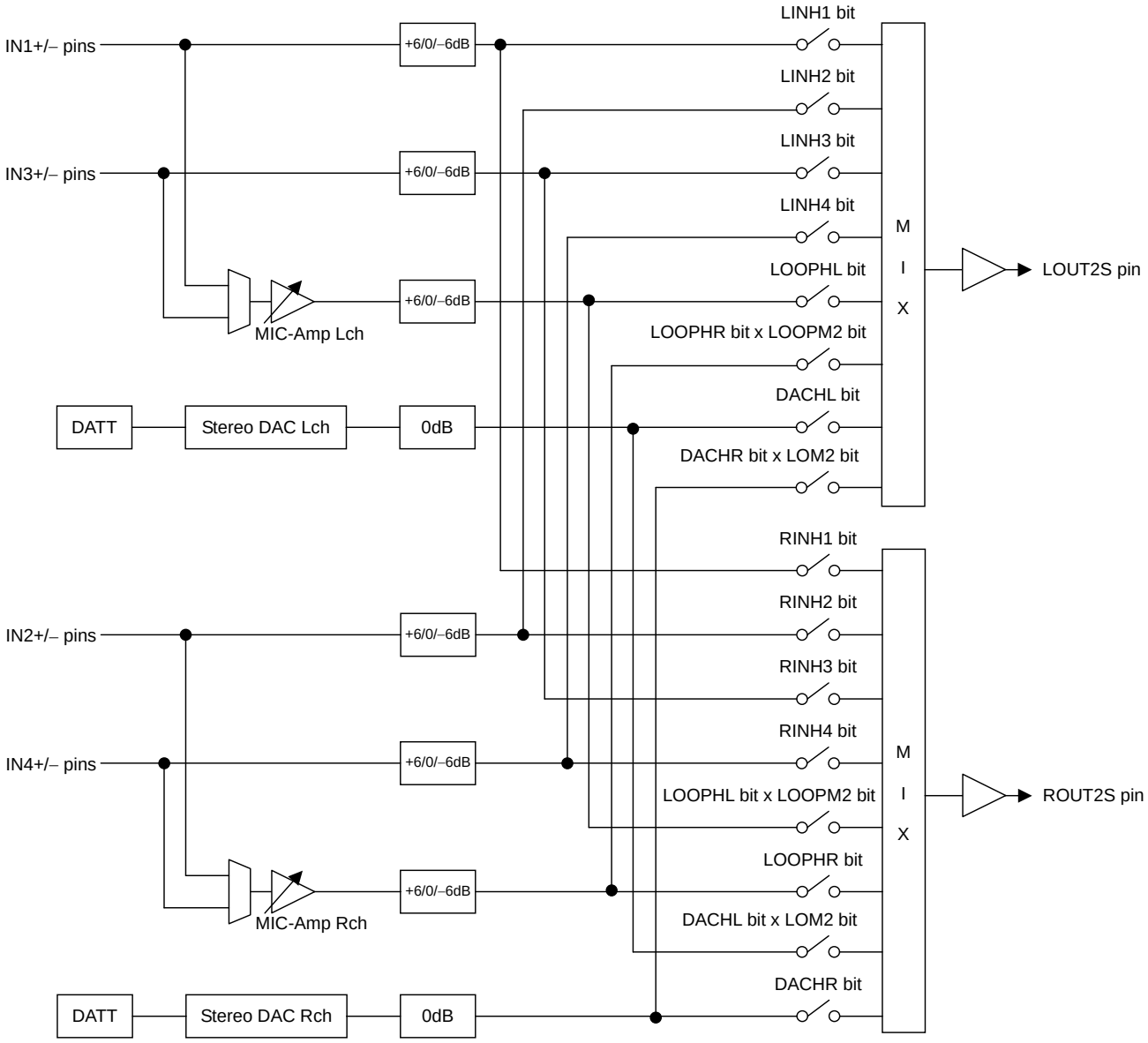


Figure 72. LOUT2S/ROUT2S Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Stereo Line Output 3 (LOUT3/ROUT3 pins)

When DACSL and DACSR bits are "1", Lch/Rch signal of DAC is output from the LOUT3/ROUT3 pins which is single-ended. When DACSL and DACSR bits are "0", output signal is muted and LOUT3/ROUT3 pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO3=PMRO3=LOPS3 bits = "0", LOUT3/ROUT3 enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS3 bit is "1", LOUT3/ROUT3 enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO3 and PMRO3 bits at LOPS3 bit = "1". In this case, output signal line should be pulled-down to VSS1 by 20kΩ after AC coupled as Figure 64. Rise/Fall time is 300ms(max) at C=1μF and AVDD=3.3V. When PMLO3=PMRO3 bits = "1" and LOPS3 bit = "0", LOUT3/ROUT3 is in normal operation.

L3VL3-0 bits control the volume of LOUT3/ROUT3.
When LOM3 bit = "1", DAC output signal is output to LOUT3 and ROUT3 pins as (L+R) mono signal.
When LOOPM3 bit = "1", the MIC-Amp signal is output to LOUT3 and ROUT3 pins as (L+R) mono signal.

LOPS3	PMLO3	Mode	LOUT3 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 70. Stereo Line Output Mode Select (LOUT3)

LOPS3	PMRO3	Mode	ROUT3 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 71. Stereo Line Output Mode Select (ROUT3)

L3VL1	L3VL0	Attenuation	
1	1	+3dB	
1	0	0dB	(default)
0	1	–3dB	
0	0	–6dB	

Table 72. Stereo Line Output Volume Setting

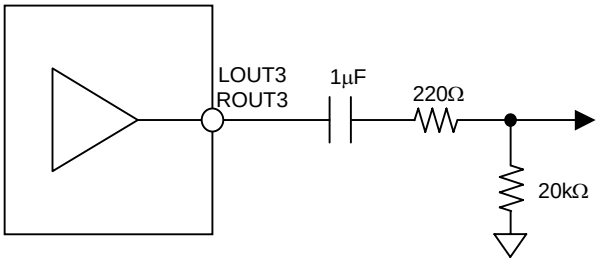


Figure 73. External Circuit for Stereo Line Output (when using Pop Noise Reduction Circuit)

<Stereo Line Output 3 Control Sequence (in case of using Pop Noise Reduction Circuit)>

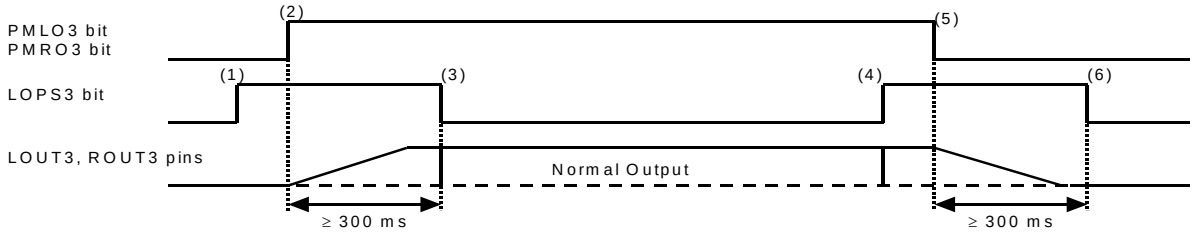


Figure 74. Stereo Line Output 3 Control Sequence (in case of using Pop Noise Reduction Circuit)

(1) Set LOPS3 bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO3=PMRO3 bits = "1". Stereo line output exits the power-down mode.
LOUT3 and ROUT3 pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(3) Set LOPS3 bit = "0" after LOUT3 and ROUT3 pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS3 bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO3=PMRO3 bits = "0". Stereo line output enters power-down mode.
LOUT3 and ROUT3 pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(6) Set LOPS3 bit = "0" after LOUT3 and ROUT3 pins fall down. Stereo line output exits the power-save mode.

<Analog Mixing Circuit for LOUT3/ROUT3>

DACSL, DACSR, LOM3, LINS1, RINS1, LINS2, RINS2, LINS3, RINS3, LINS4, RINS4, LOOPSL, LOOPSR and LOM3 bits control each path switch. The summing gain for each path is 0dB (typ).

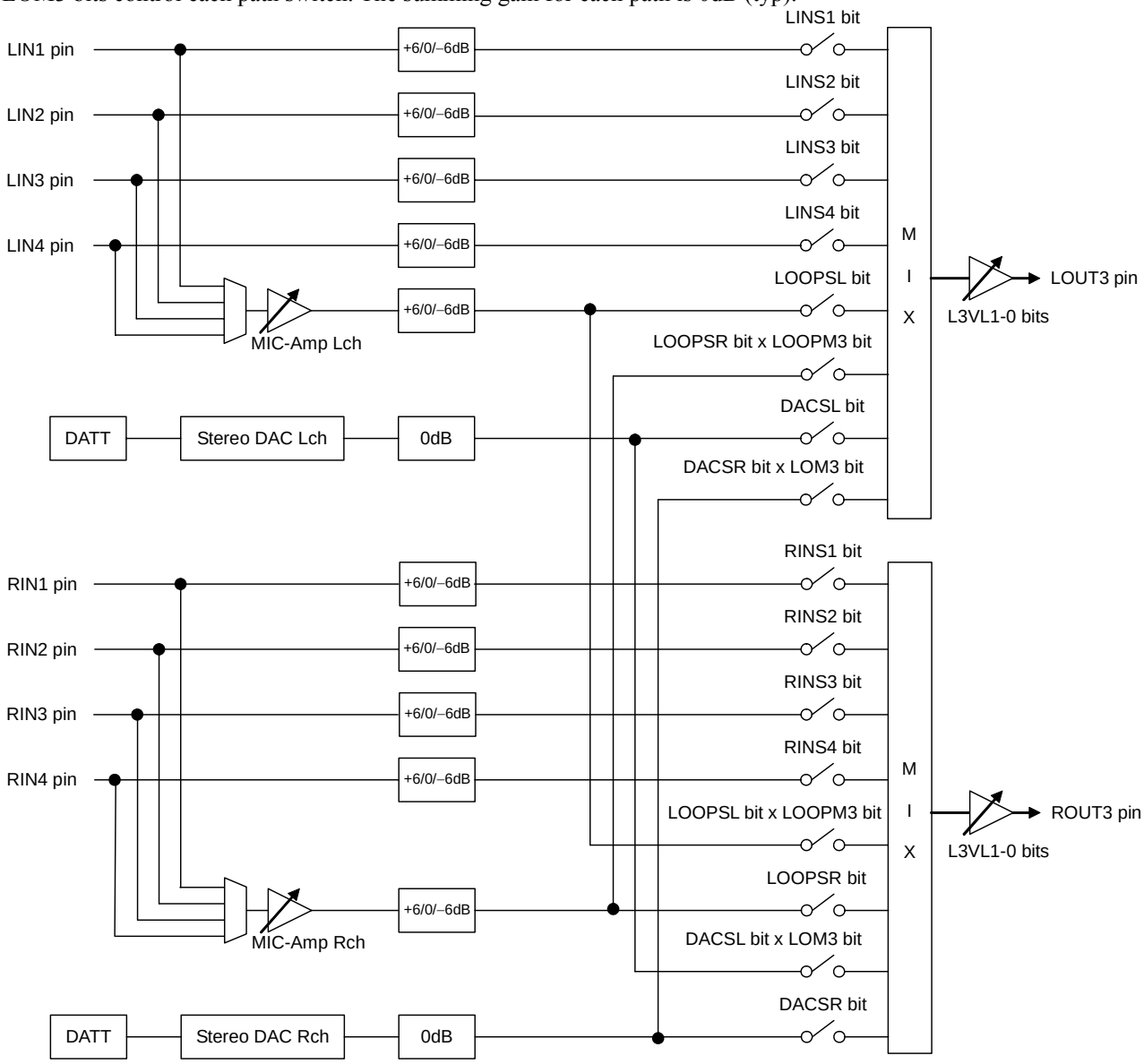


Figure 75. LOUT3/ROUT3 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

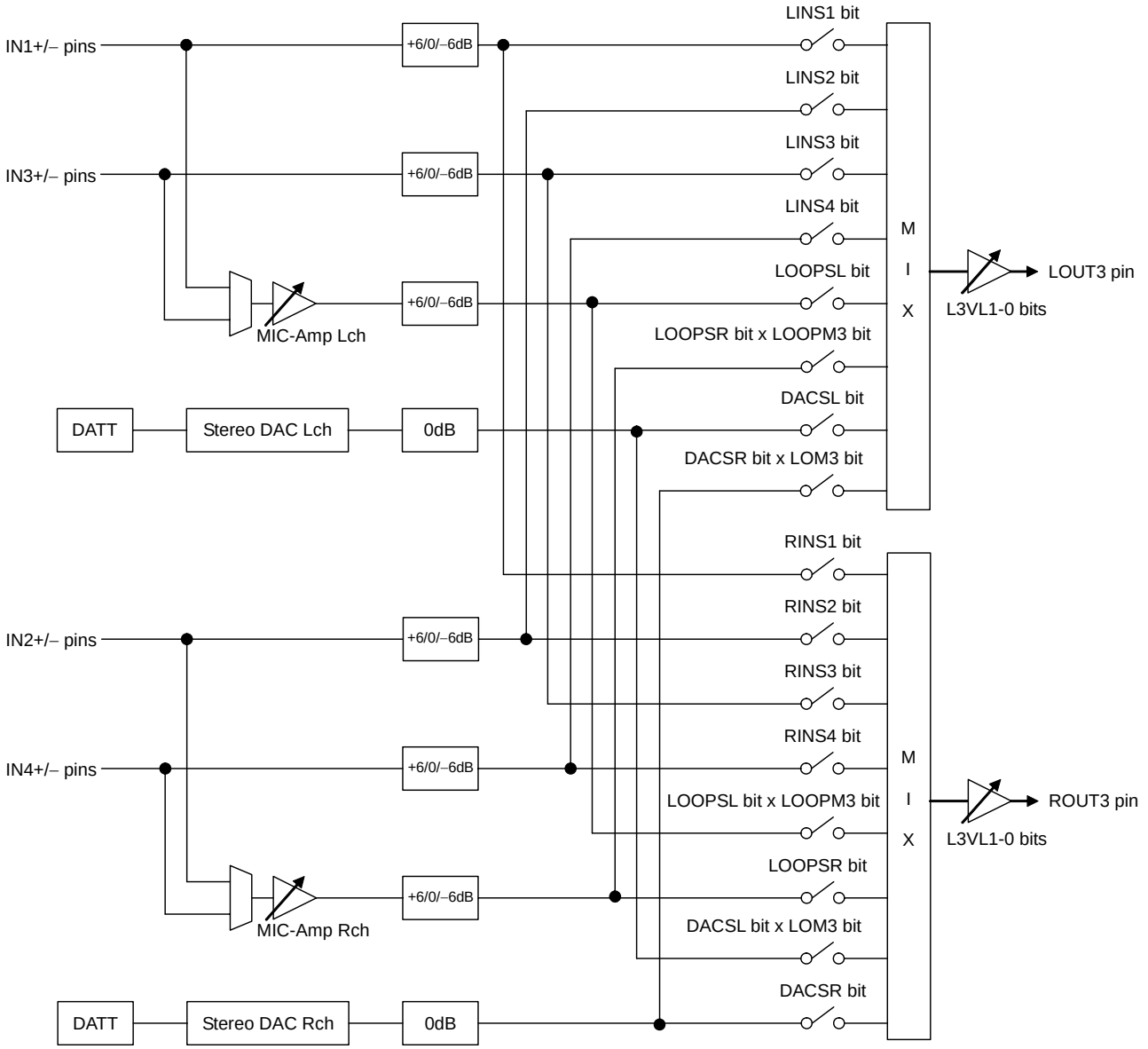


Figure 76. LOUT3/ROUT3 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Full-differential Mono Line Output (LOP/LON pins)

When LODIF bit = "1", LOUT3/ROUT3 pins become LOP/LON pins, respectively. Lch/Rch signal of DAC or LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the LOP/LON pins which is full-differential as (L+R) signal. The load impedance is 10kΩ (min) for the LOP and LON pins, respectively. When the PMLO3 = PMRO3 bits = "0", the mono line output enters power-down mode and the output is pulled-down to VSS1. When the PMLO3 = PMRO3 bits = "1" and LOPS3 bit = "1", mono line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO3 and PMRO3 bits at LOPS3 bit = "0". When PMLO3 = PMRO3 bits = "1" and LOPS3 bit = "0", mono line output enters in normal operation. L3VL1-0 bits set the volume of mono line output.

L3VL1-0	Attenuation	
3H	+9dB	
2H	+6dB	(default)
1H	+3dB	
0H	0dB	

Table 73. Mono Line Output Gain Setting

LOPS3	PMLO3/RO3	Mode	LOP/LON pins	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 74. Mono Line Output Mode Setting (x: Don't care)

<Full-differential Mono Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

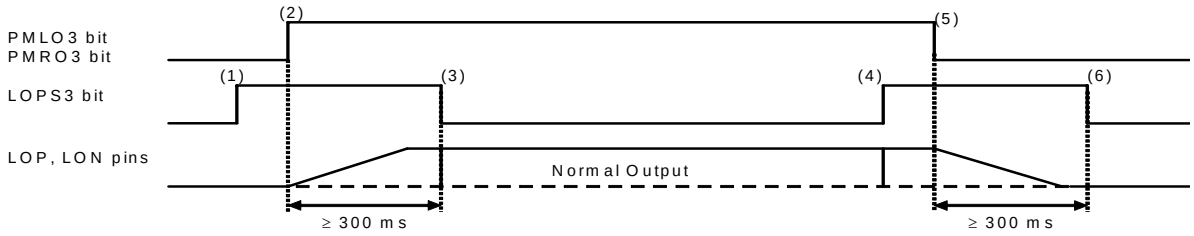


Figure 77. Mono Line Output 3 Control Sequence (when using Pop Noise Reduction Circuit)

(1) Set LOPS3 bit = "1". Mono line output enters the power-save mode.
(2) Set PMLO3 = PMRO3 bits = "1". Mono line output exits the power-down mode.
The LOP and LON pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(3) Set LOPS3 bit = "0" after LOP and LON pins rise up. Mono line output exits the power-save mode.
Mono line output is enabled.
(4) Set LOPS3 bit = "1". Mono line output enters power-save mode.
(5) Set PMLO3 = PMRO3 bits = "0". Mono line output enters power-down mode.
The LOP and LON pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
(6) Set LOPS3 bit = "0" after LOP and LON pins fall down. Mono line output exits the power-save mode.

<Analog Mixing Circuit for Mono Line Output>

DACSL, DACSR, LINS1, RINS1, LINS2, RINS2, LINS3, RINS3, LINS4, RINS4, LOOPSL and LOOPSR bits control each path switch. The summing gain for each path is 0dB (typ).
When MDIF1/2/3/4 bits = "1", RINS1/2/3/4 bits should be "0".

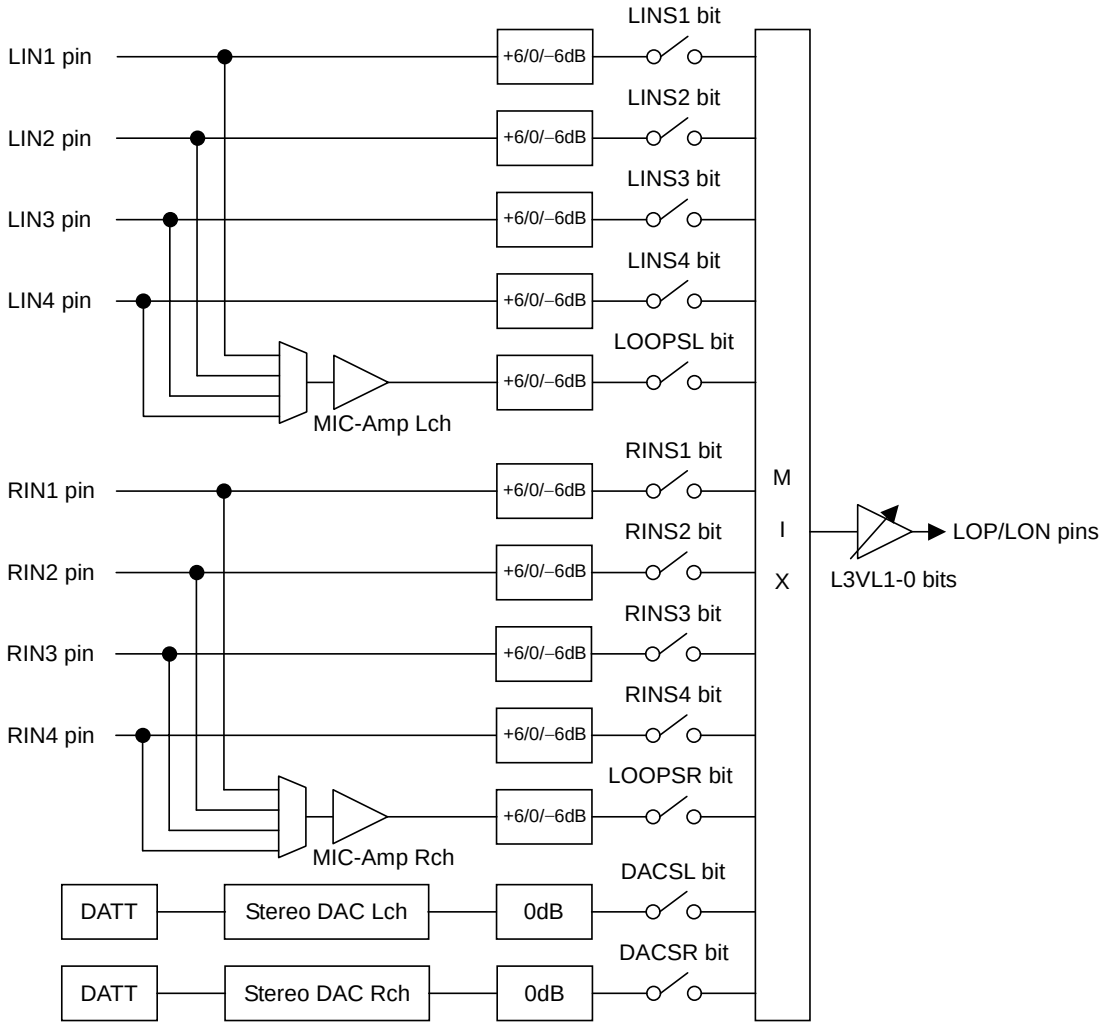


Figure 78. Mono Line Output Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

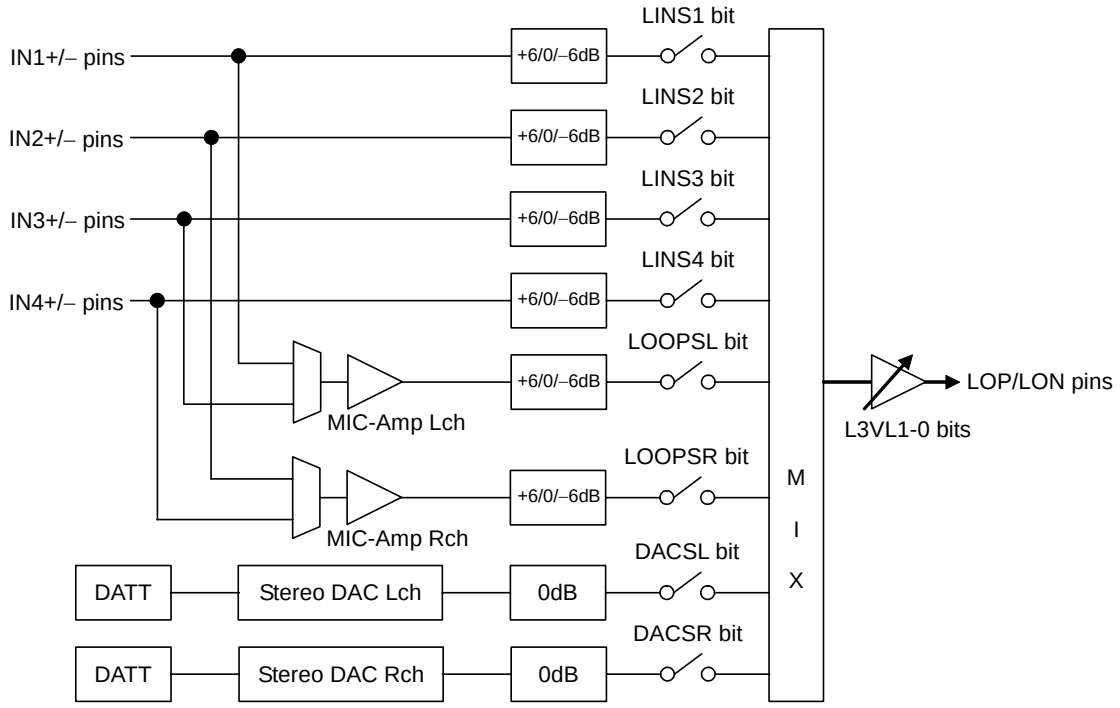


Figure 79. Mono Line Output Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Headphone Volume (LIN1A/RIN1A pins)

The AK4675 has the mixing circuits for headphone amplifier. The each mixing circuit can be controlled independently. When all input paths are OFF, the mixing circuit outputs VCOMA voltage. The volume of each input pin can be controlled independently. The input volume range is from +10 dB to –20dB by 2dB step. When the input volume is changed, pop noise may occur. The input volume has power management mode that is common to the left and right channels. The power-up/down of input volume can be controlled by PMV1 bit. The power-up time of the input volume is 16.4ms (typ.) and 26.3ms(max) at OSCN bit = "0". when OSCN bit = "1", power-up time depends on both the MSEL bit setting and the MCKIA frequency (Table 75). During power-up time, the input volume block outputs VCOMA voltage regardless of the input signal. AC coupling capacitor of 0.22μF or less should be connected at the LIN1A/RIN1A pins to reduce pop noise at the power-up of the input volume block.

MSEL bit	MCKIA Freq	Power-Up Time
0	2.048MHz	16ms (32768/MCKIA)
1	2.8224MHz	17.1ms (49152/MCKIA)
	3.072MHz	16ms (49152/MCKIA)

Table 75. Input Volume Power-Up Time (OSCN bit = "1")

L1V3-0 bits R1V3-0 bits	GAIN (dB)	Step	
FH	+10	2dB	(default)
EH	+8		
:	-		
CH	+4		
BH	+2		
AH	0		
9H	–2		
8H	–4		
:	:		
2H	–16		
1H	–18		
0H	–20		

Table 76. Input Volume Setting

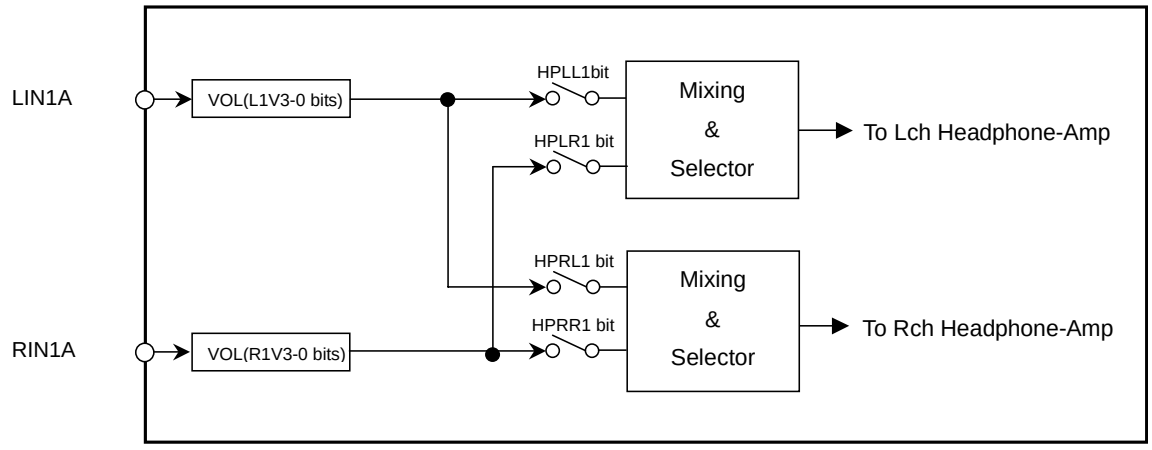


Figure 80. Input Selector & Volume

■ Headphone-Amp (HPL/HPR pins)

Power supply voltage for headphone amplifiers is applied from PVDDA and PVEE pins. The PVEE pin outputs the negative voltage generated by the internal charge pump circuit. The headphone amplifier is single-ended outputs and centered on 0V (VSS3A). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. When the input signal level is 0.7Vrms, the output voltage is 0.69Vrms (= 30mW @ 16Ω) at HPGA4-0 bits = 0dB and HPG bit = 0dB. HPGA3-0 and HPG bits control the output level of headphone-amp. HPGA4-0 bits can control from +12dB to –50dB by 2dB step and HPG bit can control 0dB or +6dB. The volume is common to L/R channels. When the volume is changed, pop noise may occur.

HPGA4-0 bits	GAIN (dB)	Step	
1FH	+12	2dB	
1EH	+10		
:	-		
1AH	+2		
19H	0		(default)
18H	–2		
17H	–4		
16H	–6		
:	:		
2H	–46		
1H	–48		
0H	–50		

Table 77. Headphone-Amp Volume Setting

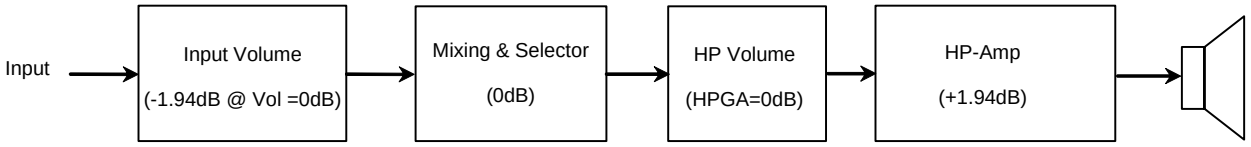


Figure 81. Headphone-Amp Path Level Diagram

The headphone output is enabled when HPMTN bit is "1" and muted when HPMTN bit is "0". PTS1-0 bits set the mute ON/OFF time when MOFF1 bit is "0". When MOFF1 bit is "1", the ON/OFF is switched immediately.

When PMHPL and PMHPR bits are "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS3 voltage via the internal pulled-down resistor. The pulled-down resistor is 20Ω (typ) at HPZ bit = "0", 25kΩ(typ) at HPZ bit = "1". The power-up/down time is 16.4ms (typ.) and 26.3ms (max.)when MOFF0 bit is "0". When MOFF1 bit is "1", the power up/down is switched immediately.

PMCP/PMVCM	PMHPL/R	HPMTN	HPZ	Mode	HPL/R pins	
x	0	x	0	Power-down & Mute	Pull-down by 20Ω (typ)	(default)
x	0	x	1	Power-down	Pull-down by 25kΩ (typ)	
1	1	0	0	Mute	VSS3A	
1	1	1	0	Normal Operation	Normal Operation	

Table 78. Headphone Amplifier Mode Setting (x: Don't care)

<Wired OR with External Headphone-Amp>

In case of OSCN bit = "0", when PMVCMA=PMCP=PMOSC bits are "1" (charge pump circuit is powered-up), the AK4675 HP-Amp can be connected to the external single supply HP-Amp by "wired OR". In case of OSCN bit = "1", when PMVCMA=PMCP=HPZ bits are "1" (charge pump circuit is powered-up), the AK4675 HP-Amp can be connected to the external single supply HP-Amp by "wired OR". The external HP-Amp can output the signal up to ±PVDDA [Vpp] after the charge pump circuit is powered-up.

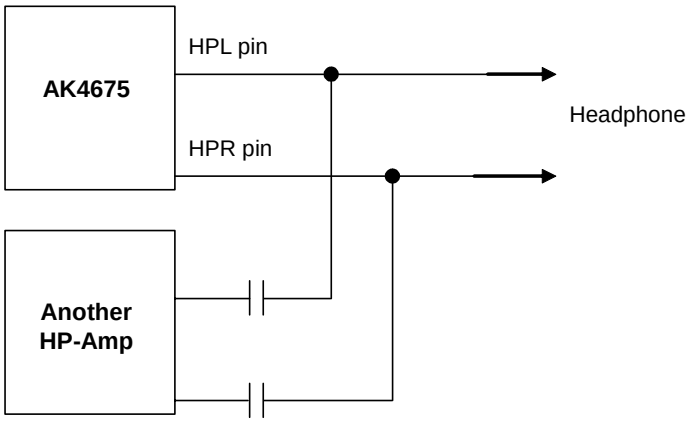


Figure 82. Wired OR with External HP-Amp

■ Charge Pump Circuit

The charge pump operates by the output of a regulator which uses PVDDA voltage. The negative power supply (PVEE) for headphone amplifiers is generated from internal charge pump circuit. The internal charge pump circuit generates negative voltage from PVDDA voltage. The generated voltage (PVEE) is used to headphone amplifiers. When PMCP bit is set to "1", the charge pump circuit is powered-up. PMVCMA and PMOSC bits must be set to "1".

PMOSC and PMVCM bits should be set to "1" when OSCN bit is "0". PMVCM bit should be set to "1" and PMOSC bit set to "0" when OSCN bit is "1". The power-up time of charge pump circuit is typically 6.2ms and maximum 10ms at OSCN bit = "0". when OSCN bit = "1", the power-up time is shown in Table 79. When PMHPL or PMHPR bit is set to "1", the Headphone-Amp is powered-up after the charge pump circuit is powered-up. Figure 87 shows the power-up sequence.

MSEL bit	MCKIA Freq	Power-Up Time
0	2.048MHz	6m (12288/MCKIA)
1	2.8224MHz	6.5ms (18432/MCKIA)
	3.072MHz	6ms (18432/MCKIA)

Table 79. Charge Pump Circuit Power-Up Time (OSCN bit = "1")

■ Transition Time

PUT1-0 bits set the power-up/down time of headphone-amp and PTS1-0 bits set the mute ON/OFF time of headphone-amp. These operations are soft transition.

MOFF bit set the Enable/Disable for the soft transition. The soft transition is disabled while these bits are "1", and ON/OFF is switched immediately.

As shown in Table 80, if the soft transition is enabled, the register value of same address must be changed by an interval more than transition time. The write operation is ignored if the same values are written as the previous write operation.

	Address	Register Name	Enable / Disable
PTS1-0 bits	0DH	HPMTN bit	MOFF bit

Table 80. Registers with Transition Time

PTS1	PTS0	MUTE ON/OFF Time				
		OSCN bit = "0"		OSCN bit = "1"		
		typ.	max	MSEL bit= "0"	MSEL bit = "1"	
0	0	16.4ms	26.3ms	32768/MCKIA	49152/MCKIA	(default)
0	1	32.8ms	51.5ms	65536/MCKIA	98304/MCKIA	
1	0	65.6ms	105.0ms	131072/MCKIA	196608/MCKIA	
1	1	131.2ms	210.0ms	262144/MCKIA	393216/MCKIA	

Table 81. Headphone-Amp Mute ON/OFF Transition Time

■ Speaker-ALC Operation

The ALC (Automatic Level Control) operation of speaker-amp output is executed by ALCA block when ALCA bit = "1". When ALCA bit is "0", the speaker volume depends on the setting value of SPGA5-0 bits.

(1) ALC Limiter Operation

During ALCA limiter operation, when either Lch or Rch exceeds the ALCA limiter detection level (LMTHA bit), the SPGA value (same value for Lch and Rch) is attenuated automatically by the ALCA limiter ATT step (LMATA1-0 bits).

When ZELMNA bit is set to "0" (zero crossing detection is enabled), the SPGA value is changed by ALCA limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTMA1-0 bits set the zero crossing timeout period of both ALCA limiter and recovery operation.

When ZELMNA bit = "1" (zero crossing detection is disabled), SPGA value is immediately changed by ALCA limiter operation. The changing period is typ. 125μs and max. 200μs at OSCN bit = "0", 256/MCKIA (=125μs @MCKIA=2.048MHz at OSCN bit = "1" & MSEL bit = "0", 384/MCKIA (= 125μs @MCKI=3.072MHz) at OSCN bit = "1" & MSEL bit = "1". Attenuation step is fixed to 1 step regardless of the setting of LMATA1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALCA limiter detection level or less. After completing the attenuation operation, unless ALCA bit is changed to "0", the operation repeats when the input signal level exceeds LMTHA bit.

LMTHA	ALCA Limiter Detection Level	ALCA Recovery Waiting Counter Reset Level	
0	ALCA Output ≥ −7.5dBV	−7.5dBV > ALCA Output ≥ −9.5dBV	(default)
1	ALCA Output ≥ −11.5dBV	−11.5dBV > ALCA Output ≥ −13.5dBV	

Note: ALCA limiter detection level and ALCA recovery waiting counter reset level do not depend on operation voltage.

Table 82. ALCA Limiter Detection Level / Recovery Counter Reset Level (2.0Vpp = −3dBV)

ZELMNA	LMATA1	LMATA0	ALCA Limiter ATT Step		
0	0	0	1 step	0.5dB	(default)
	0	1	2 step	1.0dB	
	1	0	4 step	2.0dB	
	1	1	8 step	4.0dB	
1	x	x	1step	0.5dB	

Table 83. ALCA Limiter ATT Step (x: Don't' care)

ZTMA1	ZTMA0	Zero Crossing Timeout				
		OSCN bit = "0"		OSCN bit = "1"		
		typ.	max	MSEL bit= "0"	MSEL bit = "1"	
0	0	16.4ms	26.3ms	32768/MCKIA	49152/MCKIA	
0	1	32.8ms	51.5ms	65536/MCKIA	98304/MCKIA	(default)
1	0	65.6ms	105.0ms	131072/MCKIA	196608/MCKIA	
1	1	131.2ms	210.0ms	262144/MCKIA	393216/MCKIA	

Table 84. ALCA Zero Crossing Timeout Period

(2) ALCA Recovery Operation

ALCA recovery operation waits for the WTMA2-0 bits to be set after completing ALCA limiter operation. If the input signal does not exceed "ALCA recovery waiting counter reset level" during the wait time, ALCA recovery operation is executed. The SPGA value is automatically incremented by RGAINA1-0 bits up to the set reference level (REFA5-0 bits) with zero crossing detection which timeout period is set by ZTMA1-0 bits. Then the SPGA is set to the same value for both channels. ALCA recovery operation is executed at a period set by WTMA2-0 bits. When zero cross is detected at both channels during the wait period set by WTMA2-0 bits, ALCA recovery operation waits until WTMA2-0 period and the next recovery operation is executed. The setting period of WTMA2-0 bits should be same as ZTMA1-0 bits or longer period.

When RGAINA1-0 bits are set to "10", ALCA recovery operation is not executed though ALCA limiter operation is executed.

During the ALCA recovery operation, when the ALCA output level exceeds ALCA limiter detection level (LMTHA bit), the ALCA limiter operation is done immediately.

When
"ALCA recovery waiting counter reset level ≤ ALCA Output Signal < ALCA limiter detection level (LMTHA1-0)" during the ALCA recovery operation, the waiting timer of ALCA recovery operation is reset. When
"ALCA recovery waiting counter reset level > ALCA Output Signal",
the waiting timer of ALCA recovery operation starts.

The ALCA operation corresponds to the impulse noise. When the impulse noise is input, the ALCA recovery operation becomes faster than a normal recovery operation.

WTMA2	WTMA1	WTMA0	Recovery Waiting Timer				
			OSCN bit = "0"		OSCN bit = "1"		
			typ.	max	MSEL bit = "0"	MSEL bit = "1"	
0	0	0	16.4ms	26.3ms	32768/MCKIA	49152/MCKIA	
0	0	1	32.8ms	51.5ms	65536/MCKIA	98304/MCKIA	
0	1	0	65.6ms	105.0ms	131072/MCKIA	196608/MCKIA	
0	1	1	131.2ms	210.0ms	262144/MCKIA	393216/MCKIA	
1	0	0	262.4ms	419.9ms	524288/MCKIA	786432/MCKIA	
1	0	1	524.8ms	839.7ms	1048576/MCKIA	1572864/MCKIA	(default)
1	1	0	1049.6ms	1679.4ms	2097152/MCKIA	3145728/MCKIA	
1	1	1	2099.2ms	3358.8ms	4194304/MCKIA	6291456/MCKIA	

Table 85. ALCA Recovery Waiting Timer Period

RGAINA1	RGAINA0	GAIN STEP		
0	0	1 step	0.5dB	(default)
0	1	2 step	1.0dB	
1	0	0 step	0dB	
1	1	Reserved		

Table 86. ALCA Recovery GAIN Step

REFA5-0	GAIN (dB)	Step	
3FH	+19.5	0.5dB	
3EH	+19.0		
3DH	+18.5		
3CH	+18.0		(default)
:	:		
19H	+0.5		
18H	0.0		
17H	−0.5		
:	:		
02H	−11.0		
01H	−11.5		
00H	−12.0		

Table 87. Reference Level at ALCA Recovery Operation

(3) Example of ALCA Operation

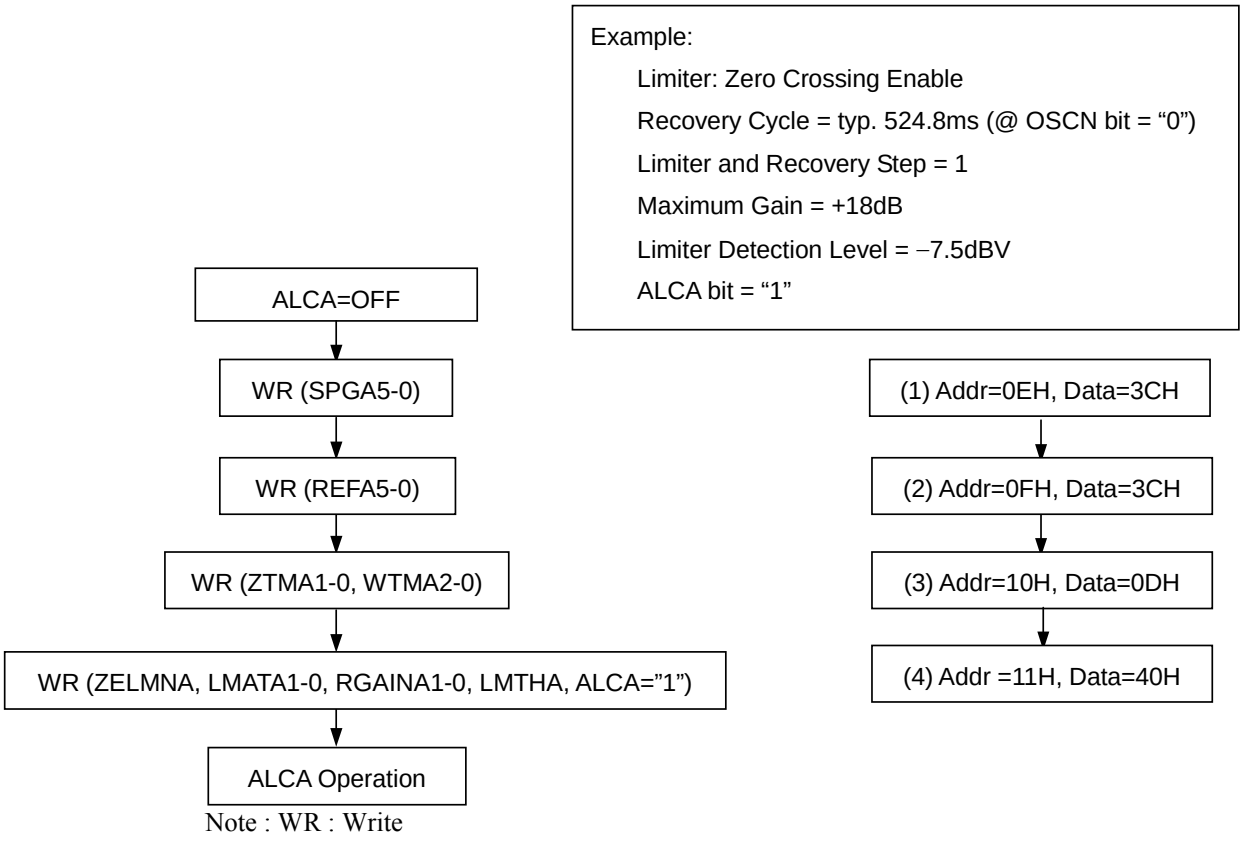
Table 88 shows the example of the ALCA setting. The ALCA starts from the value of SPGA5-0 bits.

Register Name	Comment	Data	Parameter
LMTHA	Limiter detection Level	0	−7.5dBV
ZELMNA	Limiter Zero crossing Enable	0	Limiter Zero Crossing Enable
WTMA2-0	Recovery waiting period	101	Typ. 524.8ms (@ OSCN bit = “0”)
REFA5-0	Maximum gain at recovery operation	3CH	+18dB
LMATA1-0	Limiter ATT Step	00	0.5dB
RGAINA1-0	Recovery GAIN Step	00	0.5dB
ZTMA1-0	Zero-crossing Timeout	01	Typ. 32.8ms (@ OSCN bit = “0”)
ALCA	ALCA Enable bit	1	Enable

Table 88. Example of the ALCA setting

The following registers must not be changed during ALCA operation. These bits should be changed after ALCA operation is finished by ALCA bit = “0”.

- LMTHA, LMATA1-0, WTMA2-0, RGAINA1-0, REFA5-0, ZTMA1-0, ZELMNA bits



Note : WR : Write

Figure 83. Registers set-up sequence at ALCA operation

■ Speaker Volume (SPGA: Manual Mode)

The speaker volume becomes manual mode when ALCA bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for ALCA operation (ZTMA1-0, LMTHA and etc).
2. When the registers for ALCA operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When SPGA is used as a manual volume.

SPGA5-0 bits set the gain of the volume control. The SPGA value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTMA1-0 bits. In case of OSCN bit = "0", the write operation to SPGA5-0 bits is prohibited during 1.6ms after PMSPL or PMSPR bit is set to "1". In case of OSCN bit = "1", the write operation to SPGA5-0 bits is prohibited during the power-up time of the speaker volume block (Table 91) after PMSPL or PMSPR bit is set to "1". The speaker volume is powered-up as the default value (0dB) regardless of the setting of SPKG5-0 bits.

SPGA5-0	GAIN (dB)	Step	
3FH	+19.5	0.5dB	
3EH	+19.0		
3DH	+18.5		
3CH	+18.0		
:	:		
19H	+0.5		
18H	0.0		(default)
17H	–0.5		
:	:		
02H	–11.0		
01H	–11.5		
00H	–12.0		

Table 89. Speaker-Amp Volume Setting

When writing to the SPGA5-0 bits continuously, the control register should be written in an interval more than zero crossing timeout.

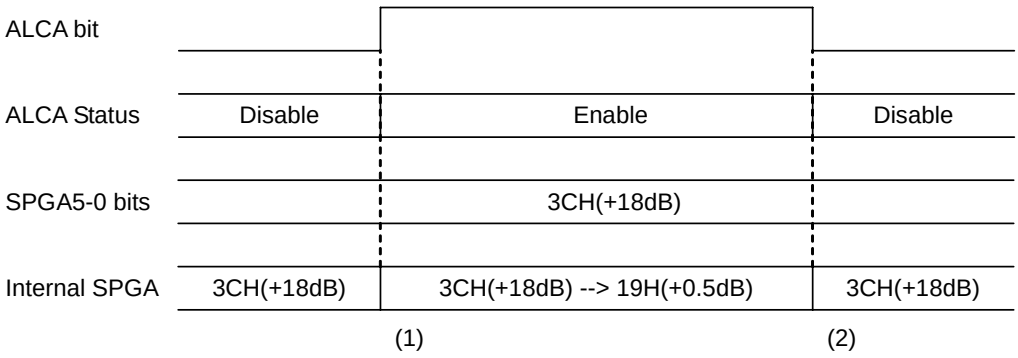


Figure 84. SPGA value during ALCA operation

(1) ALCA operation starts from the SPGA value when ALCA bit is changed to "1".
(2) Writing to SPGA registers is ignored during ALCA operation. After ALCA is disabled, the SPGA changes to the last written data by twice period of zero crossing or timeout. When ALCA is enabled again, ALCA bit should be set to "1" in an interval more than zero crossing timeout period after ALCA bit = "0".

■ Class-D Speaker-Amp

The output signal from ALC block is converted by PWM and is outputted from the SPP/SPN pins by BLT. The signal of ALC block is input from the SPIN pin. A 0.1uF capacitor should be connected between the LOUT3 (ROUT3) pin and the SPIN pin in order to cancel DC offset of Line Out circuit.

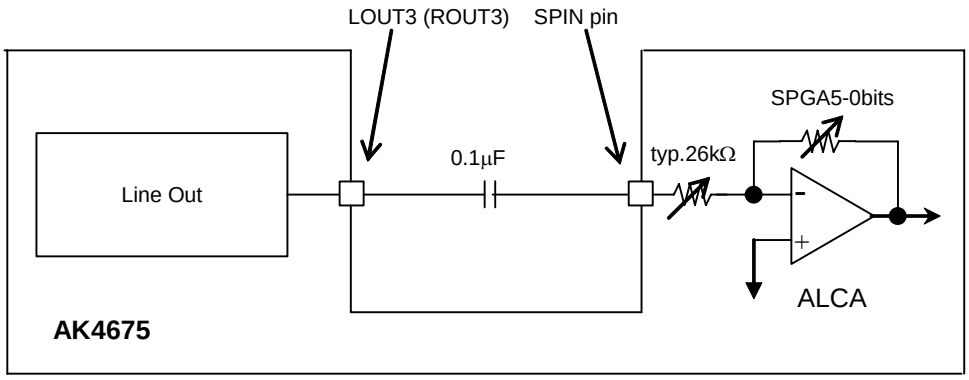


Figure 85. Example of normal connection for Speaker (fc = 66Hz @ -3dB)

When the input signal level is 0.56Vrms, the speaker-amp outputs 0.6W. The internal default gain is +11.76dB. The SPK-Amp outputs 0.6W(/1ch) when 0.56Vrm mono signal is input at single-end mode and ALC = OFF (SPGA=0dB).

When ALCA = ON (ALCA bit= "1"), ALCA outputs -7.5dBV ~ -9.5dBV if LMTHA bit = "0", and outputs -11.5dBV ~ -13.5dBV if LMTHA bit = "1". REFA5-0 bits set the reference level. The internal gain of the class-D speaker amplifier is fixed to +11.76dB.

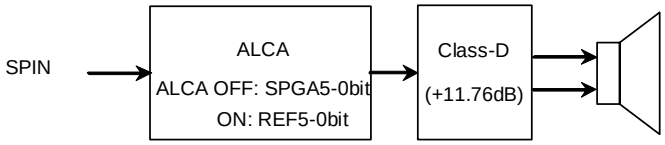


Figure 86. Speaker-Amp Path Level Diagram

When PMSPL and PMSPR bits are set to "0", the speaker block (ALC + Speaker-Amp) can be powered-down completely. In case of OSCN bit = "0", the power-up/down time is 30ms (typ.) and 48ms (max.). In case of OSCN bit = "1", the power-up/down time depends on MSEL bit setting and MCKIA frequency (Table 90).

MSEL bit	MCKIA Freq	Power-Up Time
0	2.048MHz	19.5ms (40000/MCKIA)
1	2.8224MHz	21.5ms (60000/MCKIA)
	3.072MHz	19.5ms (60000/MCKIA)

Table 90. Class D SPK-Amp Power-Up Time (OSC bit = "1")

In case of OSCN bit = "0", the write operation to SPGA5-0 bits is prohibited during 1.6ms after PMSPL or PMSPR bit is set to "1". In case of OSCN bit = "1", the write operation to SPGA5-0 bits is prohibited during the power-up time of the speaker volume block (Table 91) after PMSPL or PMSPR bit is set to "1".

MSEL bit	MCKIA Freq	Power-Up Time
0	2.048MHz	1ms (2048/MCKIA)
1	2.8224MHz	1.1ms (3072/MCKIA)
	3.072MHz	1ms (3072/MCKIA)

Table 91. Write Operation Prohibited Time of Speaker Volume after Power-up (OSCN bit = "1")

PMSP bits	Speaker-Amp	
0	Power-down & Hi-Z	(default)
1	Power-up & Output	

Table 92. Speaker-Amp Output State

■ Thermal Shutdown Function

When the internal device temperature rises up irregularly (e.g. output pins of speaker amplifier are shortened), the charge pump circuit, headphone amplifier and speaker amplifier are automatically powered-down and then THDET bit becomes "1". The powered-down charge pump circuit, headphone amplifier and speaker amplifier do not return to normal operation unless HP/SPK-Amp blocks of the AK4675 are reset by the PDNA pin "L". The device status can be monitored by THDET bit.

■ HP/SPK-Amp Operation Clock

The AK4675 includes built-in clock oscillator for the internal operation of Class-D Speaker-Amp and Charge Pump circuit. The AK4675 supports both internal oscillator mode and external clock mode (MCKIA pin). MSEL bit selects the clock frequency for the MCKIA pin.

OSCN bit	Operation Clock	
0	Internal OSC	(default)
1	External Clock (MCKIA pin)	

Table 93. Internal Oscillator / External Clock select

MSEL bit	MCKIA Frequency	
0	2.048MHz	(default)
1	2.8224MHz or 3.072MHz	

Table 94. MCKIA Input Frequency Select

■ HP/SPK-Amp Block Power-Up/Down Sequence

1) HP-Amp

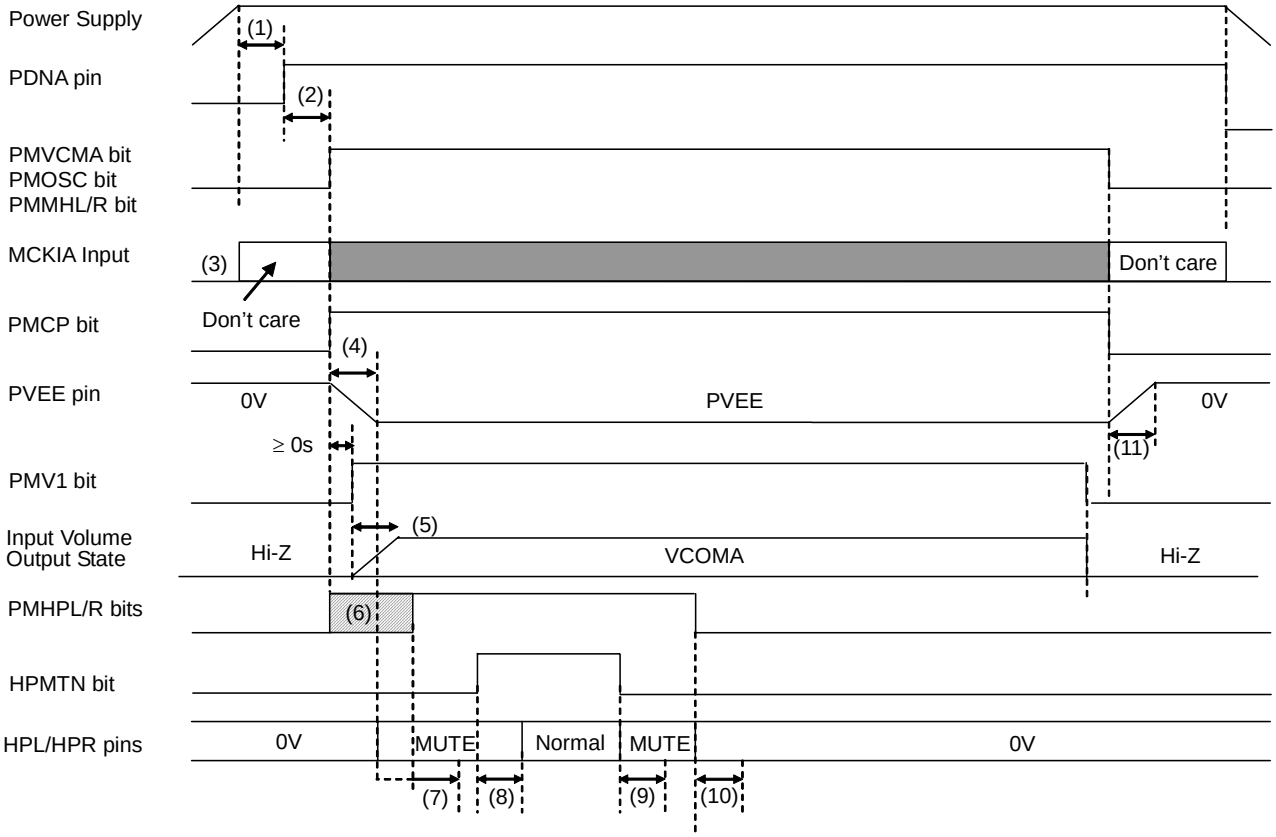


Figure 87. HP-Amp Power-up/down Sequence Example

(1) PDNA pin should be changed from "L" to "H" after power up.
"L" time of 150ns or more is needed to reset the AK4675.
The PDNA pin must be held to "L" until all power supply pins are supplied. After that, the PDNA pin should be set to "H".

(2) PTS1-0, MOFF, HPGA4-0, OSCN, MSEL bits should be set during this period.

(3) In case of OSCN bit = "0", the external clock (MCKIA pin) is not needed.
In case of OSCN bit = "1", the external clock (MCKIA pin) is needed.

(4) Power-up of Charge Pump, VCOMA and HP-Amp Mixer & Selector (and the internal clock oscillator in case of OSCN bit = "0"): PMCP = PMMHL = PMMHR = PMOSC = PMVCMA bits = "0" → "1"
The PVEE pin becomes PVEE voltage within 10ms (max.) at OSCN bit = "1" or within the time in Table 79 at OSCN bit = "1".

(5) Power-up of input volume: PMV1 bit = "0" → "1"
Input volume setting (L1V3-0, R1V3-0 bits)
Input path setting (HPLL1, HPLR1, HPRR1, HPRL1 bits)
Input volume block is powered-up within 26.3ms (max.) at OSCN bit = "0" or within the time in Table 75 at OSCN bit = "1". Input path and volume can be set when input volume block is powered up.

(6) If PMCP and PMHPL/R bits are set to "1" at the same time or PMHPL/R bits are set to "1" during the power-up time of the Charge Pump circuit, Headphone-Amp is powered-up after the Charge Pump circuit is powered-up.

(7) Headphone-Amp power-up: PMHPL/R bits = "0" → "1"
Headphone-Amp is in the mute state and outputs the DC offset. Headphone-Amp power-up time depends on the setting of OSCN bit. When OSCN bit = "0", it is 26.3ms (max.) When OSCN bit = "1", refer to Table 81.

(8) Headphone-Amp mute release: HPMTN bit = "0" → "1"
Headphone-Amp goes to the normal operation after the transition time. Headphone-Amp mute release time depends on the setting of PTS1-0 and MOFF1 bits.

(9) Headphone-Amp mute: HPMTN bit = "1" → "0"

Headphone-Amp goes to mute state after the transition time set by PTS1-0 and MOFF1 bits.

(10) Headphone-Amp power-down: PMHPL/R bits = "1" → "0"
Headphone-Amp is powered-down immediately.

(11) Power-down of Charge Pump, VCOMA and HP-Amp Mixer & Selector (and the internal clock oscillator in case of OSCN bit = "0"): PMCP = PMMHL = PMMHR = PMOSC = PMVCMA bits = "1" → "0"
The PVEE pin goes 0V according to the time constant of the capacitor at the PVEE pin and the internal resistor. The internal resistor is typ. 17.5kΩ. Charge Pump circuit can be powered-up during this period.

2) SPK-Amp (SPIN to SPP/SPN)

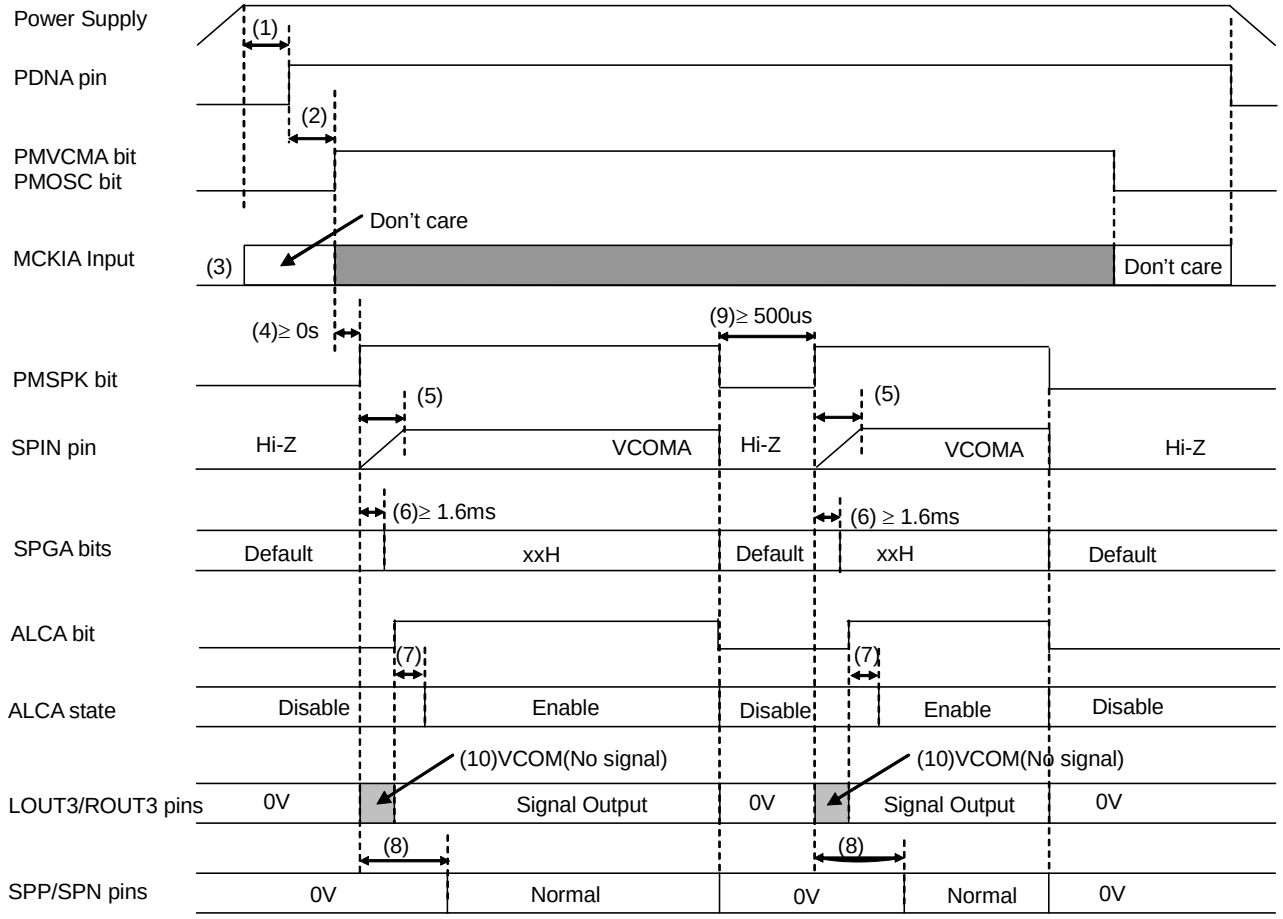


Figure 88. SPK-Amp Power-up/down Sequence Example

(1) The PDNA pin should be changed from "L" to "H" after the power is supplied.
"L" time of 150ns or more is needed to reset the AK4675.
The PDNA pin must be held to "L" until all power supply pins are applied. After that, the PDNA pin should be set to "H".

(2) Power-up of VCOMA (and the internal clock oscillator in case of OSCN bit = "0"): PMVCMA= PMOSC bits = "0" → "1". OSCN and MSEL bits should be set during this period.

(3) In case of OSCN bit = "0", the external clock (MCKIA pin) is not needed.
In case of OSCN bit = "1", the external clock (MCKIA pin) is needed.

(4) Speaker-Amp power-up: PMSPK bit = "0"→ "1"
Stereo line output3 power-up: PMLO3/RO3 bits = "0"→ "1"(LOPS3 bit = "0")

(5) The SPIN pin goes to "H" in 26.3ms (max) when OSCN bit = "0", in the time shown in Table 75 when OSCN bit= "1".

(6) SPGA5-0 bits setting: When PMSP bits = "0", SPGA5-0 bits are default value (0dB). The setting of SPKG5-0 and ALCA bits is enabled at 1.6ms or more after PMSP bits are set to "1" at OSCN bit = "0" or after the power-up time in Table 91 at OSCN bit = "1".

(7) ALCA setting: ALCA is enabled at 30ms (max.) in case of OSCN bit = "0", at 36864/MCKIA (= 18ms @ MCKIA = 2.048MHz) in case of OSCN bit = "1" & MSEL bit = "0", or 55296/MCKIA (= 18ms @ MCKIA = 3.072MHz) in case of OSCN bit = MSEL bit = "1". Refer to "Example of ALCA Operation".

(8) Speaker-Amp goes to normal operation at 48ms (max.) after PMSPL/R bits is changed to "1" in case of OSCN bit = "0" or after the power-up time in Table 90 in case of OSCN bit = "1".

(9) Once Speaker-Amp is powered-down, Speaker-Amp can be powered-up again at 500μs or more later in case of OSCN bit = "0", at 1024/MCKIA (=500μs @ MCKI = 2.048MHz) or more later in case of OSCN bit = "1" & MSEL bit = "0", 1536/MCKIA (=500μs @ MCKIA = 3.072MHz) or more later in case of OSCN bit = MSEL bit = "1".

(10) Signal input to the SPIN pin is prohibited when ALCA bit = "0". The path selecting bits of the stereo line output3 (LOUT3/ROUT3 pins) must be set OFF(DACSL/R, LINS1, LINS2, LINS3, LINS4, RINS1, RINS2, RINS3, RINS4, LOOPSL/R bits = "0").

■ System Clock (PCM I/F)

A reference clock of PLLBT is selected among the input clocks to the SYNCA, BICKA, SYNCB or BICKB pin. The required clock to PCM I/F is generated by an internal PLLBT circuit. PLLBT circuit is powered up by PMPCM bit. Input frequency is selected by PLLBT3-0 bits (Table 95). BCKO2 bit select the output clock frequency of the BICKA or BICKB pin (Table 96).

The AK4675 does not support master mode for both PCM I/F A and B nor slave mode for both PCM I/F A and B. Whether PCM I/F A or B should be set as slave mode. When PMPCM bit is "0", SYNCA, BICKA, SYNCB and BICKB pins are Hi-Z. Table 97 indicates the output data of the SDTOA and SDTOB pins in case of PMPCM bit = "0" and during lock time in Table 95, respectively. Table 98 indicates the output clock at master mode during lock time in Table 95.

The AK4675 does not support master mode for both PCM I/F A and B nor slave mode for both PCM I/F A and B. When PMPCM bit is "0", the SYNCA, BICKA, SYNCB and BICKB pins are Hi-Z.

Mode	PLLBT3	PLLBT2	PLLBT1	PLLBT0	Reference Clock Input Pin	Frequency	R, C at VCOCBT pin		Lock Time (max)	
							R	C		
0	0	0	0	0	SYNCA	1fs2	6.8k	220n	260ms	(default)
1	0	0	0	1	BICKA	16fs2	10k	4.7n	40ms	
2	0	0	1	0	BICKA	32fs2	10k	4.7n	40ms	
3	0	0	1	1	BICKA	64fs2	10k	4.7n	40ms	
4	0	1	0	0	SYNCB	1fs2	6.8k	220n	260ms	
5	0	1	0	1	BICKB	16fs2	10k	4.7n	40ms	
6	0	1	1	0	BICKB	32fs2	10k	4.7n	40ms	
7	0	1	1	1	BICKB	64fs2	10k	4.7n	40ms	
11	1	0	1	1	BICKA	48fs2	10k	4.7n	40ms	
15	1	1	1	1	BICKB	48fs2	10k	4.7n	40ms	
Others					N/A					

Note 83. Mode 1 is available at only FMTA1 bit = "0".
Note 84. Mode 5 is available at only FMTB1 bit = "0".

Table 95. PLLBT Reference Clock

BCKO2 bit	BICKA/BICKB Output Frequency	
0	16fs2	(default)
1	32fs2	

Table 96. BICKA/B Output Frequency

Mode	PMPCM bit = "0"	After PMPCM bit = "0" → "1" & Before SYNCA/SYNCB Input	PMPCM bit = "1" During Lock time
16bit Linear	L	L	"0000H"
8bit A-Law	L	H	"11010101b"
8bit μ-Law	L	H	"11111111b"

Table 97. SDTOA, SDTOB pins Output Data

Format	SYNCA, SYNCB	BICKA, BICKB
Except for I^2S	L	L
I^2S	H	L

Table 98. Output Clock during Lock Time

a) PLLBT reference clock: SYNCA or BICKA pin

The PLLBT circuit generates the required clock for PCM I/F from SYNCA or BICKA. Generated clocks are output via the SYNCB and BICKB pins.

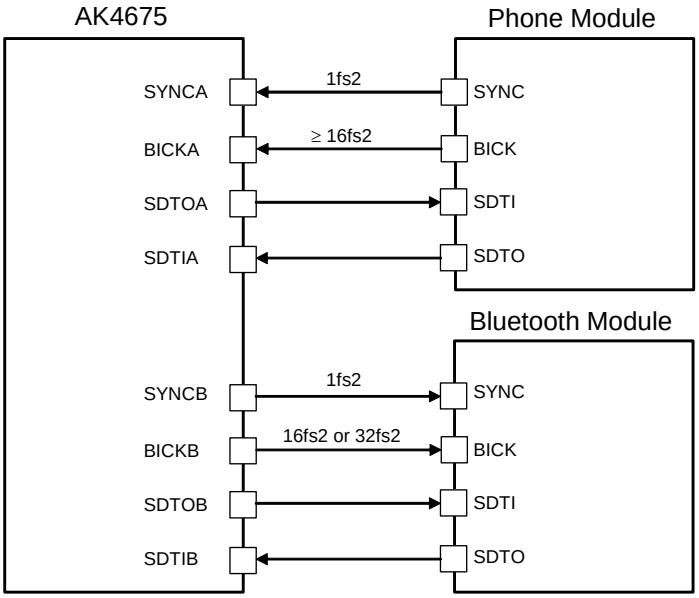


Figure 89. PCM I/F (PLLBT Reference Clock: SYNCA or BICKA pin)

b) PLLBT reference clock: SYNCB or BICKB pin

The PLLBT circuit generates the required clock for PCM I/F from SYNCB or BICKB. Generated clocks are output via the SYNCA and BICKA pins.

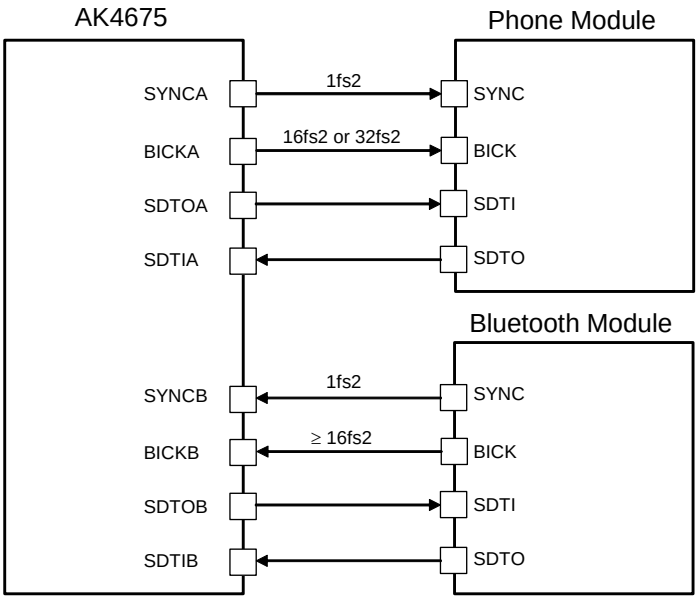


Figure 90. PCM I/F (PLLBT Reference Clock: SYNCB or BICKB pin)

PLLBT should always be powered-up (PMPCM bit = "1") whenever SRC-A or SRC-B is in operation (PMSRA bit = "1" or PMSRB bit = "1"). If PLLBT is powered-down, the AK4675 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If PLLBT is powered-down, SRC-A and SRC-B should be in the power-down mode (PMSRA=PMSRB bits = "0").

■ PCM I/F Master Mode/Slave Mode

The PLLBT2 bit selects either master or slave mode (Table 99). When either PCM I/F A or PCM I/F B is set in slave mode, the other is set in master mode. (For example, when PCM I/F B is set in slave mode, PCM I/F A is set in master mode.) When the AK4675 is power-down mode (PDN pin = "L") or PMPCM bit = "0", each clock pins (SYNCA, BICKA, SYNCB, BICKB) of PCM I/F become a Hi-Z (Table 100).

PLLBT3-0 bits should be set when PMPCM bit = "0" to avoid shorting out of the slave mode clock pins and master mode clock output.

After setting the PDN pin = "H", the PCM I/F clock pins are the Hi-Z state until PMPCM bit becomes "1". The PCM I/F clock pins of master mode should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

PLLBT2 bit	PCM I/F A	SYNCA, BICKA pins	PCM I/F B	SYNCB, BICKB pins	
0	Slave Mode	Input	Master Mode	Output	(default)
1	Master Mode	Output	Slave Mode	Input	

Table 99. Select PCM I/F Master/Slave Mode

PDN pin	PMPCM bit	SYNCA, BICKA pin	SYNCB, BICKB pin
L	-	Hi-Z	Hi-Z
H	0	Hi-Z	Hi-Z
	1	I/O Select by PLLBT2 bit (Table 99)	I/O Select by PLLBT2 bit (Table 100)

Table 100. PCM I/F Clock I/O State

■ PCM I/F A & B Format

The AK4675 supports dual PCM I/F (PCM I/F A & PCM I/F B) that supports 3 kind of I/F (16bit Linear, 8bit A-Law and 8bit μ-Law) independently (Table 101, Table 102).

Mode	LAWA1	LAWA0	Format	
0	0	0	16bit Linear	(default)
1	0	1	N/A	
2	1	0	8bit A-Law	
3	1	1	8bit μ-Law	

Table 101. PCM I/F A Mode

Mode	LAWB1	LAWB0	Format	
0	0	0	16bit Linear	(default)
1	0	1	N/A	
2	1	0	8bit A-Law	
3	1	1	8bit μ-Law	

Table 102. PCM I/F B Mode

Four types of data formats are available and are selected by setting the FMTA1-0 and FMTB1-0 bits independently (Table 103, Table 104). In 16bit Linear mode, the serial data is MSB first, 2's complement format. In 8bit A-Law and μ-Law Mode, the serial data is MSB first. PCM I/F formats can be used in both master and slave modes. SYNCA/B and BICKA/B are output from the AK4675 in master mode, but must be input to the AK4675 in slave mode.

Mode	FMTA1	FMTA0	Format	BICKA	Figure	
0	0	0	Short Frame Sync	≥ 16fs2	See Table 105	(default)
1	0	1	Long Frame Sync	≥ 16fs2	See Table 107	
2	1	0	MSB justified	≥ 32fs2	Figure 99	
3	1	1	I^2S	≥ 32fs2	Figure 100	

Table 103. PCM I/F A Format

Mode	FMTB1	FMTB0	Format	BICKB	Figure	
0	0	0	Short Frame Sync	≥ 16fs2	See Table 106	(default)
1	0	1	Long Frame Sync	≥ 16fs2	See Table 108	
2	1	0	MSB justified	≥ 32fs2	Figure 99	
3	1	1	I^2S	≥ 32fs2	Figure 100	

Table 104. PCM I/F B Format

In modes 2/ 3, the SDTOA/B is clocked out on the falling edge ("↓") of BICKA/B and the SDTIA/B is latched on the rising edge ("↑").

In Modes 0 and 1, PCM I/F A timing is changed by BCKPA and MSBSA bits, and PCM I/F B timing is changed by BCKPB and MSBSB bits.

When BCKPA bit = "0", the SDTOA is clocked out on the rising edge ("↑") of BICKA and the SDTIA is latched on the falling edge ("↓"). When BCKPA bit = "1", the SDTOA is clocked out on the falling edge ("↓") of BICKA and the SDTIA is latched on the rising edge ("↑").
MSBSA bit can shift the MSB position of SDTOA and SDTIA by half period of BICKA.

When BCKPB bit = "0", the SDTOB is clocked out on the rising edge ("↑") of BICKB and the SDTIB is latched on the falling edge ("↓"). When BCKPB bit = "1", the SDTOB is clocked out on the falling edge ("↓") of BICKB and the SDTIB is latched on the rising edge ("↑").
MSBSB bit can shift the MSB position of SDTOB and SDTIB by half period of BICKB.

MSBSA	BCKPA	Data Interface Format	Figure
0	0	MSB of SDTOA is output by the falling edge (“↓”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 91
0	1	MSB of SDTOA is output by the falling edge (“↓”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 92
1	0	MSB of SDTOA is output by the rising edge (“↑”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 93
1	1	MSB of SDTOA is output by the falling edge (“↓”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 94

Table 105. PCM I/F A Format in Mode 0

MSBSB	BCKPB	Data Interface Format	Figure
0	0	MSB of SDTOB is output by the falling edge (“↓”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 91
0	1	MSB of SDTOB is output by the falling edge (“↓”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 92
1	0	MSB of SDTOB is output by the rising edge (“↑”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 93
1	1	MSB of SDTOB is output by the falling edge (“↓”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 94

Table 106. PCM I/F B Format in Mode 0

MSBSA	BCKPA	Data Interface Format	Figure
0	0	MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 95
0	1	MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 96
1	0	MSB of SDTOA is output by the rising edge (“↑”) of the first BICKA after the falling edge (“↓”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 97
1	1	MSB of SDTOA is output by the falling edge (“↓”) of the first BICKA after the falling edge (“↓”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 98

Table 107. PCM I/F A Format in Mode 1

MSBSB	BCKPB	Data Interface Format	Figure
0	0	MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 95
0	1	MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 96
1	0	MSB of SDTOB is output by the rising edge (“↑”) of the first BICKB after the falling edge (“↓”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 97
1	1	MSB of SDTOB is output by the falling edge (“↓”) of the first BICKB after the falling edge (“↓”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 98

Table 108. PCM I/F B Format in Mode 1

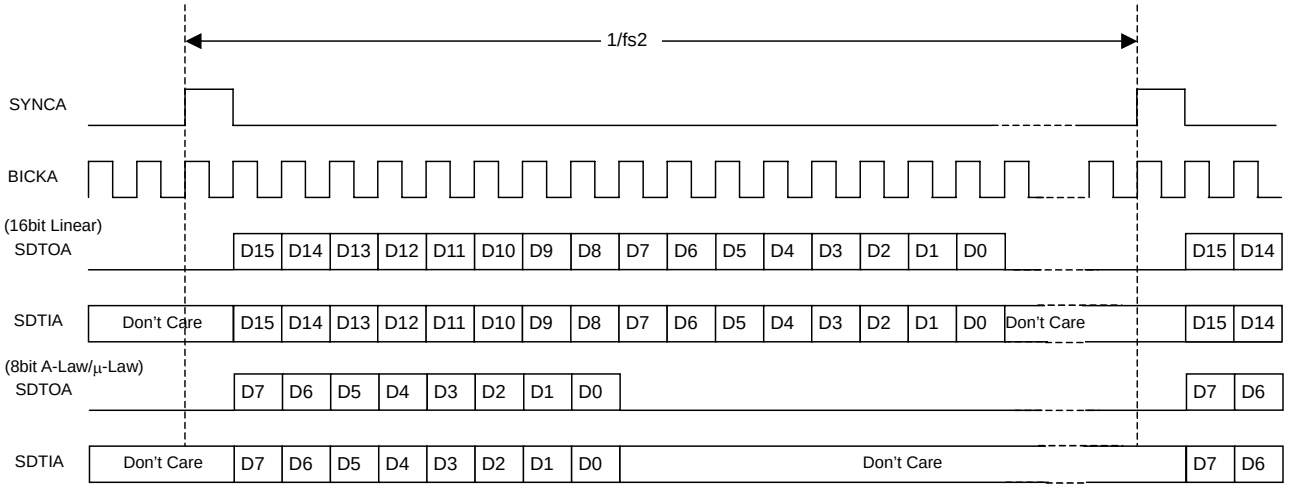


Figure 91. Timing of Short Frame Sync (MSBSA bit = "0", BCKPA bit = "0")

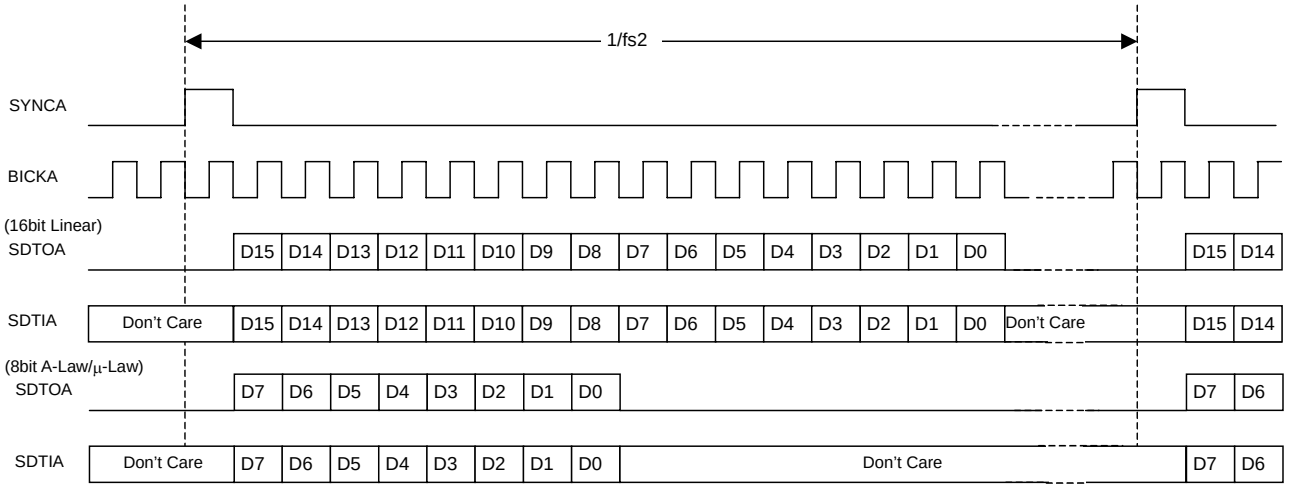


Figure 92. Timing of Short Frame Sync (MSBSA bit = "0", BCKPA bit = "1")

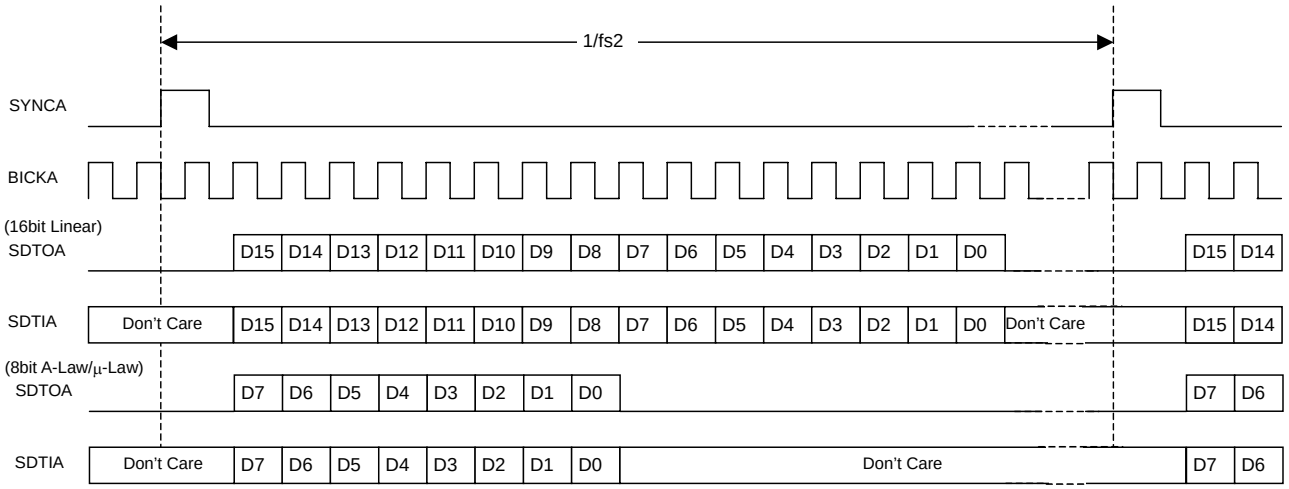


Figure 93. Timing of Short Frame Sync (MSBSA bit = "1", BCKPA bit = "0")

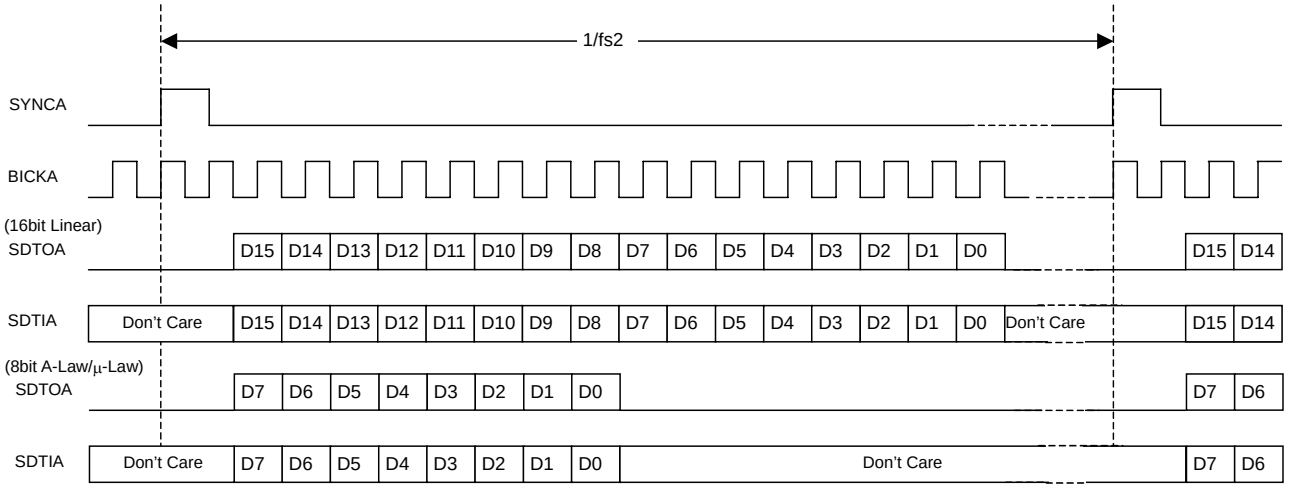


Figure 94. Timing of Short Frame Sync (MSBSA bit = "1", BCKPA bit = "1")

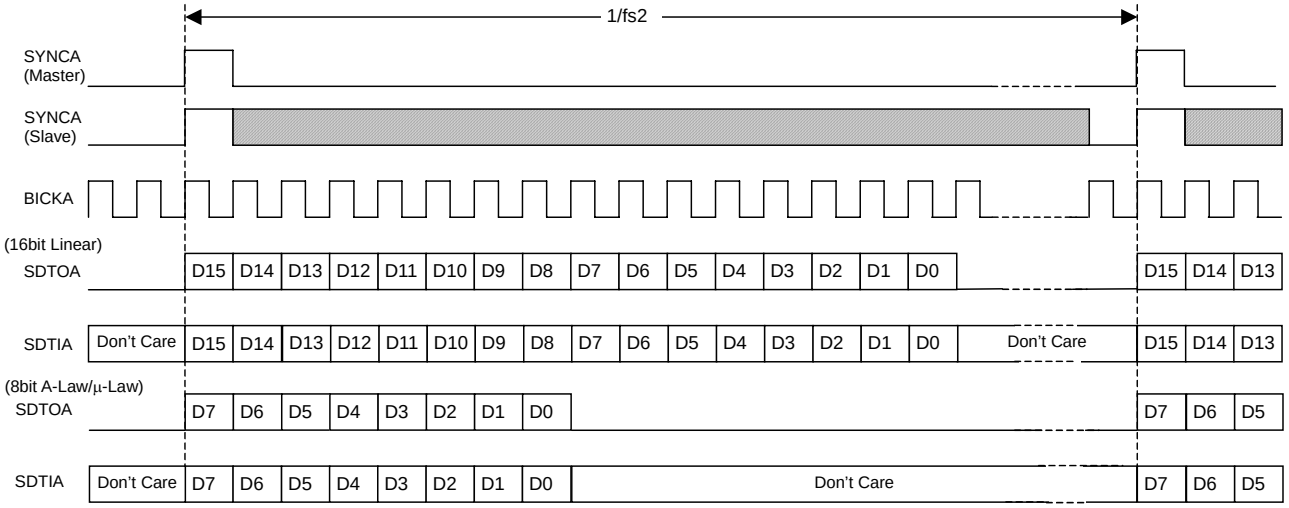


Figure 95. Timing of Long Frame Sync (MSBSA bit = "0", BCKPA bit = "0")

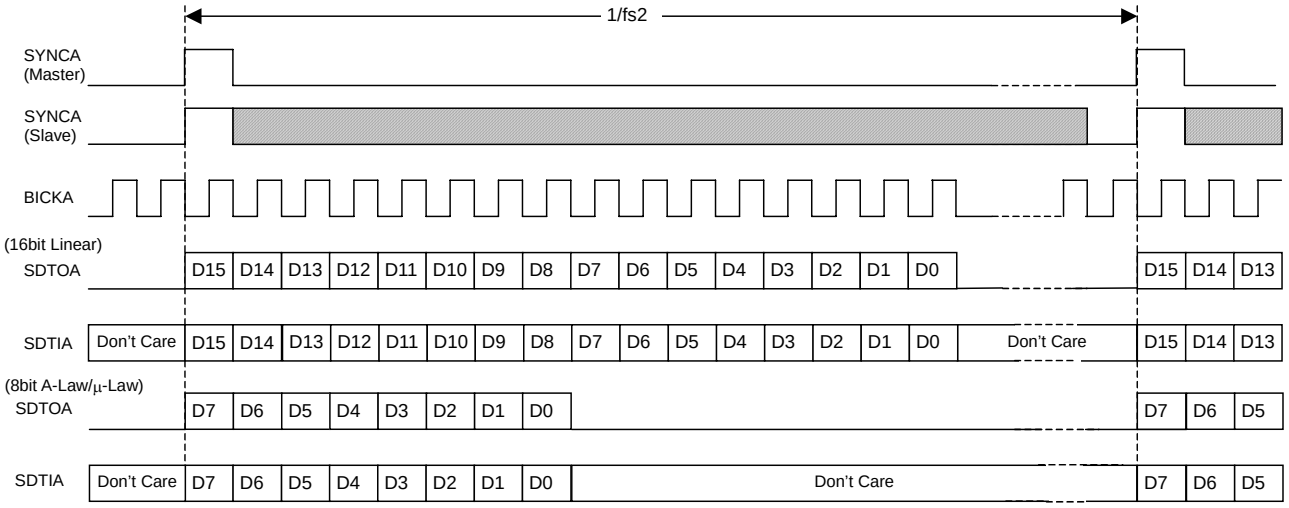


Figure 96. Timing of Long Frame Sync (MSBSA bit = "0", BCKPA bit = "1")

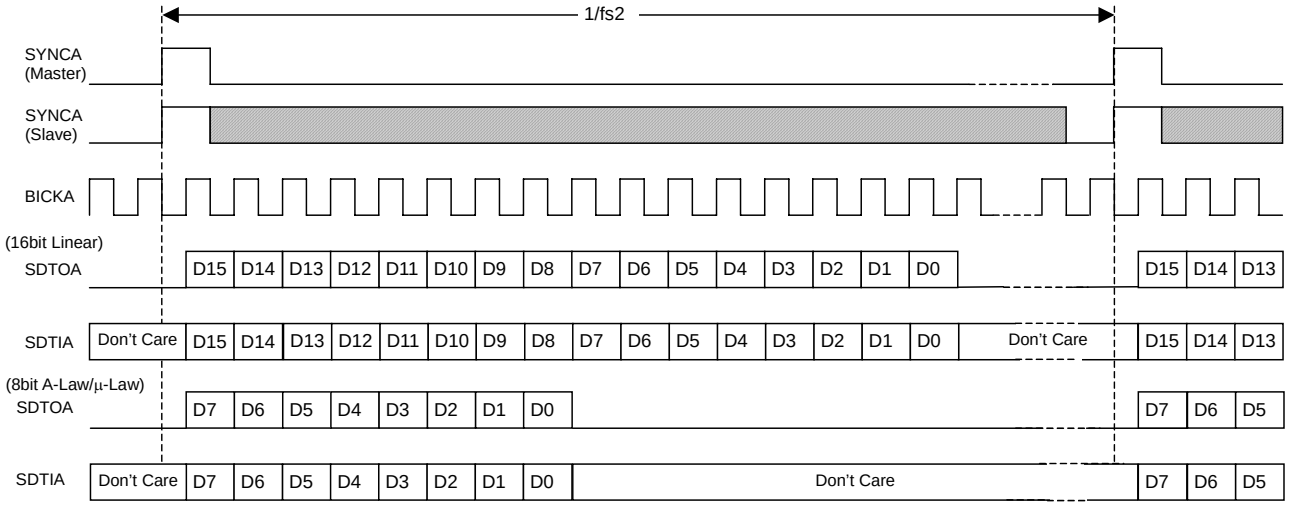


Figure 97. Timing of Long Frame Sync (MSBSA bit = "1", BCKPA bit = "0")

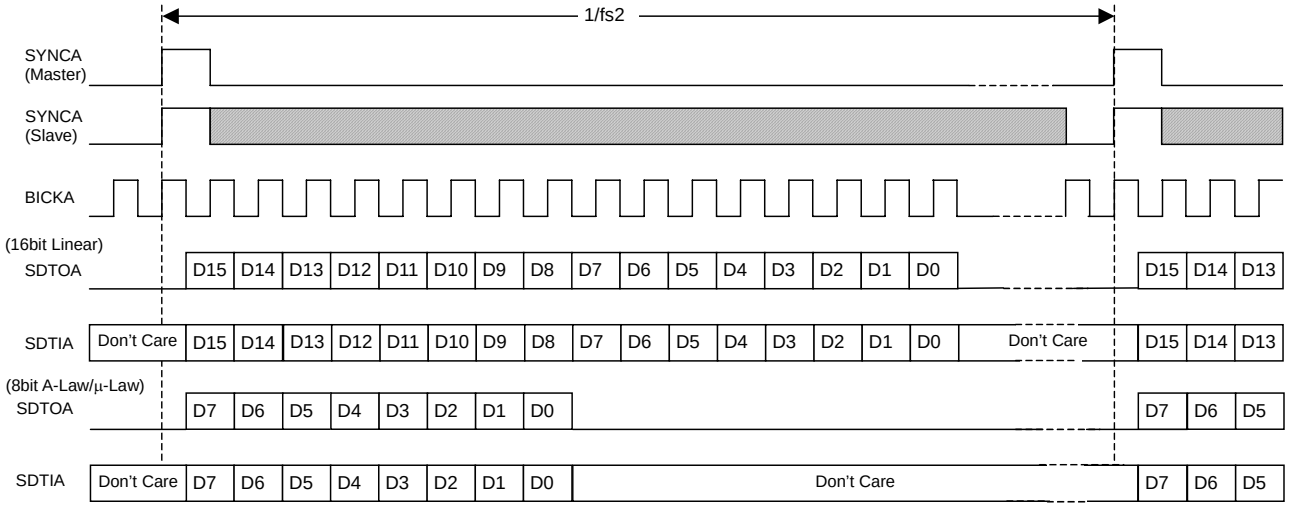


Figure 98. Timing of Long Frame Sync (MSBSA bit = "1", BCKPA bit = "1")

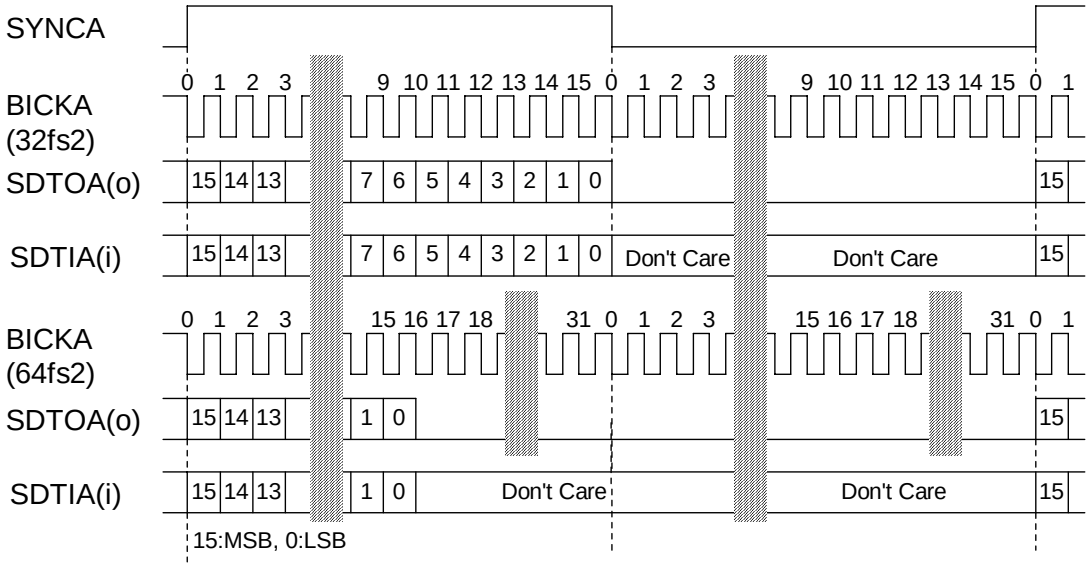


Figure 99. Timing of MSB justified

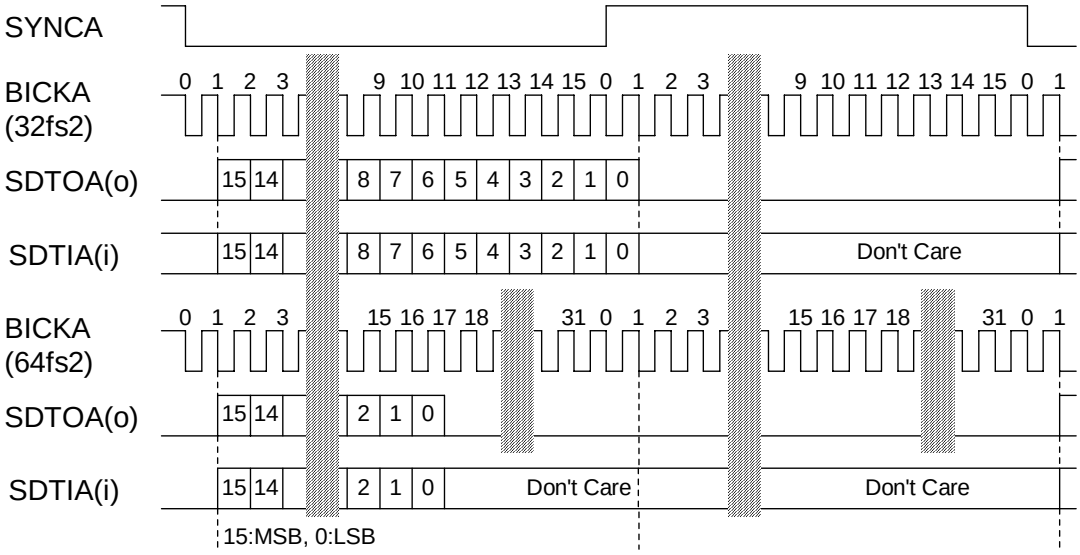


Figure 100. Timing of I^2S

■ Phone Path

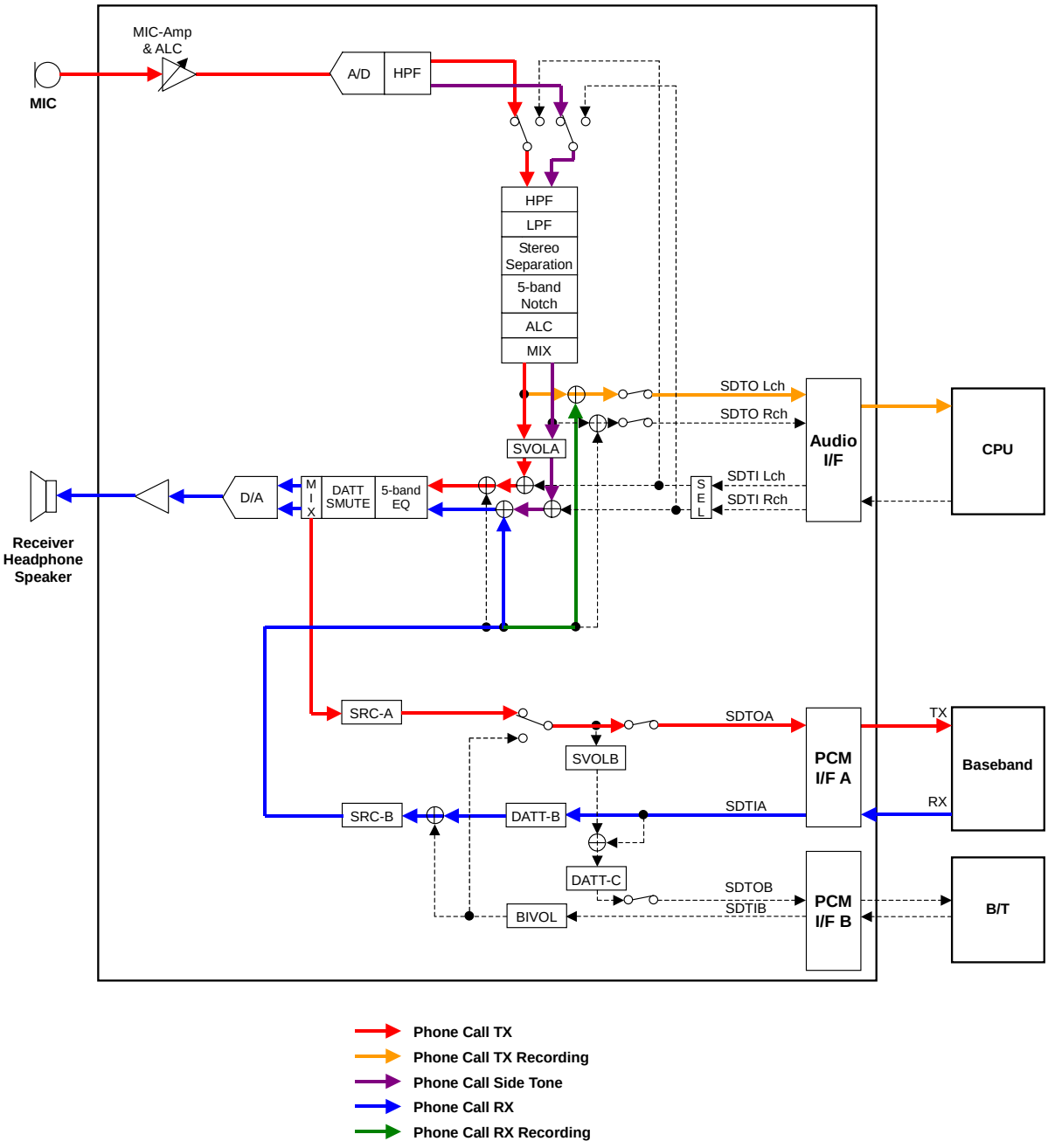


Figure 101. Internal MIC/SPK or External MIC/HP Call & Recording

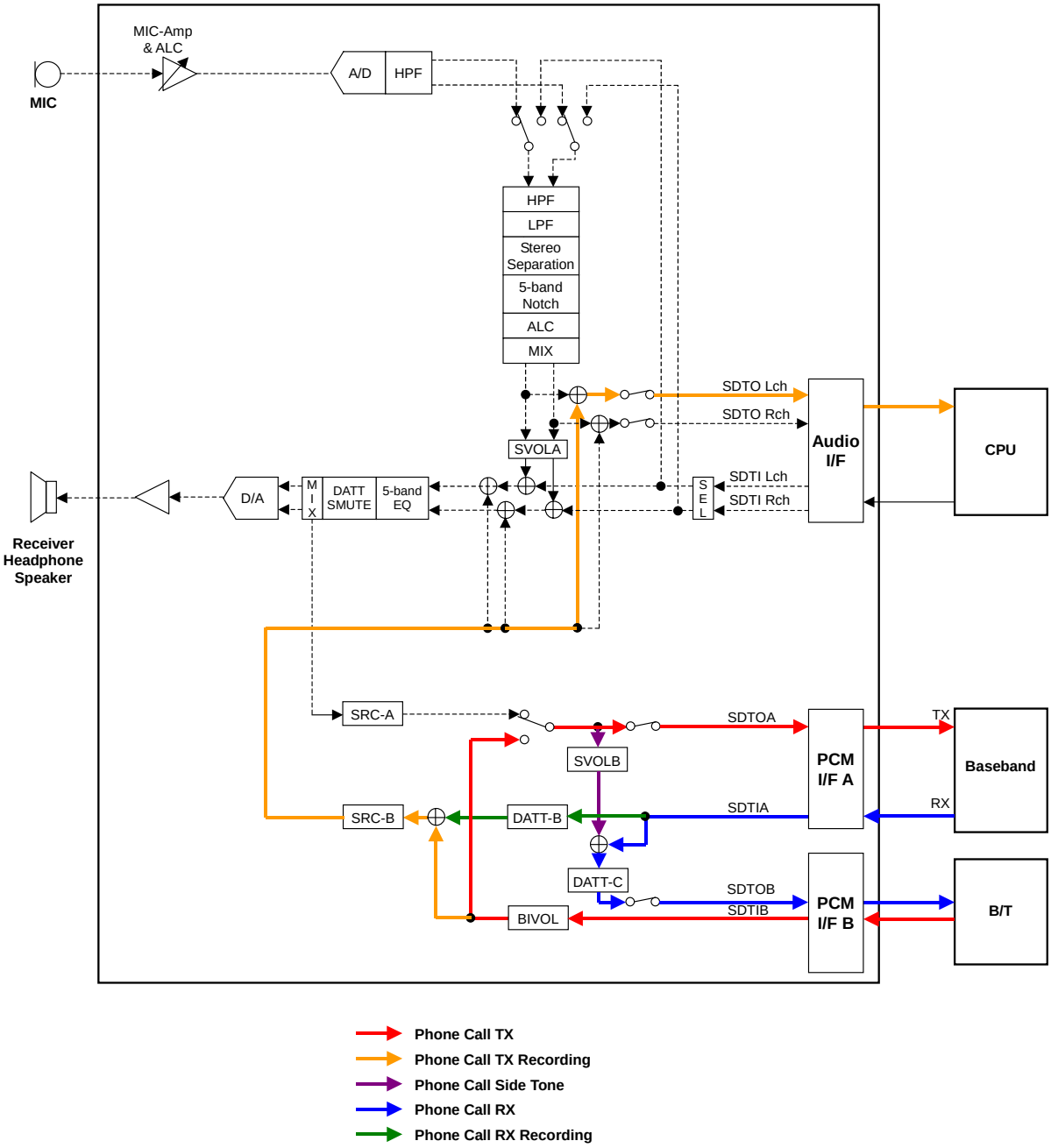


Figure 102. B/T Headset Phone Call & Recording

■ General Purpose Output

The AK4675 has General Purpose Output Pin (GPO) to control the external component.
In case of GPOM1 bit = "0", the GPO1 pin goes to "H" at GPOE1 bit = "1".

GPOE1 bit	GPO1 pin	
0	L	(default)
1	H	

Table 109. General Purpose Output 1 Pin Control (GPOM1 bit = "0")

In the case of GPOM1 bit = "1", the GPO1 pin goes to "H" if the input level of the channel selected by A0 bit (SAIN1 or SAIN2 pin) is higher than the reference voltage that is input the SAIN3 pin. In the case of GPOM1 bit = "1", the reference voltage input to the SAIN3 pin should be lower than 0.5 x AVDD.

SAIN1/2 pin	GPO1 pin	
< SAIN3 pin	L	(default)
≥ SAIN3 pin	H	

Table 110. General Purpose Output 1 Pin Control (GPOM1 bit = "1")

In the case of GPOM2 bit = "0", the GPO2 pin goes to "H" at GPOE2 bit = "0".

GPOE2 bit	GPO2 pin	
0	L	(default)
1	H	

Table 111. General Purpose Output 2 Pin Control (GPOM2 bit = "0")

In the case of GPOM2 bit = "1", the GPO2 pin outputs the mic detection result. (Table 21.)

Input Level of MDT pin	GPO2 pin	DTMIC bit	External microphone
≥ 0.075 x AVDD	H	1	Mic (Headset)
< 0.050 x AVDD	L	0	No Mic (Headphone)

Table 21. Microphone Detection Result

■ SAR 10bit ADC

The AK4675 incorporates a 10-bit successive approximation resistor A/D converter for DC measurement.
The A/D converter output is a straight binary format as shown in Table 112:

Input Voltage	Output Code
(AVDD−1.5LSB) ~ AVDD	3FFH
(AVDD−2.5LSB) ~ (AVDD−1.5LSB)	3FEH
:	:
0.5LSB ~ 1.5LSB	001H
0 ~ 0.5LSB	000H

Table 112. Output Code

When PMSAD bit is set to "1", 10bit ADC is powered-up. When the control register is read, A/D conversion is executed and data is output.

10bit ADC supports 3 kinds of analog input. A1-0 bits select the measurement modes.

Mode	A1	A0	Input Channel	
0	0	0	SAIN1	(default)
1	0	1	SAIN2	
2	1	0	SAIN3	
3	1	1	N/A	

Table 113. SAR ADC Measurement Mode

<SAR ADC Execute Sequence (in case that the interrupt function is enabled.)>

(1) Select the measurement mode by A1-0 bits and set PMSAD bit = "1" to power-up SAR ADC.
(2) Read Addr=5BH so that A/D conversion is executed and MSB 8bit data is output.
(3) Additionally read Addr=5CH then LSB 2bit data is output.

<SAR ADC Execute Sequence (in case that the interrupt function is disabled.)>

(1) GPOM1 bit should be set to "1". The GPO1 pin can be used as the interrupt output pin.
(2) Select the measurement mode by A0 bit.
(3) The GPO1 pin goes to "H" when the input DC voltage of the SAIN1 or SAIN2 pin (selected by A0 bit) is higher than the input voltage of the SAIN3 pin.
(4) After CPU detects the GPO1 pin = "H", set GPOM1 bit = "0" and PMSAD bit = "1" to power-up SAR ADC.
(5) Read Addr=5BH so that A/D conversion is executed and MSB 8bit data is output.
(6) Additionally read Addr=5CH then LSB 2bit data is output.

■ ATT Circuit for Battery Monitor

When BATCPU bit = "1", the input voltage for the VBATIN pin is divided by the internal resistors R1 (7.5k) and R2 (2.5k). The VBATO pin outputs the internally divided voltage. When BATCPU bit = "0", the VBATO pin goes to Hi-Z. This block can operate even if PMVCMA=PMOSC bits = "0".

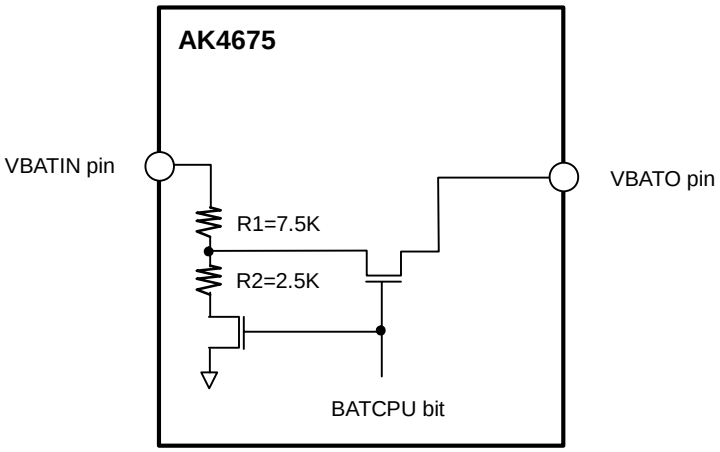


Figure 103. ATT circuit for Battery Monitor

■ Serial Control Interface

(1) I²C Bus Control Mode

The AK4675 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

(1)-1. WRITE Operations

Figure 104 shows the data transfer sequence for I²C-bus mode. All commands are preceded by START condition. HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 111). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). Addresses for CODEC and HP/SPK-Amp are fixed (Figure 105). If the slave address matches that of the AK4675, the AK4675 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 112). R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4675. The format is MSB first, and the most significant 1-bit is fixed to "0" (Figure 106). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 107). The AK4675 generates an acknowledge after each byte has been received. Data transfer is always terminated by a STOP condition generated by the master. LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 111).

The AK4675 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4675 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. In case of CODEC & SRC blocks, if the address exceeds 5AH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. In case of HP/SPK-Amp blocks, if the address exceeds 12H prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 113) except for the START and STOP conditions.

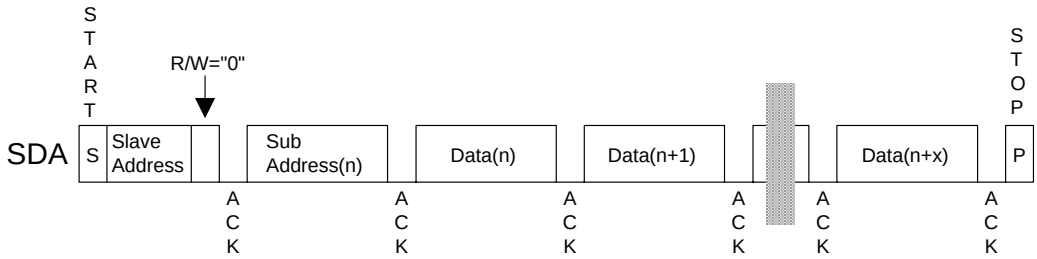


Figure 104. Data Transfer Sequence at the I^{2}C-Bus Mode

CODEC	0	0	1	0	0	1	0	R/W
AMP	0	0	1	0	0	1	1	R/W

Figure 105. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 106. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 107. Byte Structure after The Second Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4675. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 7-bit address counter is incremented by one, and the next data is automatically taken into the next address. In case of CODEC & SRC blocks, if the address exceeds 5AH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out. In case of HP/SPK-Amp blocks, if the address exceeds 12H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4675 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ (except for 10bit SAR ADC Data)

The AK4675 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit set to "1", the AK4675 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates stop condition, the AK4675 ceases transmission.

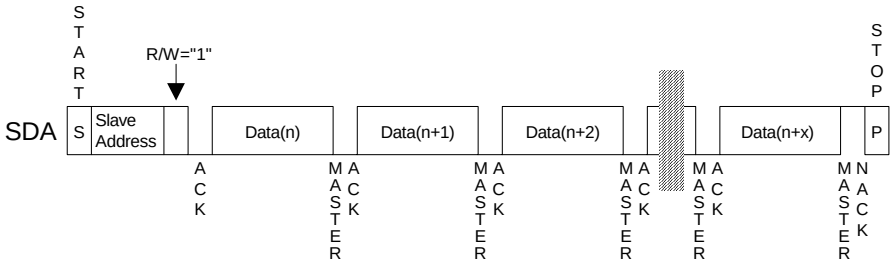


Figure 108. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform "dummy" write operation. The master issues start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4675 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4675 ceases transmission.

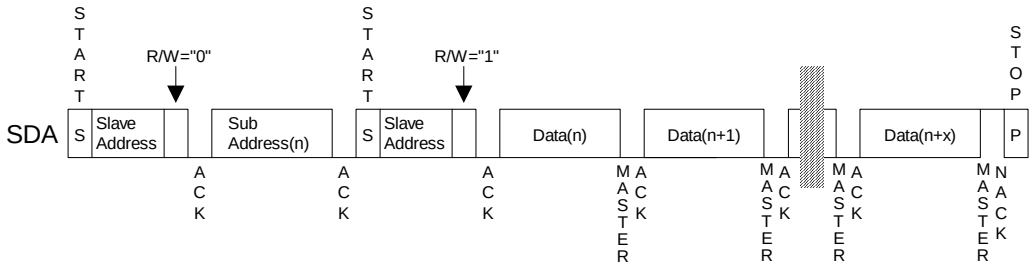


Figure 109. RANDOM ADDRESS READ

When SAR ADC data is read, register data of Addr=5BH should be read by RANDOM ADDRESS READ, then stop condition should be input.

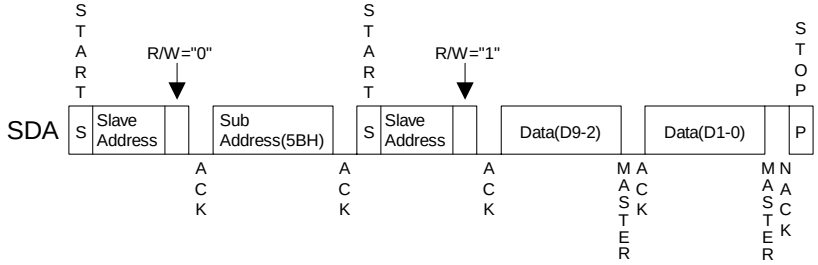


Figure 110. RANDOM ADDRESS READ of SAR ADC Data

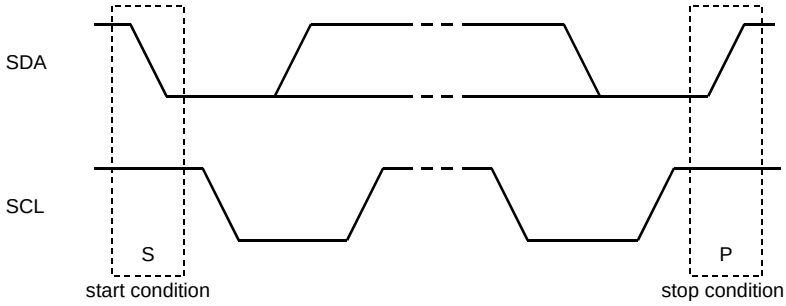


Figure 111. START and STOP Conditions

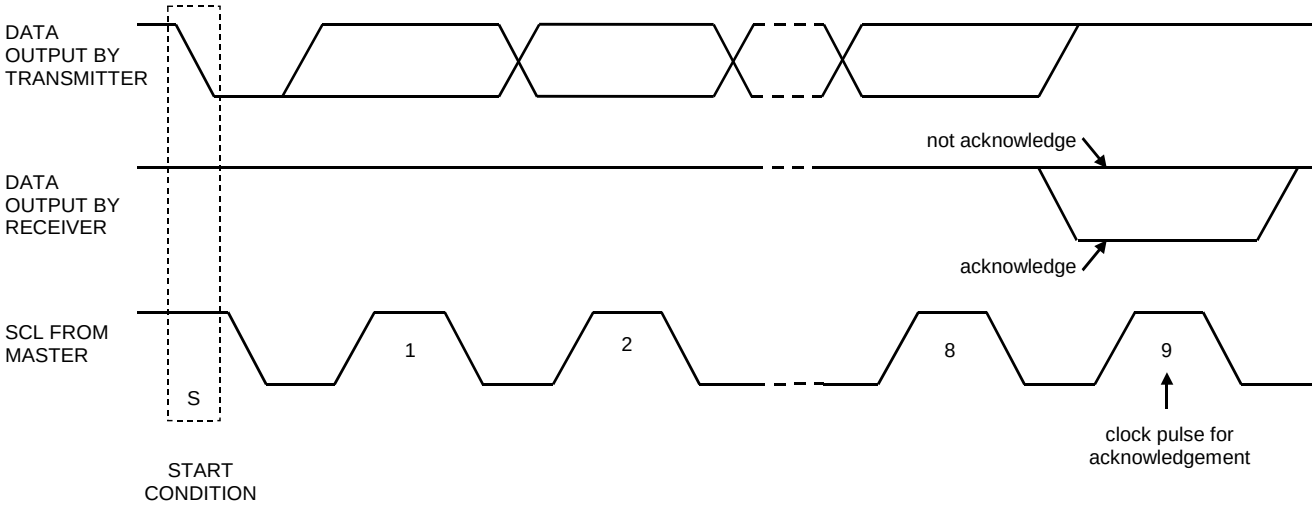


Figure 112. Acknowledge on the I^2C-Bus

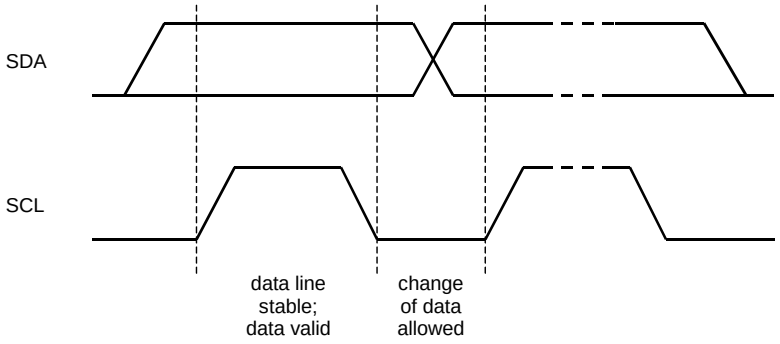


Figure 113. Bit Transfer on the I^2C-Bus

■ Register Map (CODEC & SRC Blocks)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	AD/DA Power Management	PMDAR	PMDAL	PMADR	PMADL	PMMICR	PMMICL	PMMP	PMVCM
01H	PLL Mode Select 0	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	PLL Mode Select 1	BTCLK	LP	BCKO	PS1	PS0	MCKO	M/S	PMPLL
03H	Format Select	0	0	0	SDOD	MSBS	BCKP	DIF1	DIF0
04H	MIC Signal Select	MDIF4	MDIF3	MDIF2	MDIF1	INR1	INR0	INL1	INL0
05H	MIC Amp Gain	MGNR3	MGNR2	MGNR1	MGNR0	MGNL3	MGNL2	MGNL1	MGNL0
06H	Mixing Power Management 0	0	0	0	0	0	DTMIC	PMLOOPR	PMLOOPL
07H	Mixing Power Management 1	PMAINR4	PMAINL4	PMAINR3	PMAINL3	PMAINR2	PMAINL2	PMAINR1	PMAINL1
08H	Output Volume Control	1	0	1	1	0	L1VL2	L1VL1	L1VL0
09H	LOUT1 Signal Select	L1G1	L1G0	LOOPL	LINL4	LINL3	LINL2	LINL1	DACL
0AH	ROUT1 Signal Select	L2G1	L2G0	LOOPR	RINR4	RINR3	RINR2	RINR1	DACR
0BH	LOUT2S Signal Select	L3G1	L3G0	LOOPHL	LINH4	LINH3	LINH2	LINH1	DACHL
0CH	ROUT2S Signal Select	L4G1	L4G0	LOOPHR	RINH4	RINH3	RINH2	RINH1	DACHR
0DH	LOUT3 Signal Select	LPG1	LPG0	LOOPSL	LINS4	LINS3	LINS2	LINS1	DACSL
0EH	ROUT3 Signal Select	0	0	LOOPSR	RINS4	RINS3	RINS2	RINS1	DACSR
0FH	LOUT1 Power Management	0	0	RCV	LOOPM	LOM	LOPS1	PMRO1	PMLO1
10H	LOUT2S Power Management	0	PMRO2S	PMLO2S	LOOPM2	LOM2	0	0	0
11H	LOUT3 Power Management	L3VL1	L3VL0	LODIF	LOOPM3	LOM3	LOPS3	PMRO3	PMLO3
12H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
13H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
14H	ALC Reference Select	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
15H	Digital Mixing Control	SRMXR1	SRMXR0	SRMXL1	SRMXL0	PFMXR1	PFMXR0	PFMXL1	PFMXL0
16H	ALC Timer Select	0	RFST1	RFST0	WTM2	WTM1	WTM0	ZTM1	ZTM0
17H	ALC Mode Control	0	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
18H	Mode Control 1	DAM	MIXD	SDIM1	SDIM0	EQ	ADM	IVOLC	ALC
19H	Mode Control 2	SRA1	SRA0	BIV2	BIV1	BIV0	SMUTE	OVTM	OVOLC
1AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
1BH	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
1CH	Side Tone A Control	0	0	SVAR2	SVAR1	SVAR0	SVAL2	SVAL1	SVAL0
1DH	Digital Filter Select	GN1	GN0	LPF	HPF	EQ0	FIL3	HPFAD	PFSEL
1EH	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
1FH	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
20H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
21H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
22H	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
23H	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
24H	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
25H	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
26H	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
27H	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
28H	FIL1 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
29H	FIL1 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
2AH	FIL1 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
2BH	FIL1 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
50H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
51H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
52H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
53H	PCM I/F Control 0	GPOM2	GPOE2	PLLBT2	PLLBT1	PLLBT0	PMPCM	PMSRB	PMSRA
54H	PCM I/F Control 1	SDOAD	BCKO2	MSBSA	BCKPA	LAWA1	LAWA0	FMTA1	FMTA0
55H	PCM I/F Control 2	SDOBD	PLLBT3	MSBSB	BCKPB	LAWB1	LAWB0	FMTB1	FMTB0
56H	Digital Volume B Control	BVL7	BVL6	BVL5	BVL4	BVL3	BVL2	BVL1	BVL0
57H	Digital Volume C Control	CVL7	CVL6	CVL5	CVL4	CVL3	CVL2	CVL1	CVL0
58H	Side Tone Volume Control	0	0	0	0	SDOA	SVB2	SVB1	SVB0
59H	Digital Mixing Control	SDOR1	SDOR0	SDOL1	SDOL0	BVMX1	BVMX0	SBMX1	SBMX0
5AH	SAR ADC Control	0	0	0	GPOM1	GPOE1	A1	A0	PMSAD

Note 85. PDN pin = “L” resets the registers of CODEC & SRC blocks to their default values.
Note 86. The bits defined as 0 must contain a “0” value.
Note 87. Addresses 1EH to 2FH and 32H to 4FH cannot be read.

■ Register Definitions (CODEC & SRC Blocks)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	AD/DA Power Management	PMDAR	PMDAL	PMADR	PMADL	PMMICR	PMMICL	PMMP	PMVCM
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: VCOM Power Management
0: Power down (default)
1: Power up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when all power management bits are "0".

PMMP: MPWR pin Power Management
0: Power down: Hi-Z (default)
1: Power up

PMMICL: MIC-Amp Lch Power Management
0: Power down (default)
1: Power up

PMMICR: MIC-Amp Rch Power Management
0: Power down (default)
1: Power up

PMADL: ADC Lch Power Management
0: Power down (default)
1: Power up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMADR: ADC Rch Power Management
0: Power down (default)
1: Power up

PMDAL: DAC Lch Power Management
0: Power down (default)
1: Power up

PMDAR: DAC Rch Power Management
0: Power down (default)
1: Power up

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks of CODEC & SRC are powered-down regardless of setting of this address. In this case, register of CODEC & SRC is initialized to the default value.

When all power management bits are "0", all blocks of CODEC & SRC are powered-down. The register values of CODEC & SRC remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin should be "L".

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Mode Select 0	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	1	1	0

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "0110"(MCKI pin, 12MHz)

FS3-0: Sampling Frequency Select (See Table 5 and Table 6) and MCKI Frequency Select (Table 11)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	PLL Mode Select 1	BTCLK	LP	BCKO	PS1	PS0	MCKO	M/S	PMPLL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power Down (default)
1: PLL Mode and Power up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

PS1-0: MCKO Output Frequency Select (Table 9)
Default: "00"(256fs)

BCKO: BICK Output Frequency Select at Master Mode (Table 10)

LP: Low Power Mode
0: Normal Mode (default)
1: Low Power Mode: available at fs=22.05kHz or less.

BTCLK: Clock Mode of Audio CODEC
0: Synchronized to Audio I/F (default)
1: Synchronized to PCM I/F
BTCLK bit is enabled at only PMPLL bit = "0". When BTCLK bit is "1", Audio CODEC and the digital block (Figure 56) operate by the clock generated by PLLBT.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Format Select	0	0	0	SDOD	MSBS	BCKP	DIF1	DIF0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 16)
Default: "10" (Left jutified)

BCKP: BICK Polarity at DSP Mode (Table 17)
"0": SDTO is output by the rising edge ("↑") of BICK and SDTI is latched by the falling edge ("↓"). (default)
"1": SDTO is output by the falling edge ("↓") of BICK and SDTI is latched by the rising edge ("↑").

MSBS: LRCK Phase at DSP Mode (Table 17)
"0": The rising edge ("↑") of LRCK is half clock of BICK before the channel change. (default)
"1": The rising edge ("↑") of LRCK is one clock of BICK before the channel change.

SDOD: SDTO Disable (Table 47)
"0": Enable (default)
"1": Disable ("L")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	MIC Signal Select	MDIF4	MDIF3	MDIF2	MDIF1	INR1	INR0	INL1	INL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INL1-0: MIC-Amp Lch Input Source Select (Table 18)
Default: "00" (LIN1)

INR1-0: MIC-Amp Rch Input Source Select (Table 18)
Default: "00" (RIN1)

MDIF1: Line1 Input Type Select
0: Single-ended input (LIN1/RIN1 pins: default)
1: Full-differential input (IN1+/IN1– pins)

MDIF2: Line2 Input Type Select
0: Single-ended input (LIN2/RIN2 pins: default)
1: Full-differential input (IN2+/IN2– pins)

MDIF3: Line3 Input Type Select
0: Single-ended input (LIN3/RIN3 pins: default)
1: Full-differential input (IN3+/IN3– pins)

MDIF4: Line4 Input Type Select
0: Single-ended input (LIN4/RIN4 pins: default)
1: Full-differential input (IN4+/IN4– pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	MIC Amp Gain	MGNR3	MGNR2	MGNR1	MGNR0	MGNL3	MGNL2	MGNL1	MGNL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

MGNL3-0: MIC-Amp Lch Gain Control (Table 19)
Default: "0101" (0dB)

MGNR3-0: MIC-Amp Rch Gain Control (Table 19)
Default: "0101" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mixing Power Management 0	0	0	0	0	0	DTMIC	PMLOOPR	PMLOOPL
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMLOOPL: MIC-Amp Lch Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMLOOPR: MIC-Amp Rch Mixing Circuit Power Management
0: Power down (default)
1: Power up

DTMIC: Microphone Detection Result (Read Only: Table 21)
0: Microphone is not detected. (default)
1: Microphone is detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mixing Power Management 1	PMAINR4	PMAINL4	PMAINR3	PMAINL3	PMAINR2	PMAINL2	PMAINR1	PMAINL1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMAINL1: LIN1 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINR1: RIN1 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINL2: LIN2 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINR2: RIN2 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINL3: LIN3 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINR3: RIN3 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINL4: LIN4 Mixing Circuit Power Management
0: Power down (default)
1: Power up

PMAINR4: RIN4 Mixing Circuit Power Management
0: Power down (default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Output Volume Control	1	0	1	1	0	L1VL2	L1VL1	L1VL0
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		1	0	1	1	0	1	0	1

L1VL3-0: LOUT1/ROUT1 Output Volume Control (Table 67)
Default: “5H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	LOUT1 Signal Select	L1G1	L1G0	LOOPL	LINL4	LINL3	LINL2	LINL1	DACL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACL: Switch Control from DAC Lch to LOUT1
0: OFF (default)
1: ON
When PMLO1 bit is "1", DACL bit is enabled. When PMLO1 bit is "0", the LOUT1 pin goes to VSS1.

LINL1: Switch Control from LIN1 to LOUT1
0: OFF (default)
1: ON

LINL2: Switch Control from LIN2 to LOUT1
0: OFF (default)
1: ON

LINL3: Switch Control from LIN3 to LOUT1
0: OFF (default)
1: ON

LINL4: Switch Control from LIN4 to LOUT1
0: OFF (default)
1: ON

LOOPL: Switch Control from MIC-Amp Lch to LOUT1
0: OFF (default)
1: ON

L1G1-0: LIN1/RIN1 Mixing Gain Control (Table 60)
Default: "00" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ROUT1 Signal Select	L2G1	L2G0	LOOPR	RINR4	RINR3	RINR2	RINR1	DACR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACR: Switch Control from DAC Rch to ROUT1
0: OFF (default)
1: ON
When PMRO1 bit is "1", DACR bit is enabled. When PMRO1 bit is "0", the ROUT1 pin goes to VSS1.

RINR1: Switch Control from RIN1 to ROUT1
0: OFF (default)
1: ON

RINR2: Switch Control from RIN2 to ROUT1
0: OFF (default)
1: ON

RINR3: Switch Control from RIN3 to ROUT1
0: OFF (default)
1: ON

RINR4: Switch Control from RIN4 to ROUT1
0: OFF (default)
1: ON

LOOPR: Switch Control from MIC-Amp Rch to ROUT1
0: OFF (default)
1: ON

L2G1-0: LIN2/RIN2 Mixing Gain Control (Table 61)
Default: "00" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	LOUT2S Signal Select	L3G1	L3G0	LOOPHL	LINH4	LINH3	LINH2	LINH1	DACHL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACHL: Switch Control from DAC Lch to LOUT2S
0: OFF (default)
1: ON

LINH1: Switch Control from LIN1 to LOUT2S
0: OFF (default)
1: ON

LINH2: Switch Control from LIN2 to LOUT2S
0: OFF (default)
1: ON

LINH3: Switch Control from LIN3 to LOUT2S
0: OFF (default)
1: ON

LINH4: Switch Control from LIN4 to LOUT2S
0: OFF (default)
1: ON

LOOPHL: Switch Control from MIC-Amp Lch to LOUT2S
0: OFF (default)
1: ON

L3G1-0: LIN3/RIN3 Mixing Gain Control (Table 62)
Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ROUT2S Signal Select	L4G1	L4G0	LOOPHR	RINH4	RINH3	RINH2	RINH1	DACHR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACHR: Switch Control from DAC Rch to ROUT2S
0: OFF (default)
1: ON

RINH1: Switch Control from RIN1 to ROUT2S
0: OFF (default)
1: ON

RINH2: Switch Control from RIN2 to ROUT2S
0: OFF (default)
1: ON

RINH3: Switch Control from RIN3 to ROUT2S
0: OFF (default)
1: ON

RINH4: Switch Control from RIN4 to ROUT2S
0: OFF (default)
1: ON

LOOPHR: Switch Control from MIC-Amp Rch to ROUT2S
0: OFF (default)
1: ON

L4G1-0: LIN4/RIN4 Mixing Gain Control (Table 63)
Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	LOUT3 Signal Select	LPG1	LPG0	LOOPSL	LINS4	LINS3	LINS2	LINS1	DACSL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACSL: Switch Control from DAC Lch to LOUT3
0: OFF (default)
1: ON
When PMLO3 bit is "1", DACSL bit is enabled. When PMLO3 bit is "0", the LOUT3 pin goes to VSS1.

LINS1: Switch Control from LIN1 to LOUT3
0: OFF (default)
1: ON

LINS2: Switch Control from LIN2 to LOUT3
0: OFF (default)
1: ON

LINS3: Switch Control from LIN3 to LOUT3
0: OFF (default)
1: ON

LINS4: Switch Control from LIN4 to LOUT3
0: OFF (default)
1: ON

LOOPSL: Switch Control from MIC-Amp Lch to LOUT3
0: OFF (default)
1: ON

LPG1-0: MIC-Amp Mixing Gain Control (Table 64)
Default: "00" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ROUT3 Signal Select	0	0	LOOPSR	RINS4	RINS3	RINS2	RINS1	DACSR
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACSR: Switch Control from DAC Rch to ROUT3
0: OFF (default)
1: ON
When PMRO3 bit is "1", DACR bit is enabled. When PMRO3 bit is "0", the ROUT3 pin goes to VSS1.

RINS1: Switch Control from RIN1 to ROUT3
0: OFF (default)
1: ON

RINS2: Switch Control from RIN2 to ROUT3
0: OFF (default)
1: ON

RINS3: Switch Control from RIN3 to ROUT3
0: OFF (default)
1: ON

RINS4: Switch Control from RIN4 to ROUT3
0: OFF (default)
1: ON

LOOPSR: Switch Control from MIC-Amp Rch to ROUT3
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	LOUT1 Power Management	0	0	RCV	LOOPM	LOM	LOPS1	PMRO1	PMLO1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMLO1: LOUT1 Power Management
0: Power down (default)
1: Power up

PMRO1: ROUT1 Power Management
0: Power down (default)
1: Power up

LOPS1: LOUT1/ROUT1 Power Save Mode
0: Normal Operation (default)
1: Power Save Mode

LOM: Mono Mixing from DAC to LOUT1/ROUT1
0: Stereo Mixing (default)
1: Mono Mixing

LOOPM: Mono Mixing from MIC-Amp to LOUT1/ROUT1
0: Stereo Mixing (default)
1: Mono Mixing

RCV: Receiver Select
0: Stereo Line Output (LOUT1/ROUT1 pins) (default)
1: Mono Receiver Output (RCP/RCN pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	LOUT2S Power Management	0	PMRO2S	PMLO2S	LOOPM2	LOM2	0	0	0
R/W		RD	R/W	R/W	R/W	R/W	RD	RD	RD
Default		0	0	0	0	0	0	0	0

LOM2: Mono Mixing from DAC to LOUT2S/ROUT2S
0: Stereo Mixing (default)
1: Mono Mixing

LOOPM2: Mono Mixing from MIC-Amp to LOUT2S/ROUT2S
0: Stereo Mixing (default)
1: Mono Mixing

PMLO2S: LOUT2S MIX-Amp Power Management
0: Power down (default)
1: Power up

PMRO2S: ROUT2S MIX-Amp Power Management
0: Power down (default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	LOUT3 Power Management	L3VL1	L3VL0	LODIF	LOOPM3	LOM3	LOPS3	PMRO3	PMLO3
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

PMLO3: LOUT3 Power Management
0: Power down (default)
1: Power up

PMRO3: ROUT3 Power Management
0: Power down (default)
1: Power up

LOPS3: LOUT3/ROUT3 Power Save Mode
0: Normal Operation (default)
1: Power Save Mode

LOM3: Mono Mixing from DAC to LOUT3/ROUT3
0: Stereo Mixing (default)
1: Mono Mixing

LOOPM3: Mono Mixing from MIC-Amp to LOUT3/ROUT3
0: Stereo Mixing (default)
1: Mono Mixing

LODIF: Lineout Select
0: Single-ended Stereo Line Output (LOUT3/ROUT3 pins) (default)
1: Full-differential Mono Line Output (LOP/LON pins)

L3VL1-0: LOUT3/ROUT3 Output Gain Control (Table 72)
Default: “10” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
13H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	0	0	1	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 33)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	ALC Reference Select	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation; 0.375dB step, 242 Level (Table 29)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Digital Mixing Control	SRMXR1	SRMXR0	SRMXL1	SRMXL0	PFMXR1	PFMXR0	PFMXL1	PFMXL0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PFMXL1-0: 5-band EQ Lch Input Mixing 1 (Table 49.)
Default: "00" (SDTI)

PFMXR 1-0: 5-band EQ Rch Input Mixing 1 (Table 50.)
Default: "00" (SDTI)

SRMXL1-0: 5-band EQ Lch Input Mixing 2 (Table 51.)
Default: "00" (SDTI)

SRMXR 1-0: 5-band EQ Rch Input Mixing 2 (Table 52.)
Default: "00" (SDTI)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	ALC Timer Select	0	RFST1	RFST0	WTM2	WTM1	WTM0	ZTM1	ZTM0
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 26)

Gain is changed by micro computer writing or ALC limiter operation at the zero crossing point or at the zero crossing timeout. Default value is "00" (128/fs)

WTM2-0: ALC Recovery Waiting Period (Table 27)
A period of recovery operation when any limiter operation does not occur during the ALC1 operation; Default is "000" (128/fs).

RFST1-0: ALC First recovery Speed (Table 30)
Default: "00"(4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	ALC Mode Control	0	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 24)
Default: "00"

RGAIN1-0: ALC Recovery GAIN Step (Table 28)
Default: "00"

LMAT1-0: ALC Limiter ATT Step (Table 25)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Mode Control 1	DAM	MIXD	SDIM1	SDIM0	EQ	ADM	IVOLC	ALC
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

ADM: Mono Recording (Table 44)
0: Stereo (default)
1: Mono: (L+R)/2

EQ: Select 5-Band Equalizer
0: OFF (default)
1: ON

SDIM1-0: SDTI Input Signal Select (Table 48)
Default: "00" (L=Lch, R=Rch)

MIXD: DAC and SRC-A Mono Mixing (Table 53 and Table 54.)
0: L+R (default)
1: (L+R)/2

DAM: DAC Mono Mixing (Table 53)
0: Stereo (default)
1: Mono: (L+R) or (L+R)/2 is selected by MIXD bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	Mode Control 2	SRA1	SRA0	BIV2	BIV1	BIV0	SMUTE	OVTM	OVOLC
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume level, while register values of OVL7-0 bits are not written to OVR7-0 bits. When OVOLC bit = "0", OVL7-0 bits control Lch level and OVR7-0 bits control Rch level, respectively.

OVTM: Digital Volume Transition Time Setting
0: 1061/fs (default)
1: 256/fs
This is the transition time between OVL/R7-0 bits = 00H and FFH.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

BIV2-0: SDTIB Input Volume Control (Table 41)
Default: "0H" (0dB)

SRA1-0: SRC-A Input Signal Select (Table 54)
Default: "00" (Lch)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
1BH	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

OVL7-0, OVR7-0: Output Digital Volume (Table 36)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Side Tone A Control	0	0	SVAR2	SVAR1	SVAR0	SVAL2	SVAL1	SVAL0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SVAL2-0, SVAR2-0: Side Tone Volume A (SVOLA) (Table 34)
Default: "000" (0dB))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Select	GN1	GN0	LPF	HPF	EQ0	FIL3	HPFAD	PFSEL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

PFSEL: Signal Select of Programmable Filter Block (Table 43.)
0: ADC Output Data (default)
1: SDTI Input Data

HPFAD: HPF Control of ADC
0: OFF
1: ON (default)
When HPFAD bit is "1", the settings of F1A13-0 and F1B13-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).

GN1-0: Gain Select at GAIN block (Table 23)
Default: "00" (0dB)

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3 bit is "1", the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is "0", FIL3 block is OFF (MUTE).

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ0 bit is "1", the settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit is "0", EQ0 block is through (0dB).

HPF: HPF Coefficient Setting Enable
0: Disable (default)
1: Enable
When HPF bit is "1", the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is "0", HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable
0: Disable (default)
1: Enable
When LPF bit is "1", the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is "0", LPF block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
1FH	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
20H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
21H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
22H	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
23H	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
24H	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
25H	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
26H	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
27H	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: "0000H"

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select
0: HPF (Default)
1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ0 (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	FIL1 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
29H	FIL1 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
2AH	FIL1 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
2BH	FIL1 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		W	W	W	W	W	W	W	W
Default		F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH"							

F1A13-0, F1B13-B0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)
Default: F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH" (fc=150Hz@fs=44.1kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	FIL2 Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	FIL2 Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	FIL2 Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	FIL2 Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-B0: FIL2 (LPF) Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
51H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
52H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

EQA3-0: Select the boost level of 100Hz
EQB3-0: Select the boost level of 250Hz
EQC3-0: Select the boost level of 1kHz
EQD3-0: Select the boost level of 3.5kHz
EQE3-0: Select the boost level of 10kHz
See Table 35.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
53H	PCM I/F Control 0	GPOM2	GPOE2	PLLBT2	PLLBT1	PLLBT0	PMPCM	PMSRB	PMSRA
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMSRA: SRC-A Power Management
0: Power down (default)
1: Power up

PMSRB: SRC-B Power Management
0: Power down (default)
1: Power up

PMPCM: PCM I/F Power Management
0: Power down (default)
1: Power up

PLLBT2-0: PLLBT Reference Clock Select
PLLBT3 bit is D6 of Addr=55H.
Default: “0000”: SYNCA

GPOE2: General Purpose Output 2 Enable at GPOM2 bit = “1”
“0”: GPO2 pin = “L” (default)
“1”: GPO2 pin = “H”

GPOM2: General Purpose Output 2 Operation Mode (Table 111.)
“0”: Controlled by GPOE2 bit (default)
“1”: MIC Detection Interrupt

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
54H	PCM I/F Control 2	SDOAD	BCKO2	MSBSA	BCKPA	LAWA1	LAWA0	FMTA1	FMTA0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FMTA1-0: PCM I/F A Format (Table 103)
Default: "00" (Mode 0)

LAWA1-0: PCM I/F A Mode (Table 101)
Default: "00" (Mode 0)

BCKPA: BICKA Polarity of PCM I/F A (Table 105)
"0": SDTOA is output by the rising edge ("↑") of BICKA and SDTIA is latched by the falling edge ("↓"). (default)
"1": SDTOA is output by the falling edge ("↓") of BICKA and SDTIA is latched by the rising edge ("↑").

MSBSA: SYNCA Phase of PCM I/F A (Table 105)
"0": The rising edge ("↑") of SYNCA is half clock of BICKA before the channel change. (default)
"1": The rising edge ("↑") of SYNCA is one clock of BICKA before the channel change.

BCKO2: BICKA/B Output Frequency Select at Master Mode (Table 96)
0: 16fs2 (default)
1: 32fs2

SDOAD: SDTOA Disable (Table 56.)
"0": Enable (default)
"1": Disable ("L")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
55H	PCM I/F Control 3	SDOBD	PLLBT3	MSBSB	BCKPB	LAWB1	LAWB0	FMTB1	FMTB0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FMTB1-0: PCM I/F B Format (Table 104)
Default: "00" (Mode 0)

LAWB1-0: PCM I/F B Mode (Table 102)
Default: "00" (Mode 0)

BCKPB: BICKB Polarity of PCM I/F B (Table 106)
"0": SDTOB is output by the rising edge ("↑") of BICKB and SDTIB is latched by the falling edge ("↓"). (default)
"1": SDTOB is output by the falling edge ("↓") of BICKB and SDTIB is latched by the rising edge ("↑").

MSBSB: SYNCB Phase of PCM I/F B (Table 106)
"0": The rising edge ("↑") of SYNCB is half clock of BICKB before the channel change. (default)
"1": The rising edge ("↑") of SYNCB is one clock of BICKB before the channel change.

PLLBT3: PLLBT Reference Clock Select
PLLBT2-0 bits is D5-3 of Addr=53H.
Default: "0000": SYNCA

SDOBD: SDTOB Disable (Table 58)
"0": Enable (default)
"1": Disable ("L")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	Digital Volume B Control	BVL7	BVL6	BVL5	BVL4	BVL3	BVL2	BVL1	BVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

BVL7-0: Digital Volume B (Table 38)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
57H	Digital Volume C Control	CVL7	CVL6	CVL5	CVL4	CVL3	CVL2	CVL1	CVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

CVL7-0: Digital Volume B (Table 39)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
58H	Side Tone Volume Control	0	0	0	0	SDOA	SVB2	SVB1	SVB0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SVB2-0: Side Tone Volume (Table 40)
Default: "5H" (–12dB)

SDOA: SDTOA Output Signal Select (Table 55.)
"0": SRC-A (default)
"1": SDTI-B

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
59H	Digital Mixing Control	SDOR1	SDOR0	SDOL1	SDOL0	BVMX1	BVMX0	SBMX1	SBMX0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SBMX1-0: SDTOB Output Signal Select (Table 57.)
Default: "00" (SDTIA)

BVMX1-0: SRC-B Input Signal Select (Table 59.)
Default: "00" (SDTIA)

SDOL1-0: SDTO Lch Output Mixing (Table 45.)
Default: "00" (Lch Signal Selected by Table 44)

SDOR1-0: SDTO Rch Output Mixing (Table 46.)
Default: "00" (Rch Signal Selected by Table 44)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5AH	SAR ADC Control	0	0	0	GPOM1	GPOE1	A1	A0	PMSAD
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMSAD: 10bit ADC Power Management
"0": Power down (default)
"1": Power up

A1-0: SAR ADC Measurement Mode (Table 113)
Default: "00" (SAIN1)

GPOE1: General Purpose Output 1 Enable at GPOM1 bit = "1"
"0": GPO pin = "L" (default)
"1": GPO pin = "H"

GPOM1: General Purpose Output 1 Operation Mode
"0": Controlled by GPOE1 bit (default)
"1": Controlled by A0 bit

■ Register Map (HP/SPK-Amp Blocks)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMMHR	PMMHL	PMHPR	PMHPL	PMCP	PMOSC	PMVCMA
01H	Power Management 1	GDDLY	0	0	0	0	0	0	PMSPK
02H	Power Management 2	0	0	0	0	0	0	0	PMV1
03H	Mode Control 0	THDET	0	0	0	0	0	0	0
04H	Lch Headphone Mixer	0	0	0	0	0	0	HPLR1	HPLL1
05H	Rch Headphone Mixer	0	0	0	0	0	0	HPRR1	HPRL1
06H	Reserved	0	0	0	0	0	0	0	0
07H	Reserved	0	0	0	0	0	0	0	0
08H	Input Volume #1	R1V3	R1V2	R1V1	R1V0	L1V3	L1V2	L1V1	L1V0
09H	Reserved	0	0	0	0	0	0	0	0
0AH	Reserved	0	0	0	0	0	0	0	0
0BH	Reserved	0	0	0	0	0	0	0	0
0CH	Mode Control 1	0	0	MOFF	0	PTS1	PTS0	0	0
0DH	Headphone PGA Control	0	HPZ	HPMTN	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
0EH	Speaker PGA Control	0	0	SPGA5	SPGA4	SPGA3	SPGA2	SPGA1	SPGA0
0FH	ALCA Mode Control 1	0	0	REFA5	REFA4	REFA3	REFA2	REFA1	REFA0
10H	ALCA Mode Control 2	0	0	0	ZTMA1	ZTMA0	WTMA2	WTMA1	WTMA0
11H	ALCA Mode Control 3	0	ALCA	ZELMNA	LMATA1	LMATA0	RGAINA1	RGAINA0	LMTHA
12H	Mode Control 2	0	0	0	0	0	BATCPU	MSEL	OSCN

All registers writing are inhibited at PDNA pin = "L".
The PDNA pin = "L" resets the HP/SPK-Amp's registers to their default value.

Note 88: The bits defined as 0 must contain a "0" value.
Note 89: Only write to address 00H to 12H.

■ Register Definitions (HP/SPK-Amp Blocks)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMMHR	PMMHL	PMHPR	PMHPL	PMCP	PMOSC	PMVCMA
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCMA: Power Management for VCOM and Regulator which used for Headphone-Amp
0: Power OFF (default)
1: Power ON

PMOSC: I Power Management for Internal Oscillator
0: Power OFF (default)
1: Power ON

PMCP: Power Management for Charge Pump Circuit
0: Power OFF (default)
1: Power ON

PMHPL: Power Management for Lch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMHPR: Power Management for Rch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMMHL: Power Management for Mixing & Selector Circuit of Lch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMMHR: Power Management for Mixing & Selector Circuit of Rch Headphone-Amp
0: Power OFF (default)
1: Power ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 1	GDDLY	0	0	0	0	0	0	PMSPK
R/W		R/W	RD	RD	RD	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	0

PMSPK: Power Management for Speaker-Amp
0: Power OFF (default)
1: Power ON
When PMSP bit is "0", the SPP pin and SPN pin become Hi-Z.

GDDLY: Gate driver delay setting for dulling output wave of Class-D
0: 15ns (default)
1: 60ns
Delay increase, EMI improve, Efficiency down when "0" → "1"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 2	0	0	0	0	0	0	0	PMV1
R/W		RD	RD	RD	RD	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	0

PMV1: Power Management for Input Volume #1
0: Power OFF (default)
1: Power ON

All blocks of HP/SPK-Amp blocks can be powered-down by setting the PDNA pin to "L" regardless of register values setup. In this case, all control register values of HP/SPK-Amp blocks are initilized.

When all registers in address 00H, 01H and 02H are set to "0", all blocks of HP/SPK-Amp blocks are powered-down. The register values of HP/SPK-Amp blocks remain unchanged. Power supply current is 18μA(typ). For fully shut down, set the PDNA pin to "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 0	THDET	0	0	0	0	0	0	0
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

THDET: Thermal Shutdown Detection
0: Normal Operation (default)
1: Thermal Shutdown

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch Headphone Mixer	0	0	0	0	0	0	HPLR1	HPLL1
05H	Rch Headphone Mixer	0	0	0	0	0	0	HPRR1	HPRL1
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

Input Mixers: (Figure 80)
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Input Volume #1	R1V3	R1V2	R1V1	R1V0	L1V3	L1V2	L1V1	L1V0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	0	1	0	1	0

Input Volumes: Default: 0dB (Table 76)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Mode Control 1	0	0	MOFF	0	PTS1	PTS0	0	0
	R/W	RD	RD	R/W	RD	R/W	R/W	RD	RD
	Default	0	0	0	0	0	0	0	0

PTS1-0: Headphone-Amp Mute ON/OFF Transition Time
Default: "00"; typ. 16.4ms (Table 81)

MOFF: Soft transition for changing HPMTN bit
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Headphone PGA Control	0	HPZ	HPMTN	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	1

HPGA4-0: Headphone-Amp Volume Setting
Default: 19H; 0dB (Table 77)

HPMTN: Headphone-Amp Mute
0: Mute (default)
1: Normal Output

HPZ: Headphone-Amp Pull-down Control
0: Ground Mode (default)
HPL/HPR pins are shorted to VSS3.
1: Hi-Z Mode
HPL/HPR pins are pulled-down by 25kΩ(typ) to VSS3.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Speaker PGA Control	0	0	SPGA5	SPGA4	SPGA3	SPGA2	SPGA1	SPGA0
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	0

SPGA5-0: Speaker-Amp Volume Setting
Default: 18H; 0dB (Table 89)

When PMSPK bit is set to "0", reading and writing of SPGA5-0 bits are inhibited. When changing from PMSPK bit = "0" to PMSPK bit = "1", SPGA volume becomes default value (0dB) regardless of the setting of SPGA5-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	ALCA Mode Control 1	0	0	REFA5	REFA4	REFA3	REFA2	REFA1	REFA0
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	1	1	1	1	0	0

REFA5-0: Reference value at ALC Recovery Operation
Default: 3CH; +18dB (Table 87)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	ALCA Mode Control 2	0	0	0	ZTMA1	ZTMA0	WTMA2	WTMA1	WTMA0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

WTMA2-0: ALCA Recovery Waiting Period
Default: "101", typ. 524.8ms (@OSCN bit = "0") (Table 85)

ZTMA1-0: ALCA Zero Crossing Timeout Period
Default: "01", typ. 32.8ms (@ OSCN bit = "0") (Table 84)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	ALCA Mode Control 3	0	ALCA	ZELMNA	LMATA1	LMATA0	RGAINA1	RGAINA0	LMTHA
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTHA: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level
Default: "0" (Table 82)

RGAINA1-0: ALCA Recovery GAIN Step
Default: "00"; 1 step (Table 86)

LMATA1-0: ALCA Limiter ATT Step
Default: "00"; 1 step (Table 83)

ZELMNA: Zero Crossing Detection Enable at ALCA Limiter Operation
0: Enable (default)
1: Disable

ALCA: ALCA Enable
0: ALCA Disable (default)
1: ALCA Enable
When ALC bit is set to "1", the ALCA operation is enabled. The initial value is "0" (Disable).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Mode Control 2	0	0	0	0	0	BATCPU	MSEL	OSCN
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

OSCN: Internal Oscillator / External Clock Select
0: Internal Oscillator (default)
1: External Clock (MCKIA pin)

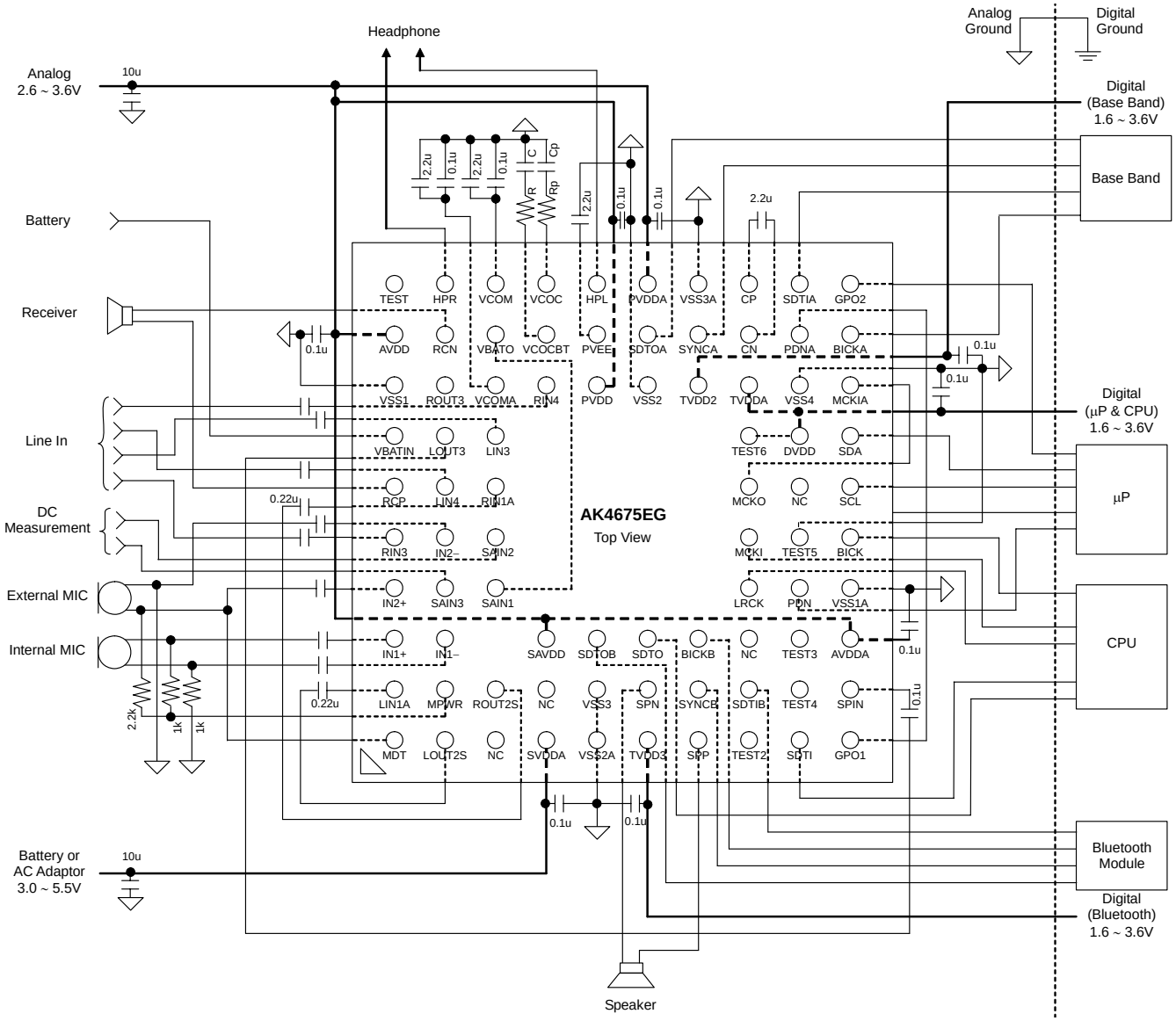
MSEL: MCKIA Input Frequency Select
0: 2.048MHz (default)
1: 2.8224MHz or 3.072MHz

BATCPU: Battery Monitor Circuit Enable
0: Disable (default)
1: Enable

SYSTEM DESIGN

Figure 114 shows the system connection diagram for the AK4675. An evaluation board [AKD4675] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

Condition: Internal Full-differential Mic, External pseudo differential Mic, Receiver Output, I²C mode; Battery Monitor is used; the PDNA pin of HP/SPK-Amp blocks is controlled by the GPO1 pin.



Notes:

- VSS1, VSS2, VSS3, VSS4, VSS1A, VSS2A and VSS3A of the AK4675 must be distributed separately from the ground of external controllers.
- All digital input pins msut not be left floating.
- When the AK4675 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC pin is not needed.
- When the AK4675 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC pin is shown in Table 4.
- When the AK4675 is in master mode, the LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor msut be connected to the LRCK and BICK pins of the AK4675.
- A resistor and capacitor of the VCOCBT pin is shown in Table 95.
- When PCM I/F is used at master mode, SYNCA, BICKA, SYNCB and BICKB pins are floating before PMPCM bit is changed to "1". Therefore, 100kΩ around pull-up or pull-down resistor msut be connected to the SYNCA, BICKA, SYNCB and SYNCB pins of the AK4675.
- These capacitors at the CP/CN pins and VSS3A/PVEE pins require low ESR (Equivalent Series Resistance) over all temperature range. When these capacitors are polarized, the positive side must be connected to the CP and VSS3A pins, respectively.
- A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin.
- A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOMA pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOMA pin.
- AC coupling capacitors of 0.22μF or smaller value msut be connected at the LIN1A/RIN1A pins respectively to reduce pop noise at Headphone-Amp power-up.
- AC coupling capacitors of 0.1μF or smaller value must be connected at the SPIN pins respectively to reduce pop noise at power-up of ALCA block for Speaker.

Figure 114. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4675 requires careful attention to power supply and grounding arrangements. AVDD, PVDD, SAVDD, DVDD, TVDD2, TVDD3, AVDDA, PVDDA, SVDDA and TVDDA are usually supplied from the system's analog supply. TVDDA must be connected to DVDD. If AVDD, PVDD, SAVDD, DVDD, TVDD2, AVDDA, PVDDA and SVDDA are supplied separately, the power-up sequence is not critical. VSS1, VSS2, VSS3, VSS4, VSS1A, VSS2A and VSS3A of the AK4675 must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4675 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of CODEC block. VCOMA is a signal ground of HP/SPK-Amp blocks. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOMA pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM/VCOMA pins. All signals, especially clocks, should be kept away from the VCOM and VCOMA pins in order to avoid unwanted coupling into the AK4675.

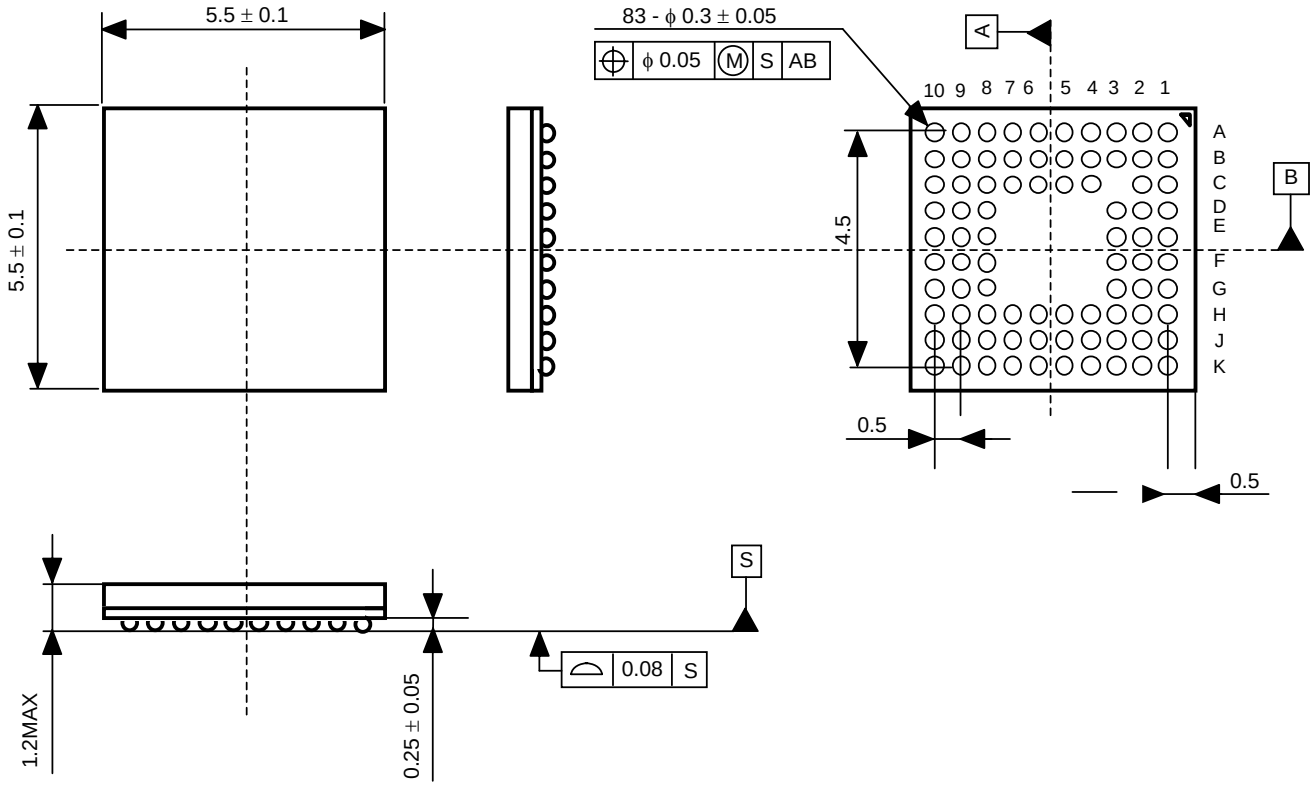
3. Analog Inputs

The Mic, Line and MIN inputs of CODEC block are single-ended. The input signal range scales with nominally at 0.6 x AVDD Vpp (typ) at MGNL=MGNR=0dB and single-ended input, centered at the internal common voltage of CODEC block (0.5 x AVDD). The inputs of HP/SPK-Amp blocks are single-ended. The input signal range is 2.0Vpp (typ) for LIN1A/RIN1A pins and 1.6Vpp (typ) for SPLIN/SPRIN pins respectively, centered at the internal common voltage of HP/SPK-Amp blocks (VCOMA=1.2V (typ)). The input signal should be AC coupled using a capacitor. The cut-off frequency is fc = 1/ (2πRC). The AK4675 can accept input voltages from VSS1 to AVDD for CODEC block and from VSS1A to AVDDA for HP/SPK-Amp blocks, respectively.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output for 0000H(@16bit) is VCOM voltage for CODEC block and VCOMA voltage for HP/SPK-Amp blocks, respectively. VCOM voltage is 0.5 x AVDD (typ) and VCOMA voltage is 1.2Vpp (typ), respectively. The output of LOUT1/RCP, ROUT1/RCN, LOUT2S, ROUT2S, LOUT3/LOP, ROUT3/LON pins must be AC coupled using a capacitor. The output of HPL and HPR pins must be directly connected to the headphone without AC coupling.

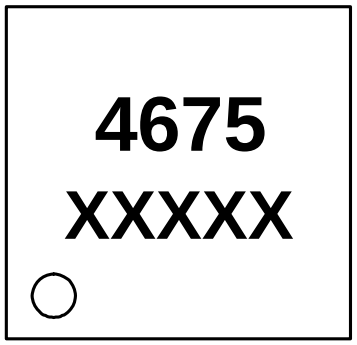
PACKAGE



■ Material & Lead finish

Package molding compound:	Epoxy
Interposer material:	BT resin
Solder ball material:	SnAgCu

MARKING



XXXXX: Date code identifier (5digits)
Pin #1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/05/23	00	First Edition		

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