

**AK4671****Stereo CODEC with MIC/RCV/HP-AMP****GENERAL DESCRIPTION**

The AK4671 is a stereo CODEC with a built-in Microphone-Amplifier, Receiver-Amplifier and Headphone-Amplifier. The AK4671 features dual PCM I/F in addition to audio I/F that allows easy interfacing in mobile phone designs with Bluetooth I/F. The AK4671 is available in a 57pin BGA, utilizing less board space than competitive offerings.

FEATURES

1. Recording Function (Stereo CODEC)
 - 4 Stereo Input Selector x 2ch
 - 4 Stereo Inputs (Single-ended) or 2 Stereo Input (Full-differential)
 - MIC Amplifier: +30dB ~ -12dB, 3dB step
 - Digital ALC (Automatic Level Control): +36dB ~ -54dB, 0.375dB Step, Mute
 - Wind-noise Reduction Filter
 - Stereo Separation Emphasis
 - 5-band Programmable Notch Filter
 - Audio Interface Format: 16bit MSB justified, I²S, DSP Mode
2. Playback Function (Stereo CODEC)
 - Digital Volume (+12dB ~ -115.0dB, 0.5dB Step, Mute)
 - Digital ALC (Automatic Level Control): +36dB ~ -54dB, 0.375dB Step, Mute
 - Stereo Separation Emphasis
 - 5-band EQ
 - Stereo Line Output
 - Mono Receiver-Amp
 - BTL Output
 - Output Power: 30mW@32Ω (AVDD=3.3V)
 - Stereo Headphone-Amp
 - Output Power: 30mW@16Ω (AVDD=3.3V)
 - Analog Mixing: 4 Stereo Input
 - Audio Interface Format:
 - 16bit MSB justified, 16bit LSB justified, 16-24bit I²S, DSP Mode
3. Dual PCM I/F for Baseband & Bluetooth Interface
 - Sample Rate Converter (Up sample: up to x6: Down sample: down to x1/6)
 - Sample Rate: 8kHz
 - Digital Volume
 - Audio Interface Format:
 - 16bit Linear, 8bit A-law, 8bit μ -law
 - Short/Long Frame, I²S, MSB justified
4. 10bit SAR ADC
 - 3 Input Selector
5. Power Management
6. Master Clock:
 - (1) PLL Mode
 - Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz, 27MHz (MCKI pin)
 - 1fs (LRCK pin)
 - 32fs or 64fs (BICK pin)
 - (2) External Clock Mode
 - Frequencies: 256fs, 384fs, 512fs, 768fs or 1024fs (MCKI pin)
7. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
8. Sampling Rate (Stereo CODEC):

- PLL Slave Mode (LRCK pin): 8kHz ~ 48kHz
 - PLL Slave Mode (BICK pin): 8kHz ~ 48kHz
 - PLL Slave Mode (MCKI pin):
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - PLL Master Mode:
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - EXT Master/Slave Mode:
8kHz ~ 48kHz (256fs, 384fs), 8kHz ~ 26kHz (512fs, 768fs),
8kHz ~ 13kHz (1024fs)
9. μ P I/F: 4-wire Serial / I²C Bus (Ver 1.0, 400kHz Fast Mode)
10. Master/Slave mode
11. Ta = -30 ~ 85°C
12. Power Supply:
- AVDD, PVDD, SAVDD: 2.2 ~ 3.6V
 - DVDD, TVDD2, TVDD3: 1.6 ~ 3.6V
13. Package : 57pin BGA (5mm x 5mm, 0.5mm pitch)

■ Block Diagram

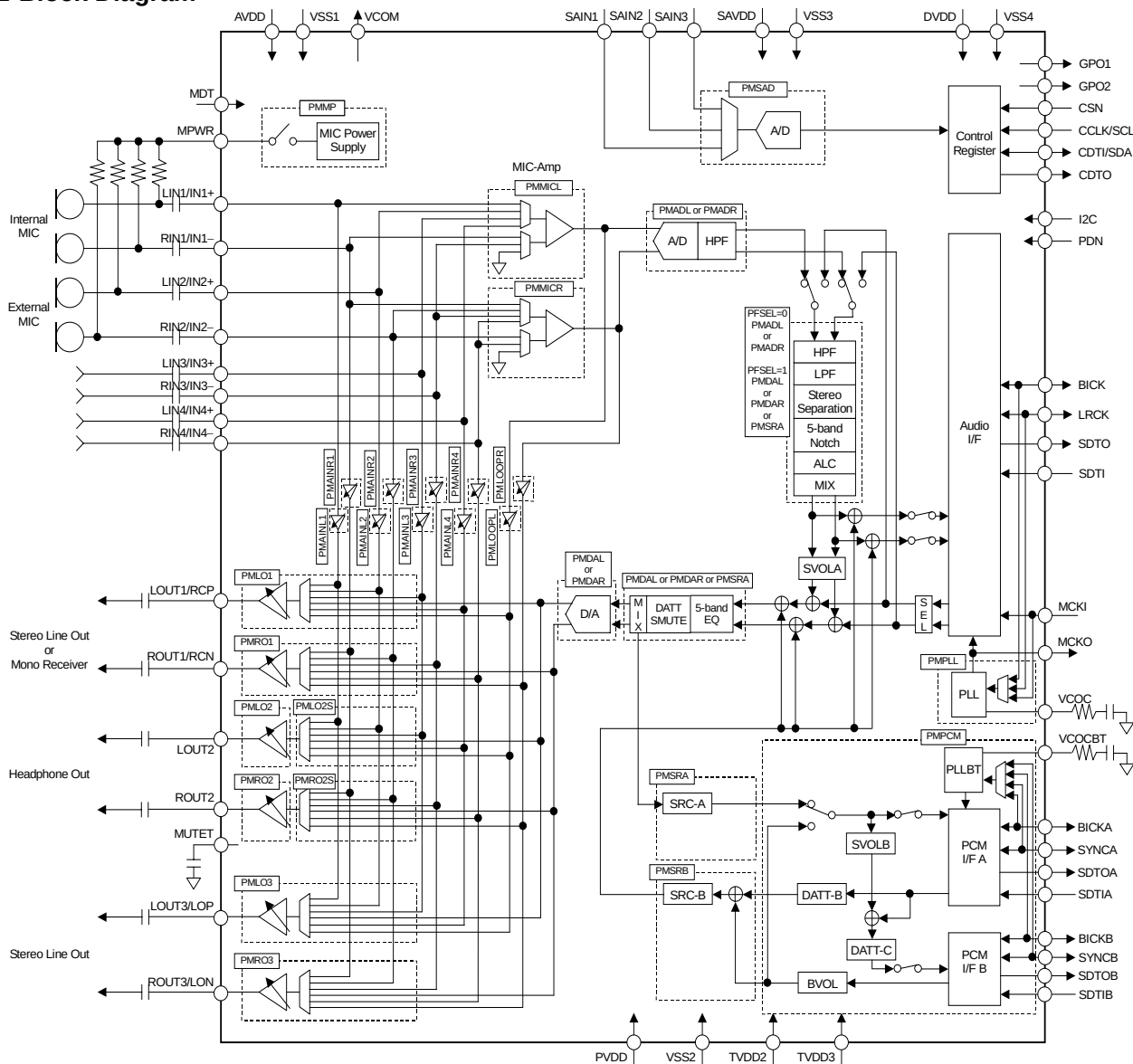


Figure 1. Block Diagram

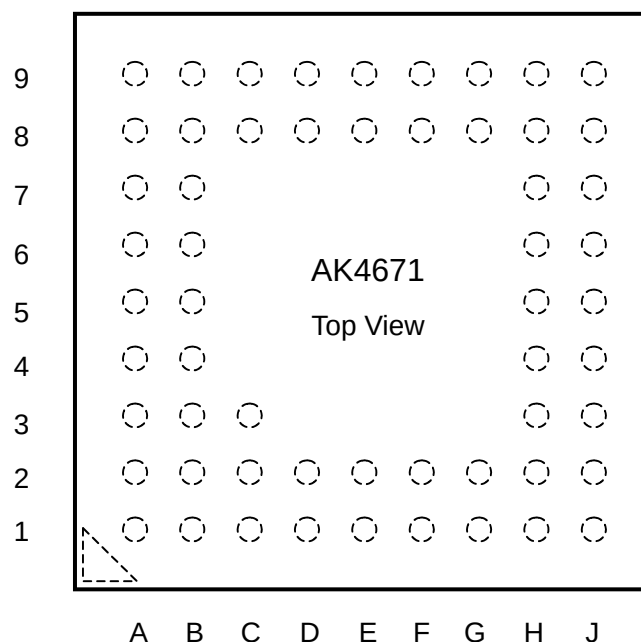
■ Ordering Guide

AK4671EG
AKD4671

−30 ~ +85°C
Evaluation board for AK4671

57pin BGA (0.5mm pitch)

■ Pin Layout



9	TEST	LOUT2	ROUT2	VCOM	VCOCBT	VSS2	SDTOA	SYNCA	GPO2
8	AVDD	VSS1	MUTET	VCOC	PVDD	TVDD2	BICKA	CDTI /SDA	SDTIA
7	LOUT1 /RCP	ROUT1 /RCN	Top View					VSS4	DVDD
6	ROUT3 /LON	LOUT3 /LOP						CCLK /SCL	CSN /CAD0
5	RIN4 /IN4−	LIN4 /IN4+						I2C	BICK
4	LIN3 /IN3+	RIN3 /IN3−						MCKI	MCKO
3	LIN2 /IN2+	RIN2 /IN2−	NC					PDN	LRCK
2	LIN1 /IN1+	RIN1 /IN1−	SAIN2	SAVDD	TVDD3	SDTOB	BICKB	SDTO	CDTO
1	MDT	MPWR	SAIN3	SAIN1	VSS3	SYNCB	SDTIB	SDTI	GPO1
	A	B	C	D	E	F	G	H	J

PIN/FUNCTION			
No.	Pin Name	I/O	Function
A1	MDT	I	MIC Detection Pin (Internal pull down by 500kΩ)
B1	MPWR	O	MIC Power Supply Pin
C1	SAIN3	I	10bit SAR ADC Analog Input 3 Pin
C2	SAIN2	I	10bit SAR ADC Analog Input 2 Pin
D1	SAIN1	I	10bit SAR ADC Analog Input 1 Pin
D2	SAVDD	-	10bit SAR ADC Power Supply Pin, 2.2 ~ 3.6V
E1	VSS3	-	Ground 3 Pin
E2	TVDD3	-	Digital I/O Power Supply 3 Pin, 1.6 ~ 3.6V
F2	SDTOB	O	Serial Data Output B Pin
F1	SYNCB	I/O	Sync Signal B Pin
G2	BICKB	I/O	Serial Data Clock B Pin
G1	SDTIB	I	Serial Data Input B Pin
H1	SDTI	I	Audio Serial Data Input Pin
J1	GPO1	O	General Purpose Output 1 Pin
J2	CDTO	O	Control Data Output Pin (I2C pin = "L": 4-wire Serial Mode) Hi-Z (I2C pin = "H": I ² C Bus Mode)
H2	SDTO	O	Audio Serial Data Output Pin
H3	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register. "L" time of 150ns or more after power-up is needed to reset the AK4671.
J3	LRCK	I/O	Input / Output Channel Clock Pin
H4	MCKI	I	External Master Clock Input Pin
J4	MCKO	O	Master Clock Output Pin
H5	I2C	I	Control Mode Select Pin "H": I ² C Bus, "L": 4-wire Serial
J5	BICK	I/O	Audio Serial Data Clock Pin
J6	CSN	I	Chip Select Pin (I2C pin = "L": 4-wire Serial Mode)
	CAD0	I	Chip Address 0 Select Pin (I2C pin = "H": I ² C Bus Mode)
H6	CCLK	I	Control Data Clock Pin (I2C pin = "L": 4-wire Serial Mode)
	SCL	I	Control Data Clock Pin (I2C pin = "H": I ² C Bus Mode)
H7	VSS4	-	Ground 4 Pin
J7	DVDD	-	Digital Power Supply Pin, 1.6 ~ 3.6V
H8	CDTI	I	Control Data Input Pin (I2C pin = "L": 4-wire Serial Mode)
	SDA	I/O	Control Data Input Pin (I2C pin = "H": I ² C Bus Mode)
J9	GPO2	O	General Purpose Output 2 Pin

No.	Pin Name	I/O	Function
J8	SDTIA	I	Serial Data Input A Pin
G8	BICKA	I/O	Serial Data Clock A Pin
H9	SYNCA	I/O	Sync Signal A Pin
G9	SDTOA	O	Serial Data Output A Pin
F8	TVDD2	-	Digital I/O Power Supply 2 Pin, 1.6 ~ 3.6V
F9	VSS2	-	Ground 2 Pin
E8	PVDD	-	PLLBT Power Supply Pin, 2.2 ~ 3.6V
E9	VCOCBT	O	Output Pin for Loop Filter of PLLBT Circuit This pin should be connected to VSS2 pin with one resistor and capacitor in series.
D8	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to VSS1 pin with one resistor and capacitor in series.
D9	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs and DAC outputs.
C8	MUTET	O	Mute Time Constant Control Pin Connected to VSS1 pin with a capacitor for mute time constant.
C9	ROUT2	O	Rch Headphone-Amp Output Pin
B9	LOUT2	O	Lch Headphone-Amp Output Pin
A9	TEST	-	Test Pin This pin should be open.
A8	AVDD	-	Analog Power Supply Pin, 2.2 ~ 3.6V
B8	VSS1	-	Ground 1 Pin
B7	ROUT1	O	Rch Stereo Line Output 1 Pin (RCV bit = "0": Stereo Line Output)
	RCN	O	Receiver-Amp Negative Output Pin (RCV bit = "1": Receiver Output)
A7	LOUT1	O	Lch Stereo Line Output 1 Pin (RCV bit = "0": Stereo Line Output)
	RCP	O	Receiver-Amp Positive Output Pin (RCV bit = "1": Receiver Output)
A6	ROUT3	O	Rch Stereo Line Output 3 Pin (LODIF bit = "0": Single-ended Stereo Output)
	LON	O	Negative Line Output Pin (LODIF bit = "1": Full-differential Mono Output)
B6	LOUT3	O	Lch Stereo Line Output 3 Pin (LODIF bit = "0": Single-ended Stereo Output)
	LOP	O	Positive Line Output Pin (LODIF bit = "1": Full-differential Mono Output)
A5	RIN4	I	Rch Analog Input 4 Pin (MDIF4 bit = "0": Single-ended Input)
	IN4-	I	Negative Line Input 4 Pin (MDIF4 bit = "1": Full-differential Input)
B5	LIN4	I	Lch Analog Input 4 Pin (MDIF4 bit = "0": Single-ended Input)
	IN4+	I	Positive Line Input 4 Pin (MDIF4 bit = "1": Full-differential Input)
B4	RIN3	I	Rch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input)
	IN3-	I	Negative Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input)
A4	LIN3	I	Lch Analog Input 3 Pin (MDIF3 bit = "0": Single-ended Input)
	IN3+	I	Positive Line Input 3 Pin (MDIF3 bit = "1": Full-differential Input)
B3	RIN2	I	Rch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input)
	IN2-	I	Negative Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input)
A3	LIN2	I	Lch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input)
	IN2+	I	Positive Line Input 2 Pin (MDIF2 bit = "1": Full-differential Input)
B2	RIN1	I	Rch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input)
	IN1-	I	Negative Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input)
A2	LIN1	I	Lch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input)
	IN1+	I	Positive Line Input 1 Pin (MDIF1 bit = "1": Full-differential Input)
C3	NC	-	No Connect Pin No internal bonding. This pin should be open or connected to the ground.

Note 1. All input pins except analog input pins (MDT, LIN1/IN1+, RIN1/IN1-, LIN2/IN2+, RIN2/IN2-, LIN3/IN3+, RIN3/IN3-, LIN4/IN4+, RIN4/IN4-, SAIN1, SAIN2, SAIN3) should not be left floating.
I/O pins except SDA pin (LRCK, BICK, SYNCA, BICKA, SYNCB, BICKB) should be processed appropriately.
Please refer the "[Master Mode/Slave Mode](#)" (P.45) and "[PCM I/F Master Mode/Slave Mode](#)" (P.105). SDA pin should be pulled-up by a resistor externally and be connected to (DVDD+0.3)V or less voltage.

■ Handling of Unused Pin on the System

The unused I/O pins on the system should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, MDT, VCOC, ROUT3/LON, LOUT3/LOP, ROUT2, LOUT2, MUTET, ROUT1/RCN, LOUT1/RCP, RIN4/IN4-, LIN4/IN4+, RIN3/IN3-, LIN3/IN3+, RIN2/IN2-, LIN2/IN2+, RIN1/IN1-, LIN1/IN1+, VCOCBT, SAIN1, SAIN2, SAIN3	These pins should be open.
Digital	MCKO, SDTOA, SDTOB, GPO1, GPO2, CDTO	These pins should be open.
	MCKI, SDTIA, SDTIB	These pins should be connected to VSS4.
	BICKA, SYNCA, BICKB, SYNCB	When all pins are unused, these pins should be connected to VSS4 and PMPCM bit must be always "0". When either PCM I/F A(BICKA/ SYNCA) or PCM I/F B(BICKB/SYNCB) is used, unused pins are connected to pull-down/up resistor of about 100kΩ.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; [Note 2](#), [Note 3](#))

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	−0.3	4.0	V
	PLLBT	PVDD	−0.3	4.0	V
	10bit SAR ADC	SAVDD	−0.3	4.0	V
	Digital	DVDD	−0.3	4.0	V
	Digital I/O 2	TVDD2	−0.3	4.0	V
	Digital I/O 3	TVDD3	−0.3	4.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage 1 (Note 4)		VINA1	−0.3	AVDD+0.3	V
Analog Input Voltage 2 (Note 5)		VINA2	−0.3	SAVDD+0.3	V
Digital Input Voltage 1 (Note 6)		VIND1	−0.3	DVDD+0.3	V
Digital Input Voltage 2 (Note 7)		VIND2	−0.3	TVDD2+0.3	V
Digital Input Voltage 3 (Note 8)		VIND3	−0.3	TVDD3+0.3	V
Ambient Temperature (powered applied)		Ta	−30	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground.

Note 3. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.

Note 4. RIN4/IN4⁻, LIN4/IN4⁺, RIN3/IN3⁻, LIN3/IN3⁺, RIN2/IN2⁻, LIN2/IN2⁺, RIN1/IN1⁻, LIN1/IN1⁺ pins

Note 5. SAIN1, SAIN2, SAIN3 pins

Note 6. PDN, I2C, CSN/CAD0, CCLK/SCL, CDTI/SDA, SDTI, LRCK, BICK, MCKI pins

Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

Note 7. BICKA, SYNCA, SDTIA pins

Note 8. BICKB, SYNCB, SDTIB pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 9)	Analog	AVDD	2.2	3.3	3.6	V
	PLLBT	PVDD	2.2	3.3	3.6	V
	10bit SAR ADC	SAVDD	2.2	3.3	3.6	V
	Digital	DVDD	1.6	3.3	3.6	V
	Digital I/O 2	TVDD2	1.6	3.3	3.6	V
	Digital I/O 3	TVDD3	1.6	3.3	3.6	V
	Difference	AVDD–PVDD	–0.1	0	+0.1	V

Note 2. All voltages with respect to ground.

Note 9. The power-up sequence between AVDD, PVDD, SAVDD, DVDD, TVDD2 and TVDD3 is not critical.

The PDN pin should be held to “L” when power-up. The PDN pin should be set to “H” after all power supplies are powered-up. The AK4671 should be operated by the recommended power-up/down sequence shown in “[System Design \(Grounding and Power Supply Decoupling\)](#)” to avoid pop noise at receiver output, headphone output and line output.

When the power is OFF partially except for DVDD, all power management bits (PMVCM, PMMP, PMM1CL, PMM1CR, PMADL, PMADR, PMDAL, PMDAR, PMPLL, PMLOOPL, PMLOOPR, PMAINL1, PMAINR1, PMAINL2, PMAINR2, PMAINL3, PMAINR3, PMAINL4, PMAINR4, PMLO1, PMRO1, PMLO2, PMRO2, PMLO2S, PMRO2S, PMLO3, PMRO3, PMSRA, PMSRB, PMPCM, PMSAD) should be “0” or the PDN pin should be “L”. DVDD should not be powered OFF while AVDD, PVDD, SAVDD, TVDD2 or TVDD3 is powered ON. When only DVDD is OFF, the current of 10mA to 100mA around may occur.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=3.3V; VSS1=VSS2=VSS3=VSS4=0V;
Signal Frequency=1kHz; 16bit Data; fs=44.1kHz, BICK=64fs; Measurement frequency=20Hz ~ 20kHz; unless
otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins; PMAINL1/R1/L2/R2/L3/R3/L4/R4 bits = "0"					
Input Resistance					
	MGNL/R0 bit = "0"	28	42	56	kΩ
	MGNL/R0 bit = "1"	20	30	40	kΩ
Gain (Note 10)					
	Max (MGNL/R3-0 bits = "FH")	-	+30	-	dB
	Min (MGNL/R3-0 bits = "1H")	-	-12	-	dB
MIC Power Supply: MPWR pin					
Output Voltage (Note 11)		2.47	2.64	2.81	V
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
MIC Detection: MDT pin					
Comparator Voltage Level (Note 12)		0.165		0.247	mV
Internal pull down Resistance		250	500	750	kΩ
Stereo ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins → Stereo ADC → IVOL, IVOL=0dB, ALC=OFF					
Resolution		-	-	16	Bits
Input Voltage (Note 13)	(Note 14)	0.150	0.176	0.203	V _{pp}
	(Note 15)	1.68	1.98	2.28	V _{pp}
S/(N+D) (-1dBFS)	(Note 14)	72	82	-	dB
	(Note 15)	-	87	-	dB
D-Range (-60dBFS, A-weighted)	(Note 14)	75	85	-	dB
	(Note 15)	-	95	-	dB
S/N (A-weighted)	(Note 14)	75	85	-	dB
	(Note 15)	-	95	-	dB
Interchannel Isolation	(Note 14)	75	90	-	dB
	(Note 15)	-	100	-	dB
Interchannel Gain Mismatch	(Note 14)	-	0.1	0.8	dB
	(Note 15)	-	0.1	0.8	dB

Note 10. In case of full-differential input, MGAIN=0dB (min) and AVDD=2.4V (min).

Note 11. Output voltage is proportional to AVDD voltage. V_{out} = 0.8 x AVDD (typ).

Note 12. Comparator Voltage Level is proportional to AVDD voltage. V_{th} = 0.05 x AVDD(min), 0.075 x AVDD(max).

Note 13. Input voltage is proportional to AVDD voltage. V_{in} = 0.053 x AVDD (typ)@MGNL3-0=MGNR3-0 bits = "CH" (+21dB), V_{in} = 0.6 x AVDD(typ)@MGNL3-0=MGNR3-0 bits = "5H" (0dB).

Note 14. MGNL3-0=MGNR3-0 bits = "CH" (+21dB).

Note 15. MGNL3-0=MGNR3-0 bits = "5H" (0dB).

Parameter	min	typ	max	Units
Stereo DAC Characteristics:				
Resolution	-	-	16	Bits
Stereo Line Output Characteristics: Stereo DAC → LOUT1/ROUT1/LOUT3/ROUT3 pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L1VL=L3VL=0dB, RCV bit = "0", $R_L=10k\Omega$; unless otherwise specified.				
Output Voltage (Note 16)	1.78	1.98	2.18	V _{pp}
S/(N+D) (0dBFS)	75	85	-	dB
S/N (A-weighted)	82	92	-	dB
Interchannel Isolation	85	100	-	dB
Interchannel Gain Mismatch	-	0.1	0.8	dB
Load Resistance	10	-	-	k Ω
Load Capacitance	-	-	30	pF
Mono Receiver-Amp Output Characteristics: Stereo DAC → RCP/RCN pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L1VL=0dB, RCV bit = "1", $R_L=32\Omega$, BTL; unless otherwise specified.				
Output Voltage (Note 17)				
-6dBFS, $R_L=32\Omega$ (Po=15mW)	1.76	1.96	2.16	V _{pp}
-3dBFS, $R_L=32\Omega$ (Po=30mW)	-	2.77	-	V _{pp}
S/(N+D)				
-6dBFS, $R_L=32\Omega$ (Po=15mW)	40	60	-	dB
-3dBFS, $R_L=32\Omega$ (Po=30mW)	-	20	-	dB
S/N (A-weighted)	82	92	-	dB
Load Resistance	32	-	-	Ω
Load Capacitance (Note 18)	-	-	30	pF
Headphone-Amp Characteristics: DAC → LOUT2/ROUT2 pins, ALC=OFF, IVOL=0dB, OVOL=0dB, HPG=0dB, $R_L=16\Omega$				
Output Voltage (Note 19)				
-6dBFS (Po=7.6mW)	0.89	0.99	1.09	V _{pp}
0dBFS (Po=30mW)	-	1.98	-	V _{pp}
S/(N+D)				
-6dBFS (Po=7.6mW)	40	60	-	dB
0dBFS (Po=30mW)	-	40	-	dB
S/N (A-weighted)	80	90	-	dB
Interchannel Isolation	65	75	-	dB
Interchannel Gain Mismatch	-	0.1	0.8	dB
Load Resistance	16	-	-	Ω
Load Capacitance	C1 in Figure 2	-	30	pF
	C2 in Figure 2	-	300	pF

Note 16. Output voltage is proportional to AVDD voltage. $V_{out} = 0.6 \times AVDD$ (typ).

Note 17. Output voltage is proportional to AVDD voltage. $V_{out} = (RCP) - (RCN) = 0.59 \times AVDD$ (typ)@-6dBFS.

Note 18. Load Capacitance for VSS1.

Note 19. Output voltage is proportional to AVDD voltage. $V_{out} = 0.3 \times AVDD$ (typ)@-6dBFS.

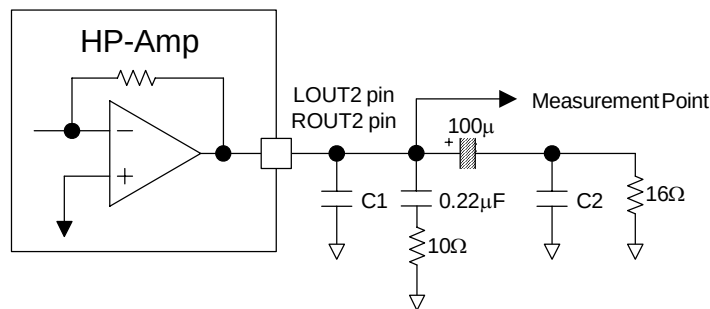


Figure 2. Headphone-Amp output circuit

Parameter	min	typ	max	Units
Mono Line Output Characteristics: Stereo DAC → LOP/LON pins, ALC=OFF, IVOL=0dB, OVOL=0dB, L3VL=0dB, LODIF bit = "1", $R_L=10k\Omega$ for each pin (Full-differential)				
Output Voltage (Note 20)	3.52	3.96	4.36	V _{pp}
S/(N+D) (0dBFS)	75	85	-	dB
S/N (A-weighted)	85	95	-	dB
Load Resistance (LOP/LON pins, respectively)	10	-	-	k Ω
Load Capacitance (LOP/LON pins, respectively) (Note 21)	-	-	30	pF
Single-ended Line Input: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins; (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")				
Maximum Input Voltage (Note 22)	-	1.98	-	V _{pp}
Gain				
Input → LOUT1/ROUT1/LOUT2/ROUT2/LOUT3/ROUT3 (LODIF=RCV bits = "0")				
	-1	0	+1	dB
Input → RCP/RCN/LOP/LON (LODIF=RCV bits = "1")				
	-	+6	-	dB
Full-differential Line Input: IN1+/-, IN2+/-, IN3+/-, IN4+/- pins; (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")				
Maximum Input Voltage (Note 23)	-	1.98	-	V _{pp}
Gain				
Input → LOUT1/ROUT1/LOUT2/ROUT2/LOUT3/ROUT3 (LODIF=RCV bits = "0")				
	-1	0	+1	dB
Input → RCP/RCN/LOP/LON (LODIF=RCV bits = "1", Note 24)				
	-	+6	-	dB
Power Supply Current:				
Power Up (PDN pin = "H", All Circuits Power-up)				
AVDD+PVDD+DVDD (Note 25)	-	21	-	mA
+TVDD2+TVDD3+SAVDD (Note 26)	-	23	30	mA
(Note 27)	-	8	12	mA
Power Down (PDN pin = "L") (Note 28)				
AVDD+PVDD+DVDD	-	1	30	μ A
+TVDD2+TVDD3+SAVDD	-			

Note 20. Output voltage is proportional to AVDD voltage. $V_{out} = (LOP) - (LON) = 1.2 \times AVDD$ (typ).

Note 21. Load Capacitance for VSS1.

Note 22. Maximum Input voltage which analog output does not clip is proportional to AVDD voltage. $V_{in} = 0.6 \times AVDD$ (typ).

Note 23. Maximum Input voltage which analog output does not clip is proportional to AVDD voltage. $V_{in} = (IN4+) - (IN4-) = 0.6 \times AVDD$ (typ).

Note 24. $V_{out} = (RCP) - (RCN)$ at RCV bit = "1", $V_{out} = (LOP) - (LON)$ at LODIF bit = "1".

Note 25. EXT Slave Mode and LP bit = "0", $f_s=44.1kHz$, PMMICL = PMMICR = PMADL = PMADR = PMDAL = PMDAR = PMLO1 = PMRO1 = PMLO2 = PMRO2 = PMLO2S = PMRO2S = PMLO3 = PMRO3 = PMSAD =

PMVCM = MUTEN bits = "1", PMPLL = MCKO = PMMP = M/S = PMSRA = PMSRB = PMPCM bits = "0".
 AVDD=13.2mA (typ), PVDD=0mA (typ), DVDD=6.7mA (typ), TVDD2=0mA (typ), TVDD3=0mA (typ),
 SAVDD=0.8mA (typ).

Note 26. PLL Master Mode and LP bit = "0", fs=44.1kHz, PMADL = PMMICL = PMMICR = PMADR = PMDAL =
 PMDAR = PMLO1 = PMRO1 = PMLO2 = PMRO2 = PMLO2S = PMRO2S = PMLO3 = PMRO3 = PMSAD =
 PMVCM = PMPLL = M/S = PMMP = MUTEN bits = "1", MCKO = PMSRA = PMSRB = PMPCM bits = "0",
 PLL Reference Clock = MCKI = 11.2896MHz.

AVDD=14.7mA (typ), PVDD=0mA (typ), DVDD=7.0mA (typ), TVDD2=0mA (typ), TVDD3=0mA (typ),
 SAVDD=0.8mA (typ).

Note 27. In case of LP bit = "1", fs=8kHz, EXT Slave Mode and PMVCM = PMMP = PMMICL = PMADL = PMDAR =
 RCV = PMLO1 = PMRO1 = PMSRA = PMSRB = PMPCM bits = "1".

AVDD=5.2mA (typ), PVDD=0.6mA (typ), DVDD=2.2mA (typ), TVDD2=0mA (typ), TVDD3=0mA (typ),
 SAVDD=0mA (typ).

Note 28. All digital input pins are fixed to each supply pin (DVDD, TVDD2 or TVDD3) or VSS4.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD=TVDD2=TVDD3=3.3V; VSS1=VSS2=VSS3=VSS4=0V;
 Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics (Down Sampling: SRC-A): SDTI → SRC-A → SDTOA/SDTOB					
Resolution		-	-	16	Bits
Input Sample Rate	FSI (fs)	8	-	48	kHz
Output Sample Rate	FSO (fs2)	-	8	-	kHz
THD+N (Input = 1kHz, -1dBFS, Note 29) FSO/FSI = 8kHz/44.1kHz		-	-94	-	dB
Dynamic Range (Input = 1kHz, -60dBFS, Note 29) FSO/FSI = 8kHz/44.1kHz		-	97	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		1	-
SRC Characteristics (Up Sampling: SRC-B): SDTIA/SDTIB → SRC-B → SDTO					
Resolution		-	-	16	Bits
Input Sample Rate	FSI (fs2)	-	8	-	kHz
Output Sample Rate	FSO (fs)	8	-	48	kHz
THD+N (Input = 1kHz, -1dBFS, Note 29) FSO/FSI = 44.1kHz/8kHz		-	-95	-	dB
Dynamic Range (Input = 1kHz, -60dBFS, Note 29) FSO/FSI = 44.1kHz/8kHz		-	100	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1		6	-

Note 29. Measured by Audio Precision System Two Cascade.

Note 30. fs is the sampling frequency for Stereo CODEC. fs2 is for PCM I/F.

ANALOG CHARACTERISTICS (10bit SAR ADC)

(Ta=25°C; AVDD=PVDD=SAVDD=DVDD =TVDD2 =TVDD3=3.3V; VSS1=VSS2=VSS3=VSS4=0V; unless otherwise specified)

Parameter	min	typ	max	Units
10bit SAR ADC Characteristics				
Resolution	-	10	-	Bits
No Missing Codes	9	10	-	Bits
Integral Linearity Error	-	-	±2	LSB
DNL	-	±1	-	LSB
Analog Input Voltage Range	0	-	SAVDD	V
Offset Error	-	-	±3	LSB
Gain Error	-	-	±2	LSB
Accuracy (Note 31)	-	-	±1	%

Note 31. Accuracy is the difference between the output code when 1.1V is input to SAIN1, SAIN2 or SAIN3 pin and the “ideal” code at 1.1V.

FILTER CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=PVDD =SAVDD=2.2 ~ 3.6V; DVDD=TVDD2 =TVDD3=1.6 ~ 3.6V; fs=44.1kHz; Programmable Filter=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 32)	±0.16dB	PB	0	-	17.3	kHz
	−0.66dB		-	19.4	-	kHz
	−1.1dB		-	19.9	-	kHz
	−6.9dB		-	22.1	-	kHz
Stopband		SB	25.9	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 33)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
DAC Digital Filter (LPF):						
Passband (Note 32)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 33)		GD	-	19	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.4	-	dB

Note 32. The passband and stopband frequencies scale with fs (system sampling rate).

For example, DAC is PB=0.454 x fs (@-0.7dB). Each response refers to that of 1kHz.

Note 33. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC.

For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal.

FILTER CHARACTERISTICS (SRC)

(Ta=25°C; AVDD=PVDD = SAVDD=2.2 ~ 3.6V; DVDD=TVDD2 =TVDD3=1.6 ~ 3.6V; fs2=8kHz; Programmable Filter=OFF)

Parameter		Symbol	min	typ	max	Units
Down Sampling (SRC-A): fs=8kHz						
Passband	±0.15dB	PB	0	-	3.0	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	5	-	ms
Down Sampling (SRC-A): fs=11.025kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	4	-	ms
Down Sampling (SRC-A): fs=12kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	4	-	ms
Down Sampling (SRC-A): fs=16kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=22.05kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=24kHz						
Passband	±0.15dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.15	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms

Note 34. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Down Sampling (SRC-A): fs=32kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=44.1kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms
Down Sampling (SRC-A): fs=48kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	69	-	-	dB
Group Delay (Note 34)		GD	-	3	-	ms

Note 34. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Up Sampling (SRC-B): fs=8kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=11.025kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=12kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=16kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=22.05kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=24kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms

Note 34. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

Parameter		Symbol	min	typ	max	Units
Up Sampling (SRC-B): fs=32kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=44.1kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms
Up Sampling (SRC-B): fs=48kHz						
Passband	±0.1dB	PB	0	-	3.1	kHz
Stopband		SB	4.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay (Note 34)		GD	-	2	-	ms

Note 34. The calculated delay time caused by digital filtering. This time is from setting the 16-bit data from the input register to the output register.

DC CHARACTERISTICS

(Ta=25°C; AVDD=PVDD =SAVDD=2.2 ~ 3.6V; DVDD=TVDD2 =TVDD3=1.6 ~ 3.6V)

Parameter		Symbol	min	Typ	max	Units
High-Level Input Voltage 1 (Note 35)	2.2V≤DVDD≤3.6V	VIH1	70%DVDD	-	-	V
	1.6V≤DVDD<2.2V	VIH1	80%DVDD	-	-	V
Low-Level Input Voltage 1 (Note 35)	2.2V≤DVDD≤3.6V	VIL1	-	-	30%DVDD	V
	1.6V≤DVDD<2.2V	VIL1	-	-	20%DVDD	V
High-Level Input Voltage 2 (Note 36)	2.2V≤TVDD2≤3.6V	VIH2	70%TVDD2	-	-	V
	1.6V≤TVDD2<2.2V	VIH2	80%TVDD2	-	-	V
Low-Level Input Voltage 2 (Note 36)	2.2V≤TVDD2≤3.6V	VIL2	-	-	30%TVDD2	V
	1.6V≤TVDD2<2.2V	VIL2	-	-	20%TVDD2	V
High-Level Input Voltage 3 (Note 37)	2.2V≤TVDD3≤3.6V	VIH3	70%TVDD3	-	-	V
	1.6V≤TVDD3<2.2V	VIH3	80%TVDD3	-	-	V
Low-Level Input Voltage 3 (Note 37)	2.2V≤TVDD3≤3.6V	VIL3	-	-	30%TVDD3	V
	1.6V≤TVDD3<2.2V	VIL3	-	-	20%TVDD3	V
High-Level Output Voltage						
(Note 38) (Iout=-200μA)		VOH1	DVDD-0.2	-	-	V
(Note 39) (Iout=-200μA)		VOH2	TVDD2-0.2	-	-	V
(Note 40) (Iout=-200μA)		VOH3	TVDD3-0.2	-	-	V
Low-Level Output Voltage						
(Except SDA pin: Iout=200μA)		VOL1	-	-	0.2	V
(SDA pin, 2.0V≤DVDD≤3.6V: Iout=3mA)		VOL2	-	-	0.4	V
(SDA pin, 1.6V≤DVDD<2.0V: Iout=3mA)		VOL2	-	-	20%DVDD	V
Input Leakage Current						
(Note 41)		Iind	-	-	±2	μA
(Note 42)		Iina	-	-	±2	μA

Note 35. CSN/CAD0, CCLK/SCL, CDTI/SDA, I2C, PDN, BICK, LRCK, SDTI, MCKI pins.

Note 36. BICKA, SYNCA, SDTIA pins.

Note 37. BICKB, SYNCB, SDTIB pins.

Note 38. MCKO, BICK, LRCK, SDTO, CDTO, GPO1, GPO2 pins.

Note 39. BICKA, SYNCA, SDTOA pins.

Note 40. BICKB, SYNCB, SDTOB pins.

Note 41. SYNCB, BICKB, SDTIB, SDTI, LRCK, MCKI, BICK, CSN/CAD0, CCLK/SCL, CDTI/SDA, SDTIA, BICKA, SYNCA pins.

I/O pins (SYNCB, BICKB, LRCK, BICK, SDA, BICKA, SYNCA) are at the time of Input state.

Note 42. SAIN1, SAIN2, SAIN3 pins.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=PVDD =SAVDD=2.2 ~ 3.6V; DVDD=TVDD2 =TVDD3=1.6 ~ 3.6V; CL=20pF (except SDA pin) or 400pF (SDA pin); unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.256	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
LRCK Output Timing					
Frequency	fs	8	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle	Duty	-	50	-	%
BICK Output Timing					
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	ns
Duty Cycle		dBCK	-	50	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.256	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
LRCK Input Timing					
Frequency	fs	8	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK-60	-	1/fs - tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
BICK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns

Parameter	Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = LRCK pin)					
LRCK Input Timing					
Frequency	fs	8	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK-60	-	1/fs - tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
BICK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)					
LRCK Input Timing					
Frequency	fs	8	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK-60	-	1/fs - tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
BICK Input Timing					
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode					
MCKI Input Timing					
Frequency	256fs	fCLK	2.048	-	12.288 MHz
	384fs	fCLK	3.072	-	18.432 MHz
	512fs	fCLK	4.096	-	13.312 MHz
	768fs	fCLK	6.144	-	19.968 MHz
	1024fs	fCLK	8.192	-	13.312 MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing					
Frequency	256fs/384fs	fs	8	-	48 kHz
	512fs/768fs	fs	8	-	26 kHz
	1024fs	fs	8	-	13 kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK-60	-	1/fs - tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
BICK Input Timing					
Period	tBCK	312.5	-	-	ns
Pulse Width Low	tBCKL	130	-	-	ns
Pulse Width High	tBCKH	130	-	-	ns
External Master Mode					
MCKI Input Timing					
Frequency	256fs	fCLK	2.048	-	12.288 MHz
	384fs	fCLK	3.072	-	18.432 MHz
	512fs	fCLK	4.096	-	13.312 MHz
	768fs	fCLK	6.144	-	19.968 MHz
	1024fs	fCLK	8.192	-	13.312 MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing					
Frequency	fs	8	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle	Duty	-	50	-	%
BICK Output Timing					
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	ns
Duty Cycle	dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK “↑” to BICK “↑” (Note 43)	tDBF	$0.5 \times \text{tBCK} - 40$	$0.5 \times \text{tBCK}$	$0.5 \times \text{tBCK} + 40$	ns
LRCK “↑” to BICK “↓” (Note 44)	tDBF	$0.5 \times \text{tBCK} - 40$	$0.5 \times \text{tBCK}$	$0.5 \times \text{tBCK} + 40$	ns
BICK “↑” to SDTO (BCKP bit = “0”)	tBSD	-70	-	70	ns
BICK “↓” to SDTO (BCKP bit = “1”)	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK “↑” to BICK “↑” (Note 43)	tLRB	$0.4 \times \text{tBCK}$	-	-	ns
LRCK “↑” to BICK “↓” (Note 44)	tLRB	$0.4 \times \text{tBCK}$	-	-	ns
BICK “↑” to LRCK “↑” (Note 43)	tBLR	$0.4 \times \text{tBCK}$	-	-	ns
BICK “↓” to LRCK “↑” (Note 44)	tBLR	$0.4 \times \text{tBCK}$	-	-	ns
BICK “↑” to SDTO (BCKP bit = “0”)	tBSD	-	-	80	ns
BICK “↓” to SDTO (BCKP bit = “1”)	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Audio Interface Timing (Right/Left justified & I²S)					
Master Mode					
BICK “↓” to LRCK Edge (Note 45)	tMBLR	-40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)	tLRD	-70	-	70	ns
BICK “↓” to SDTO	tBSD	-70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK “↑” (Note 45)	tLRB	50	-	-	ns
BICK “↑” to LRCK Edge (Note 45)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)	tLRD	-	-	80	ns
BICK “↓” to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 43. MSBS, BCKP bits = “00” or “11”.

Note 44. MSBS, BCKP bits = “01” or “10”.

Note 45. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKA, SYNCA, SDTIA, SDTOA pins; Slave Mode):					
SYNCA Timing					
Frequency	fs2	-	8	-	kHz
Serial Interface Timing at Short/long Frame Sync					
BICKA Frequency	fBCK2	128	-	2048	kHz
BICKA Period	tBCK2	488	-	-	ns
BICKA Pulse Width Low	tBCKL2	200	-	-	ns
Pulse Width High	tBCKH2	200	-	-	ns
SYNCA Edge to BICKA “↓” (Note 46)	tSYB2	50	-	-	ns
SYNCA Edge to BICKA “↑” (Note 47)	tSYB2	50	-	-	ns
BICKA “↓” to SYNCA Edge (Note 46)	tBSY2	50	-	-	ns
BICKA “↑” to SYNCA Edge (Note 47)	tBSY2	50	-	-	ns
SYNCA to SDTOA (MSB) (Except Short Frame)	tSYD2	-	-	80	ns
BICKA “↑” to SDTOA (BCKPA bit = “0”)	tBSD2	-	-	80	ns
BICKA “↓” to SDTOA (BCKPA bit = “1”)	tBSD2	-	-	80	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Pulse Width Low	tSYL2	0.8 x tBCK2	-	-	ns
Pulse Width High	tSYH2	0.8 x tBCK2	-	-	ns
Serial Interface Timing at MSB justified and I²S					
BICKA Frequency	fBCK2	256	-	2048	kHz
BICKA Period	tBCK2	488	-	-	ns
BICKA Pulse Width Low	tBCKL2	200	-	-	ns
Pulse Width High	tBCKH2	200	-	-	ns
SYNCA Edge to BICKA “↑”	tSYB2	50	-	-	ns
BICKA “↑” to SYNCA Edge	tBSY2	50	-	-	ns
SYNCA to SDTOA (MSB) (Except I ² S mode)	tSYD2	-	-	80	ns
BICKA “↓” to SDTOA	tBSD2	-	-	80	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Duty Cycle	dSYC2	45	50	55	%

Note 46. MSBSA, BCKPA bits = “00” or “11”.

Note 47. MSBSA, BCKPA bits = “01” or “10”.

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKA, SYNCA, SDTIA, SDTOA pins; Master Mode):					
SYNCA Timing					
Frequency	fs2	-	8	-	kHz
BICKA Timing					
Period (BCKO2 bit = "0")	tBCK2	-	1/(16fs2)	-	ns
(BCKO2 bit = "1")	tBCK2	-	1/(32fs2)	-	ns
Duty Cycle	dBCK2	-	50	-	%
Serial Interface Timing at Short/long Frame Sync					
SYNCA Edge to BICKA "↓" (Note 46)	tSYB2	0.5 x tBCK2 - 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
SYNCA Edge to BICKA "↑" (Note 47)	tSYB2	0.5 x tBCK2 - 40	0.5 x tBCK2	0.5 x tBCK2 + 40	ns
BICKA "↑" to SDTOA (BCKPA bit = "0")	tBSD2	-70	-	70	ns
BICKA "↓" to SDTOA (BCKPA bit = "1")	tBSD2	-70	-	70	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Pulse Width High	tSYH2	-	tBCK2	-	ns
Serial Interface Timing at MSB justified and I²S					
BICKA "↓" to SYNCA Edge	tMBSY2	-40	-	40	ns
SYNCA to SDTOA (MSB) (Except I ² S mode)	tSYD2	-70	-	70	ns
BICKA "↓" to SDTOA	tBSD2	-70	-	70	ns
SDTIA Hold Time	tSDH2	50	-	-	ns
SDTIA Setup Time	tSDS2	50	-	-	ns
SYNCA Duty Cycle	dSYC2	-	50	-	%

Note 46. MSBSA, BCKPA bits = "00" or "11".

Note 47. MSBSA, BCKPA bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKB, SYNCB, SDTIB, SDTOB pins; Slave Mode):					
SYNCB Timing					
Frequency	fs2	-	8	-	kHz
Serial Interface Timing at Short/long Frame Sync					
BICKB Frequency	fBCK3	128	-	2048	kHz
BICKB Period	tBCK3	488	-	-	ns
BICKB Pulse Width Low	tBCKL3	200	-	-	ns
Pulse Width High	tBCKH3	200	-	-	ns
SYNCB Edge to BICKB “↓” (Note 48)	tSYB3	50	-	-	ns
SYNCB Edge to BICKB “↑” (Note 49)	tSYB3	50	-	-	ns
BICKB “↓” to SYNCB Edge (Note 48)	tBSY3	50	-	-	ns
BICKB “↑” to SYNCB Edge (Note 49)	tBSY3	50	-	-	ns
SYNCB to SDTOB (MSB) (Except Short Frame)	tSYD3	-	-	80	ns
BICKB “↑” to SDTOB (BCKPB bit = “0”)	tBSD3	-	-	80	ns
BICKB “↓” to SDTOB (BCKPB bit = “1”)	tBSD3	-	-	80	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Pulse Width Low	tSYL3	0.8 x tBCK3	-	-	ns
Pulse Width High	tSYH3	0.8 x tBCK3	-	-	ns
Serial Interface Timing at MSB justified and I²S					
BICKB Frequency	fBCK3	256	-	2048	kHz
BICKB Period	tBCK3	488	-	-	ns
BICKB Pulse Width Low	tBCKL3	200	-	-	ns
Pulse Width High	tBCKH3	200	-	-	ns
SYNCB Edge to BICKB “↑”	tSYB3	50	-	-	ns
BICKB “↑” to SYNCB Edge	tBSY3	50	-	-	ns
SYNCB to SDTOB (MSB) (Except I ² S mode)	tSYD3	-	-	80	ns
BICKB “↓” to SDTOB	tBSD3	-	-	80	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Duty Cycle	dSYC3	45	50	55	%

Note 48. MSBSB, BCKPB bits = “00” or “11”.

Note 49. MSBSB, BCKPB bits = “01” or “10”.

Parameter	Symbol	min	typ	max	Units
PCM Interface Timing (BICKB, SYNCB, SDTIB, SDTOB pins; Master Mode):					
SYNCB Timing					
Frequency	fs2	-	8	-	kHz
BICKB Timing					
Period (BCKO2 bit = "0")	tBCK3	-	1/(16fs2)	-	ns
(BCKO2 bit = "1")	tBCK3	-	1/(32fs2)	-	ns
Duty Cycle	dBCK3	-	50	-	%
Serial Interface Timing at Short/long Frame Sync					
SYNCB Edge to BICKB "↓" (Note 48)	tSYB3	0.5 x tBCK3 - 40	0.5 x tBCK3	0.5 x tBCK3 + 40	ns
SYNCB Edge to BICKB "↑" (Note 49)	tSYB3	0.5 x tBCK3 - 40	0.5 x tBCK3	0.5 x tBCK3 + 40	ns
BICKB "↑" to SDTOB (BCKPB bit = "0")	tBSD3	-70	-	70	ns
BICKB "↓" to SDTOB (BCKPB bit = "1")	tBSD3	-70	-	70	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Pulse Width High	tSYH3	-	tBCK3	-	ns
Serial Interface Timing at MSB justified and I²S					
BICKB "↓" to SYNCB Edge	tMBSY3	-40	-	40	ns
SYNCB to SDTOB (MSB) (Except I ² S mode)	tSYD3	-70	-	70	ns
BICKB "↓" to SDTOB	tBSD3	-70	-	70	ns
SDTIB Hold Time	tSDH3	50	-	-	ns
SDTIB Setup Time	tSDS3	50	-	-	ns
SYNCB Duty Cycle	dSYC3	-	50	-	%

Note 48. MSBSB, BCKPB bits = "00" or "11".

Note 49. MSBSB, BCKPB bits = "01" or "10".

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire Serial mode)					
CCLK Period (Note 51)	tCCK	200	-	33000	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
CCLK Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN “H” Time	tCSW	150	-	-	ns
CSN Edge to CCLK “↑” (Note 52)	tCSS	50	-	-	ns
CCLK “↑” to CSN Edge (Note 52)	tCSH	50	-	-	ns
CDTO Delay	tDCD	-	-	70	ns
CSN “↑” to CDTO Hi-Z	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus mode): (Note 50)					
SCL Clock Frequency (Note 53)	fSCL	30	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 54)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 55)	tPD	150	-	-	ns
PMADL or PMADR “↑” to SDTO valid (Note 56)	tPDV	-	1059	-	1/fs
PMSRA “↑” to SDTOA valid (Note 57)	tPDV2	-	21	-	1/fs2
PMSRB “↑” to SDTO valid (Note 58)	tPDV3	-	135	-	1/fs

Note 50. I²C-bus is a trademark of NXP B.V.

Note 51. CCLK should be input succeedingly until 10bit data of SAR ADC is read out at 4-wire serial mode (Figure 97).

Note 52. CCLK rising edge must not occur at the same time as CSN edge.

Note 53. In case that SAR ADC data is read out via I²C bus, SCL should be input succeedingly corresponding 2 byte data including ACK (Figure 104).

Note 54. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 55. The AK4671 can be reset by bringing PDN pin = “L” to “H” only upon power up.

Note 56. This is the count of LRCK “↑” from the PMADL or PMADR bit = “1” at PMSRB bit = “1”.

Note 57. The signal path is SDTI → SRC-A → SDTOA and PLLBT is locked.

Note 58. The signal path is SDTIA → SRC-B → SDTO.

■ Timing Diagram

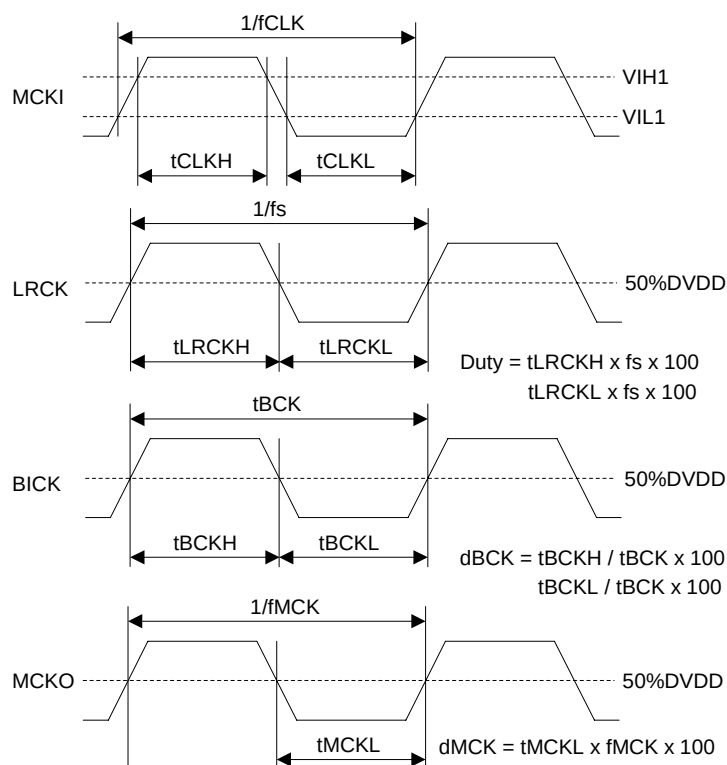


Figure 3. Clock Timing (PLL/EXT Master mode)

Note 59. MCKO is not available at EXT Master mode.

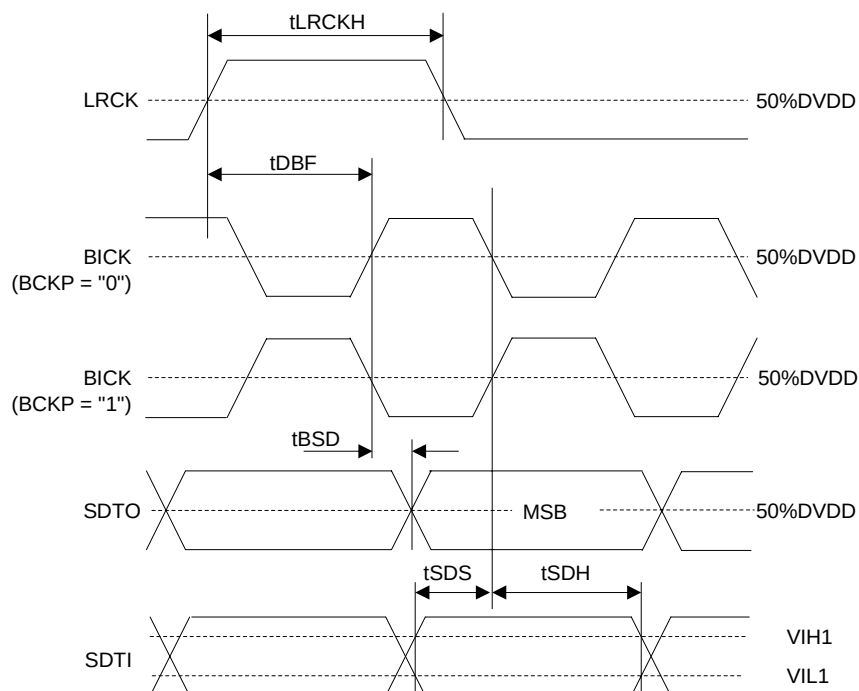


Figure 4. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "0")

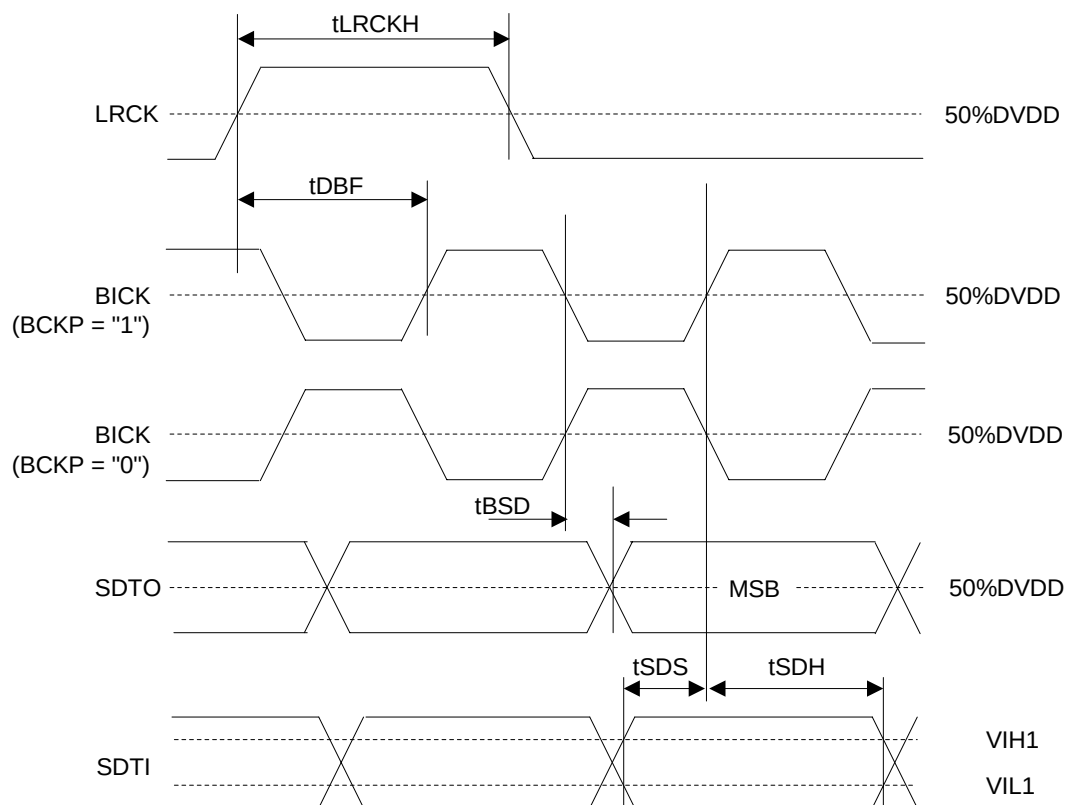


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

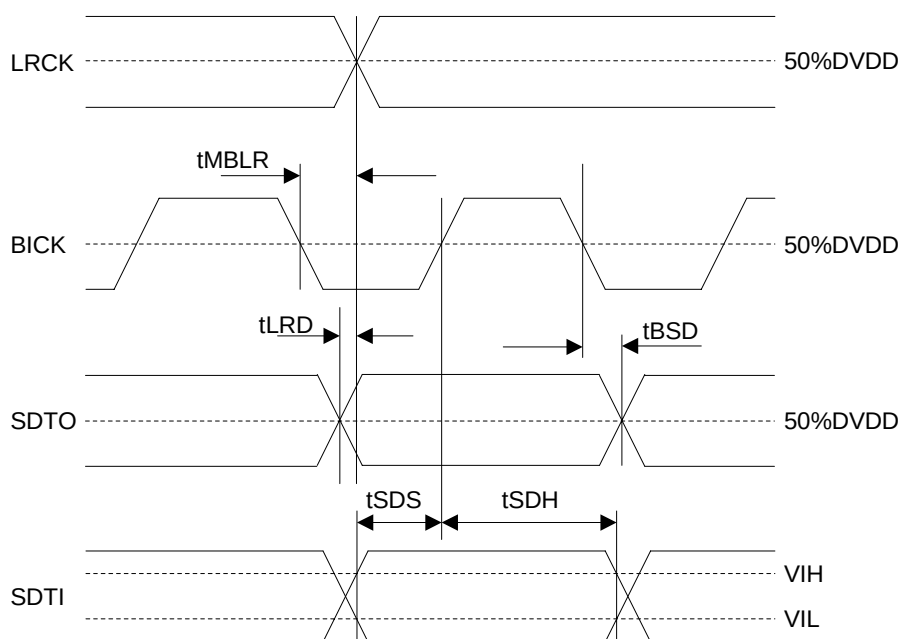


Figure 6. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

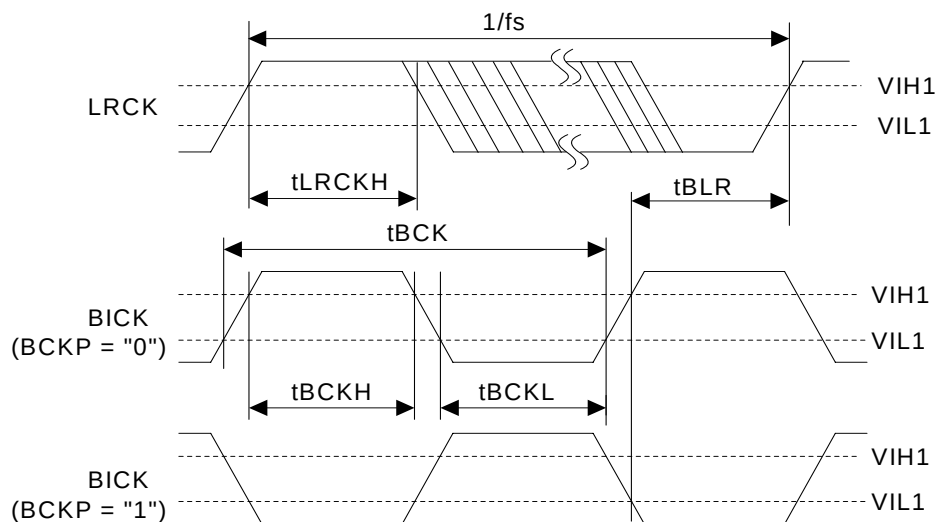


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "0")

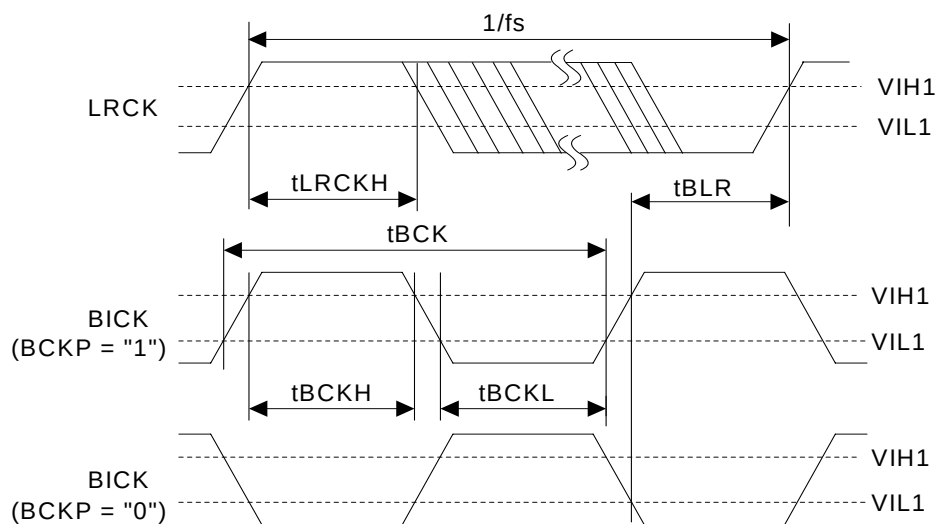


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "1")

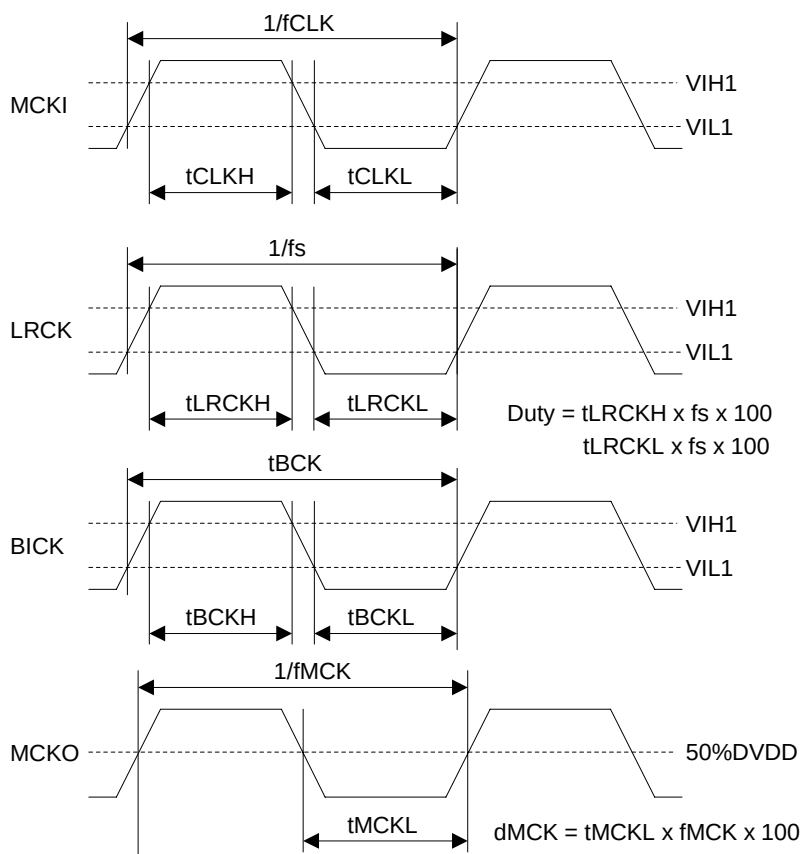


Figure 9. Clock Timing (PLL Slave mode; Except DSP mode)

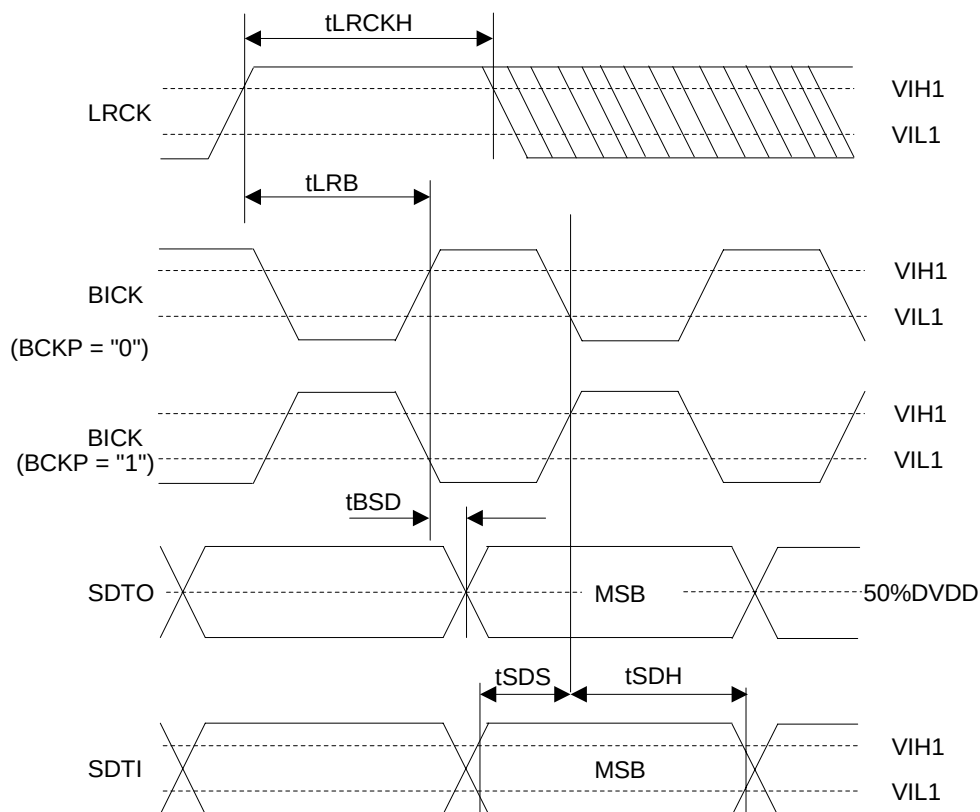


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = "0")

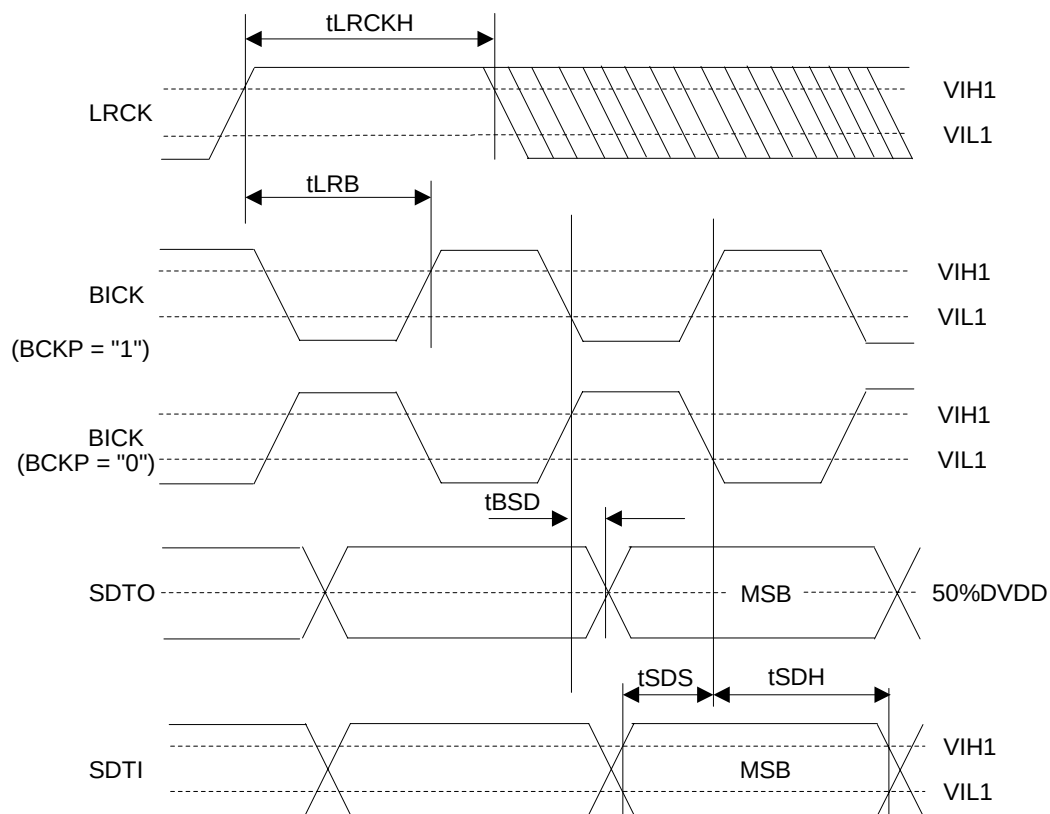


Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = "1")

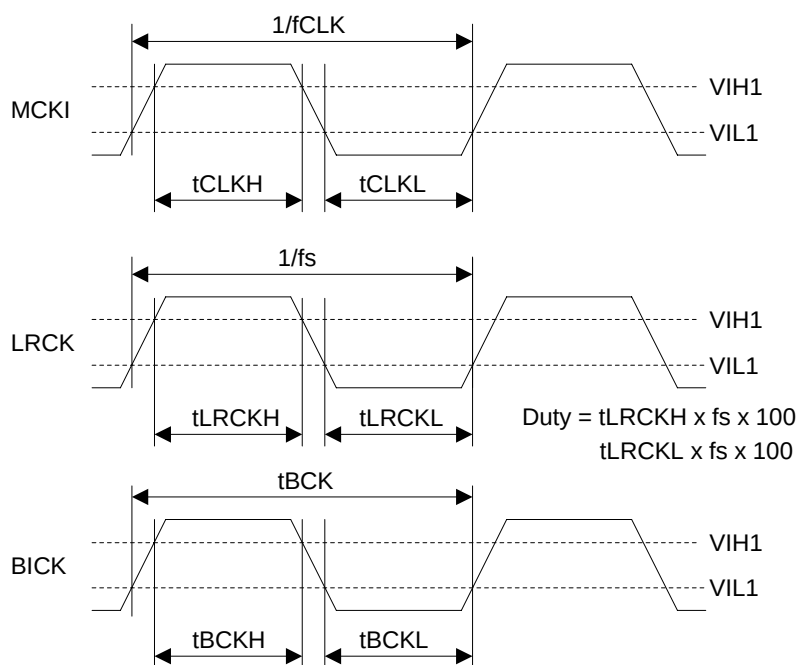


Figure 12. Clock Timing (EXT Slave mode)

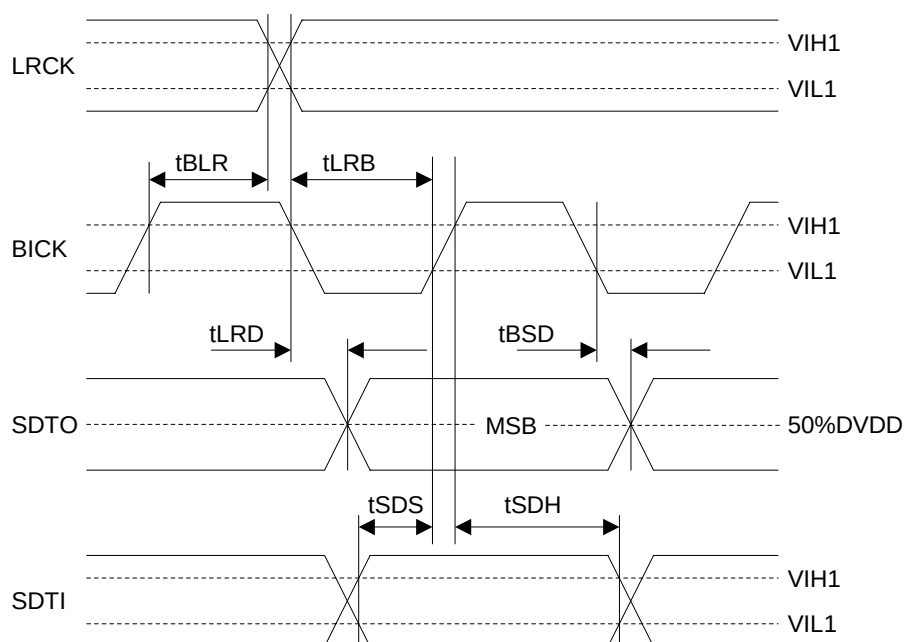


Figure 13. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

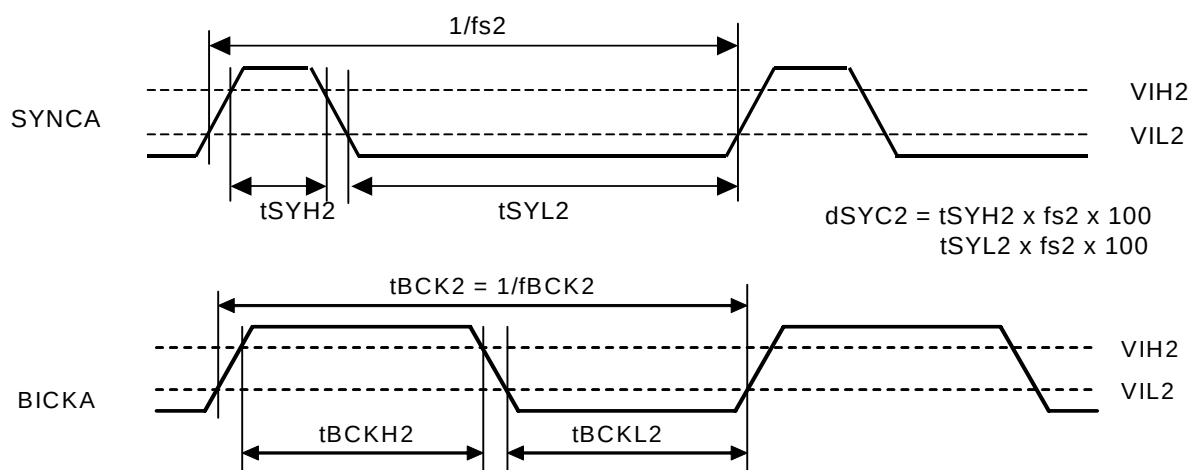


Figure 14. Clock Timing of PCM I/F A (Slave mode)

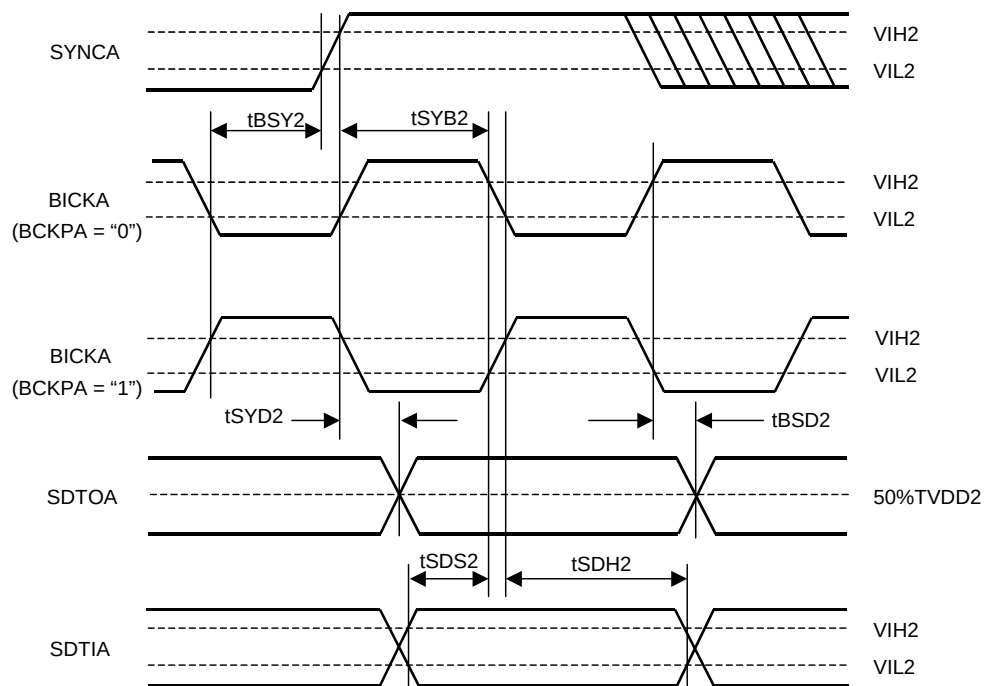


Figure 15. PCM I/F A Timing at short and long frame sync (Slave mode; MSBSA = "0")

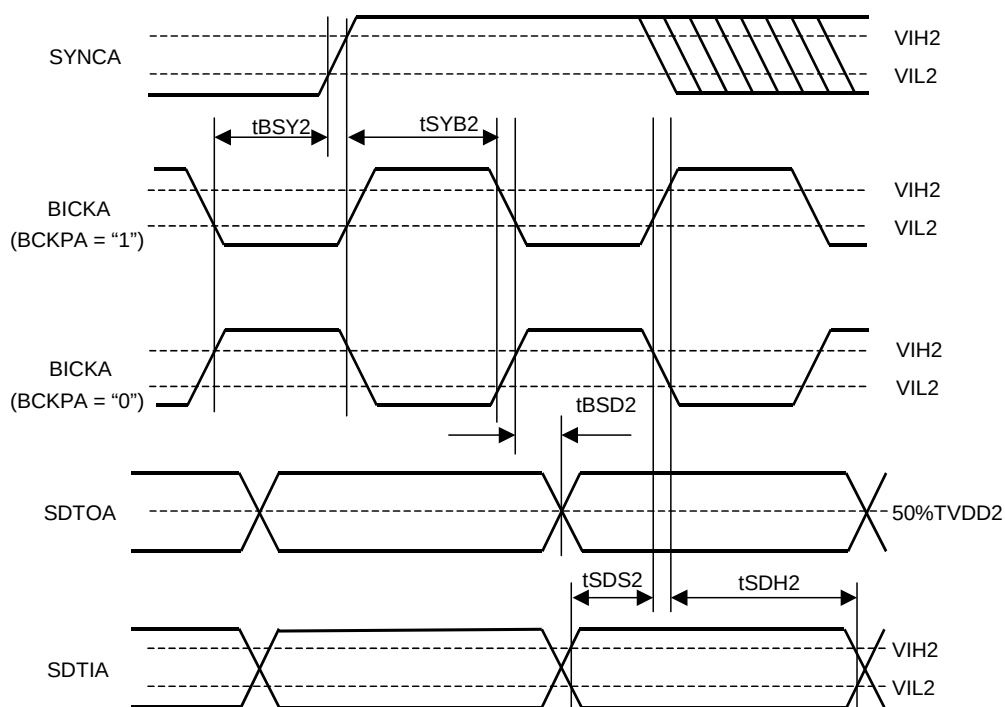


Figure 16. PCM I/F A Timing at short and long frame sync (Slave mode; MSBSA = "1")

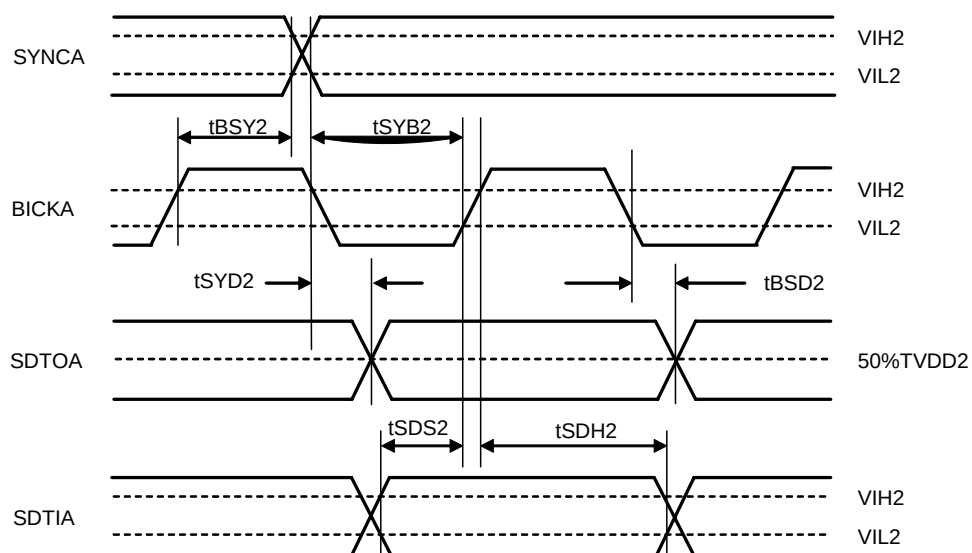
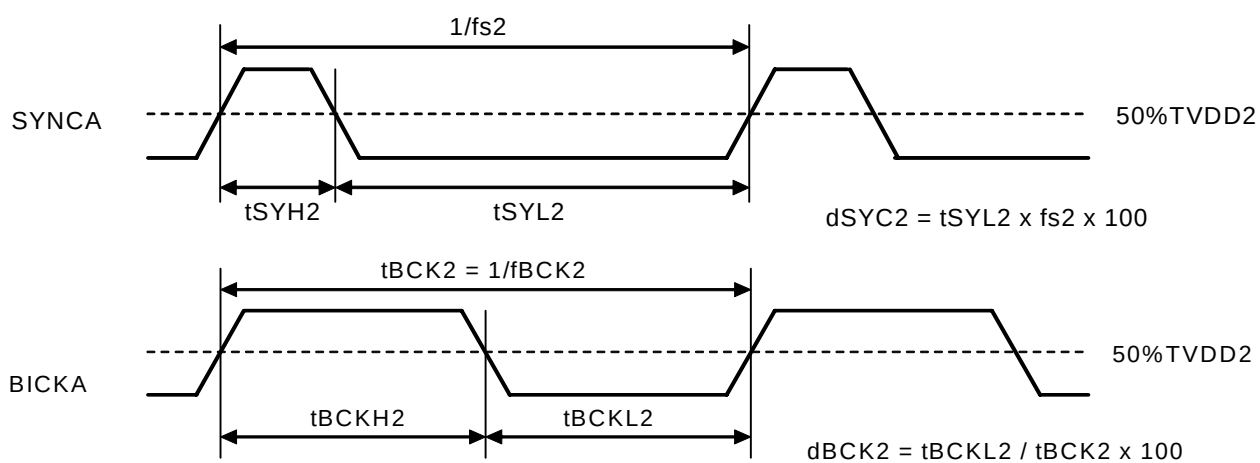
Figure 17. PCM I/F A Timing at MSB justified and I²S (Slave mode)

Figure 18. Clock Timing of PCM I/F A (Master mode)

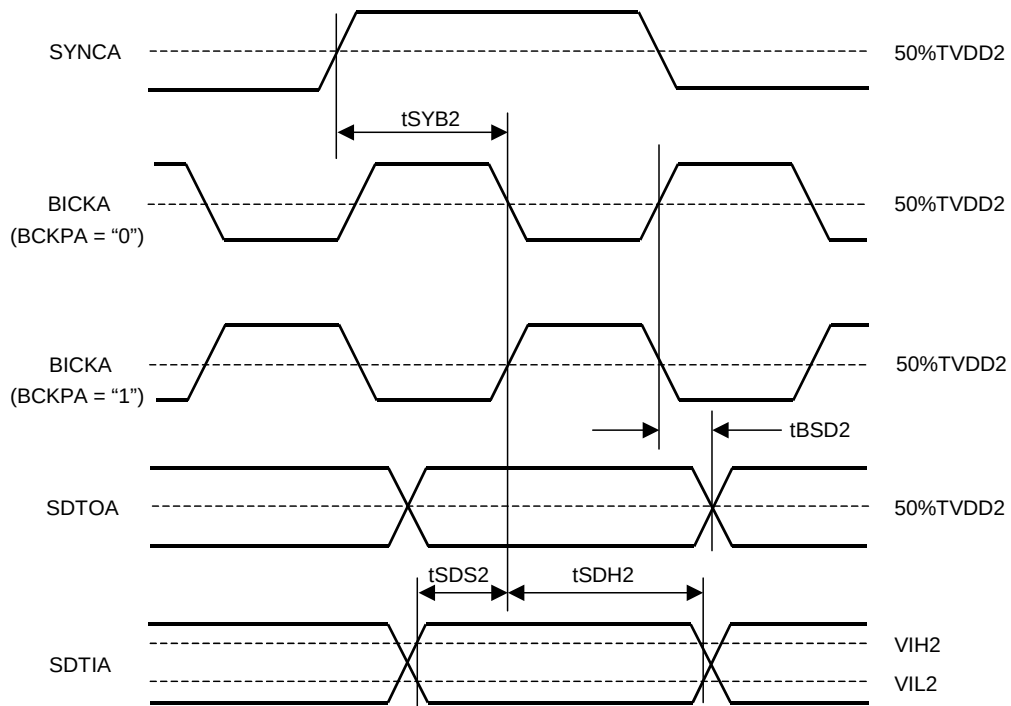


Figure 19. PCM I/F A Timing at short and long frame sync (Master mode; MSBSA = "0")

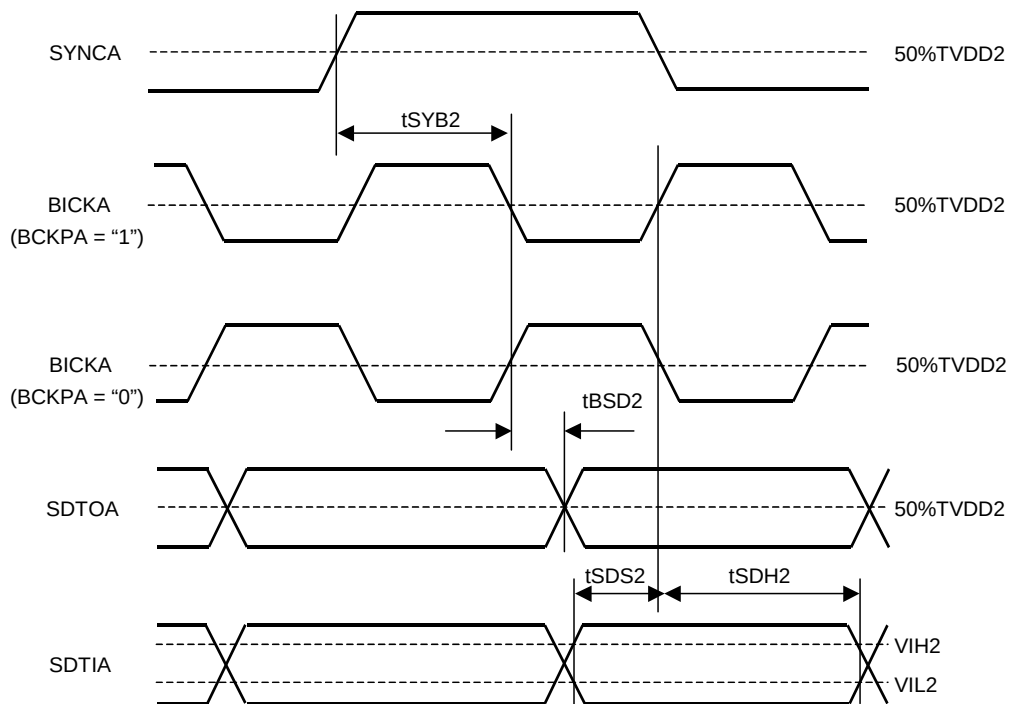


Figure 20. PCM I/F A Timing at short and long frame sync (Master mode; MSBSA = "1")

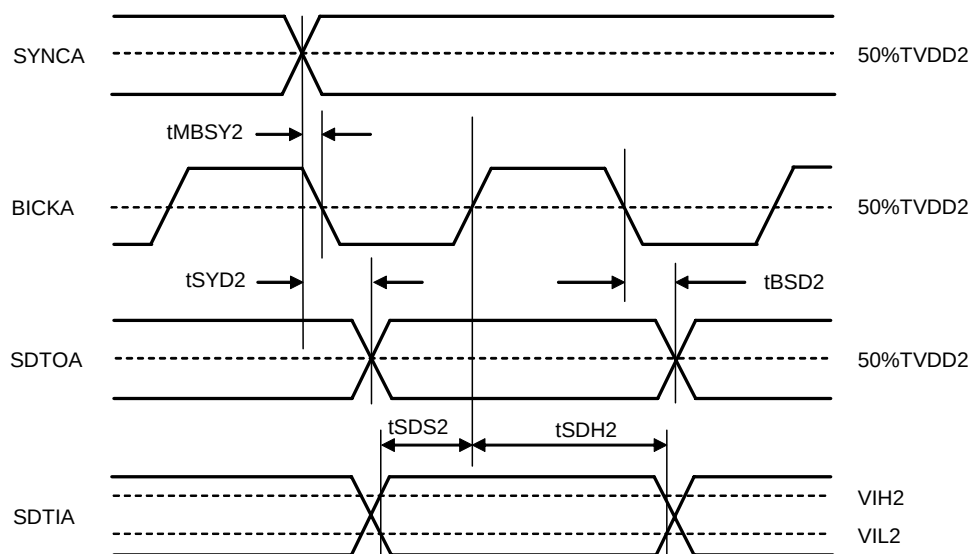
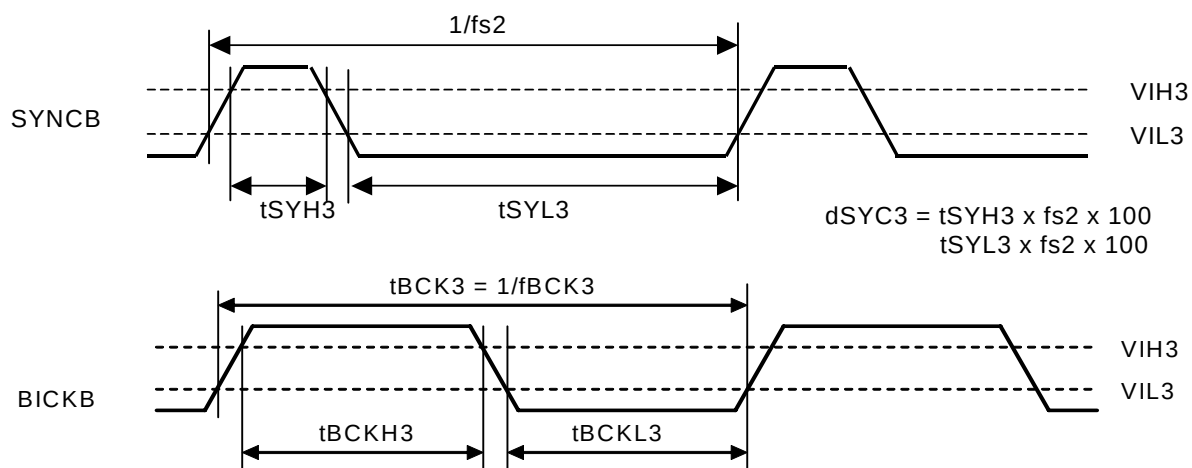
Figure 21. PCM I/F A Timing at MSB justified and I²S (Master mode)

Figure 22. Clock Timing of PCM I/F B (Slave mode)

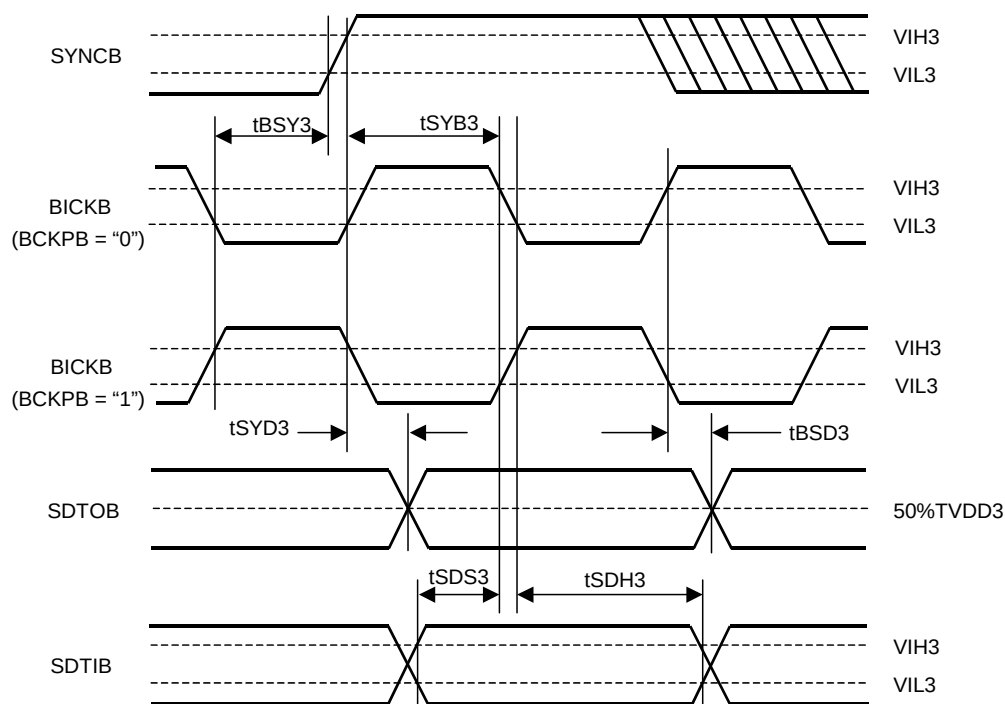


Figure 23. PCM I/F B Timing at short and long frame sync (Slave mode; MSBSB = "0")

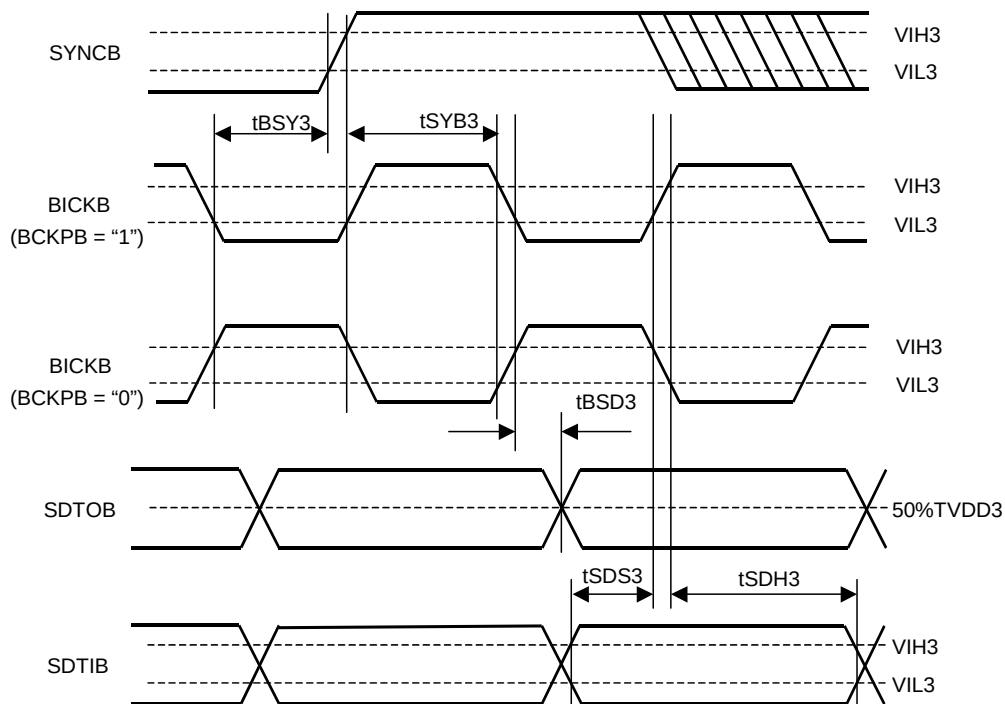


Figure 24. PCM I/F B Timing at short and long frame sync (Slave mode; MSBSB = "1")

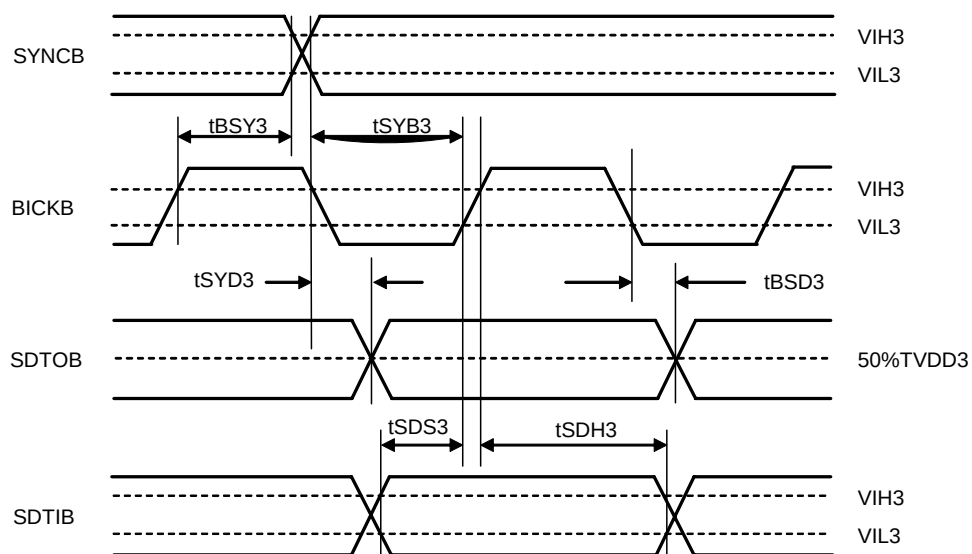
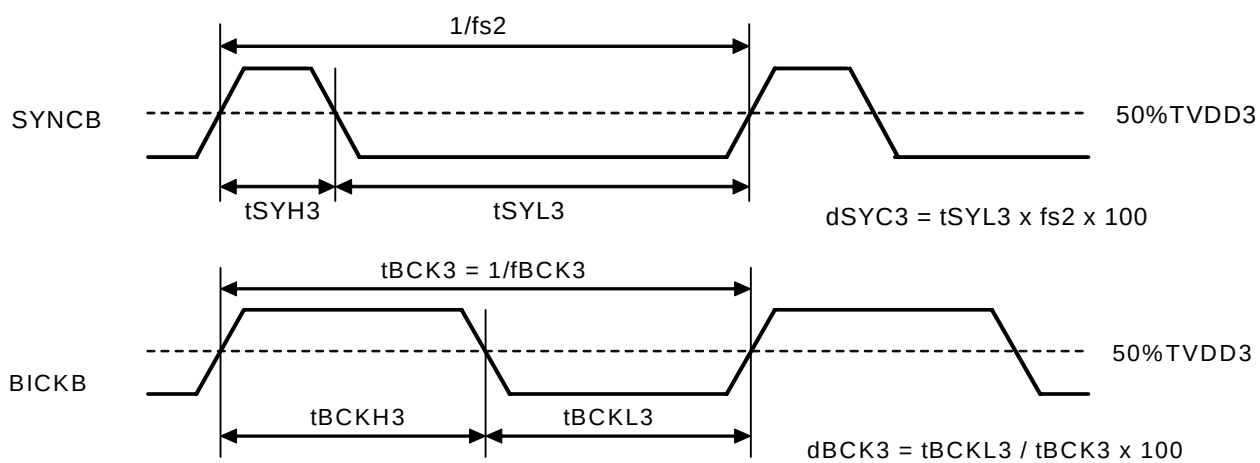
Figure 25. PCM I/F B Timing at MSB justified and I²S (Slave mode)

Figure 26. Clock Timing of PCM I/F B (Master mode)

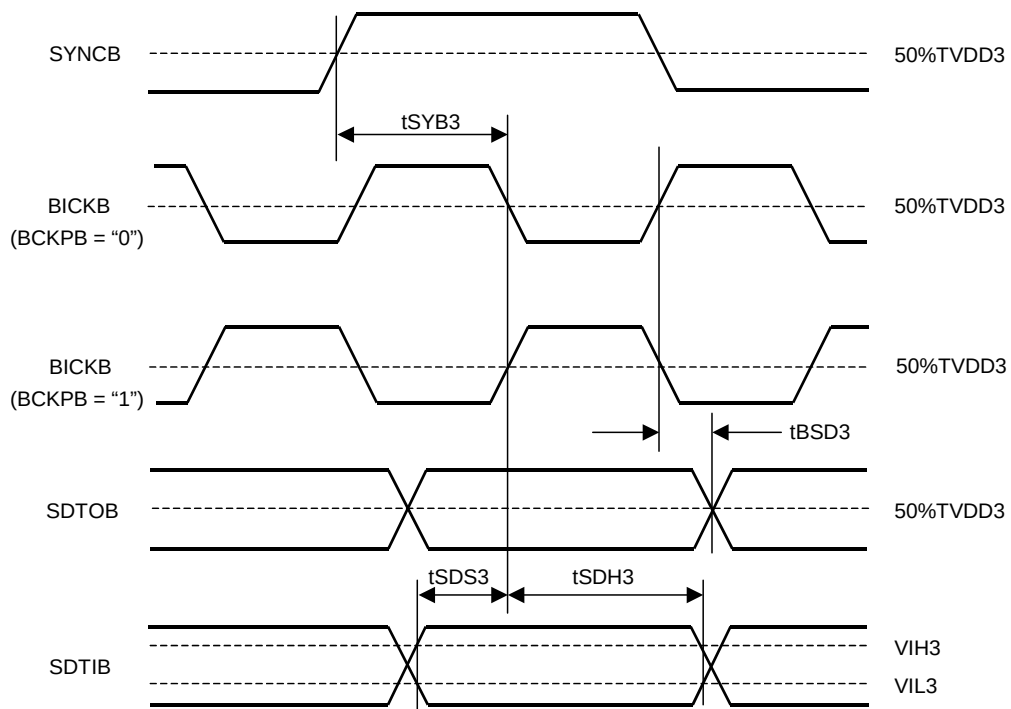


Figure 27. PCM I/F B Timing at short and long frame sync (Master mode; MSBSB = "0")

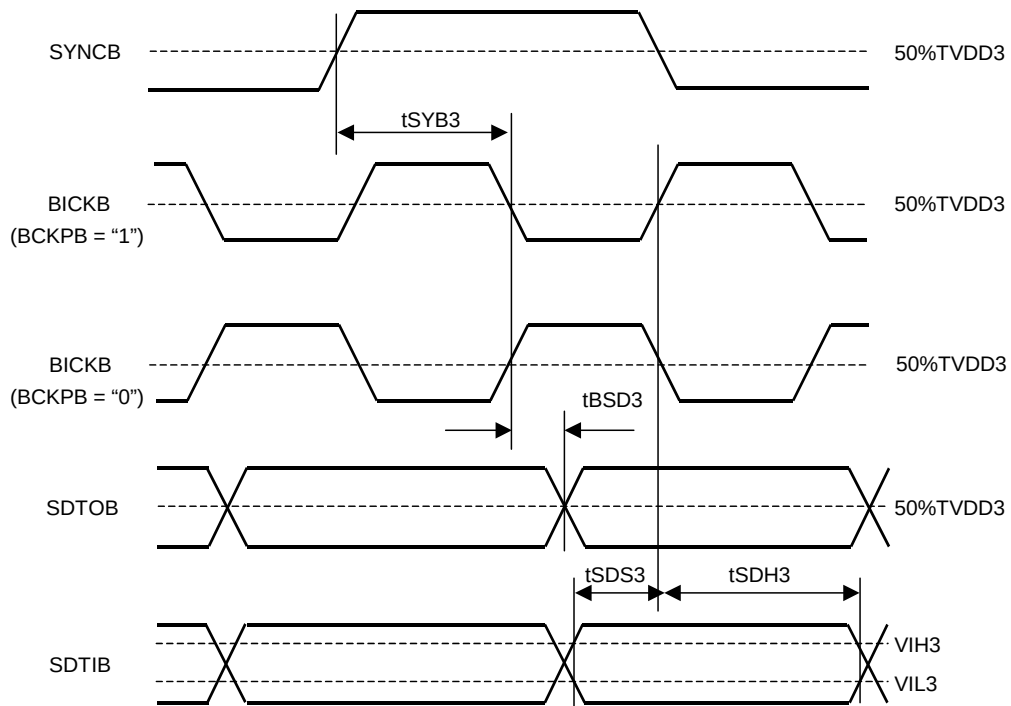


Figure 28. PCM I/F B Timing at short and long frame sync (Master mode; MSBSB = "1")

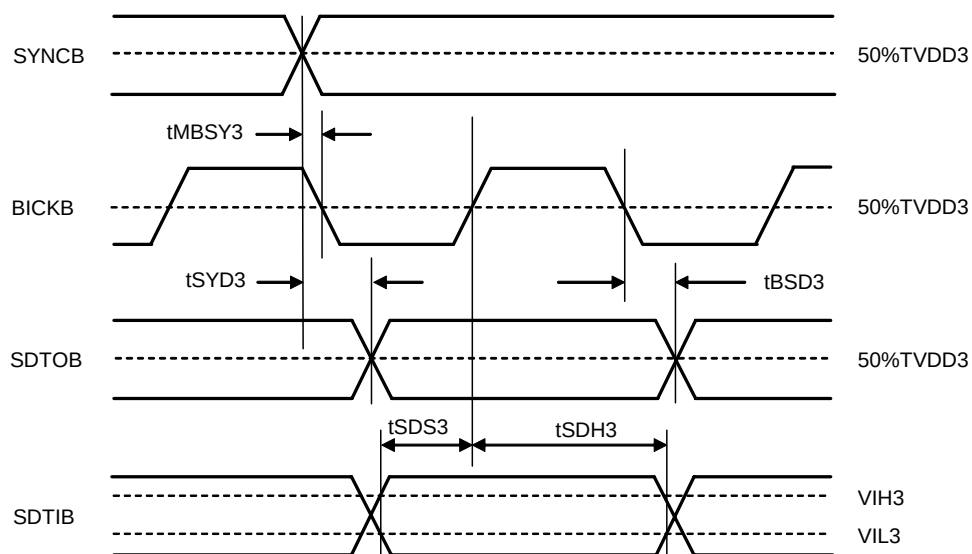
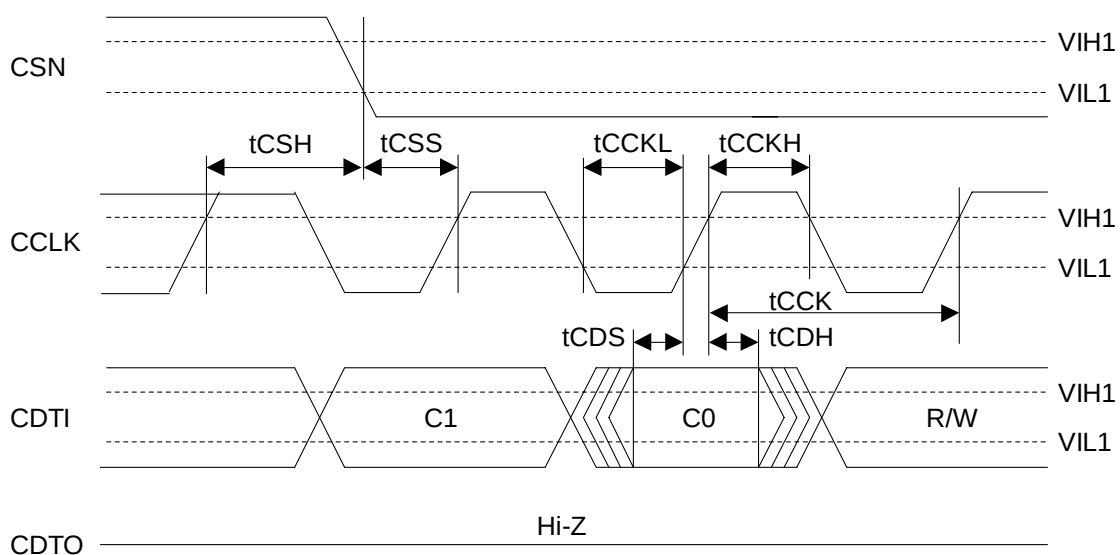
Figure 29. PCM I/F B Timing at MSB justified and I²S (Master mode)

Figure 30. WRITE Command Input Timing

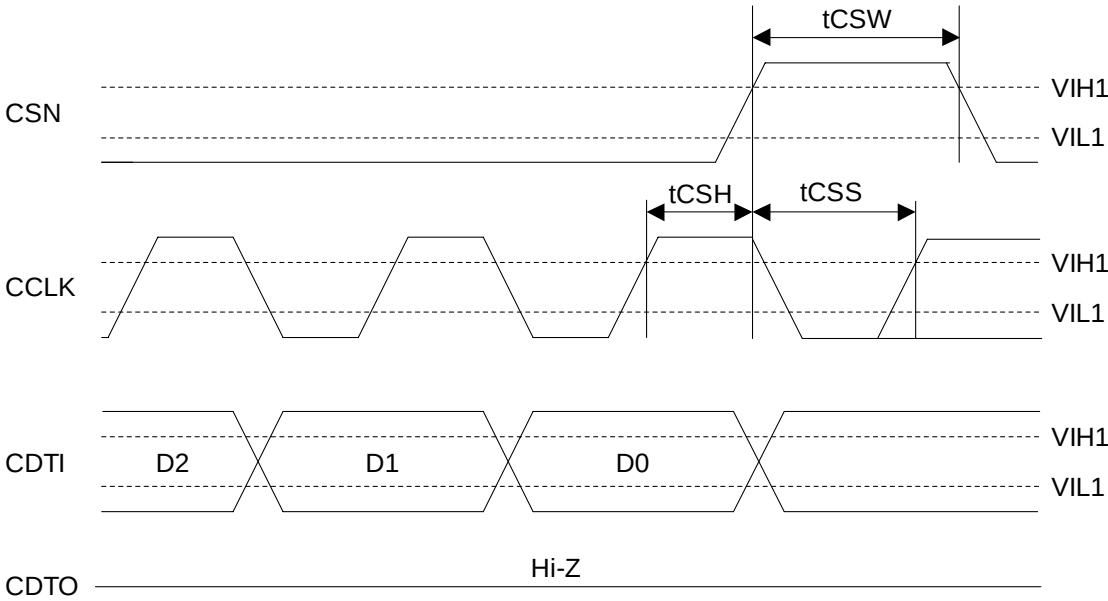


Figure 31. WRITE Data Input Timing

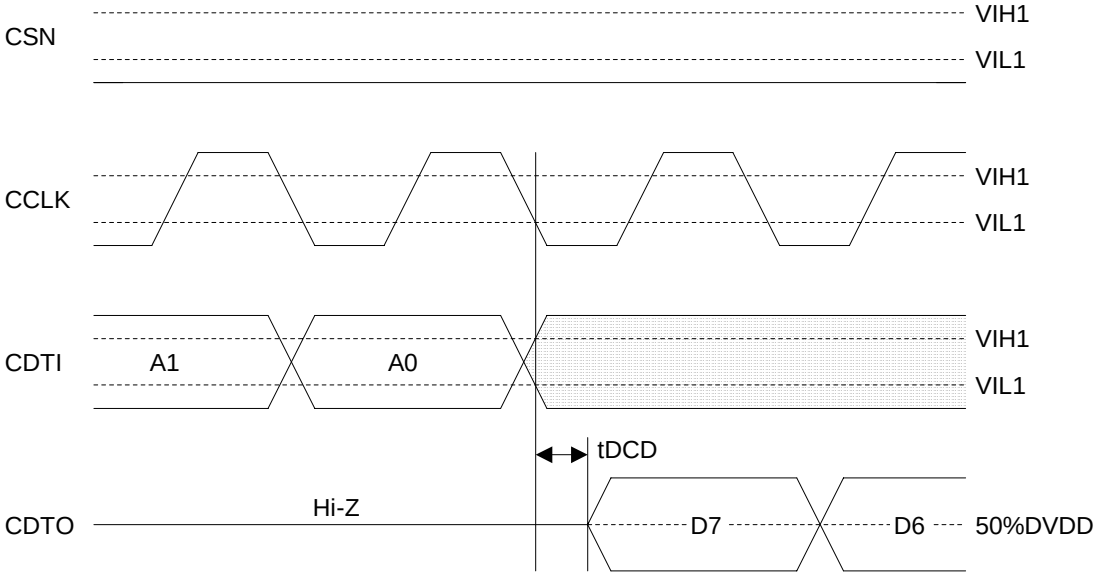


Figure 32. READ Data Output Timing 1

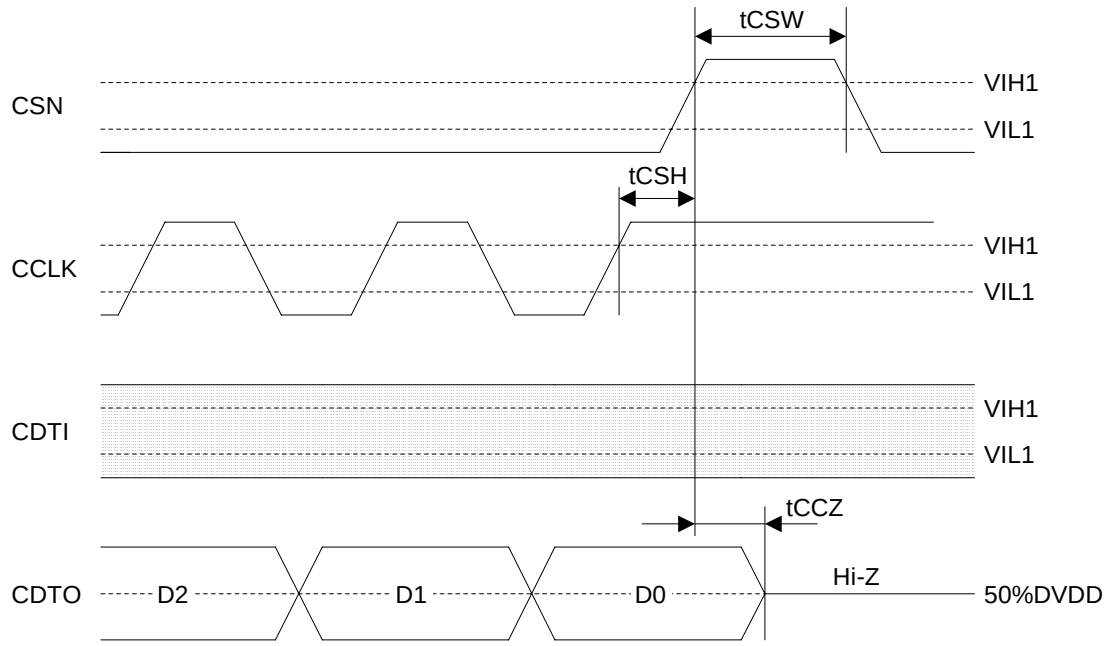


Figure 33. READ Data Output Timing 2

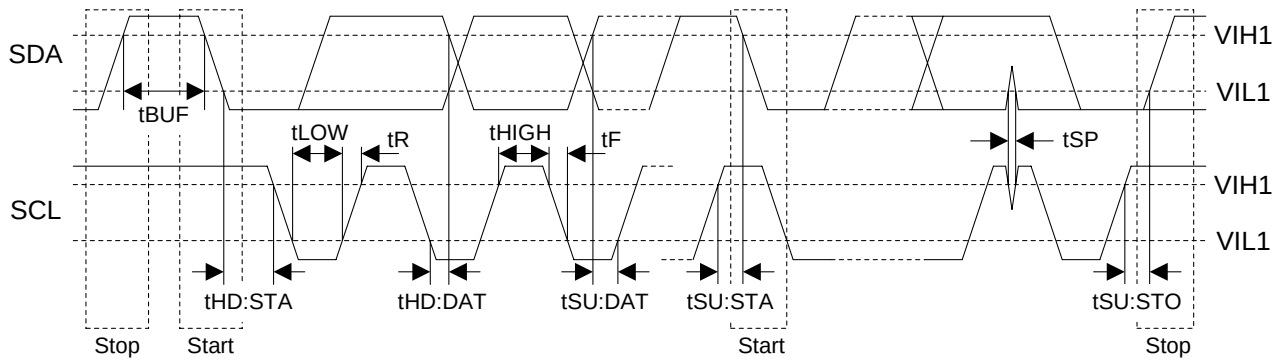


Figure 34. I²C Bus Mode Timing

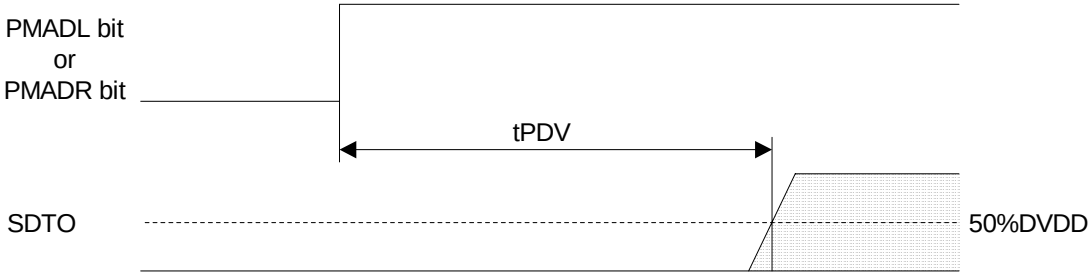


Figure 35. Power Down & Reset Timing 1

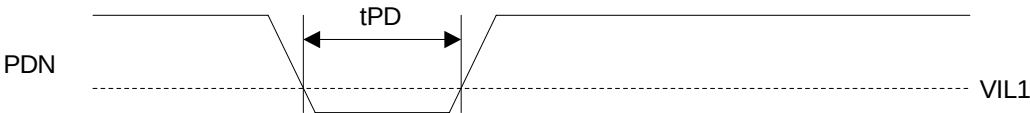


Figure 36. Power Down & Reset Timing 2

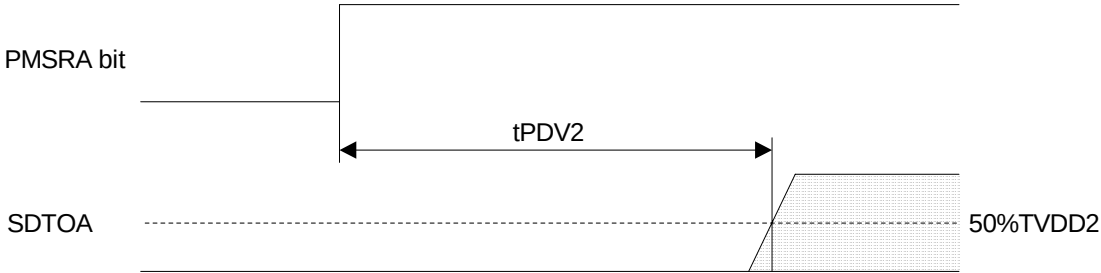


Figure 37. Power Down & Reset Timing 3

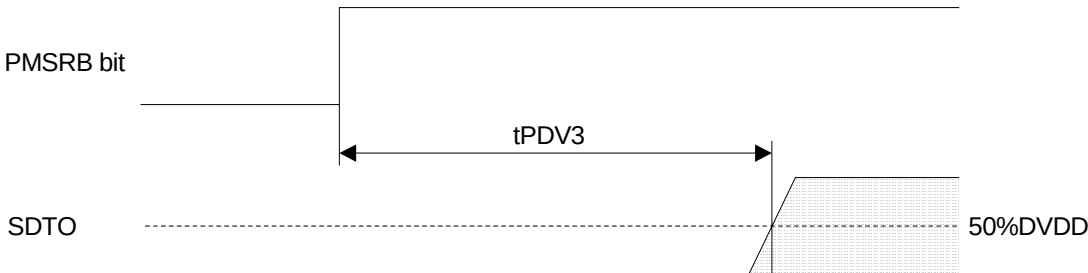


Figure 38. Power Down & Reset Timing 4

OPERATION OVERVIEW

■ System Clock (Audio I/F)

There are the following five clock modes to interface with external devices. (Table 1 and Table 2)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 60)	1	1	See Table 4	Figure 39
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 40
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	See Table 4	Figure 41 Figure 42
EXT Slave Mode	0	0	x	Figure 43
EXT Master Mode	0	1	x	Figure 44

Note 60. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	L	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS1-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4671 is power-down mode (PDN pin = "L") and exits reset state, the AK4671 is slave mode. After exiting reset state, the AK4671 goes to master mode by changing M/S bit = "1".

When the AK4671 is used by master mode, LRCK and BICK pins are a Hi-Z state until M/S bit becomes "1". LRCK and BICK pins of the AK4671 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode
0	Slave Mode
1	Master Mode

(default)

Table 3. Select Master/Slave Mode

■ PLL Mode (PMPLL bit = “1”)

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK4671 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or sampling frequency changes. When AIN3 bit = “1”, the PLL is not available.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)
							R[Ω]	C[F]	
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms
							10k	10n	4ms
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms
							10k	10n	4ms
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms
6	0	1	1	0	MCKI pin	12MHz	10k	10n	40ms
7	0	1	1	1	MCKI pin	24MHz	10k	10n	40ms
8	1	0	0	0	MCKI pin	19.2MHz	10k	4.7n	40ms
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms
14	1	1	1	0	MCKI pin	13MHz	10k	220n	60ms
15	1	1	1	1	MCKI pin	26MHz	10k	220n	60ms
Others	Others				N/A				

(default)

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency
0	0	0	0	0	8kHz
1	0	0	0	1	12kHz
2	0	0	1	0	16kHz
3	0	0	1	1	24kHz
5	0	1	0	1	11.025kHz
7	0	1	1	1	22.05kHz
10	1	0	1	0	32kHz
11	1	0	1	1	48kHz
15	1	1	1	1	44.1kHz
Others	Others				N/A

(default)

(N/A: Not available)

Table 5. Setting of Sampling Frequency at PMPLL bit = “1” (Reference Clock = MCKI pin)

When PLL reference clock input is LRCK or BICK pin, the sampling frequency is selected by FS3-2 bits (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range
0	0	0	x	x	$8\text{kHz} \leq f_s \leq 12\text{kHz}$
1	0	1	x	x	$12\text{kHz} < f_s \leq 24\text{kHz}$
2	1	x	x	x	$24\text{kHz} < f_s \leq 48\text{kHz}$
Others	Others				N/A

(default)

(x: Don't care, N/A: Not available)

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" (Reference Clock = LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin changes to "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of $1/f_s$.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 9	See Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL and DACH bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

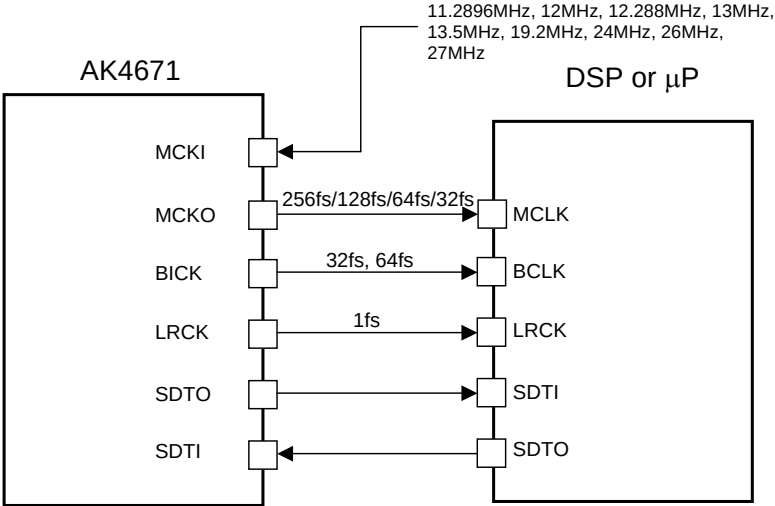


Figure 39. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = “1”)

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock to the AK4671 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK does not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

In case that the CODEC is used without Audio I/F (like phone call), the CODEC can be operated by MCKI only. In this case, BICK and LRCK can be stopped.

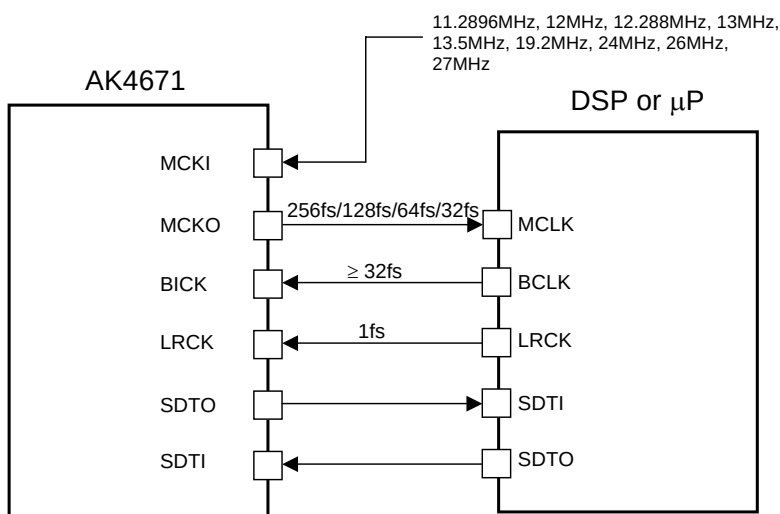


Figure 40. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 8kHz to 48kHz by changing FS3-0 bits (Table 6).

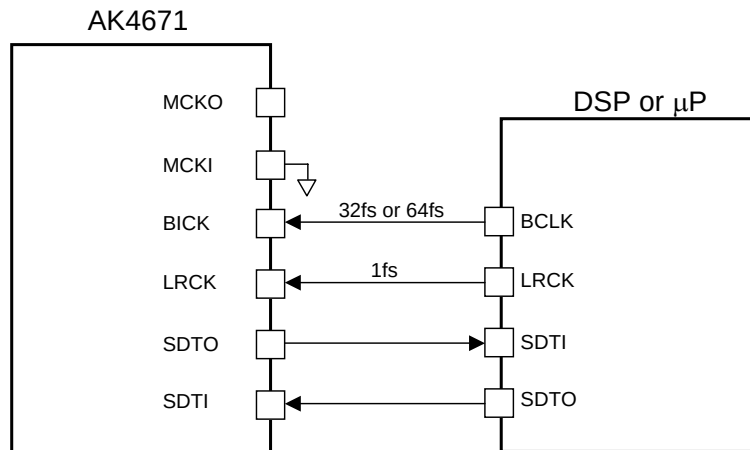


Figure 41. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

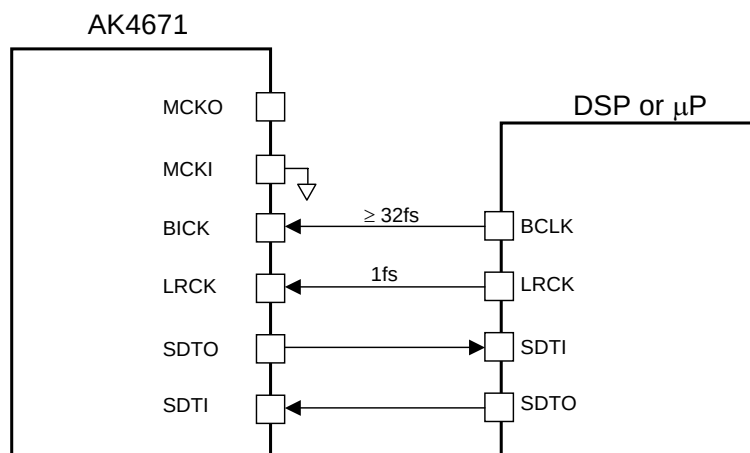


Figure 42. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1”, PMDAL bit = “1” or PMDAR bit = “1”). If MCKI is not provided, the AK4671 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = “0”).

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4671 becomes EXT mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate the AK4671 are MCKI (256fs, 384fs, 512fs, 768fs or 1024fs), LRCK (fs) and BICK (≥ 32 fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS2-0 bits (Table 11).

In case that the CODEC is used without Audio I/F (like phone call), the CODEC can be operated by MCKI only. In this case, BICK and LRCK can be stopped.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range
0	x	0	0	0	256fs	8kHz ~ 48kHz
1	x	0	0	1	1024fs	8kHz ~ 13kHz
4	x	1	0	0	384fs	8kHz ~ 48kHz
5	x	1	0	1	768fs	8kHz ~ 26kHz
6	x	1	1	0	512fs	8kHz ~ 26kHz
7	x	1	1	1	256fs	8kHz ~ 48kHz
Others	Others				N/A	N/A

(default)

(x: Don't care, N/A: Not available)

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs, 384fs	83dB
512fs, 768fs	93dB
1024fs	93dB

Table 12. Relationship between MCKI and S/N of LOUT1/ROUT1 pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1”, PMDAL bit = “1” or PMDAR bit = “1”). If MCKI is not provided, the AK4671 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = “0”).

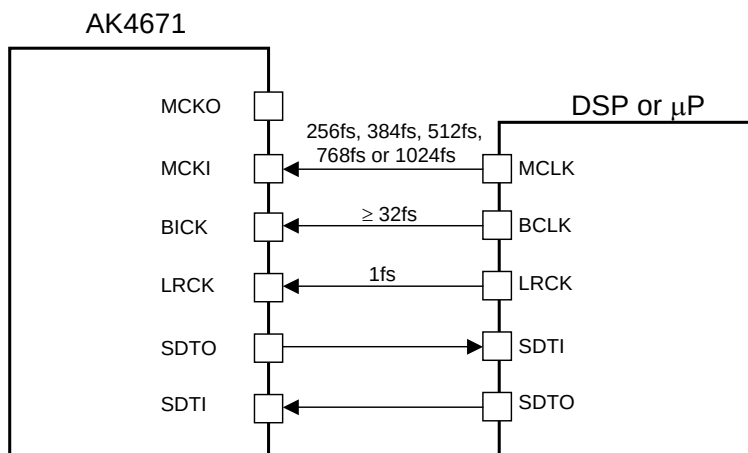


Figure 43. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4671 becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 384fs, 512fs, 768fs or 1024fs). The input frequency of MCKI is selected by FS2-0 bits (Table 13).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range
0	x	0	0	0	256fs	8kHz ~ 48kHz
1	x	0	0	1	1024fs	8kHz ~ 13kHz
4	x	1	0	0	384fs	8kHz ~ 48kHz
5	x	1	0	1	768fs	8kHz ~ 26kHz
6	x	1	1	0	512fs	8kHz ~ 26kHz
7	x	1	1	1	256fs	8kHz ~ 48kHz
Others	Others				N/A	N/A

(default)

(x: Don't care, N/A: Not available)

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs, 384fs	83dB
512fs, 768fs	93dB
1024fs	93dB

Table 14. Relationship between MCKI and S/N of LOUT1/ROUT1 pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1”, PMDAL bit = “1” or PMDAR bit = “1”). If MCKI is not provided, the AK4671 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAL=PMDAR bits = “0”).

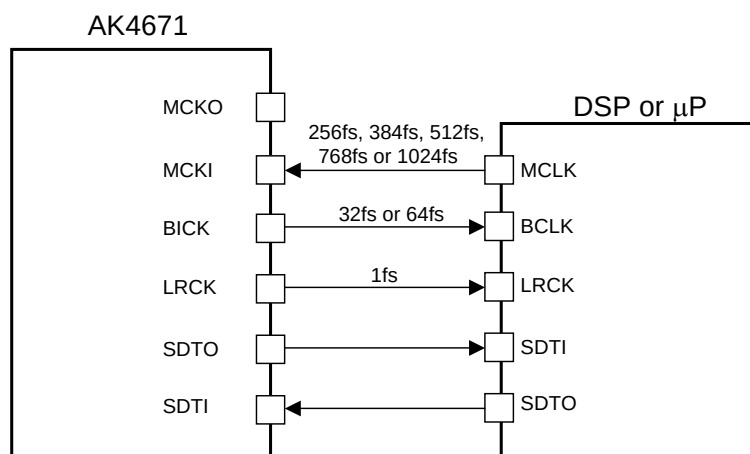


Figure 44. EXT Master Mode

BCKO bit	BICK Output Frequency
0	32fs
1	64fs

(default)

Table 15. BICK Output Frequency at Master Mode

■ System Reset

When power-up, the AK4671 should be reset by bringing the PDN pin = “L”. This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADL or PMADR bit is changed from “0” to “1” at PMDAL and PMDAR bits are “0”. The initialization cycle time is $1059/f_s = 24\text{ms}@f_s = 44.1\text{kHz}$. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2’s complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When PMDAL or PMDAR is “1”, the ADC does not require an initialization cycle.

■ Audio Interface Format

Four types of data formats are available and can be selected by setting the DIF1-0 bits (Table 16). In all modes, the serial data is MSB first, 2’s complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4671 in master mode, but must be input to the AK4671 in slave mode.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure
0	0	0	DSP Mode	DSP Mode	$\geq 32f_s$	Table 17
1	0	1	MSB justified	LSB justified	$\geq 32f_s$	Figure 49
2	1	0	MSB justified	MSB justified	$\geq 32f_s$	Figure 50
3	1	1	I ² S compatible	I ² S compatible	$\geq 32f_s$	Figure 51

(default)

Table 16. Audio Interface Format

In modes 1, 2 and 3, the SDTO is clocked out on the falling edge (“↓”) of BICK and the SDTI is latched on the rising edge (“↑”).

In Modes 0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 17).

DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure
0	0	0	0	MSB of SDTO is output by the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO’s MSB.	Figure 45
		0	1	MSB of SDTO is output by the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO’s MSB.	Figure 46
		1	0	MSB of SDTO is output by next rising edge (“↑”) of the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO’s MSB.	Figure 47
		1	1	MSB of SDTO is output by next falling edge (“↓”) of the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO’s MSB.	Figure 48

(default)

Table 17. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, “-1” at 16bit data is converted to “-1” at 8-bit data. And when the DAC playbacks this 8-bit data, “-1” at 8-bit data will be converted to “-256” at 16-bit data and this is a large offset. This offset can be removed by adding the offset of “128” to 16-bit data before converting to 8-bit data.

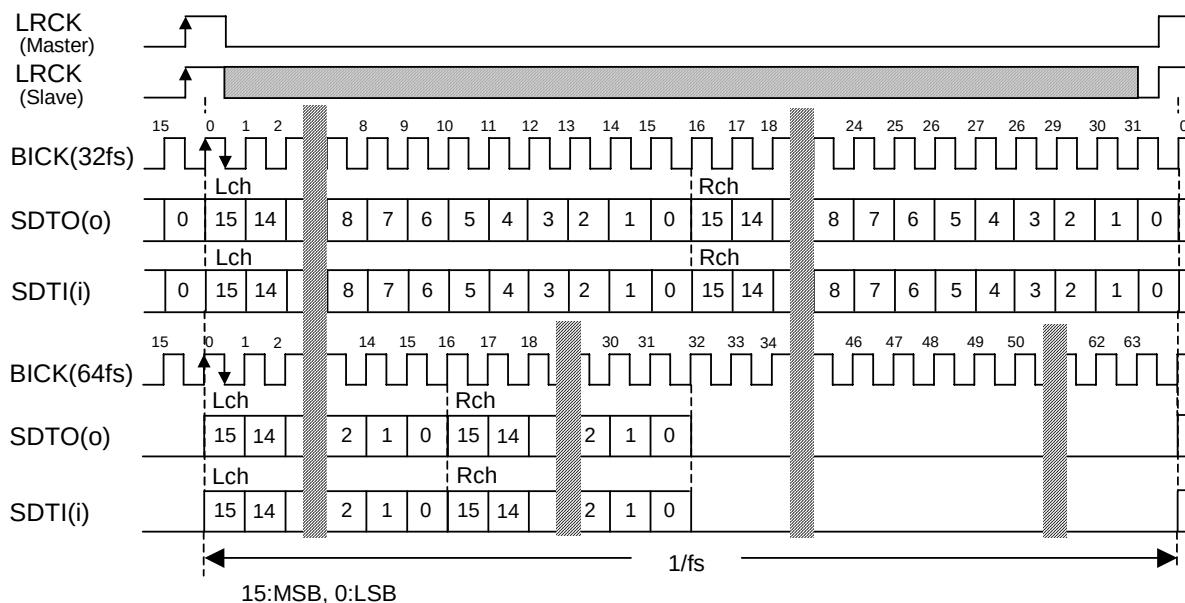


Figure 45. Mode 0 Timing (BCKP = "0", MSBS = "0")

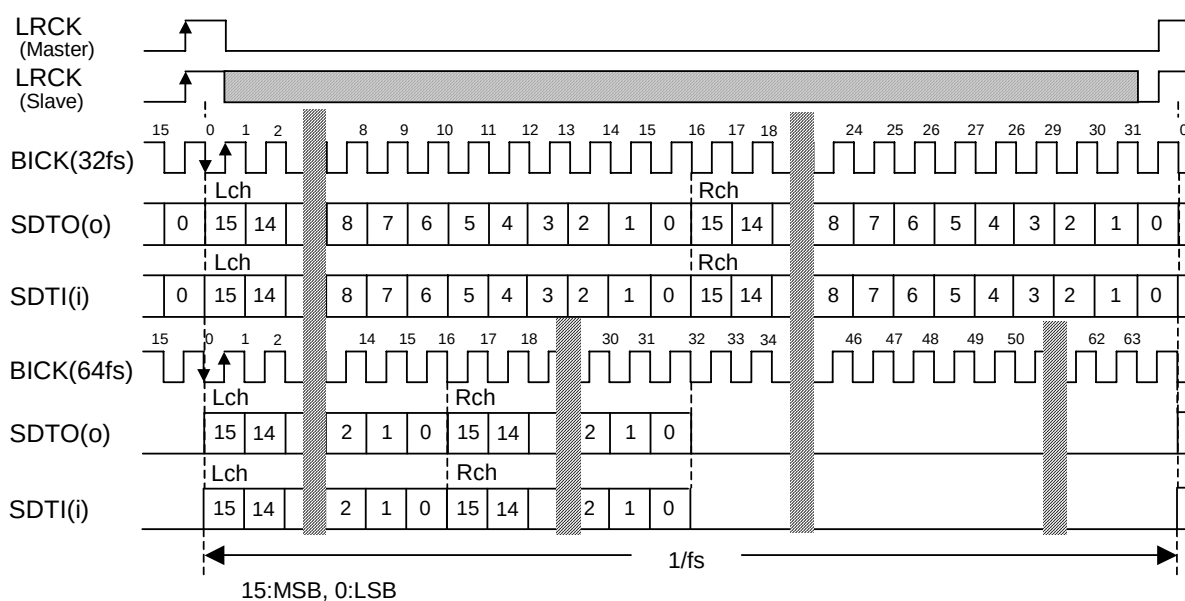


Figure 46. Mode 0 Timing (BCKP = "1", MSBS = "0")

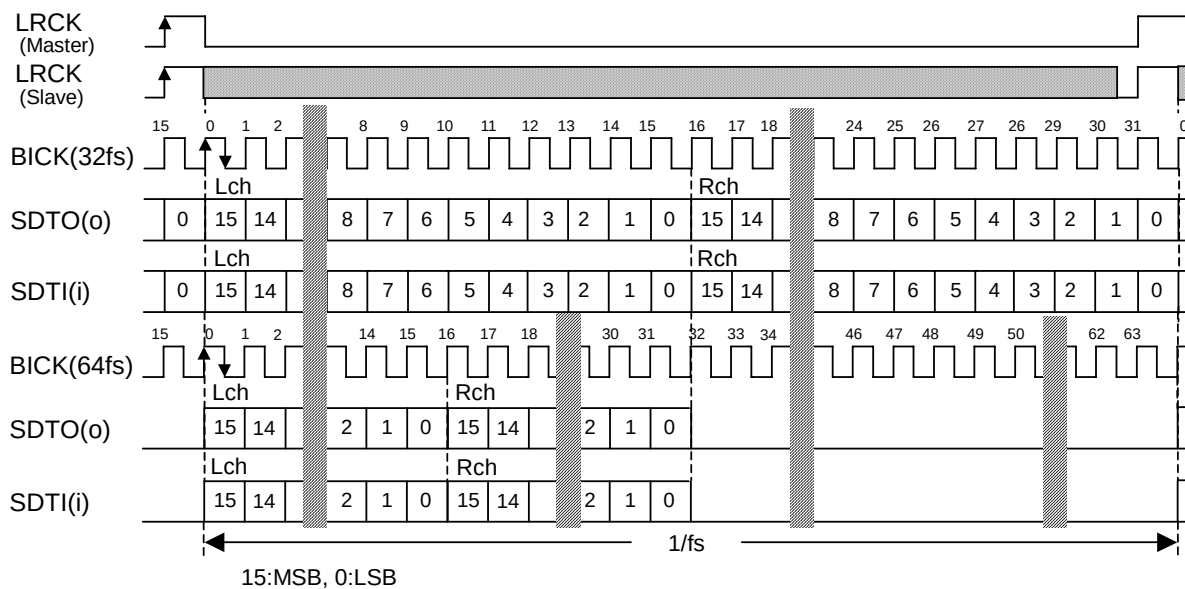


Figure 47. Mode 0 Timing (BCKP = "0", MSBS = "1")

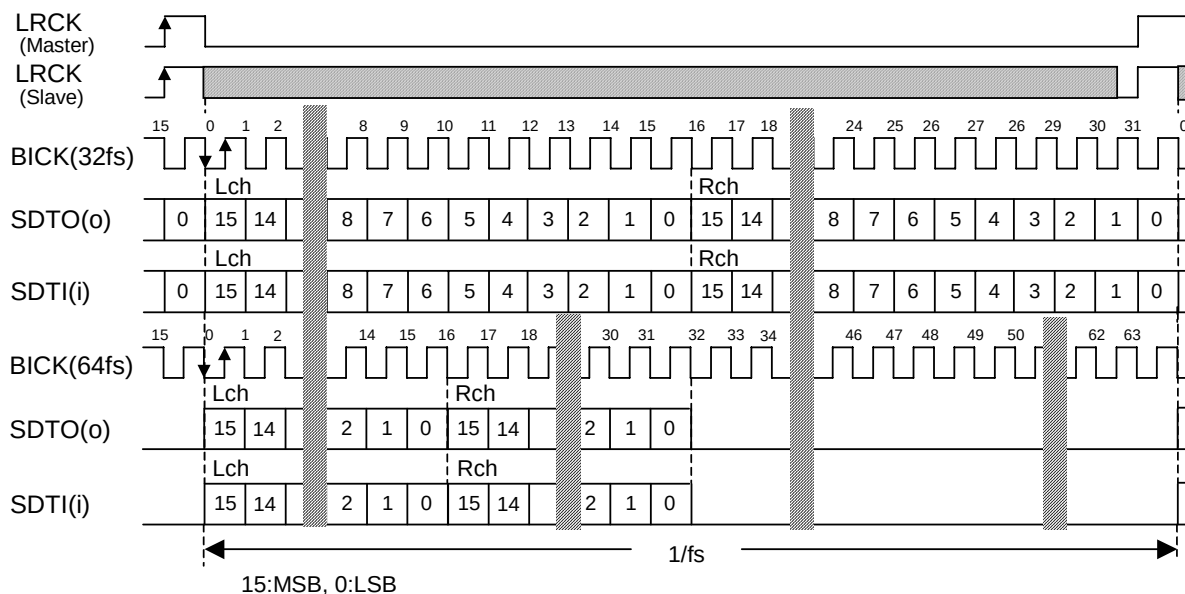


Figure 48. Mode 0 Timing (BCKP = "1", MSBS = "1")

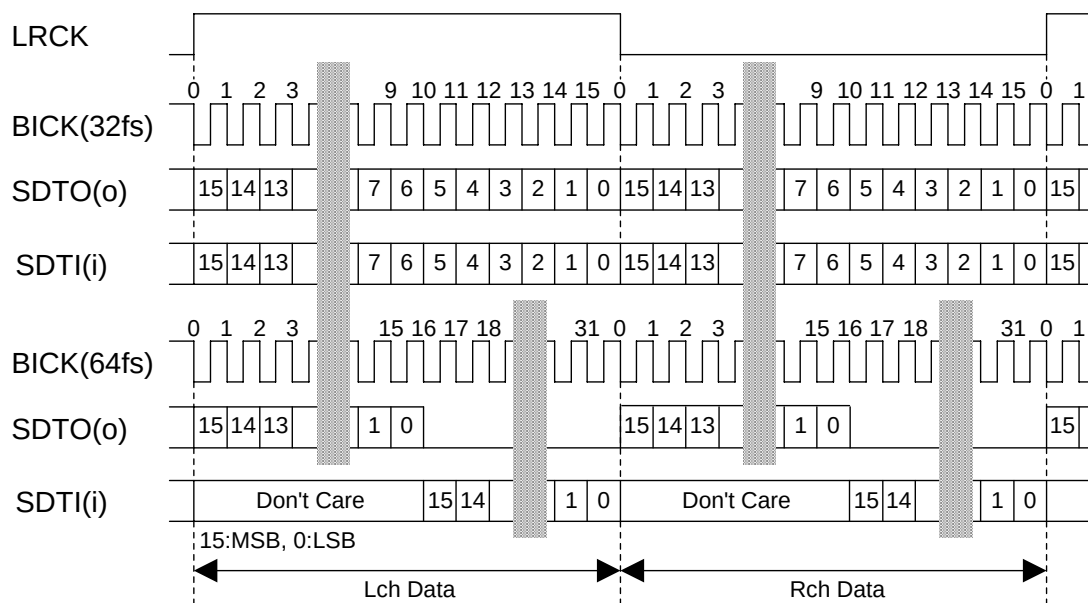


Figure 49. Mode 1 Timing

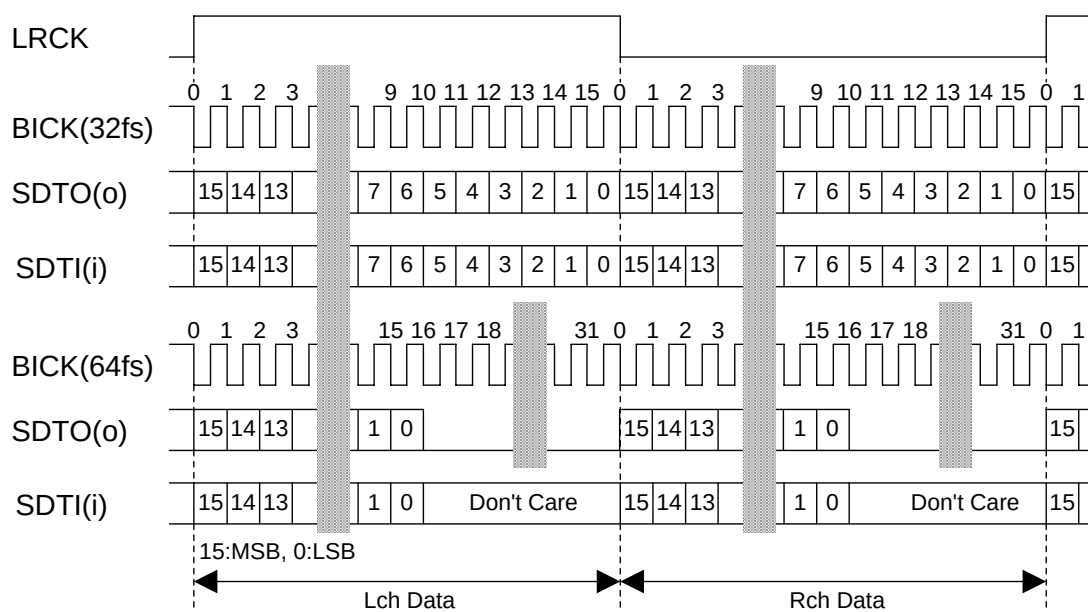


Figure 50. Mode 2 Timing

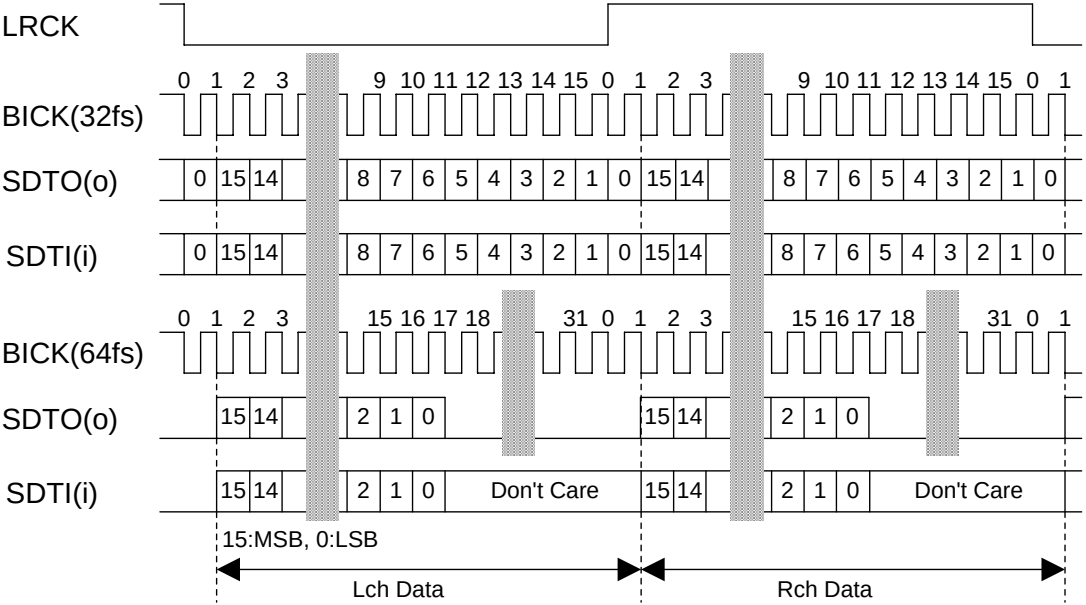


Figure 51. Mode 3 Timing

■ MIC/LINE Input Selector

The AK4671 has input selector. When MDIF1, MDIF2, MDIF3 and MDIF4 bits are “0”, INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3/LIN4 and RIN1/RIN2/RIN3/RIN4, respectively. When MDIF1, MDIF2, MDIF3 and MDIF4 bits are “1”, LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 pins become IN1+/-, IN2+/-, IN3+/- and IN4+/- pins, respectively. In this case, full-differential input is available ([Figure 53](#)).

MDIF1	MDIF2	MDIF3	MDIF4	INL1	INL0	INR1	INR0	Lch	Rch	(default)
0	0	0	0	0	0	0	0	LIN1	RIN1	
0	0	0	0	0	0	0	1	LIN1	RIN2	
0	0	0	0	0	0	1	0	LIN1	RIN3	
0	0	0	0	0	0	1	1	LIN1	RIN4	
0	0	0	0	0	1	0	0	LIN2	RIN1	
0	0	0	0	0	1	0	1	LIN2	RIN2	
0	0	0	0	0	1	1	0	LIN2	RIN3	
0	0	0	0	0	1	1	1	LIN2	RIN4	
0	0	0	0	1	0	0	0	LIN3	RIN1	
0	0	0	0	1	0	0	1	LIN3	RIN2	
0	0	0	0	1	0	1	0	LIN3	RIN3	
0	0	0	0	1	0	1	1	LIN3	RIN4	
0	0	0	0	1	1	0	0	LIN4	RIN1	
0	0	0	0	1	1	0	1	LIN4	RIN2	
0	0	0	0	1	1	1	0	LIN4	RIN3	
0	0	0	0	1	1	1	1	LIN4	RIN4	
0	0	0	1	0	0	1	1	LIN1	IN4+/-	
0	0	0	1	0	1	1	1	LIN2	IN4+/-	
0	0	0	1	1	0	1	1	LIN3	IN4+/-	
0	0	1	0	1	0	0	0	IN3+/-	RIN1	
0	0	1	0	1	0	0	1	IN3+/-	RIN2	
0	0	1	0	1	0	1	1	IN3+/-	RIN4	
0	0	1	1	1	0	1	1	IN3+/-	IN4+/-	
0	1	0	0	0	0	0	1	LIN1	IN2+/-	
0	1	0	0	1	0	0	1	LIN3	IN2+/-	
0	1	0	0	1	1	0	1	LIN4	IN2+/-	
0	1	1	0	1	0	0	1	IN3+/-	IN2+/-	
1	0	0	0	0	0	0	1	IN1+/-	RIN2	
1	0	0	0	0	0	1	0	IN1+/-	RIN3	
1	0	0	0	0	0	1	1	IN1+/-	RIN4	
1	0	0	1	0	0	1	1	IN1+/-	IN4+/-	
1	1	0	0	0	0	0	1	IN1+/-	IN2+/-	
Others								N/A		

Table 18. MIC-Amp Input Signal (N/A: Not available)

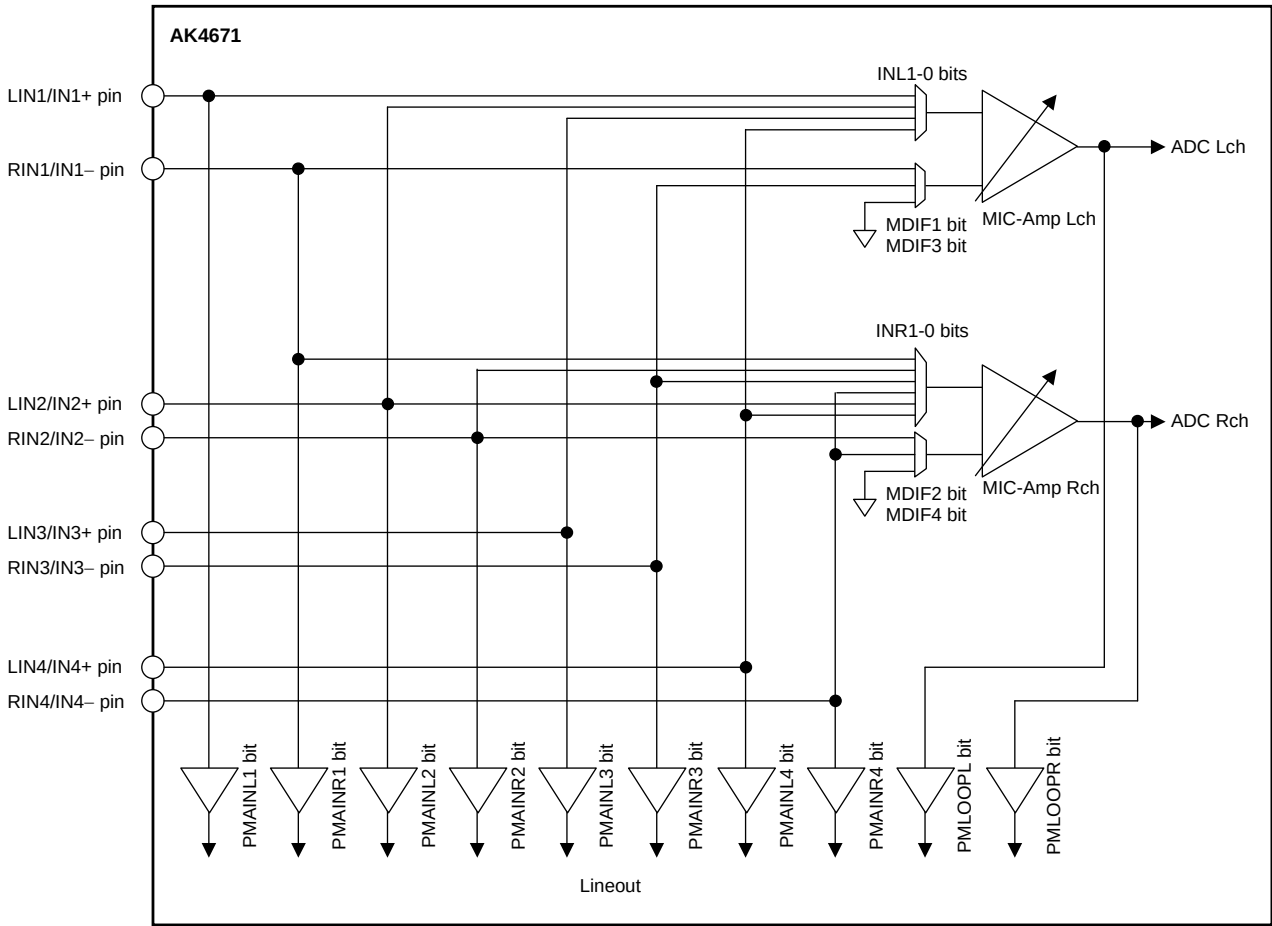


Figure 52. Mic/Line Input Selector

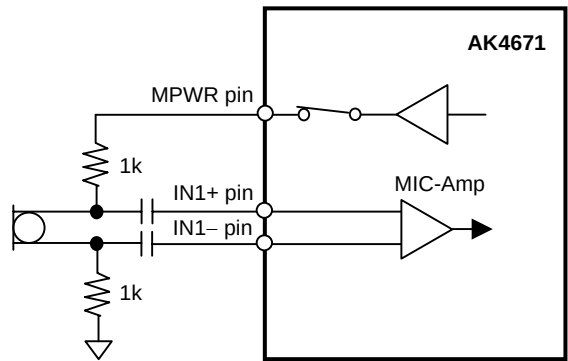


Figure 53. Connection Example for Full-differential Mic Input (MDIF1/2/3/4 bits = "1")

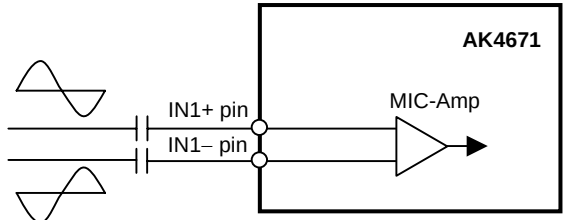


Figure 54. Connection Example for Full-differential Mic Input (MDIF1/2/3/4 bits = "1")

■ MIC Gain Amplifier

The AK4671 has a gain amplifier for microphone input. The gain of MIC-Amp Lch and Rch is independently selected by the MGNL3-0 and MGNR3-0 bits (Table 19). The typical input impedance is $42\text{k}\Omega(\text{typ})$ @MGNL/R0 bits = “0” or $30\text{k}\Omega(\text{typ})$ @MGNL/R0 bits = “1”.

Mode	MGNL3 MGNR3	MGNL2 MGNR2	MGNL1 MGNR1	MGNL0 MGNR0	Input Gain	Input Resistance
0	0	0	0	0	N/A	N/A
1	0	0	0	1	-12dB	30k Ω
2	0	0	1	0	-9dB	42k Ω
3	0	0	1	1	-6dB	30k Ω
4	0	1	0	0	-3dB	42k Ω
5	0	1	0	1	0dB	30k Ω
6	0	1	1	0	+3dB	42k Ω
7	0	1	1	1	+6dB	30k Ω
8	1	0	0	0	+9dB	42k Ω
9	1	0	0	1	+12dB	30k Ω
10	1	0	1	0	+15dB	42k Ω
11	1	0	1	1	+18dB	30k Ω
12	1	1	0	0	+21dB	42k Ω
13	1	1	0	1	+24dB	30k Ω
14	1	1	1	0	+27dB	42k Ω
15	1	1	1	1	+30dB	30k Ω

(default)

Table 19. Mic Input Gain (N/A: Not available)

■ MIC Power

When PMMP bit = “1”, the MPWR pin supplies power for the microphone. This output voltage is typically $0.8 \times AVDD$ and the load resistance is minimum $0.5k\Omega$. In case of using two sets of stereo mic, the load resistance is minimum $2k\Omega$ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 55).

PMMP bit	MPWR pin
0	Hi-Z
1	Output

(default)

Table 20. MIC Power

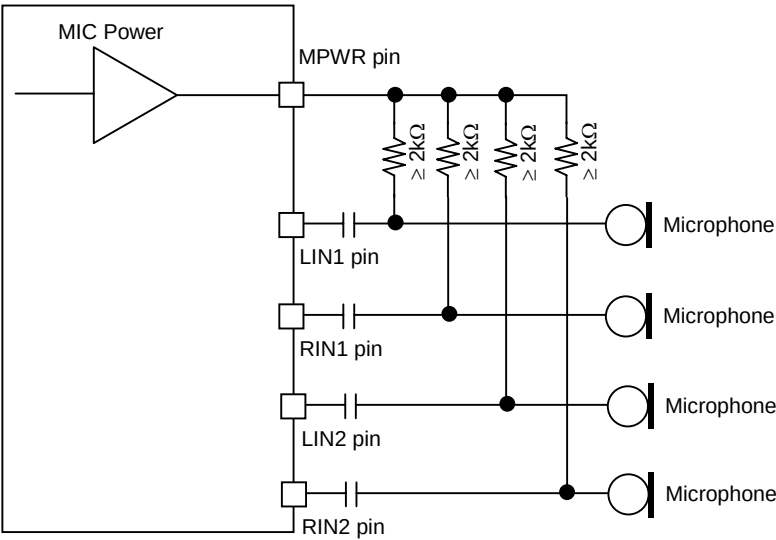


Figure 55. MIC Block Circuit

■ MIC Detection

The AK4671 has the detecting function of microphone. The external circuit is showed in Figure 56.

The followings show the example of external microphone detection sequence:

- (1) PMMP bit should be set to “1” after CPU detects the jack insertion of microphone or headphone.
- (2) The MPWR pin drives external microphone.
- (3) The GPO2 pin (at GPOM2 bit = “1”) and DTMIC bit are set as Table 21. In case of Headset (with Mic), the input voltage of MDT pin is higher than $0.075 \times AVDD$ because of the relationship between the bias resistance at the MPWR pin (typ. $2.2k\Omega$) and the microphone impedance. In case of Headphone (No Mic), the input voltage of MDT pin is 0V because the pin of headphone jack connected to the MDT pin is assigned as ground.

Input Level of MDT pin	GPO2 pin	DTMIC bit	Result
$\geq 0.075 \times AVDD$	H	1	Mic (Headset)
$< 0.050 \times AVDD$	L	0	No Mic (Headphone)

Table 21. Microphone Detection Result

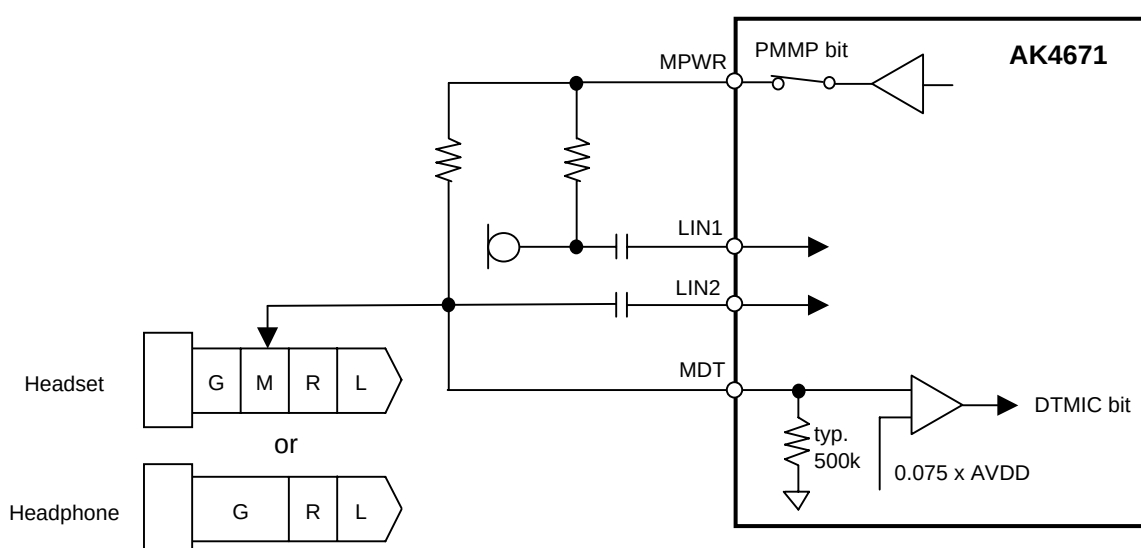


Figure 56. Microphone Power Supply and Mic Detection

■ Digital Block

Digital block is composed as Figure 57. Each block can be powered-down by power management bits (PMADL, PMADR, PMDAL, PMDAR, PMSRA, PMSRB and PMPCM bits). When blocks from HPF to MIX are powered-down, both MIX and SVOLA blocks should not be selected by SDOL/R bits and PFMXL/R bits.

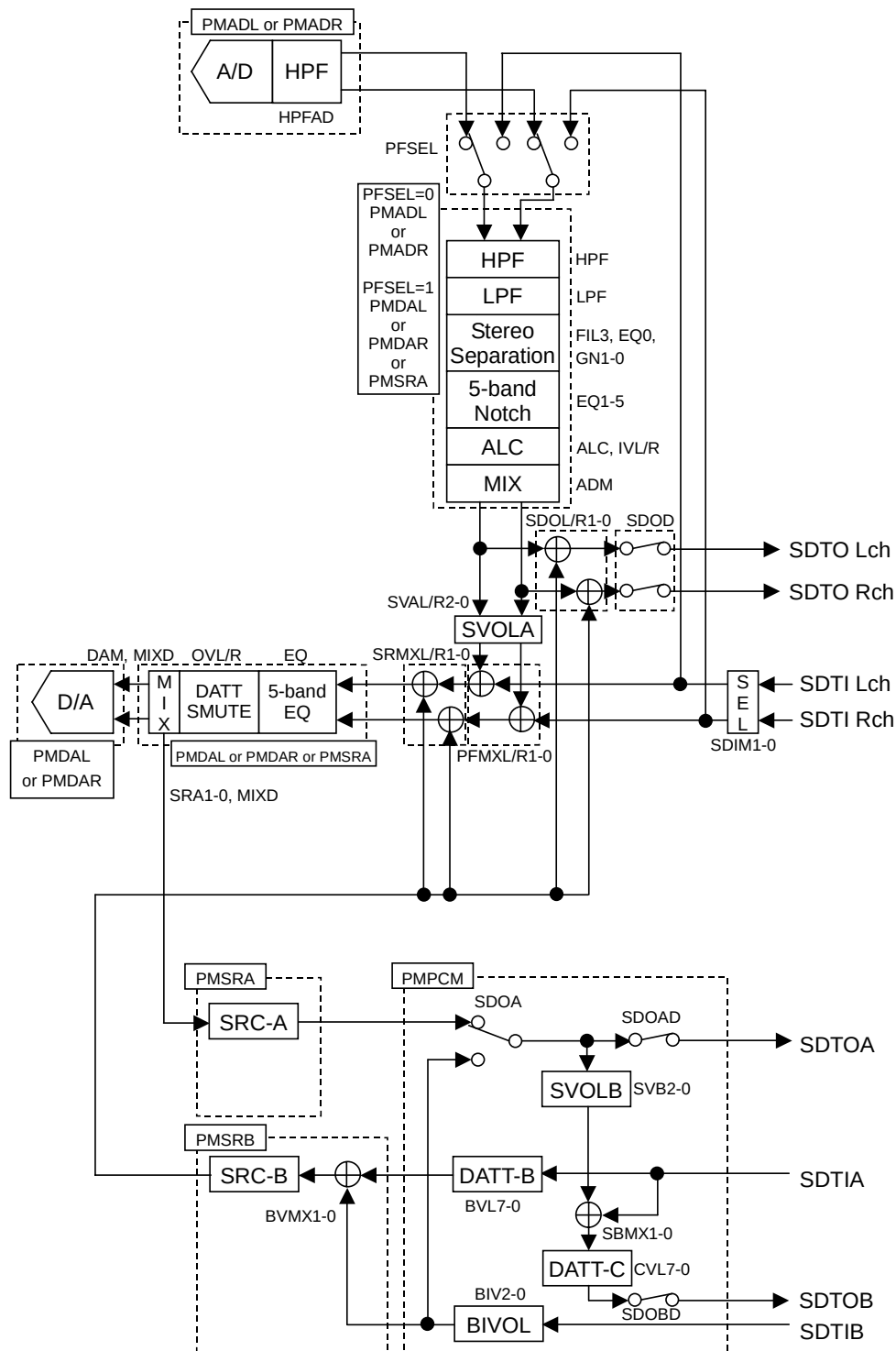


Figure 57. Path Select of Digital Block

1. ADC: Include the Digital Filter (LPF) for ADC as shown in “[FILTER CHARACTERISTICS](#)”.
2. DAC: Include the Digital Filter (LPF) for DAC as shown in “[FILTER CHARACTERISTICS](#)”.
3. HPF: High Pass Filter. Applicable to use as Wind-Noise Reduction Filter. (See “[Digital Programmable Filter](#)”.)
4. LPF: Low Pass Filter (See “[Digital Programmable Filter](#)”.)
5. Stereo Separation: Stereo Separation Emphasis Filter & Gain Compensation. (See “[Digital Programmable Filter](#)”.)
Gain Compensation is composed with EQ0 and Gain blocks. This block adjusts the frequency response after Stereo Separation Emphasis.
6. 5-Band Notch: Applicable to use as Equalizer or Notch Filter. (See “[Digital Programmable Filter](#)”.)
7. ALC: Input Digital Volume with ALC function. (See “[Input Digital Volume](#)” and “[ALC Operation](#)”.)
8. SVOLA: Side Tone Volume at Internal MIC/SPK or External Headset Phone Call. (See “[Side Tone Volume](#)”.)
9. 5-Band EQ: Equalizer for playback path. (See “[5-band Equalizer](#)”.)
10. DATT: Digital Volume for playback path. (See “[Digital Output Volume](#)”.)
11. SMUTE: Soft mute. (See “[Soft Mute](#)”.)
12. DATT-B: Digital Volume for Recording of Received Voice. (See “[Digital Volume for Recording of Received Voice](#)”.)
13. DATT-C: Digital Volume of Received Voice. (See “[Digital Volume for Received Voice](#)”.)
14. SVOLA: Side Tone Volume at B/T Headset Phone Call. (See “[Side Tone Volume for B/T Phone Call](#)”.)

Mode	PMADL	PMADR	PMDAL	PMDAR	PFSEL	Figure
Recording Mode	1	1	0	0	0	Figure 58
	1	0	0	0	0	
	0	1	0	0	0	
Recording & Playback Mode	1	1	1	1	0	Figure 59
	1	0	1	1	0	
	0	1	1	1	0	
Playback Mode	0	0	1	1	1	Figure 60

Table 22. Recode/Playback Mode

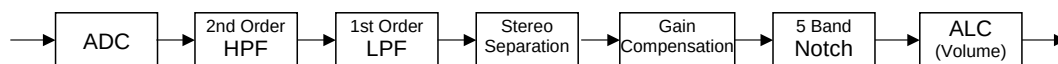


Figure 58. Path at Recording Mode

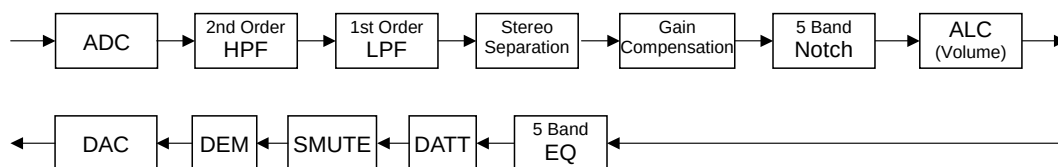


Figure 59. Path at Recording & Playback Mode

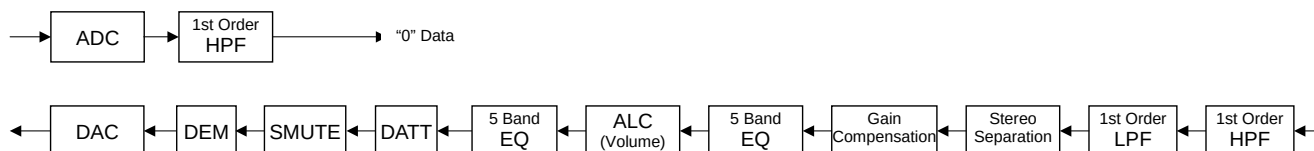


Figure 60. Path at Playback Mode

■ Digital Programmable Filter

(1) High Pass Filter (HPF)

Normally, this HPF is used for a Wind-Noise Reduction Filter. This is composed of 2 steps of 1st order HPF. The coefficient of both HPF is the same and set by F1A13-0 bits and F1B13-0 bits. HPFAD bit controls ON/OFF of the 1st step HPF and HPF bit controls ON/OFF of the 2nd step HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when HPFAD=HPF bits = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency

fc: Cut-off frequency

Register setting (Note 61)

HPF: F1A[13:0] bits =A, F1B[13:0] bits =B

(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc/fs \geq 0.0001 \quad (fc \text{ min} = 4.41\text{Hz at } 44.1\text{kHz})$$

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when LPF bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency

fc: Cut-off frequency

Register setting (Note 61)

LPF: F2A[13:0] bits =A, F2B[13:0] bits =B

(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.

$$fc/fs \geq 0.05 \quad (fc \text{ min} = 2205\text{Hz at } 44.1\text{kHz})$$

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo mic recording data or playback data. F3A13-0 and F3B13-0 bits set the filter coefficient of FIL3. FIL3 becomes High Pass Filter (HPF) at F3AS bit = "0", and Low Pass Filter (LPF) at F3AS bit = "1". FIL3 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit = "0" or PMADL = PMADR = PMDAL = PMDAR bits = "0".

1) When FIL3 is set to "HPF"

fs: Sampling frequency

fc: Cut-off frequency

K: Filter gain [dB] (0dB ≥ K ≥ -10dB)

Register setting (Note 61)

FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency

fc: Cut-off frequency

K: Filter gain [dB] (0dB ≥ K ≥ -10dB)

Register setting (Note 61)

FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed with Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0, E0B13-0 and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 23). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency

fc₁: Pole frequency

fc₂: Zero-point frequency

K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 61)

E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C

(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi f_{c2}/f_s)}{1 + 1 / \tan(\pi f_{c1}/f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f_{c1}/f_s)}{1 + 1 / \tan(\pi f_{c1}/f_s)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi f_{c2}/f_s)}{1 + 1 / \tan(\pi f_{c1}/f_s)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

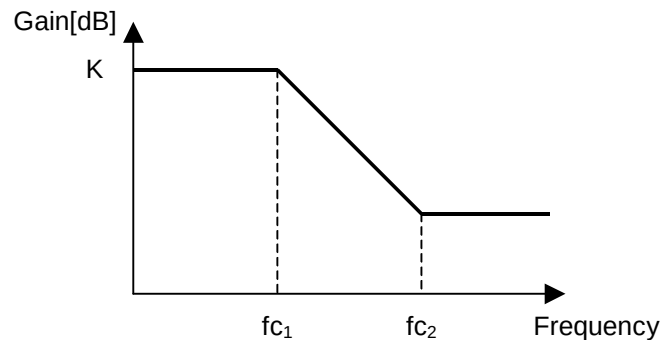


Figure 61. EQ0 Frequency Response

GN1	GN0	Gain
0	0	0dB
0	1	+12dB
1	x	+24dB

(default)

Table 23. Gain select of gain block (x: Don't care)

(5) 5-band Notch

This block can be used as Equalizer or Notch Filter. 5-band Equalizer (EQ1, EQ2, EQ3, EQ4 and EQ5) is ON/OFF independently by EQ1, EQ2, EQ3, EQ4 and EQ5 bits. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient should be set when EQx bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency

fo₁ ~ fo₅: Center frequency

fb₁ ~ fb₅: Band width where the gain is 3dB different from center frequency

K₁ ~ K₅: Gain (−1 ≤ K_n ≤ 3)

Register setting (Note 61)

EQ1: E1A[15:0] bits =A₁, E1B[15:0] bits =B₁, E1C[15:0] bits =C₁

EQ2: E2A[15:0] bits =A₂, E2B[15:0] bits =B₂, E2C[15:0] bits =C₂

EQ3: E3A[15:0] bits =A₃, E3B[15:0] bits =B₃, E3C[15:0] bits =C₃

EQ4: E4A[15:0] bits =A₄, E4B[15:0] bits =B₄, E4C[15:0] bits =C₄

EQ5: E5A[15:0] bits =A₅, E5B[15:0] bits =B₅, E5C[15:0] bits =C₅

(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1 + \tan(\pi fb_n/fs)}, \quad C_n = -\frac{1 - \tan(\pi fb_n/fs)}{1 + \tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = 1 + h_1(z) + h_2(z) + h_3(z) + h_4(z) + h_5(z)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency should be set as below.

$$fo_n / fs < 0.497$$

Note 61. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

$$X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$$

X should be rounded to integer, and then should be translated to binary code (2's complement).

MSB of each filter coefficient setting register is sign bit.

■ ALC Operation

The ALC (Automatic Level Control) is executed by ALC block when ALC bit is “1”. ALC circuit operates at playback path for Playback mode and operates at recording path for Recording mode as shown in Figure 60.

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 24), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 25).

When ZELMN bit = “0” (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 26). IVL and IVR values are attenuated 1 step immediately (period: 1/fs) by ALC limiter operation when output level is over FS (Digital Full Scale). When output level is not over FS, the IVL and IVR values are changed at the individual zero crossing points of Lch and Rch or at the zero crossing timeout.

When ZELMN bit = “1” (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuation operation is done continuously until the input signal level becomes ALC limiter detection level (Table 24) or less. After completing the attenuate operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limier Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output $\geq -2.5\text{dBFS}$	$-2.5\text{dBFS} > \text{ALC Output} \geq -4.1\text{dBFS}$	(default)
0	1	ALC Output $\geq -4.1\text{dBFS}$	$-4.1\text{dBFS} > \text{ALC Output} \geq -6.0\text{dBFS}$	
1	0	ALC Output $\geq -6.0\text{dBFS}$	$-6.0\text{dBFS} > \text{ALC Output} \geq -8.5\text{dBFS}$	
1	1	ALC Output $\geq -8.5\text{dBFS}$	$-8.5\text{dBFS} > \text{ALC Output} \geq -12\text{dBFS}$	

Table 24. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1	LMAT0	ALC Limiter ATT Step				
		ALC Output $\geq \text{LMTH}$	ALC Output $\geq \text{FS}$	ALC Output $\geq \text{FS} + 6\text{dB}$	ALC Output $\geq \text{FS} + 12\text{dB}$	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 25. ALC Limiter ATT Step

ZTM1	ZTM0	Zero Crossing Timeout Period				
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 26. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 27) to be set after completing the ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 24) during the wait time, the ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 28) up to the set reference level (Table 29) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 26). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed in a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed. If ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is executed in a period set by ZTM1-0 bits.

For example, when the current IVL and IVR values are 30H and RGAIN1-0 bits are set to “01”, IVL and IVR values are changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVL and IVR values exceed the reference level (REF7-0 bits), the IVL and IVR values are not increased.

When

“ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

“ALC recovery waiting counter reset level (LMTH1-0) > Output Signal”, the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 30).

WTM2	WTM1	WTM0	ALC Recovery Operation Waiting Period				
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 27. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		(default)
0	0	1 step	0.375dB	
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 28. ALC Recovery GAIN Step

(default)	REF7-0 bits	GAIN (dB)	Step
	F1H	+36.0	0.375dB
	F0H	+35.625	
	EFH	+35.25	
	:	:	
	E1H	+30.0	
	:	:	
	92H	+0.375	
	91H	0.0	
	90H	-0.375	
	:	:	
	2H	-53.625	
	1H	-54.0	
	0H	MUTE	

Table 29. Reference Level at ALC Recovery Operation

RFST1 bit	RFST0 bit	Recovery Speed	(default)
0	0	4 times	
0	1	8 times	
1	0	16times	
1	1	N/A	

Table 30. Fast Recovery Speed Setting (N/A: Not available)

3. Example of ALC Operation

Table 31 and Table 32 show the examples of the ALC setting for mic recording and playback, respectively.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	−4.1dBFS	01	−4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period * ZTM1-0 bits should be equal to or shorter than WTM2-0 bits.	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period	001	32ms	100	46.4ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC	ALC enable	1	Enable	1	Enable

Table 31. Example of the ALC setting (Recording Path)

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	−4.1dBFS	01	−4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same or longer data as ZTM1-0 bits	001	32ms	100	46.4ms
REF5-0	Maximum gain at recovery operation	A1H	+6dB	A1H	+6dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC	ALC enable	1	Enable	1	Enable

Table 32. Example of the ALC setting (Playback Path)

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0".

- LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0

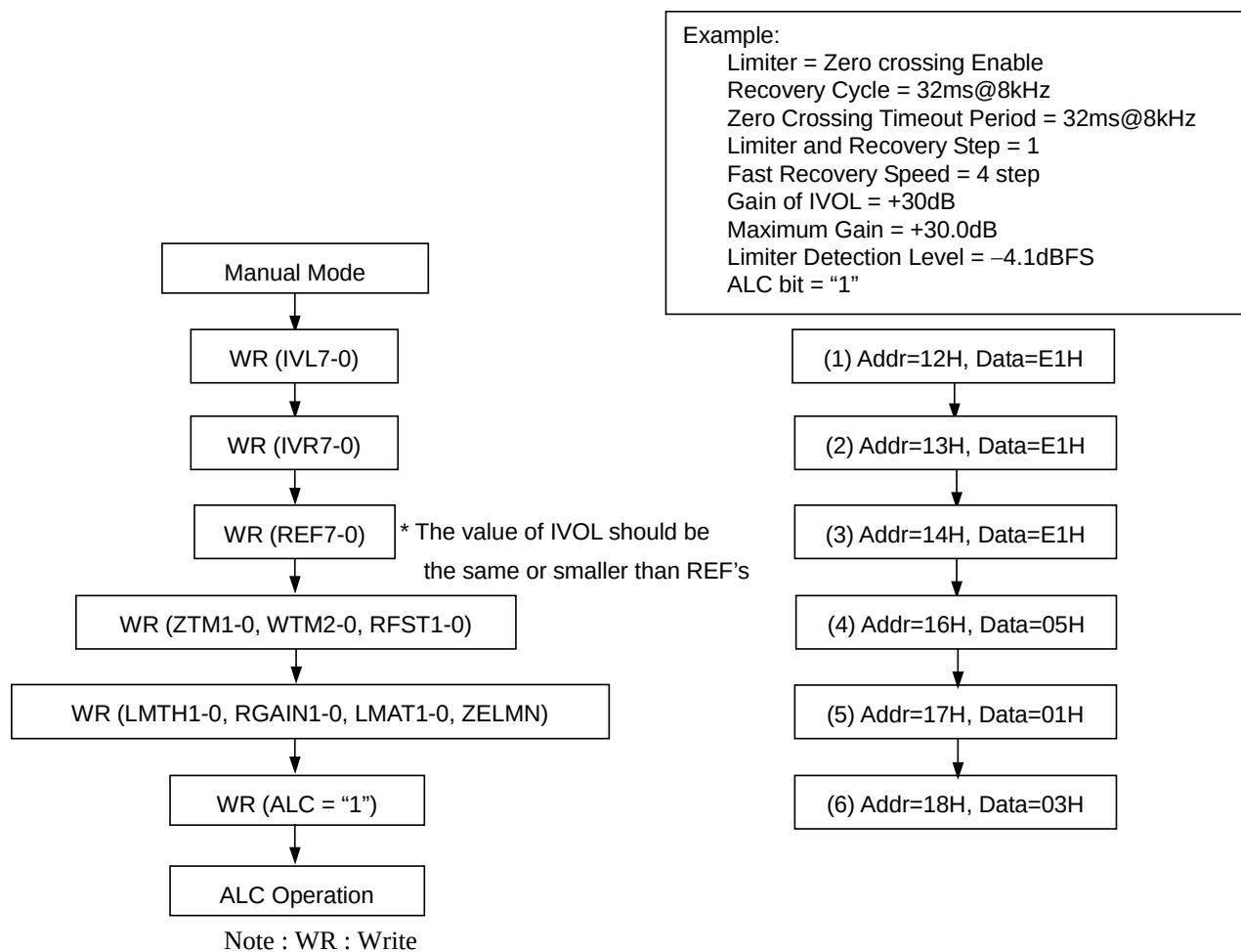


Figure 62. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is “0”. This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed.
For example, in case of changing the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 33). When IVOLC bit is “0”, IVL7-0 and IVR7-0 bits control Lch and Rch volume values independently. When IVOLC bit is “1”, IVL7-0 bits controls both channels. The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = “0”, IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to “1”.

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step
F1H	+36.0	0.375dB
F0H	+35.625	
EFH	+35.25	
:	:	
92H	+0.375	
91H	0.0	
90H	-0.375	
:	:	
03H	-53.25	
02H	-53.625	
01H	-54	
00H	MUTE	

Table 33. Input Digital Volume Setting

■ Side Tone Volume (SVOLA)

The AK4671 has the channel independent side tone volume (5 levels, 6dB step). The volume can be set by the SVAL/R2-0 bits. The volume is included at mixing path from ALC to 5-band EQ. The output data of ALC is changed from 0 to -24dB.

SVL2-0	Gain	(default)
0H	0dB	
1H	-6dB	
2H	-12dB	
3H	-18dB	
4H	-24dB	
Others	N/A	

Table 34. Side Tone Volume A Code Table (N/A: Not available)

■ 5-Band Equalizer

The AK4671 has 5-Band Equalizer before DAC of Stereo CODEC.

The center frequencies and cut/boost amount are the followings.

- Center frequency: 100Hz, 250Hz, 1kHz, 3.5kHz and 10kHz ([Note 62](#), [Note 63](#), [Note 64](#))
- Cut/Boost amount: -10.5dB ~ +12dB, 1.5dB step

Note 62. These are the frequencies when the sampling frequency is 44.1kHz. These frequencies are proportional to the sampling frequency.

Note 63. 100Hz is not center frequency but the frequency component lower than 100Hz is controlled.

Note 64. 10kHz is not center frequency but the frequency component higher than 10kHz is controlled.

EQ bit controls ON/OFF of this Equalizer and these Boost amount are set by EQA3-0, EQB3-0, EQC3-0, EQD3-0 and EQE3-0 bits, respectively, as shown in [Table 35](#).

EQA3-0: Select the boost level of 100Hz

EQB3-0: Select the boost level of 250Hz

EQC3-0: Select the boost level of 1kHz

EQD3-0: Select the boost level of 3.5kHz

EQE3-0: Select the boost level of 10kHz

EQx3-0	Boost amount	
0H	+12.0dB	
1H	+10.5dB	
2H	+9.0dB	
3H	+7.5dB	
:	:	
8H	0dB	(default)
:	:	
DH	-7.5dB	
EH	-9.0dB	
FH	-10.5dB	

Table 35. Boost amount of 5-Band Equalizer

■ Digital Output Volume

The AK4671 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the OVL7-0 and OVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to −115dB or MUTE. When the OVOLC bit = “1”, the OVL7-0 bits control both Lch and Rch attenuation levels. When the OVOLC bit = “0”, the OVL7-0 bits control Lch level and OVR7-0 bits control Rch level. This volume has a soft transition function. The OVTM bit sets the transition time between set values of OVL/R7-0 bits as either 1061/fs or 256/fs (Table 37). When OVTM bit = “0”, a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=24ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

(default)	OVL/R7-0	Gain	Step
	00H	+12.0dB	0.5dB
	01H	+11.5dB	
	02H	+11.0dB	
	:	:	
	18H	0dB	
	:	:	
	FDH	−114.5dB	
	FEH	−115.0dB	
	FFH	MUTE (−∞)	

Table 36. Digital Volume Code Table

OVTM bit	Transition time between DVL/R7-0 bits = 00H and FFH			(default)
	Setting	fs=8kHz	fs=44.1kHz	
0	1061/fs	133ms	24ms	(default)
1	256/fs	32ms	6ms	

Table 37. Transition Time Setting of Digital Output Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is changed to “1”, the output signal is attenuated to $-\infty$ (“0”) during the cycle set by the OVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by the OVL/R7-0 bits during the cycle set of the OVTM bit. If the soft mute is cancelled within the cycle set by the OVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the OVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 63).

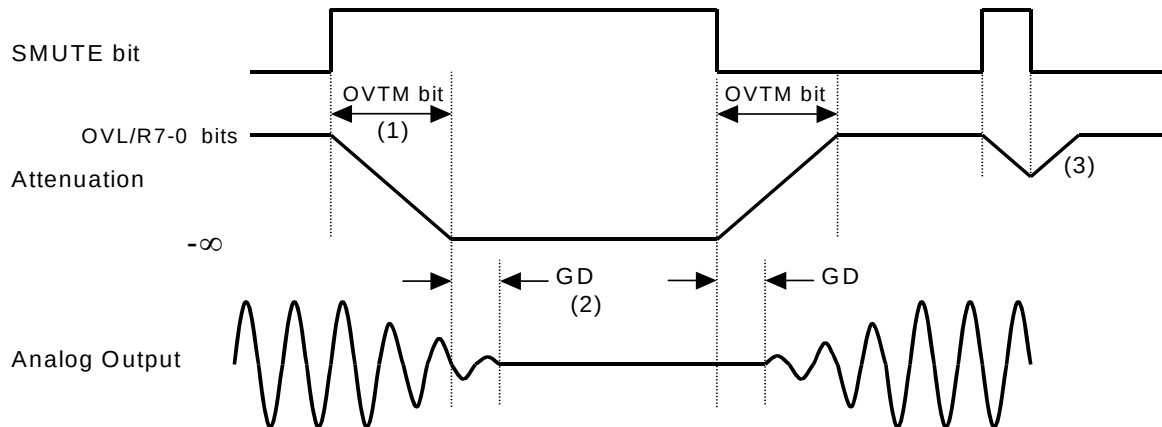


Figure 63. Soft Mute Function

- (1) The output signal is attenuated until $-\infty$ (“0”) in the cycle set by the OVTM bit.
- (2) Analog output corresponding to digital input has the group delay (GD).
- (3) If the soft mute is cancelled within the cycle set by the OVTM bit, the attenuation is discounted and returned to the value set by the OVL/R7-0 bits.

■ Digital Volume for Recording of Received Voice (DATT-B)

The AK4671 has a digital output volume (DATT-B: 256 levels, 0.5dB step, Mute) for recording of received voice. The volume can be set by the BVL7-0 bits. The volume is included in front of an SRC-B block. The input data of SRC-B is changed from +12 to -115dB or MUTE. This volume has a soft transit function. The transition time between set values of BVL7-0 bits is 256/fs2. It takes 256/fs2 (=32ms@fs2=8kHz) from 00H (+12dB) to FFH (MUTE).

(default)	BVL7-0	Gain	Step
	00H	+12.0dB	0.5dB
	01H	+11.5dB	
	02H	+11.0dB	
	:	:	
	18H	0dB	
	:	:	
	FDH	-114.5dB	
	FEH	-115.0dB	
	FFH	MUTE ($-\infty$)	

Table 38. Digital Volume B Code Table

■ Digital Volume for Received Voice (DATT-C)

The AK4671 has a digital output volume (DATT-C: 256 levels, 0.5dB step, Mute) for received voice. The volume can be set by the CVL7-0 bits. The volume is included in front of SDTOB output. The input data of SRC-C is changed from +12 to -115dB or MUTE. This volume has a soft transition function. The transition time between set values of CVL7-0 bits is 256/fs2. It takes 256/fs2 (=32ms@fs2=8kHz) from 00H (+12dB) to FFH (MUTE).

(default)	CVL7-0	Gain	Step
	00H	+12.0dB	0.5dB
	01H	+11.5dB	
	02H	+11.0dB	
	:	:	
	18H	0dB	
	:	:	
	FDH	-114.5dB	
	FEH	-115.0dB	
	FFH	MUTE ($-\infty$)	

Table 39. Digital Volume C Code Table

■ Side Tone Volume for B/T Phone Call (SVOLB)

The AK4671 has the side tone volume (5 levels, 6dB step) for B/T phone call. The volume can be set by the SVL2-0 bits. The volume is included at mixing path from SRC-A to DATT-C. The output data of SRC-A is changed from 0 to -24dB.

SVB2-0	Gain	(default)
0H	0dB	
1H	-6dB	
2H	-12dB	
3H	-18dB	
4H	-24dB	
Others	N/A	

Table 40. Side Tone Volume B Code Table (N/A: Not available)

■ Digital Volume for B/T MIC Input (BIVOL)

The AK4671 has the digital volume (5 levels, 6dB step) for B/T mic input. The volume can be set by the BIV2-0 bits. The volume is included at SDTIB input. The input data is changed from 0 to -24dB.

BIV2-0	Gain	(default)
0H	0dB	
1H	-6dB	
2H	-12dB	
3H	-18dB	
4H	-24dB	
Others	N/A	

Table 41. SDTIB Volume Code Table (N/A: Not available)

■ Path & Mixing Setting of Digital Block (Figure 57)

PMADL and PMADR bits set both ADC power management and output data selection. In case of mono operation, the same data is output to both channel slots.

PMADL	PMADR	ADC Lch data	ADC Rch data	(default)
0	0	All "0"	All "0"	
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 42. ADC Mono/Stereo Select

PFSEL bit select the input data of programmable filter.

PFSEL	Programmable Filter Input	(default)
0	ADC Output (selected by Table 42)	
1	SDTI Input (selected by Table 48)	

Table 43. Programmable Filter Input Signal Select

When ADM bit is "1", ALC output data is output to both channels of SDTO and SVOLA as (L+R)/2, respectively.

ADM	Lch	Rch	(default)
0	L	R	
1	(L+R)/2	(L+R)/2	

Table 44. ALC Output Mono Mixing

SDOL1-0 and SDOR1-0 bits set the data mixing for each channel of SDTO from the data selected by Table 44 and SRC-B output data.

SDOL1	SDOL0	SDTO Lch	(default)
0	0	Lch Signal selected by Table 44	
0	1	SRC-B	
1	0	(Lch Signal selected by Table 44) + (SRC-B)	
1	1	N/A	

Table 45. SDTO Lch Output Mixing (N/A: Not available)

SDOR1	SDOR0	SDTO Rch	(default)
0	0	Rch Signal selected by Table 44	
0	1	SRC-B	
1	0	(Rch Signal selected by Table 44) + (SRC-B)	
1	1	N/A	

Table 46. SDTO Rch Output Mixing (N/A: Not available)

When SDOD bit is “1”, SDTO output data can be disabled (fixed to “L”). Input data of SVOLA is not disabled.

SDOD	SDTO	(default)
0	Enable (Output)	
1	Disable (“L”)	

Table 47. SDTO Disable

SDIM1-0 bits select stereo or mono of SDTI input data. In case of mono mode, the same data is input to both channels.

SDIM1	SDIM0	Lch	Rch	(default)
0	0	L	R	
0	1	L	L	
1	0	R	R	
1	1	N/A		

Table 48. SDTI Stereo/Mono Select (N/A: Not available)

PFMXL1-0 and PFMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by Table 48 and SVOLA output data.

PFMXL1	PFMXL0	5-band EQ Lch Input	(default)
0	0	Lch Signal selected by Table 48	
0	1	SVOLA Lch	
1	0	(Lch Signal selected by Table 48) + (SVOLA Lch)	
1	1	N/A	

Table 49. 5-band EQ Lch Input Mixing 1 (N/A: Not available)

PFM XR1	PFM XR0	5-band EQ Rch Input	(default)
0	0	Rch Signal selected by Table 48	
0	1	SVOLA Rch	
1	0	(Rch Signal selected by Table 48) + (SVOLA Rch)	
1	1	N/A	

Table 50. 5-band EQ Rch Input Mixing 1 (N/A: Not available)

SRMXL1-0 and SRMXR1-0 bits set the data mixing for each channel of 5-band EQ from the data selected by [Table 49/](#)[Table 50](#) and SVOLA output data.

SRMXL1	SRMXL0	5-band EQ Lch Input	(default)
0	0	Signal selected by Table 49	
0	1	SRC-B	
1	0	(Signal selected by Table 49) + (SRC-B)	
1	1	N/A	

Table 51. 5-band EQ Lch Input Mixing 2 (N/A: Not available)

SRMXR1	SRMXR0	5-band EQ Rch Input	(default)
0	0	Signal selected by Table 50	
0	1	SRC-B	
1	0	(Signal selected by Table 50) + (SRC-B)	
1	1	N/A	

Table 52. 5-band EQ Rch Input Mixing 2 (N/A: Not available)

DAM and MIXD bits set the data mixing for DAC input.

DAM	MIXD	Lch	Rch	(default)
0	x	L	R	
1	0	L+R	L+R	
1	1	(L+R)/2	(L+R)/2	

Table 53. DAC Mono Mixing (x: Don't care)

SRA1-0 and MIXD bits set the data mixing for SRC-A input.

SRA1	SRA0	MIXD	SRC-A	(default)
0	0	x	L	
0	1	x	R	
1	0	0	L+R	
1	0	1	(L+R)/2	
1	1	x	N/A	

Table 54. SRC-A Input Mixing (x: Don't care, N/A: Not available)

SDOA bit selects the output data of SDTOA.

SDOA	SDTOA	(default)
0	SRC-A	
1	SDTIB	

Table 55. SDTOA Output Select

When SDOAD bit is "1", SDTOA output data can be disabled (fixed to "L"). Input data of SVOLB is not disabled.

SDOAD	SDTOA	(default)
0	Enable (Output)	
1	Disable ("L")	

Table 56. SDTOA Disable

SBMX1-0 bits set the data mixing from SDTIA input and SVOLB output. The mixed data is output to SDTOB via DATT-C.

SBMX1	SBMX0	DATT-C Input	(default)
0	0	SDTIA	
0	1	SVOLB	
1	0	(SDTIA) + (SVOLB)	
1	1	N/A	

Table 57. SDTOB Mixing (N/A: Not available)

When SDOBD bit is “1”, SDTOB output data can be disabled (fixed to “L”).

SDOBD	SDTOB	(default)
0	Enable (Output)	
1	Disable (“L”)	

Table 58. SDTOB Disable

BVMX1-0 bits set the data mixing for SRC-B from SDTIA input (DATT-B output) and SDTIB input (BIVOL output).

BVMX1	BVMX0	SRC-B Input	(default)
0	0	SDTIA	
0	1	SDTIB	
1	0	(SDTIA) + (SDTIB)	
1	1	N/A	

Table 59. SRC-B Input Mixing (N/A: Not available)

■ Analog Mixing: Single-ended Input (LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins)

AK4671 supports analog mixing function from each line input to each line output (Figure 64).

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is “1”. When PMAINL1=PMAINR1=PMAINL2=PMAINR2=PMAINL3=PMAINR3=PMAINL4=PMAINR4=PMMICL=PMMICR bits = “1”, the input resistance of LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 pins becomes 25k Ω (typ) at MGNL/R0 bits = “0” and 20k Ω (typ) at MGNL/R0 bits = “1”, respectively.

L1G1-0, L2G1-0, L3G1-0, L4G1-0 and LPG1-0 bits adjust the gain for each path (Table 60, Table 61, Table 62, Table 63, Table 64).

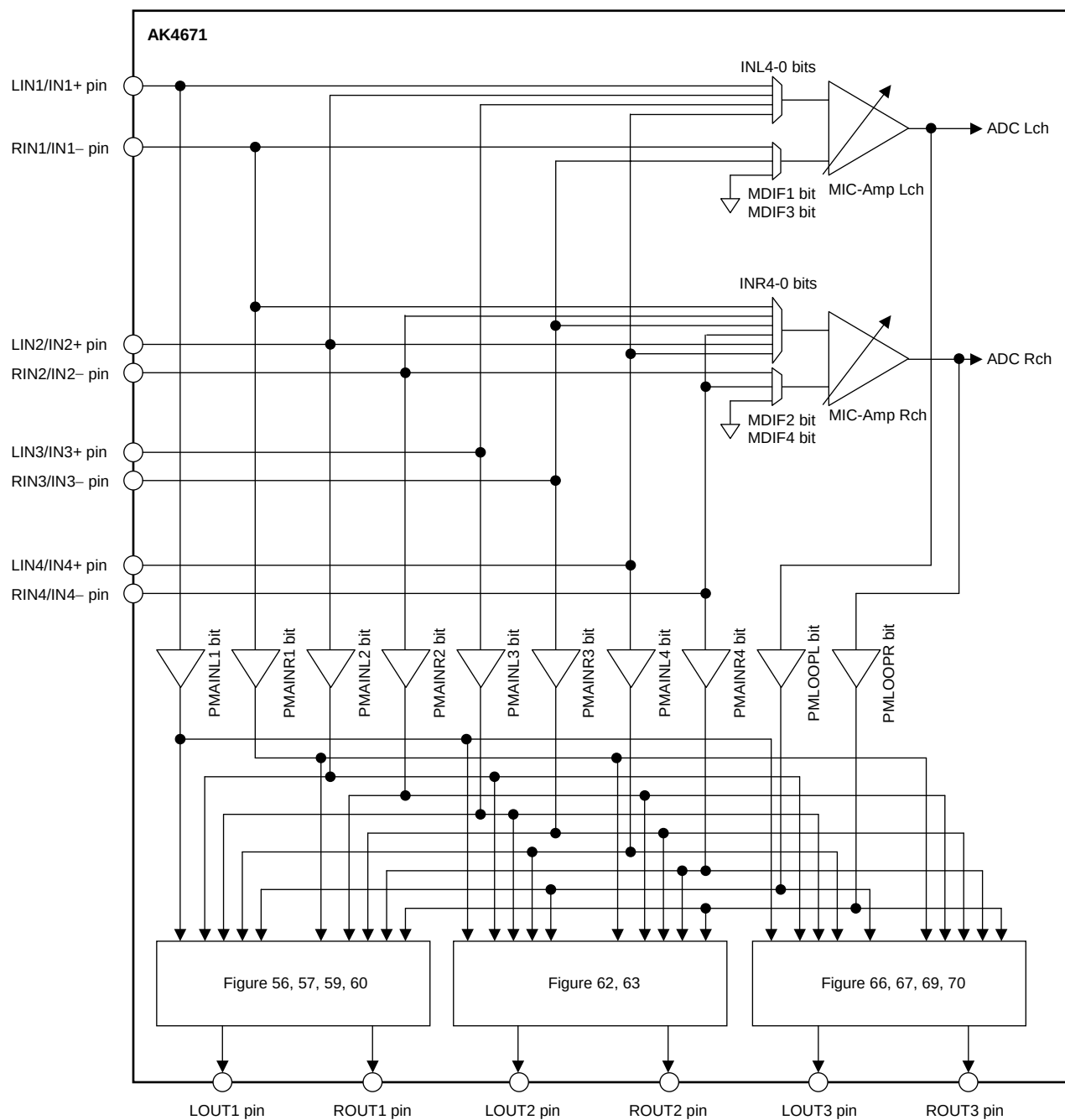


Figure 64. Analog Mixing Circuit

L1G1 bit	L1G0 bit	Gain
0	0	0dB
0	1	+6dB
1	0	-6dB
1	1	N/A

(default)

Table 60. LIN1/RIN1 (or IN1+/-) Mixing Gain (typ) (N/A: Not available)

L2G1 bit	L2G0 bit	Gain
0	0	0dB
0	1	+6dB
1	0	-6dB
1	1	N/A

(default)

Table 61. LIN2/RIN2 (or IN2+/-) Mixing Gain (typ) (N/A: Not available)

L3G1 bit	L3G0 bit	Gain
0	0	0dB
0	1	+6dB
1	0	-6dB
1	1	N/A

(default)

Table 62. LIN3/RIN3 (or IN3+/-) Mixing Gain (typ) (N/A: Not available)

L4G1 bit	L4G0 bit	Gain
0	0	0dB
0	1	+6dB
1	0	-6dB
1	1	N/A

(default)

Table 63. LIN4/RIN4 (or IN4+/-) Mixing Gain (typ) (N/A: Not available)

LPG1 bit	LPG0 bit	Gain
0	0	0dB
0	1	+6dB
1	0	-6dB
1	1	N/A

(default)

Table 64. MIC-Amp Mixing Gain (typ) (N/A: Not available)

■ Analog Mixing: Full-differential Input (IN1+/IN1-/IN2+/IN2-/IN3+/IN3-/IN4+/IN4- pins)

When MDIF1, MDIF2, MDIF3 and MDIF4 bits are “1”, LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 pins become IN1+/-, IN2+/-, IN3+/- and IN4+/- pins, respectively, and analog mixing is available.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is “1”. When PMAINL1=PMAINR1=PMAINL2=PMAINR2=PMAINL3=PMAINR3=PMAINL4=PMAINR4=PMMICL=PMMICR bits = “1”, the input resistance of IN1+/-, IN2+/-, IN3+/- and IN4+/- pins becomes 25kΩ (typ) at MGNL/R0 bits = “0” and 20kΩ (typ) at MGNL/R0 bits = “1”, respectively.

L1G1-0, L2G1-0, L3G1-0, L4G1-0 and LPG1-0 bits adjust the gain for each path (Table 60, Table 61, Table 62, Table 63, Table 64).

■ Stereo Line Output (LOUT1/ROUT1 pins)

When DACL and DACR bits are “1”, Lch/Rch signal of DAC is output from the LOOUT1/ROUT1 pins which is single-ended. When DACL and DACR bits are “0”, output signal is muted and LOOUT1/ROUT1 pins output VCOM voltage. The load impedance is 10k Ω (min.). When the PMLO1=PMRO1=LOPS1 bits = “0”, LOOUT1/ROUT1 enters power-down mode and the output is pulled-down to VSS1 by 100k Ω (typ). When the LOPS1 bit is “1”, LOOUT1/ROUT1 enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO1 and PMRO1 bits at LOPS1 bit = “1”. In this case, output signal line should be pulled-down to VSS1 by 20k Ω after AC coupled as Figure 65. Rise/Fall time is 300ms(max) at C=1 μ F and AVDD=3.3V. When PMLO1=PMRO1 bits = “1” and LOPS1 bit = “0”, LOOUT1/ROUT1 is in normal operation.

L1VL3-0 bits control the volume of LOOUT1/ROUT1.

When LOM bit = “1”, DAC output signal is output to LOOUT1 and ROUT1 pins as (L+R) mono signal.

When LOOPM bit = “1”, the MIC-Amp signal is output to LOOUT1 and ROUT1 pins as (L+R) mono signal.

LOPS1	PMLO1	Mode	LOOUT1 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 65. Stereo Line Output Mode Select (LOOUT1)

LOPS1	PMRO1	Mode	ROUT1 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 66. Stereo Line Output Mode Select (ROUT1)

L1VL2-0	Attenuation	
6H	+6dB	(default)
5H	0dB	
4H	-6dB	
3H	-12dB	
2H	-18dB	
1H	-24dB	
0H	MUTE	

Table 67. Stereo Line Output Volume Setting

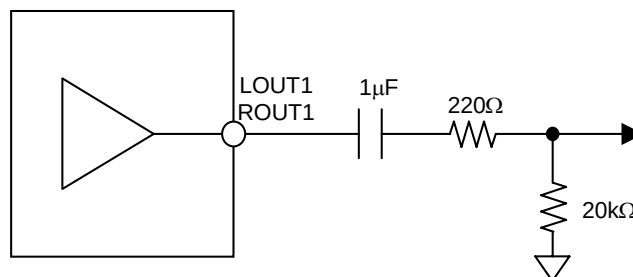


Figure 65. External Circuit for Stereo Line Output (in case of using Pop Noise Reduction Circuit)

<Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

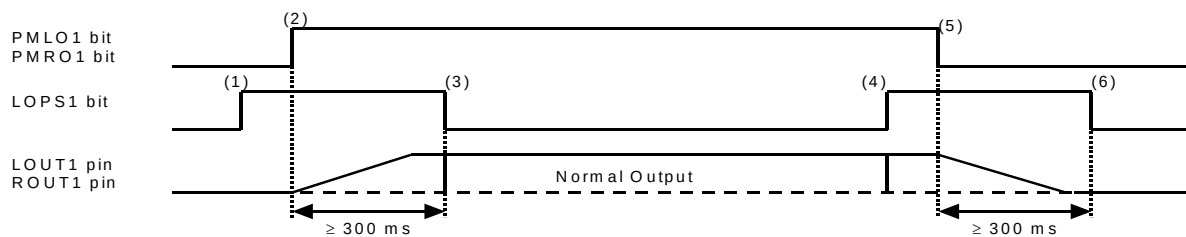


Figure 66. Stereo Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)

- (1) Set LOPS1 bit = "1". Stereo line output enters the power-save mode.
- (2) Set PMLO1=PMRO1 bits = "1". Stereo line output exits the power-down mode.
LOUT1 and ROUT1 pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
- (3) Set LOPS1 bit = "0" after LOUT1 and ROUT1 pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
- (4) Set LOPS1 bit = "1". Stereo line output enters power-save mode.
- (5) Set PMLO1=PMRO1 bits = "0". Stereo line output enters power-down mode.
LOUT1 and ROUT1 pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
- (6) Set LOPS1 bit = "0" after LOUT1 and ROUT1 pins fall down. Stereo line output exits the power-save mode.

<Analog Mixing Circuit for LOUT1/ROUT1>

DACL, DACR, LOM, LINL1, RINR1, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, LOOPL, LOOPR and LOOPM bits control each path switch.

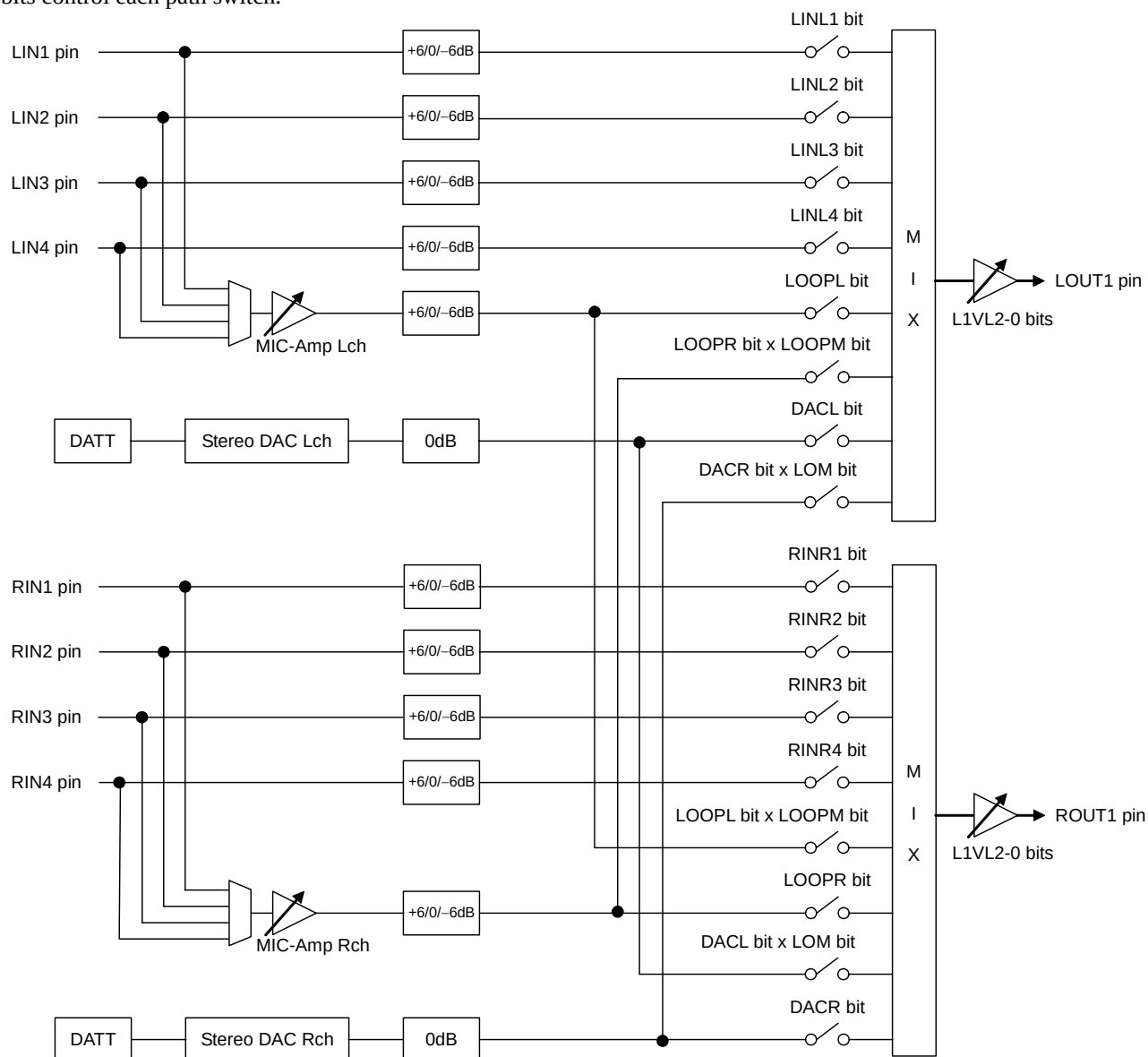


Figure 67. LOUT1/ROUT1 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

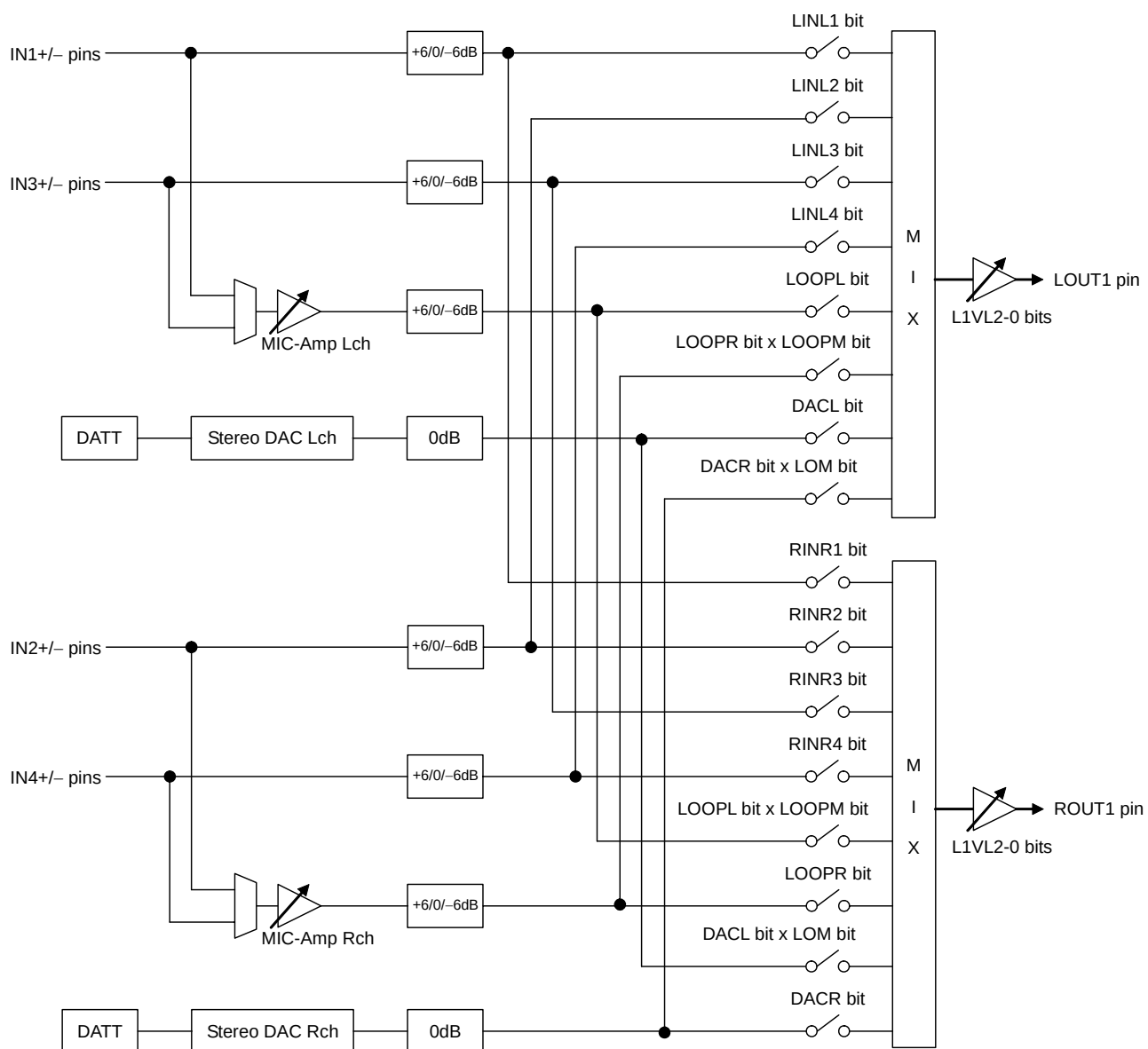


Figure 68. LOUT1/ROUT1 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Receiver-Amp (RCP/RCN pins)

When RCV bit = “1”, LOUT1/ROUT1 pins become RCP/RCN pins, respectively. Lch/Rch signal of DAC or LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the RCP/RCN pins which is BTL as (L+R) signal. The load impedance is 32Ω (min). When the PMLO1 = PMRO1 bits = “0”, the mono receiver output enters power-down mode and the output is Hi-Z. When the PMLO1 = PMRO1 bits = “1” and LOPS1 bit = “1”, mono receiver output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO1 and PMRO1 bits at LOPS1 bit = “0”. When PMLO1 = PMRO1 bits = “1” and LOPS1 bit = “0”, mono receiver output enters in normal operation. L1VL3-0 bits control the volume of mono receiver output.

L1VL2-0	Attenuation
6H	+12dB
5H	+6dB
4H	0dB
3H	-6dB
2H	-12dB
1H	-18dB
0H	MUTE

(default)

Table 68. Mono Receiver Output Volume Setting

PMLO1/RO1	LOPS1	Mode	RCP	RCN
0	x	Power-down	Hi-Z	Hi-Z
1	1	Power-save	Hi-Z	VCOM
	0	Normal Operation	Normal Operation	Normal Operation

(default)

Table 69. Receiver-Amp Mode Setting (x: Don't care)

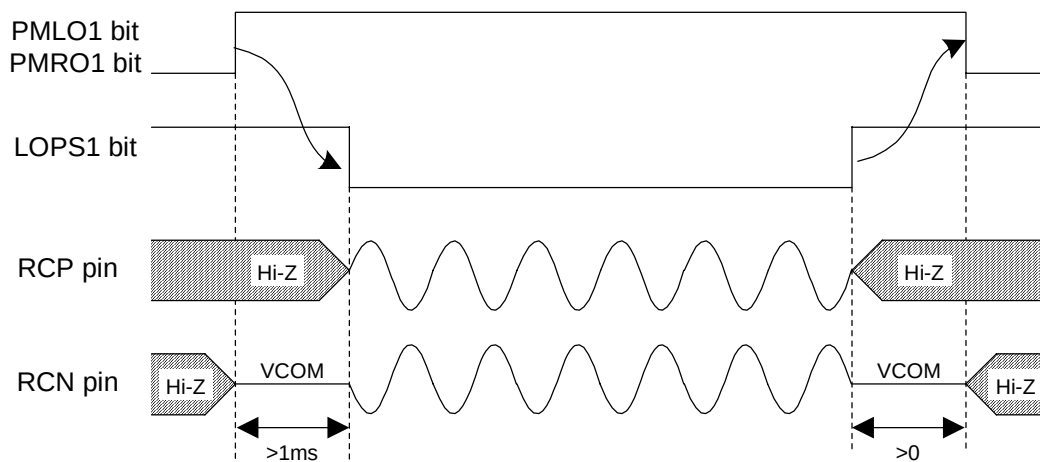


Figure 69. Power-up/Power-down Timing for Receiver-Amp

<Analog Mixing Circuit for Receiver Output>

DACL, DACR, LINL1, RINR1, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, LOOPL and LOOPR bits control each path switch.

When MDIF1/2/3/4 bits = "1", RINR1/2/3/4 bits should be "0".

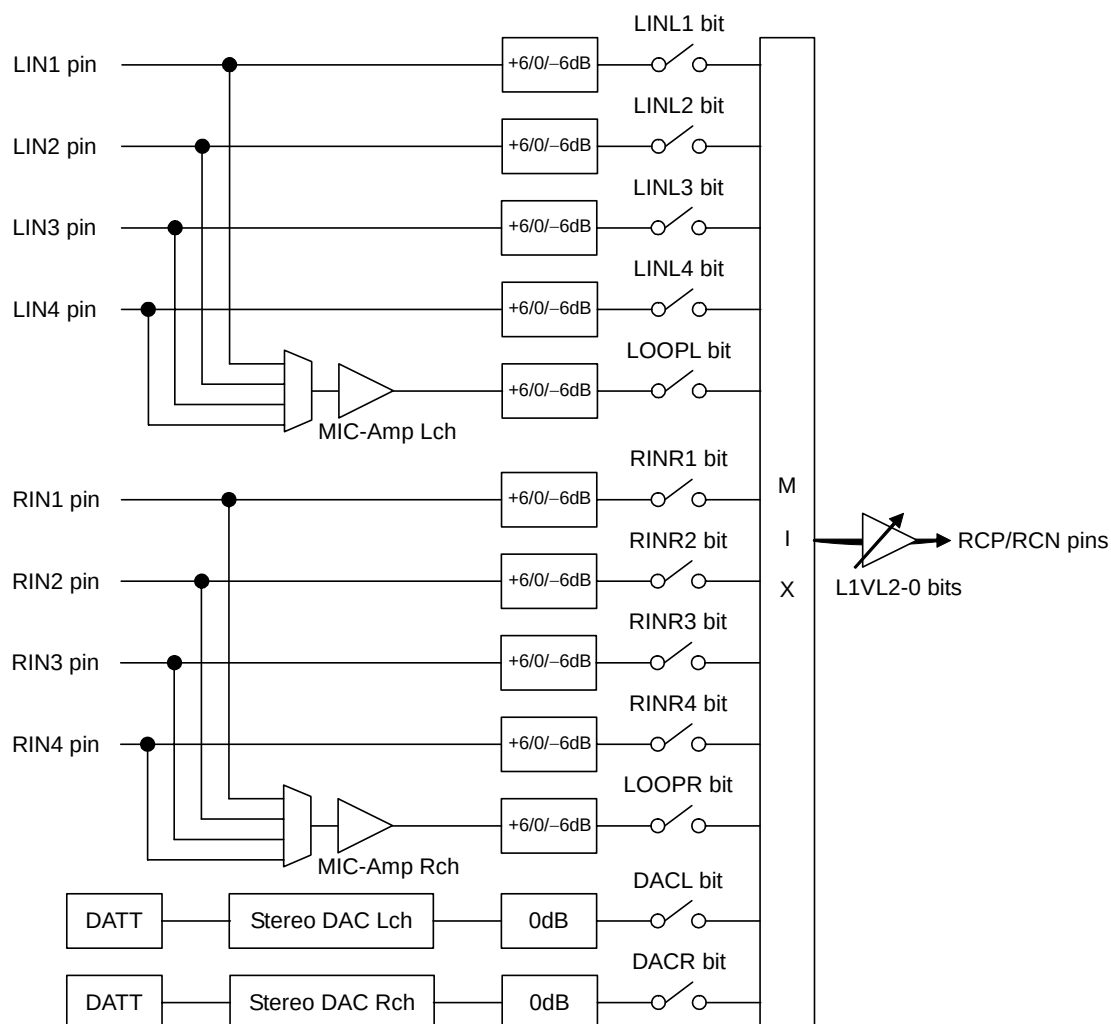


Figure 70. Receiver Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

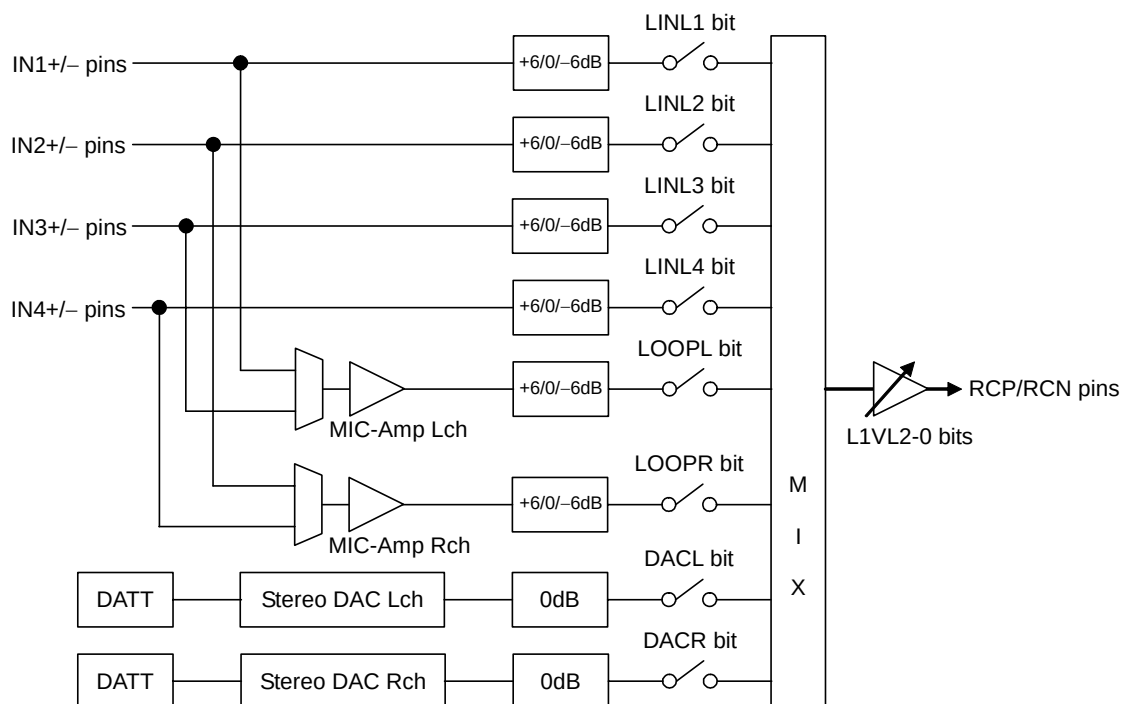


Figure 71. Receiver Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Headphone Output (LOUT2/ROUT2 pins)

Power supply voltage for the LOUT2/ROUT2 is supplied from the AVDD pin and centered on the $0.5 \times AVDD$ (typ) voltage. The load resistance is 16Ω (min). HPG3-0 bits control the output volume (Table 70).

When LOM2 bit = “1”, DAC output signal is output to LOUT2 and ROUT2 pins as (L+R) mono signal.

When LOOPM2 bit = “1”, the MIC-Amp signal is output to LOUT2 and ROUT2 pins as (L+R) mono signal.

HPG3-0	Attenuation
DH	+6dB
CH	+3dB
BH	0dB
AH	-3dB
:	:
:	:
2H	-27dB
1H	-30dB
0H	MUTE

(default)

Table 70. LOUT2/ROUT2 Output Volume

When the MUTEN bit is “0”, the common voltage of LOUT2/ROUT2 falls and the outputs (LOUT2 and ROUT2 pins) change to “L” (VSS1). When the MUTEN bit is “1”, the common voltage rises to VCOM voltage. A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to AVDD voltage and the capacitor at MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = $1.0\mu\text{F}$, AVDD=3.3V:

Rise/fall time constant: $\tau = 100\text{ms}(\text{typ})$, $250\text{ms}(\text{max})$

Time until the common goes to VSS1 when MUTEN bit = “1” → “0”: $500\text{ms}(\text{max})$

When PMLO2, PMRO2, PMLO2S and PMRO2S bits are “0”, the LOUT2/ROUT2 is powered-down, and the outputs (LOUT2 and ROUT2 pins) go to “L” (VSS1).

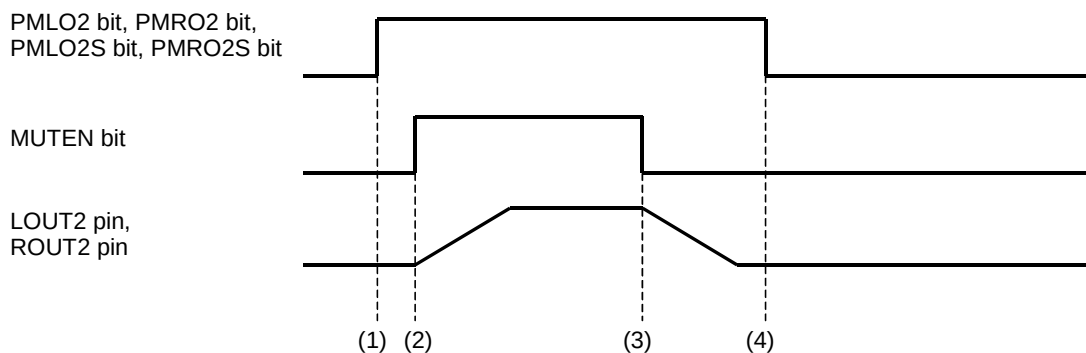


Figure 72. Power-up/Power-down Timing for LOUT2/ROUT2

(1) LOUT2/ROUT2 power-up (PMLO2, PMRO2, PMLO2S, PMRO2S bit = “1”). The outputs are still VSS1.

(2) LOUT2/ROUT2 common voltage rises up (MUTEN bit = “1”).

(3) LOUT2/ROUT2 common voltage falls down (MUTEN bit = “0”).

(4) LOUT2/ROUT2 power-down (PMLO2, PMRO2, PMLO2S, PMRO2S bit = “0”). The outputs are VSS1. If the power supply is switched off or LOUT2/ROUT2 is powered-down before the common voltage goes to VSS1, some POP noise occurs.

<Analog Mixing Circuit for LOUT2/ROUT2>

DACHL, DACHR, LOM2, LINH1, RINH1, LINH2, RINH2, LINH3, RINH3, LINH4, RINH4, LOOPHL, LOOPHR and LOOPM2 bits control each path switch.

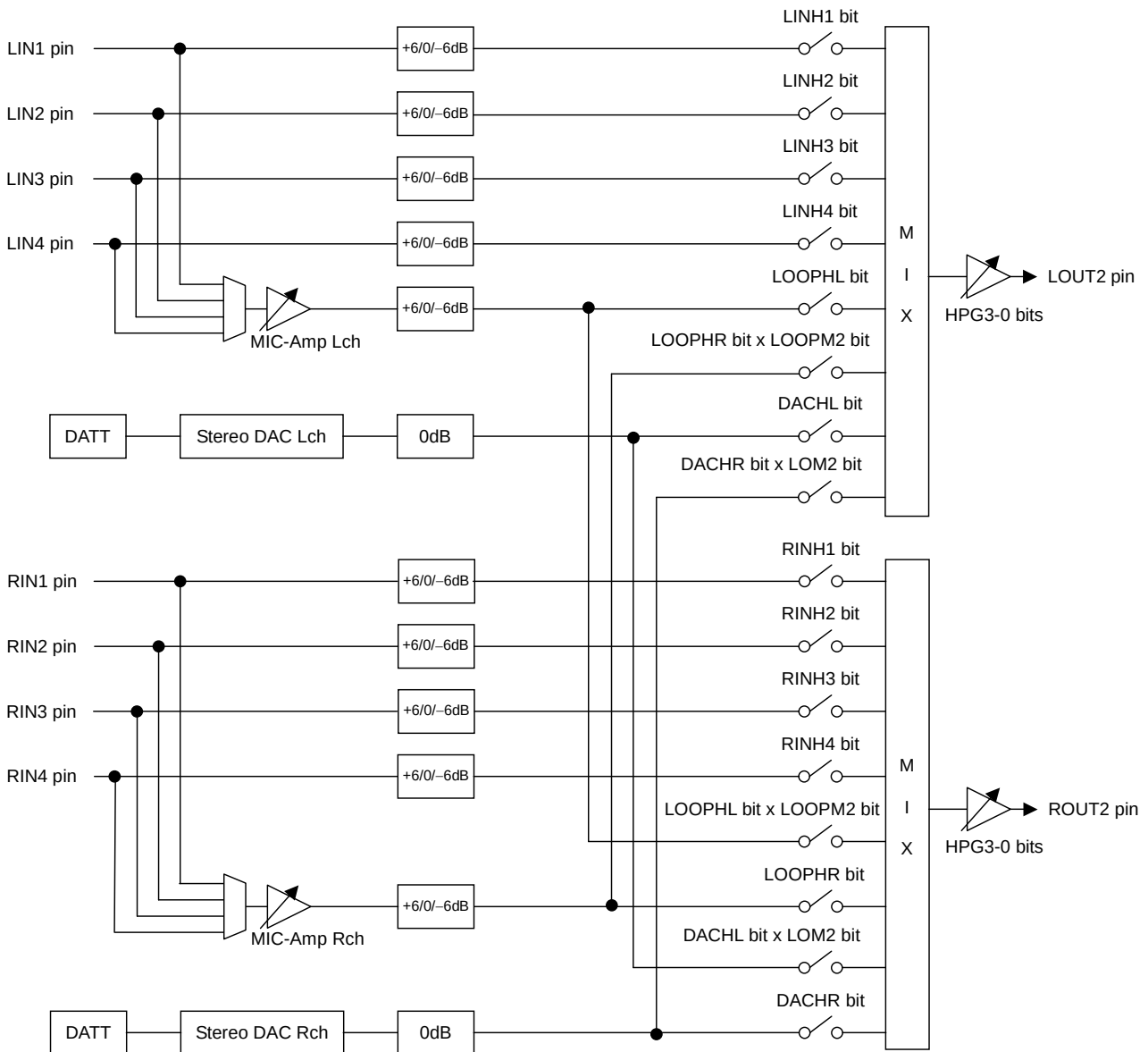


Figure 73. LOUT2/ROUT2 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

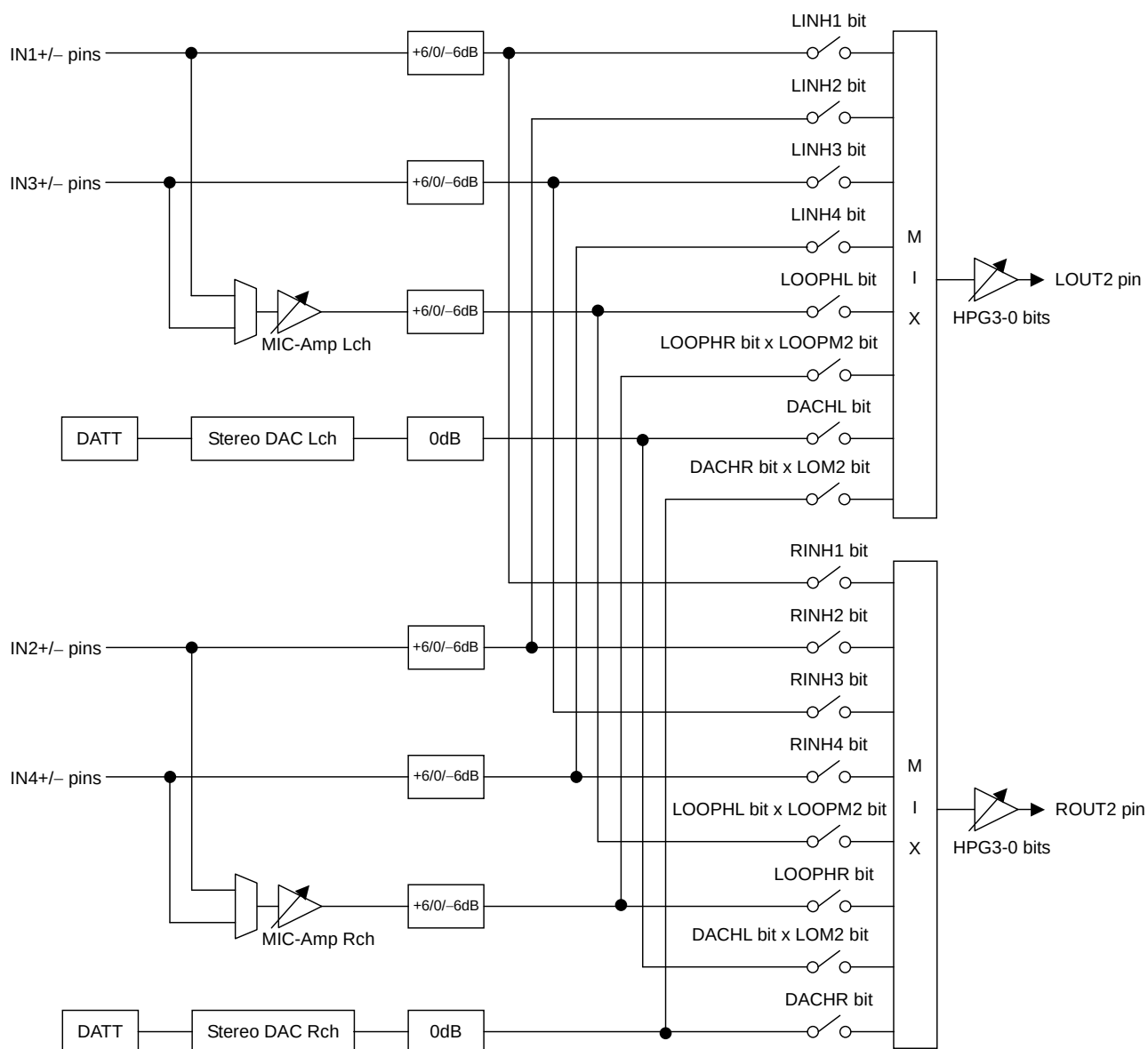


Figure 74. LOUT2/ROUT2 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Stereo Line Output 3 (LOUT3/ROUT3 pins)

When DACSL and DACSR bits are “1”, Lch/Rch signal of DAC is output from the LOUT3/ROUT3 pins which is single-ended. When DACSL and DACSR bits are “0”, output signal is muted and LOUT3/ROUT3 pins output VCOM voltage. The load impedance is 10k Ω (min.). When the PMLO3=PMRO3=LOPS3 bits = “0”, LOUT3/ROUT3 enters power-down mode and the output is pulled-down to VSS1 by 100k Ω (typ). When the LOPS3 bit is “1”, LOUT3/ROUT3 enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO3 and PMRO3 bits at LOPS3 bit = “1”. In this case, output signal line should be pulled-down to VSS1 by 20k Ω after AC coupled as [Figure 75](#). Rise/Fall time is 300ms(max) at C=1 μ F and AVDD=3.3V. When PMLO3=PMRO3 bits = “1” and LOPS3 bit = “0”, LOUT3/ROUT3 is in normal operation.

L3VL3-0 bits control the volume of LOUT3/ROUT3.

When LOM3 bit = “1”, DAC output signal is output to LOUT3 and ROUT3 pins as (L+R) mono signal.

When LOOPM3 bit = “1”, the MIC-Amp signal is output to LOUT3 and ROUT3 pins as (L+R) mono signal.

LOPS3	PMLO3	Mode	LOUT3 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 71. Stereo Line Output Mode Select (LOUT3)

LOPS3	PMRO3	Mode	ROUT3 pin	
0	0	Power-down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS1	
	1	Power-save	Rise up to VCOM	

Table 72. Stereo Line Output Mode Select (ROUT3)

L3VL1	L3VL0	Attenuation	
1	1	+3dB	(default)
1	0	0dB	
0	1	-3dB	
0	0	-6dB	

Table 73. Stereo Line Output Volume Setting

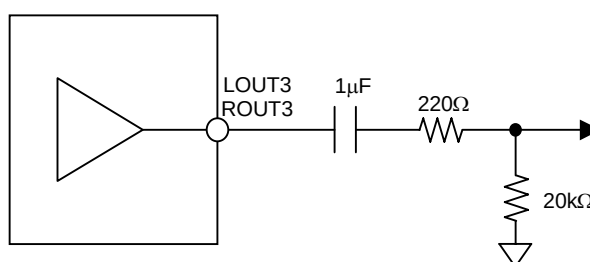


Figure 75. External Circuit for Stereo Line Output (in case of using Pop Noise Reduction Circuit)

<Stereo Line Output 3 Control Sequence (in case of using Pop Noise Reduction Circuit)>

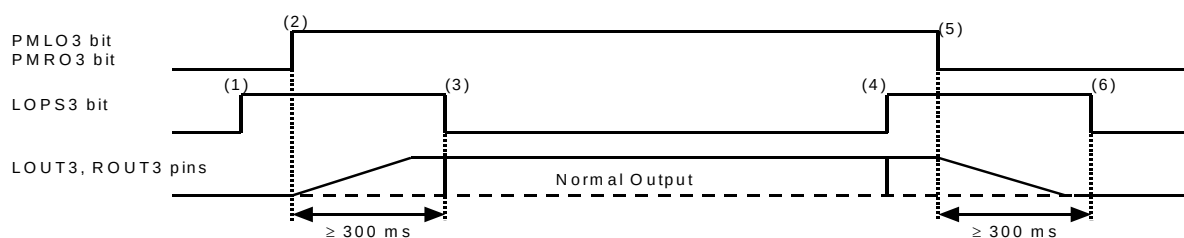


Figure 76. Stereo Line Output 3 Control Sequence (in case of using Pop Noise Reduction Circuit)

- (1) Set LOPS3 bit = "1". Stereo line output enters the power-save mode.
- (2) Set PMLO3=PMRO3 bits = "1". Stereo line output exits the power-down mode.
LOUT3 and ROUT3 pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
- (3) Set LOPS3 bit = "0" after LOUT3 and ROUT3 pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
- (4) Set LOPS3 bit = "1". Stereo line output enters power-save mode.
- (5) Set PMLO3=PMRO3 bits = "0". Stereo line output enters power-down mode.
LOUT3 and ROUT3 pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1μF and AVDD=3.3V.
- (6) Set LOPS3 bit = "0" after LOUT3 and ROUT3 pins fall down. Stereo line output exits the power-save mode.

<Analog Mixing Circuit for LOUT3/ROUT3>

DACSL, DACSR, LOM3, LINS1, RINS1, LINS2, RINS2, LINS3, RINS3, LINS4, RINS4, LOOPSL, LOOPSR and LOM3 bits control each path switch.

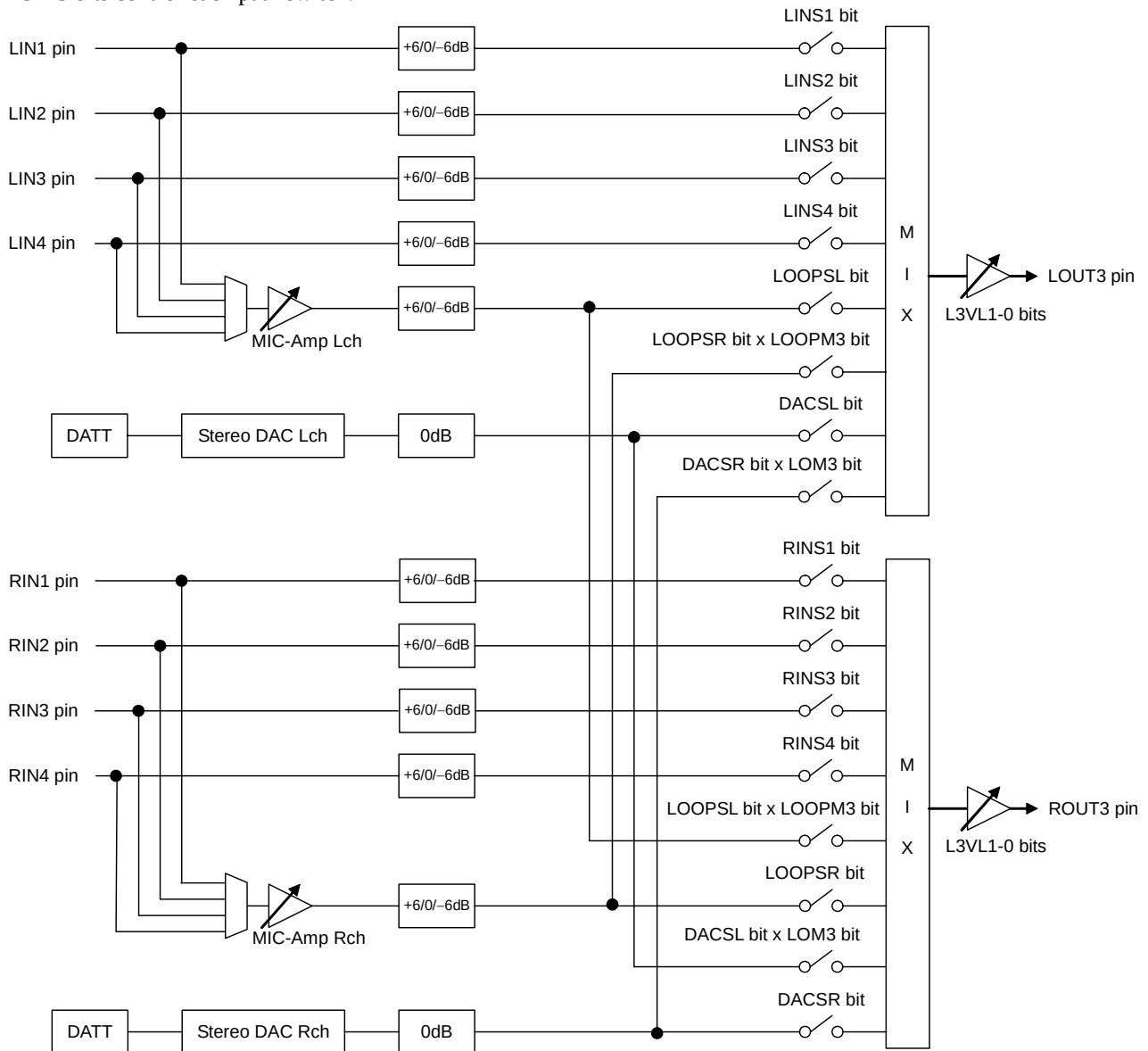


Figure 77. LOUT3/ROUT3 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

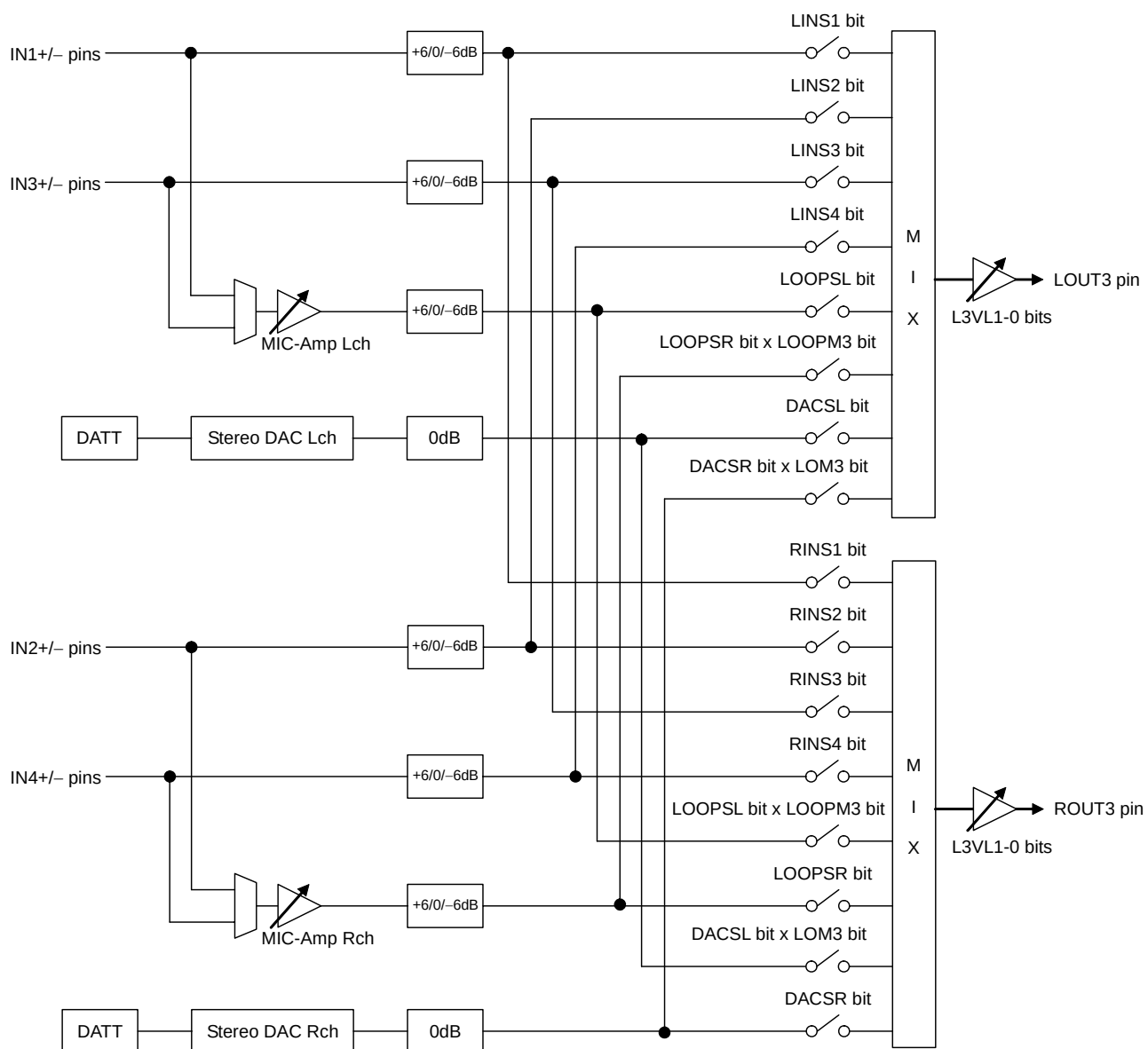


Figure 78. LOUT3/ROUT3 Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "1")

■ Full-differential Mono Line Output (LOP/LON pins)

When LODIF bit = “1”, LOUT3/ROUT3 pins become LOP/LON pins, respectively. Lch/Rch signal of DAC or LIN1/RIN1/LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the LOP/LON pins which is full-differential as (L+R) signal. The load impedance is 10k Ω (min) for LOP and LON pins, respectively. When the PMLO3 = PMRO3 bits = “0”, the mono line output enters power-down mode and the output is pulled-down to VSS1. When the PMLO3 = PMRO3 bits = “1” and LOPS3 bit = “1”, mono line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO3 and PMRO3 bits at LOPS3 bit = “0”. When PMLO3 = PMRO3 bits = “1” and LOPS3 bit = “0”, mono line output enters in normal operation. L3VL1-0 bits set the volume of mono line output.

L3VL1-0	Attenuation
3H	+9dB
2H	+6dB
1H	+3dB
0H	0dB

(default)

Table 74. Mono Line Output Gain Setting

LOPS3	PMLO3/RO3	Mode	LOUT3 pin
0	0	Power-down	Pull-down to VSS1
	1	Normal Operation	Normal Operation
1	0	Power-save	Fall down to VSS1
	1	Power-save	Rise up to VCOM

(default)

Table 75. Mono Line Output Mode Setting

<Full-differential Mono Line Output Control Sequence (in case of using Pop Noise Reduction Circuit)>

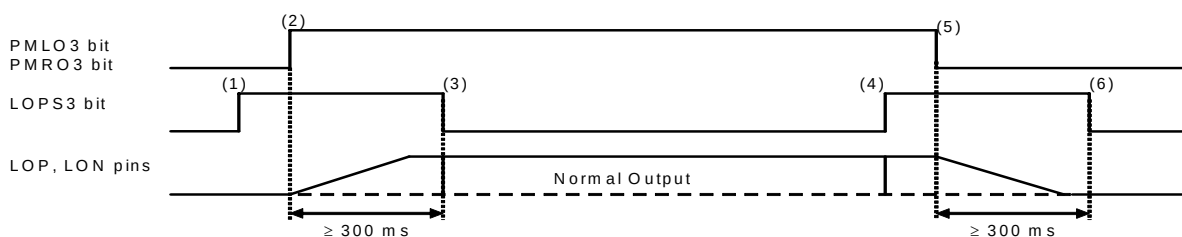


Figure 79. Mono Line Output 3 Control Sequence (in case of using Pop Noise Reduction Circuit)

- (1) Set LOPS3 bit = “1”. Mono line output enters the power-save mode.
- (2) Set PMLO3 = PMRO3 bits = “1”. Mono line output exits the power-down mode.
LOP and LON pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1 μ F and AVDD=3.3V.
- (3) Set LOPS3 bit = “0” after LOP and LON pins rise up. Mono line output exits the power-save mode.
Mono line output is enabled.
- (4) Set LOPS3 bit = “1”. Mono line output enters power-save mode.
- (5) Set PMLO3 = PMRO3 bits = “0”. Mono line output enters power-down mode.
LOP and LON pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1 μ F and AVDD=3.3V.
- (6) Set LOPS3 bit = “0” after LOP and LON pins fall down. Mono line output exits the power-save mode.

<Analog Mixing Circuit for Mono Line Output>

DACSL, DACSR, LINS1, RINS1, LINS2, RINS2, LINS3, RINS3, LINS4, RINS4, LOOPSL and LOOPSR bits control each path switch.

When MDIF1/2/3/4 bits = "1", RINS1/2/3/4 bits should be "0".

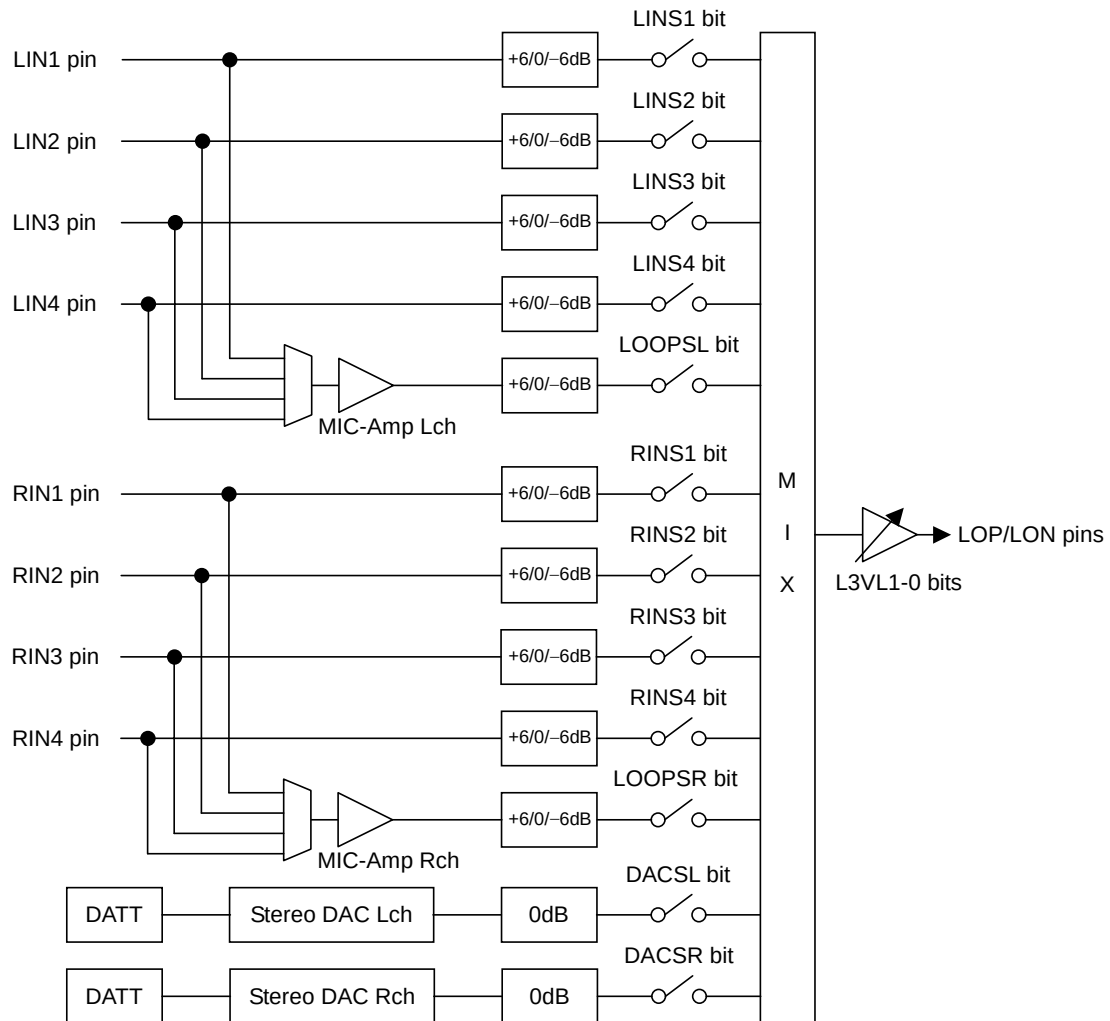


Figure 80. Mono Line Output Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = "0")

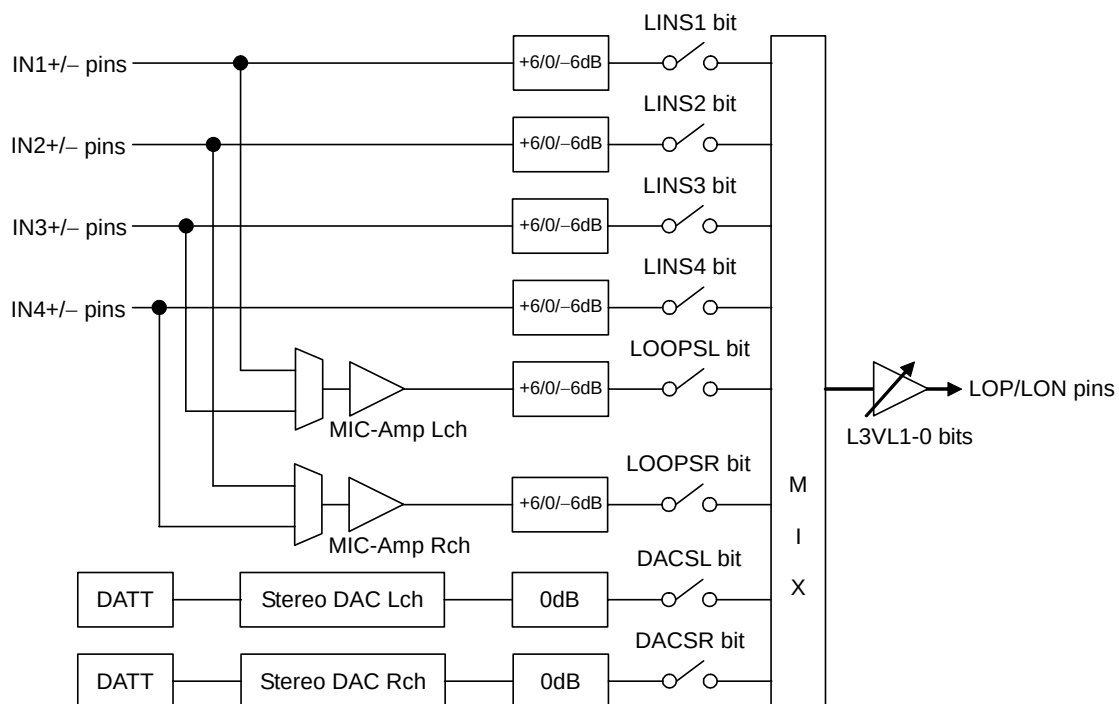


Figure 81. Mono Line Output Mixing Circuit (MDIF1=MDIF2=MDIF3=MDIF4 bits = “1”)

■ System Clock (PCM I/F)

A reference clock of PLLBT is selected among the input clocks to SYNCA, BICKA, SYNCB or BICKB pin. The required clock to PCM I/F is generated by an internal PLLBT circuit. PLLBT circuit is powered up by PMPCM bit. Input frequency is selected by PLLBT3-0 bits (Table 76). BCKO2 bit select the output clock frequency of BICKA or BICKB pin (Table 77). AK4671 does not support master mode for both PCM I/F A and B nor slave mode for both PCM I/F A and B. Whether PCM I/F A or B should be set as slave mode. When PMPCM bit is “0”, SYNCA, BICKA, SYNCB and BICKB pins are Hi-Z. Table 78 indicates the output data of SDTOA and SDTOB pins in case of PMPCM bit = “0” and during lock time in Table 76, respectively. Table 79 indicates the output clock at master mode during lock time in Table 76.

Mode	PLLBT3	PLLBT2	PLLBT1	PLLBT0	Reference Clock Input Pin	Frequency	R, C at VCOCBT pin		Lock Time (max)	(default)
							R	C		
0	0	0	0	0	SYNCA	1fs2	6.8k	220n	260ms	
1	0	0	0	1	BICKA	16fs2	10k	4.7n	40ms	
2	0	0	1	0	BICKA	32fs2	10k	4.7n	40ms	
3	0	0	1	1	BICKA	64fs2	10k	4.7n	40ms	
4	0	1	0	0	SYNCB	1fs2	6.8k	220n	260ms	
5	0	1	0	1	BICKB	16fs2	10k	4.7n	40ms	
6	0	1	1	0	BICKB	32fs2	10k	4.7n	40ms	
7	0	1	1	1	BICKB	64fs2	10k	4.7n	40ms	
11	1	0	1	1	BICKA	48fs2	10k	4.7n	40ms	
15	1	1	1	1	BICKB	48fs2	10k	4.7n	40ms	
Others					N/A					

Table 76. PLLBT Reference Clock (N/A: Not available)

Note 65. Mode 1 is available at only FMTA1 bit = “0”.

Note 66. Mode 5 is available at only FMTB1 bit = “0”.

BCKO2 bit	BICKA/BICKB Output Frequency	(default)
0	16fs2	
1	32fs2	

Table 77. BICKA/B Output Frequency

Mode	PMPCM bit = “0”	After PMPCM bit = “0” → “1” & Before SYNCA/SYNCB Input	PMPCM bit = “1” During Locktime
16bit Linear	L	L	0000H
8bit A-Law	L	H	11010101b
8bit μ -Law	L	H	11111111b

Table 78. SDTOA, SDTOB pins Output Data

Format	SYNCA, SYNCB	BICKA, BICKB
Except for I ² S	L	L
I ² S	H	L

Table 79. Output Clock during Lock Time

a) PLLBT reference clock: SYNCA or BICKA pin

The PLLBT circuit generates the required clock for PCM I/F from SYNCA or BICKA. Generated clocks are output via SYNCB and BICKB pins.

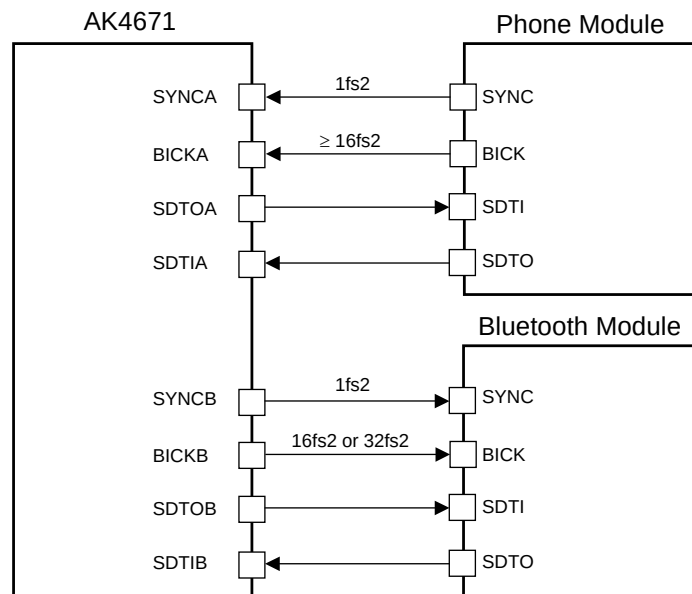


Figure 82. PCM I/F (PLLBT Reference Clock: SYNCA or BICKA pin)

b) PLLBT reference clock: SYNCB or BICKB pin

The PLLBT circuit generates the required clock for PCM I/F from SYNCB or BICKB. Generated clocks are output via SYNCA and BICKA pins.

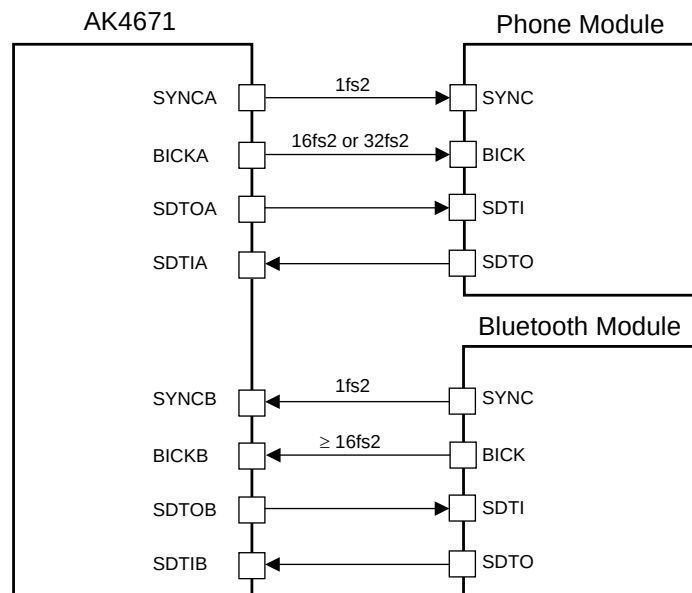


Figure 83. PCM I/F (PLLBT Reference Clock: SYNCB or BICKB pin)

PLLBT should always be powered-up (PMPCM bit = "1") whenever SRC-A or SRC-B is in operation (PMSRA bit = "1" or PMSRB bit = "1"). If PLLBT is powered-down, the AK4671 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If PLLBT is powered-down, SRC-A, SRC-B and SRC-C should be in the power-down mode (PMSRA=PMSRB bits = "0").

■ PCM I/F Master Mode/Slave Mode

The PLLBT2 bit selects either master or slave mode (Table 80). When either PCM I/F A or PCM I/F B is set in slave mode, the other is set in master mode. (For example, when PCM I/F B is set in slave mode, PCM I/F A is set in master mode.) When the AK4671 is power-down mode (PDN pin = “L”) or PMPCM bit = “0”, each clock pins (SYNCA, BICKA, SYNCB, BICKB) of PCM I/F become a Hi-Z (Table 81).

PLLBT3-0 bits should be set when PMPCM bit = “0” to avoid shorting out of the slave mode clock pins and master mode clock output.

After setting the PDN pin = “H”, the PCM I/F clock pins are the Hi-Z state until PMPCM bit becomes “1”. The PCM I/F clock pins of master mode should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

PLLBT2 bit	PCM I/F A	SYNCA, BICKA pins	PCM I/F B	SYNCB, BICKB pins	(default)
0	Slave Mode	Input	Master Mode	Output	
1	Master Mode	Output	Slave Mode	Input	

Table 80. Select PCM I/F Master/Slave Mode

PDN pin	PMPCM bit	SYNCA, BICKA pin	SYNCB, BICKB pin
L	-	Hi-Z	Hi-Z
H	0	Hi-Z	Hi-Z
	1	I/O Select by PLLBT2 bit (Table 80)	I/O Select by PLLBT2 bit (Table 80)

Table 81. PCM I/F Clock I/O State

■ PCM I/F A & B Format

AK4671 supports dual PCM I/F (PCM I/F A & PCM I/F B) that supports 3 kind of I/F (16bit Linear, 8bit A-Law and 8bit μ -Law) independently (Table 82 and Table 83).

Mode	LAWA1	LAWA0	Format	
0	0	0	16bit Linear	(default)
1	0	1	N/A	
2	1	0	8bit A-Law	
3	1	1	8bit μ -Law	

Table 82. PCM I/F A Mode (N/A: Not available)

Mode	LAWB1	LAWB0	Format	
0	0	0	16bit Linear	(default)
1	0	1	N/A	
2	1	0	8bit A-Law	
3	1	1	8bit μ -Law	

Table 83. PCM I/F B Mode (N/A: Not available)

Four types of data formats are available and are selected by setting the FMTA1-0 and FMTB1-0 bits independently (Table 84 and Table 85). In 16bit Linear mode, the serial data is MSB first, 2's complement format. In 8bit A-Law and μ -Law Mode, the serial data is MSB first. PCM I/F formats can be used in both master and slave modes. SYNCA/B and BICKA/B are output from the AK4671 in master mode, but must be input to the AK4671 in slave mode.

Mode	FMTA1	FMTA0	Format	BICKA	Figure	
0	0	0	Short Frame Sync	$\geq 16fs2$	See Table 86	(default)
1	0	1	Long Frame Sync	$\geq 16fs2$	See Table 88	
2	1	0	MSB justified	$\geq 32fs2$	Figure 92	
3	1	1	I ² S	$\geq 32fs2$	Figure 93	

Table 84. PCM I/F A Format

Mode	FMTB1	FMTB0	Format	BICKB	Figure	
0	0	0	Short Frame Sync	$\geq 16fs2$	See Table 87	(default)
1	0	1	Long Frame Sync	$\geq 16fs2$	See Table 89	
2	1	0	MSB justified	$\geq 32fs2$	Figure 92	
3	1	1	I ² S	$\geq 32fs2$	Figure 93	

Table 85. PCM I/F B Format

In modes 2 and 3, the SDTOA/B is clocked out on the falling edge (“↓”) of BICKA/B and the SDTIA/B is latched on the rising edge (“↑”).

In Modes 0 and 1, PCM I/F A timing is changed by BCKPA and MSBSA bits, and PCM I/F B timing is changed by BCKPB and MSBSB bits.

When BCKPA bit = “0”, the SDTOA is clocked out on the rising edge (“↑”) of BICKA and the SDTIA is latched on the falling edge (“↓”). When BCKPA bit = “1”, the SDTOA is clocked out on the falling edge (“↓”) of BICKA and the SDTIA is latched on the rising edge (“↑”).

MSBSA bit can shift the MSB position of SDTOA and SDTIA by half period of BICKA.

When BCKPB bit = “0”, the SDTOB is clocked out on the rising edge (“↑”) of BICKB and the SDTIB is latched on the falling edge (“↓”). When BCKPB bit = “1”, the SDTOB is clocked out on the falling edge (“↓”) of BICKB and the SDTIB is latched on the rising edge (“↑”).

MSBSB bit can shift the MSB position of SDTOB and SDTIB by half period of BICKB.

MSBSA	BCKPA	Data Interface Format	Figure
0	0	MSB of SDTOA is output by next rising edge (“↑”) of the falling edge (“↓”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 84
0	1	MSB of SDTOA is output by next falling edge (“↓”) of the rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 85
1	0	MSB of SDTOA is output by the 2nd rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 86
1	1	MSB of SDTOA is output by the 2nd falling edge (“↓”) of BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 87

Table 86. PCM I/F A Format in Mode 0

MSBSB	BCKPB	Data Interface Format	Figure
0	0	MSB of SDTOB is output by next rising edge (“↑”) of the falling edge (“↓”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 84
0	1	MSB of SDTOB is output by next falling edge (“↓”) of the rising edge (“↑”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 85
1	0	MSB of SDTOB is output by the 2nd rising edge (“↑”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 86
1	1	MSB of SDTOB is output by the 2nd falling edge (“↓”) of BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 87

Table 87. PCM I/F B Format in Mode 0

MSBSA	BCKPA	Data Interface Format	Figure
0	0	MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 88
0	1	MSB of SDTOA is output by the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 89
1	0	MSB of SDTOA is output by the rising edge (“↑”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the falling edge (“↓”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 90
1	1	MSB of SDTOA is output by the falling edge (“↓”) of the first BICKA after the rising edge (“↑”) of SYNCA. MSB of SDTIA is latched by the rising edge (“↑”) of the BICKA just after the output timing of SDTOA’s MSB.	Figure 91

Table 88. PCM I/F A Format in Mode 1

MSBSB	BCKPB	Data Interface Format	Figure
0	0	MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 88
0	1	MSB of SDTOB is output by the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 89
1	0	MSB of SDTOB is output by the rising edge (“↑”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the falling edge (“↓”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 90
1	1	MSB of SDTOB is output by the falling edge (“↓”) of the first BICKB after the rising edge (“↑”) of SYNCB. MSB of SDTIB is latched by the rising edge (“↑”) of the BICKB just after the output timing of SDTOB’s MSB.	Figure 91

Table 89. PCM I/F B Format in Mode 1

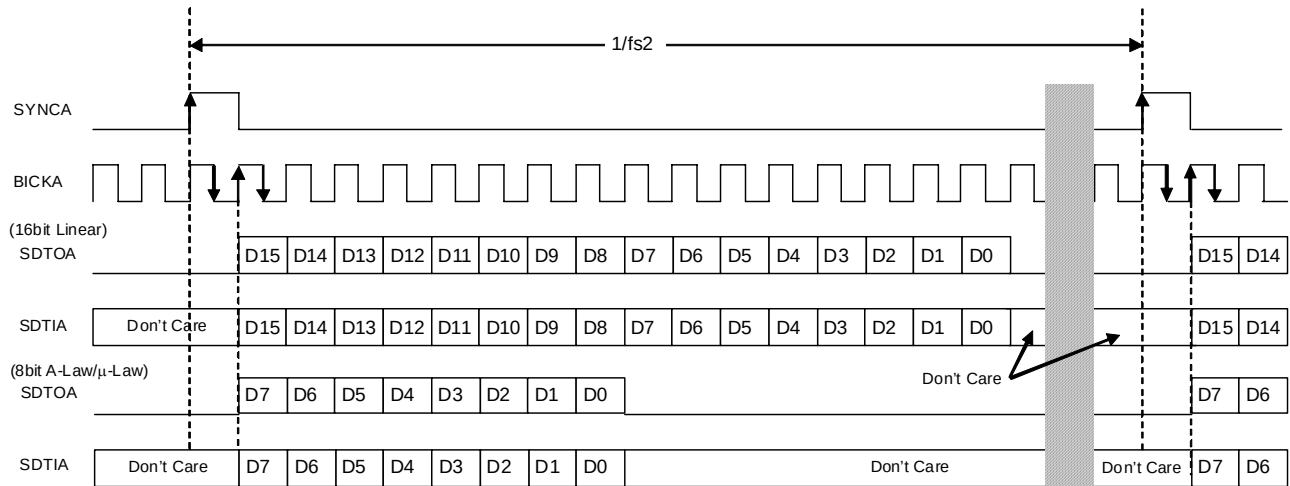


Figure 84. Timing of Short Frame Sync (MSBSA bit = "0", BCKPA bit = "0")

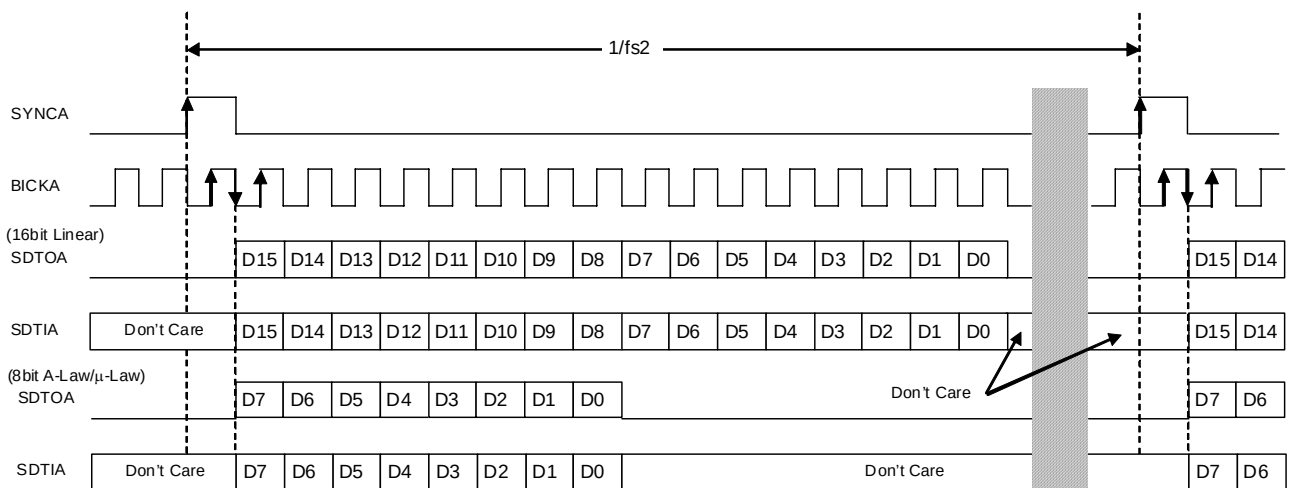


Figure 85. Timing of Short Frame Sync (MSBSA bit = "0", BCKPA bit = "1")

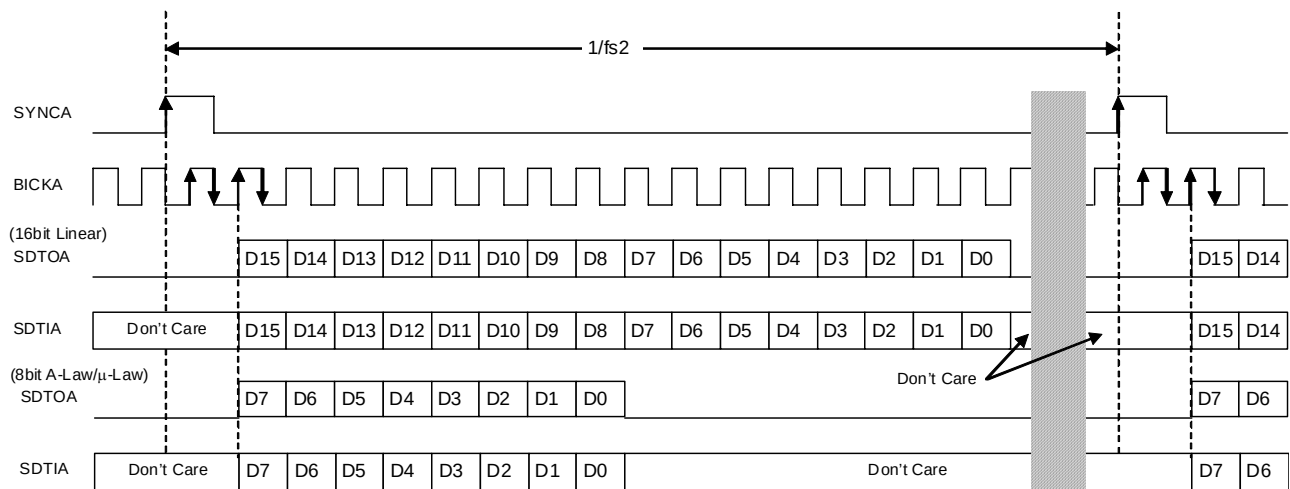


Figure 86. Timing of Short Frame Sync (MSBSA bit = "1", BCKPA bit = "0")

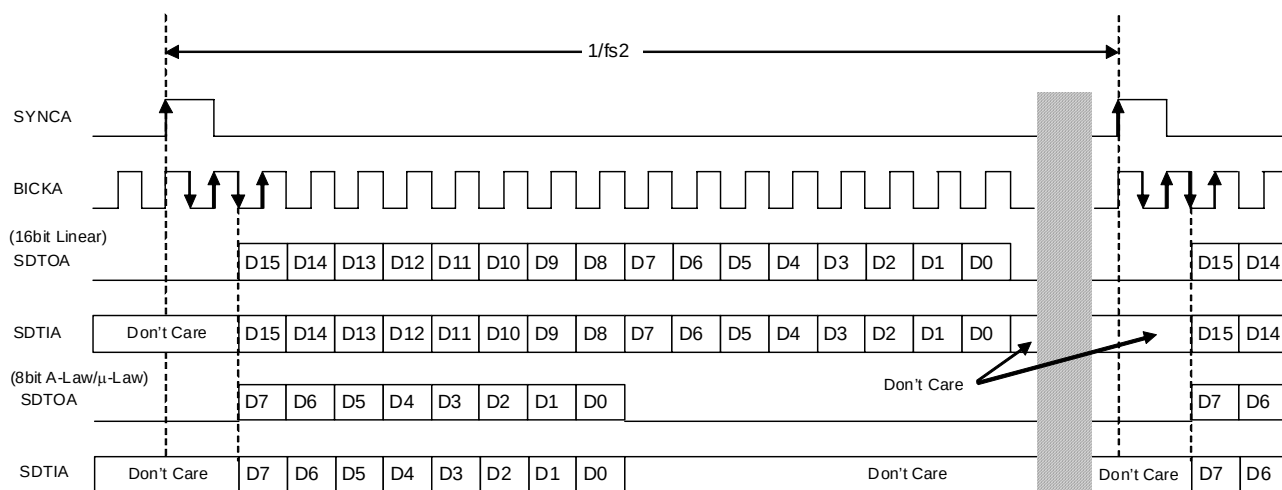


Figure 87. Timing of Short Frame Sync (MSBSA bit = "1", BCKPA bit = "1")

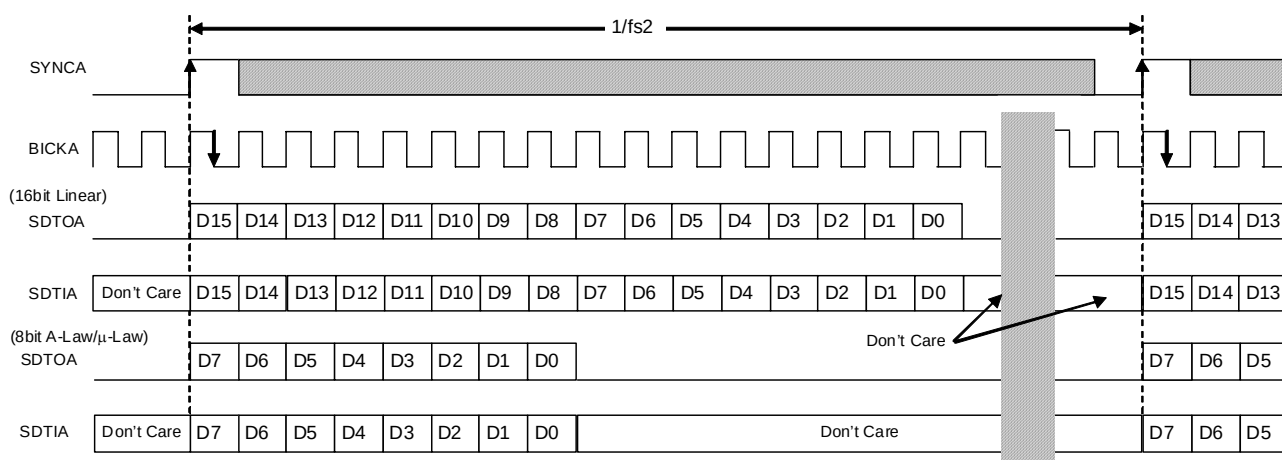


Figure 88. Timing of Long Frame Sync (MSBSA bit = "0", BCKPA bit = "0")

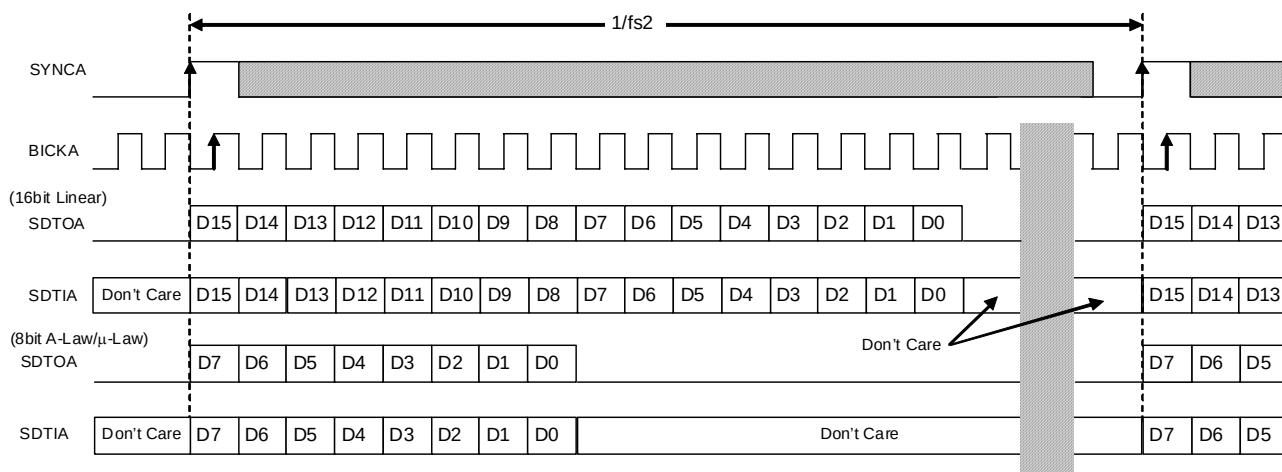


Figure 89. Timing of Long Frame Sync (MSBSA bit = "0", BCKPA bit = "1")

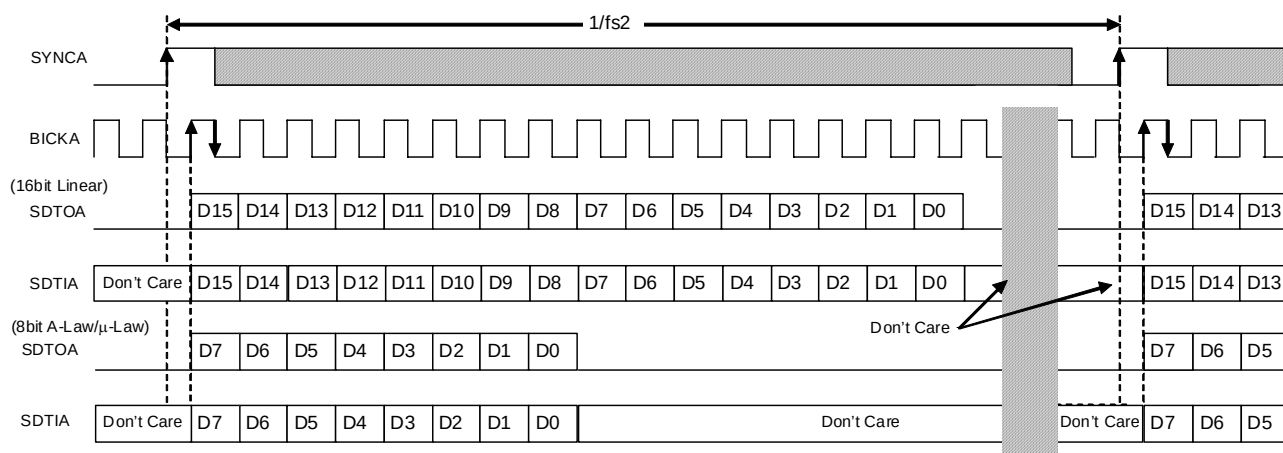


Figure 90. Timing of Long Frame Sync (MSBSA bit = "1", BCKPA bit = "0")

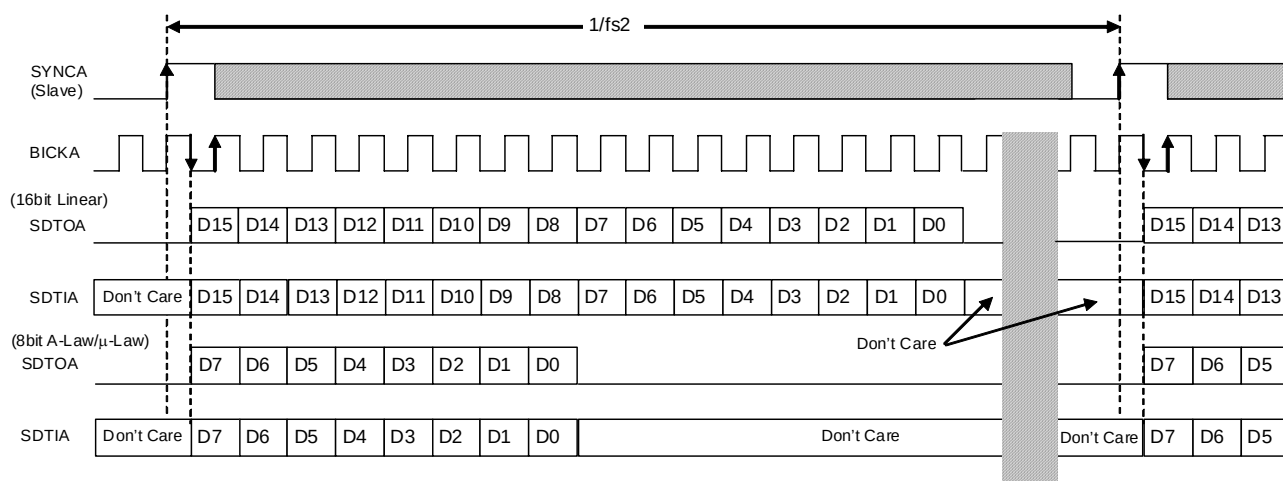


Figure 91. Timing of Long Frame Sync (MSBSA bit = "1", BCKPA bit = "1")

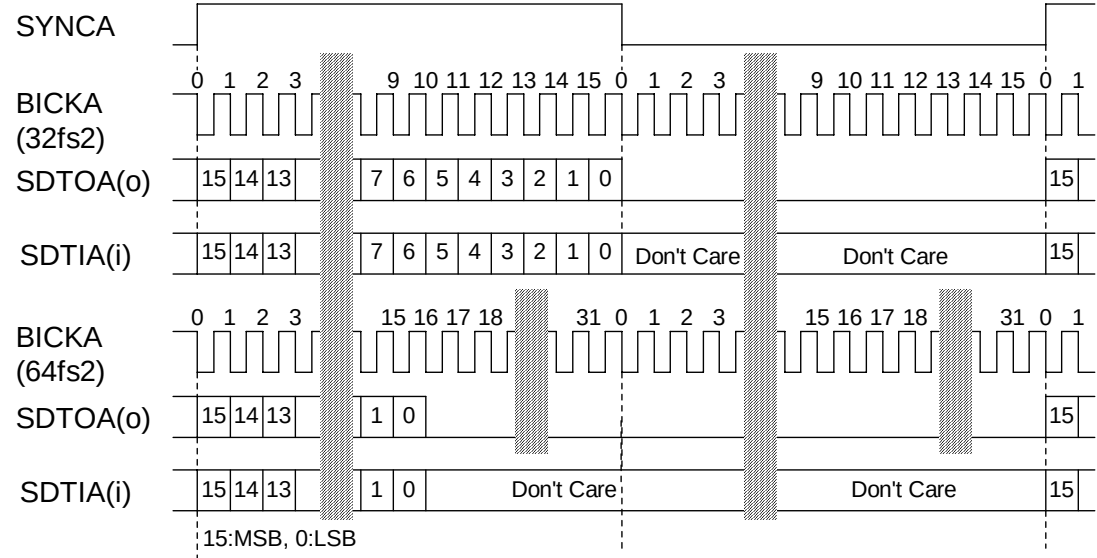


Figure 92. Timing of MSB justified

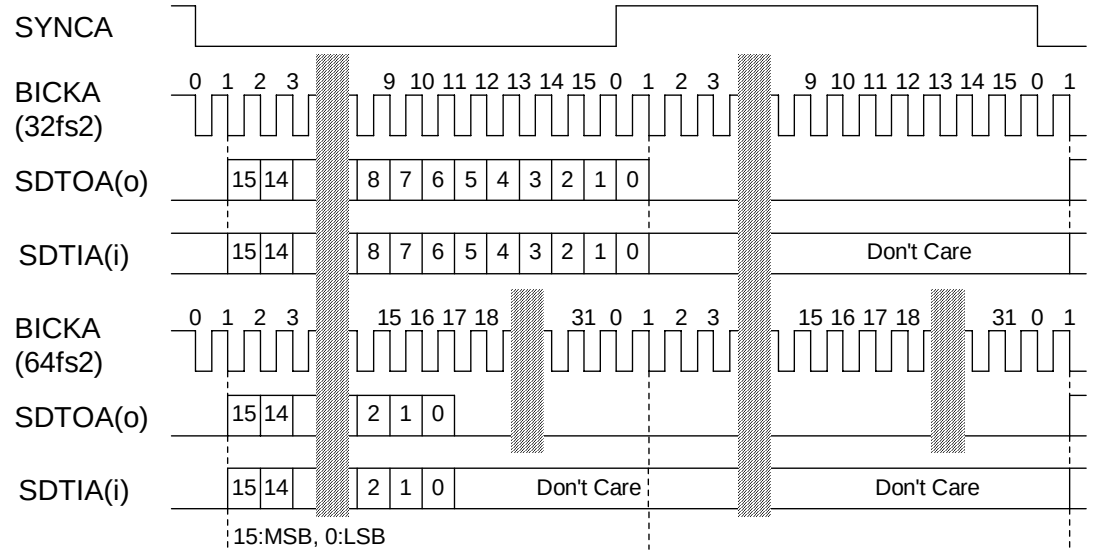


Figure 93. Timing of I²S

■ Phone Path

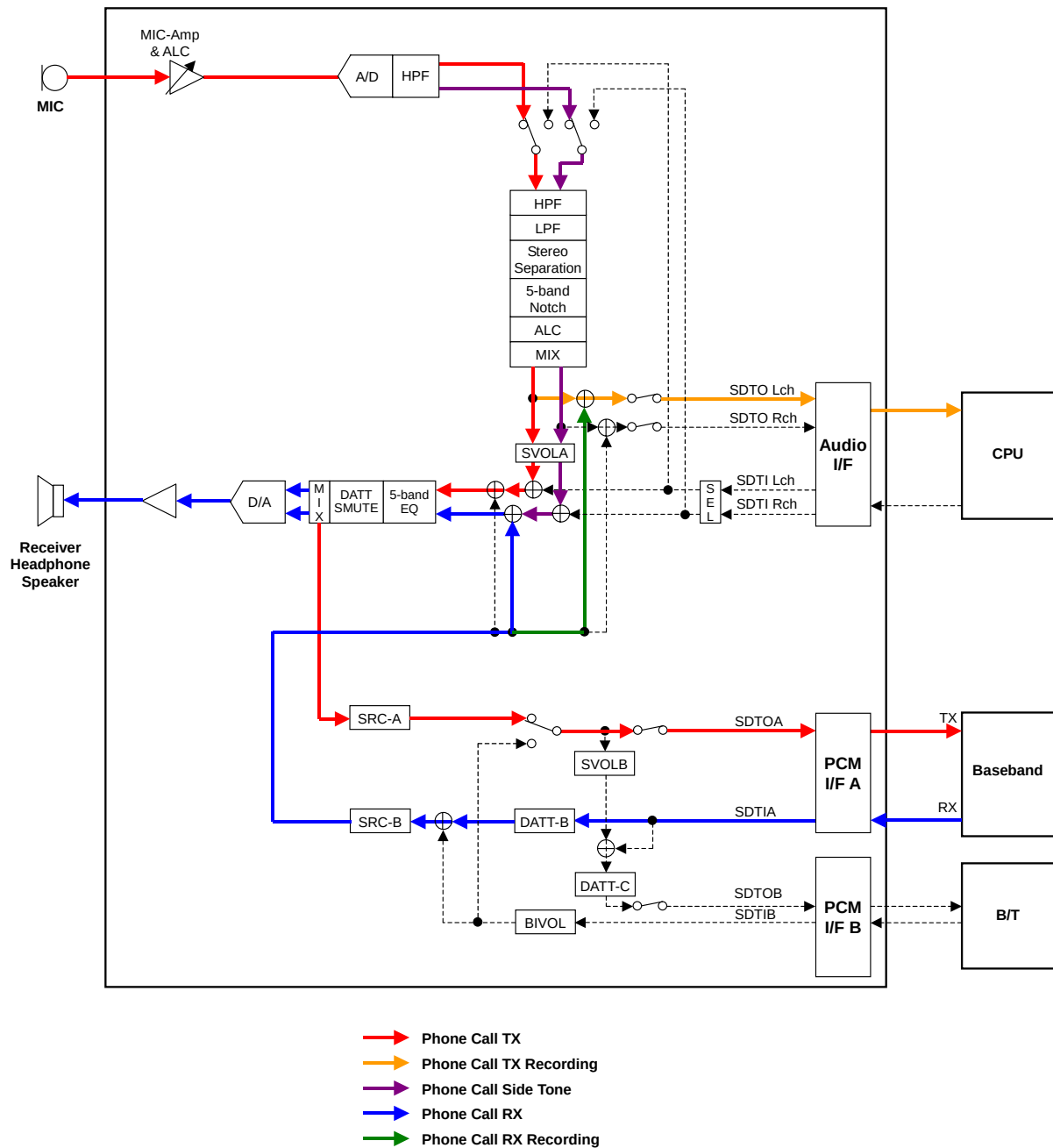


Figure 94. Internal MIC/SPK or External MIC/HP Phone Call & Recoring

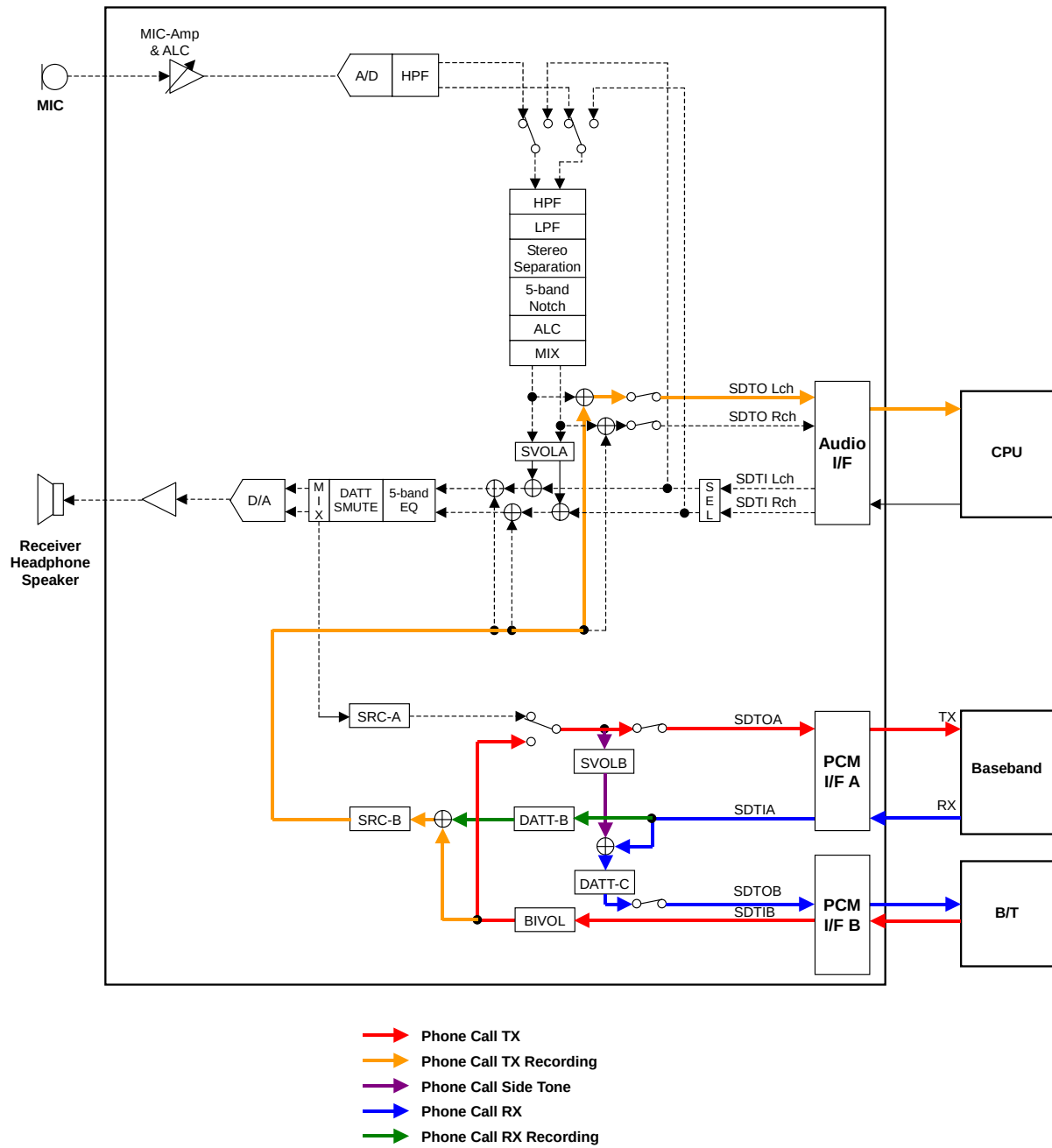


Figure 95. B/T Headset Phone Call & Recording

■ General Purpose Output

AK4671 supports General Purpose Output Pin (GPO) to control the external component.
In the case of GPOM1 bit = “0”, GPO1 pin goes to “H” at GPOE1 bit = “1”.

GPOE1 bit	GPO1 pin	
0	L	(default)
1	H	

Table 90. General Purpose Output 1 Pin Control (at GPOM1 bit = “0”)

In the case of GPOM1 bit = “1”, GPO1 pin goes to “H” if the input level of the channel selected by A0 bit (SAIN1 or SAIN2 pin) is higher than the reference voltage that is input to the SAIN3 pin. In the case of GPOM1 bit = “1”, the reference voltage input to SAIN3 pin should be lower than $0.5 \times \text{SAVDD}$.

SAIN1/2 pin	GPO1 pin	
< SAIN3 pin	L	(default)
$\geq$ SAIN3 pin	H	

Table 91. General Purpose Output 1 Pin Control (at GPOM1 bit = “1”)

In the case of GPOM2 bit = “0”, GPO2 pin goes to “H” at GPOE2 bit = “0”.

GPOE2 bit	GPO2 pin	
0	L	(default)
1	H	

Table 92. General Purpose Output 2 Pin Control (at GPOM2 bit = “0”)

In the case of GPOM2 bit = “1”, GPO2 pin outputs the mic detection result. ([Table 21](#))

Input Level of MDT pin	GPO2 pin	DTMIC bit	Result
$\geq 0.075 \times \text{AVDD}$	H	1	Mic (Headset)
$< 0.050 \times \text{AVDD}$	L	0	No Mic (Headphone)

Table 21. Microphone Detection Result

■ SAR 10bit ADC

The AK4671 incorporates a 10-bit successive approximation resistor A/D converter for DC measurement.

The A/D converter output is a straight binary format as shown in Table 93:

Input Voltage	Output Code
(AVDD–1.5LSB) ~ AVDD	3FFH
(AVDD–2.5LSB) ~ (AVDD–1.5LSB)	3FEH
⋮	⋮
0.5LSB ~ 1.5LSB	001H
0 ~ 0.5LSB	000H

Table 93. Output Code

When PMSAD bit is set to “1”, 10bit ADC is powered-up. When the control register is read, A/D conversion is executed and data is output. In case of 4-wire serial control mode, 10bit A/D data is output from 9th to 18th CCLK clock when 4th bit is set to “1” just after R/W bit.

10bit ADC supports 3 kinds of analog input. A1-0 bits select the measurement modes.

Mode	A1	A0	Input Channel	(default)
0	0	0	SAIN1	
1	0	1	SAIN2	
2	1	0	SAIN3	
3	1	1	N/A	

Table 94. SAR ADC Measurement Mode (N/A: Not available)

<SAR ADC Execute Sequence (in case that the interrupt function is not used.)>

[4-wire Serial Mode]

- (1) Select the measurement mode by A1-0 bits and set PMSAD bit = "1" to power-up SAR ADC.
- (2) Input "1" at the 4th bit just after R/W bit so that A/D conversion is executed and 10bit A/D data is output from 9th to 18th CCLK clock.

[I²C Mode]

- (1) Select the measurement mode by A1-0 bits and set PMSAD bit = "1" to power-up SAR ADC.
- (2) Read Addr=5BH so that A/D conversion is executed and MSB 8bit data is output.
- (3) Continuously read Addr=5CH then LSB 2bit data is output.

<SAR ADC Execute Sequence (in case that the interrupt function is used.)>

[4-wire Serial Mode]

- (1) GPOM1 bit should be set to "1". The GPO1 pin can be used as the interrupt output pin.
- (2) Select the measurement mode by A0 bit.
- (3) The GPO1 pin goes to "H" when the input DC voltage of SAIN1 or SAIN2 pin (selected by A0 bit) is higher than the input voltage of SAIN3 pin.
- (4) After CPU detects GPO1 pin = "H", set GPOM1 bit = "0" and PMSAD bit = "1" to power-up SAR ADC.
- (5) Input "1" at the 4th bit just after R/W bit so that A/D conversion is executed and 10bit A/D data is output from 9th to 18th CCLK clock.

[I²C Mode]

- (1) GPOM1 bit should be set to "1". The GPO1 pin can be used as the interrupt output pin.
- (2) Select the measurement mode by A0 bit.
- (3) The GPO1 pin goes to "H" when the input DC voltage of SAIN1 or SAIN2 pin (selected by A0 bit) is higher than the input voltage of SAIN3 pin.
- (4) After CPU detects GPO1 pin = "H", set GPOM1 bit = "0" and PMSAD bit = "1" to power-up SAR ADC.
- (5) Read Addr=5BH so that A/D conversion is executed and MSB 8bit data is output.
- (6) Continuously read Addr=5CH then LSB 2bit data is output.

Serial Control Interface

(1) 4-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written by using the 4-wire μ P interface pins (CSN, CCLK, CDTI and CDTO).

In case except for 10bit SAR ADC data read, the data on this interface consists of a 3-bit Chip address (fixed to "100"), Read/Write (1bit), Register address (MSB first, 7bits) and Control data (MSB first, 8bits).

In case of 10bit SAR ADC data read, the data on this interface consists of a 3-bit Chip address (fixed to "101"), Read/Write (1bit: fixed to "0") and SAR ADC Data (MSB first, 10bits).

Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. Address and data are latched on the 24th CCLK rising edge ("↑") after CSN falling edge ("↓") for write operations and CDTO bit goes to Hi-Z after CSN rising edge ("↑"). CSN should be set to "H" once after 24th CCLK for each address. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = "L".

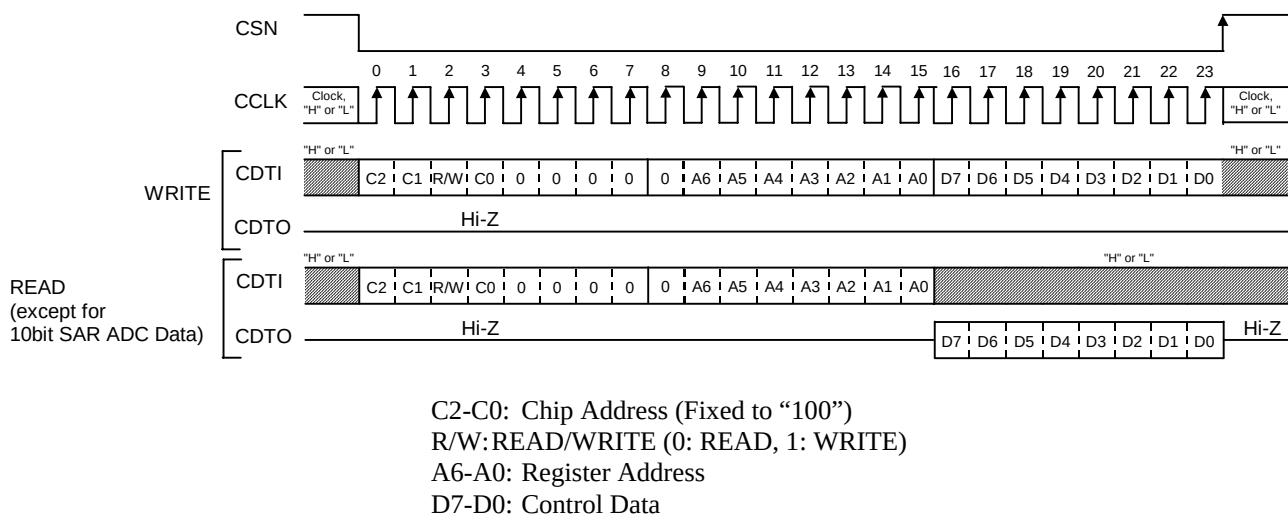


Figure 96. Serial Control I/F Timing (Except for 10bit SAR ADC Data)

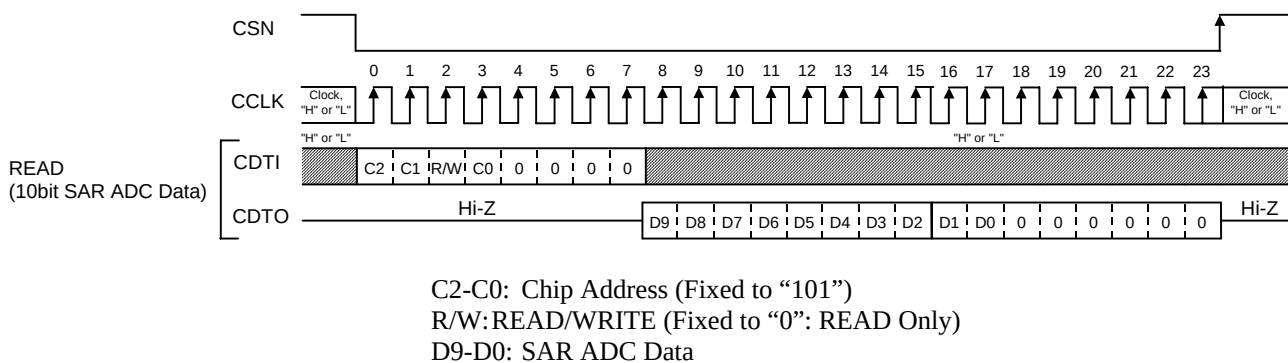


Figure 97. Serial Control I/F Timing (10bit SAR ADC Data)

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4671 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 98 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 105). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 99). If the slave address matches that of the AK4671, the AK4671 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 106). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4671. The format is MSB first, and the most significant 1-bit is fixed to "0" (Figure 100). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 101). The AK4671 generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 105).

The AK4671 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4671 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 5AH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 107) except for the START and STOP conditions.

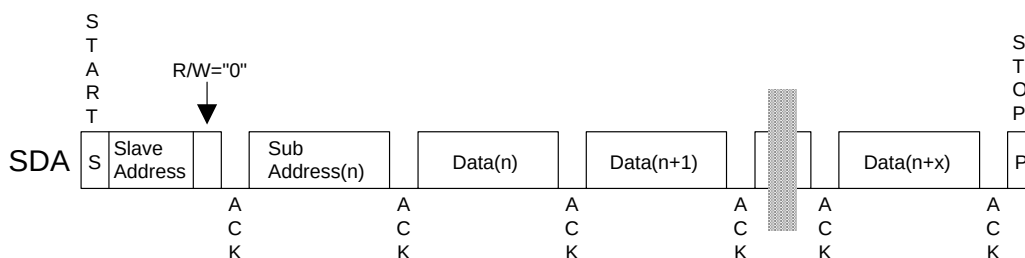


Figure 98. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	1	CAD0	R/W
---	---	---	---	---	---	------	-----

(The CAD0 should match with CAD0 pin.)

Figure 99. The First Byte

0	A6	A5	A4	A3	A2	A1	A0
---	----	----	----	----	----	----	----

Figure 100. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Figure 101. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4671. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 7-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 5AH prior to generating a stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4671 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ (except for 10bit SAR ADC Data)

The AK4671 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4671 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4671 ceases transmission.

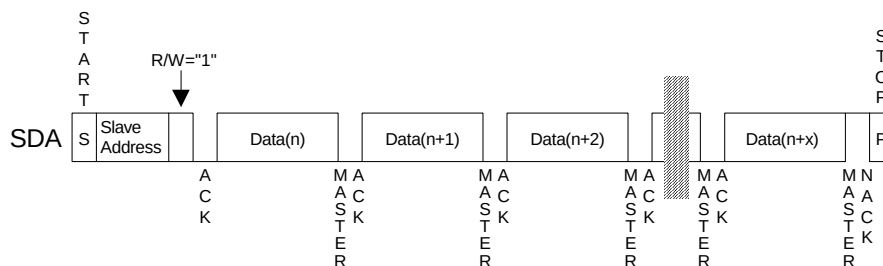


Figure 102. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4671 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4671 ceases transmission.

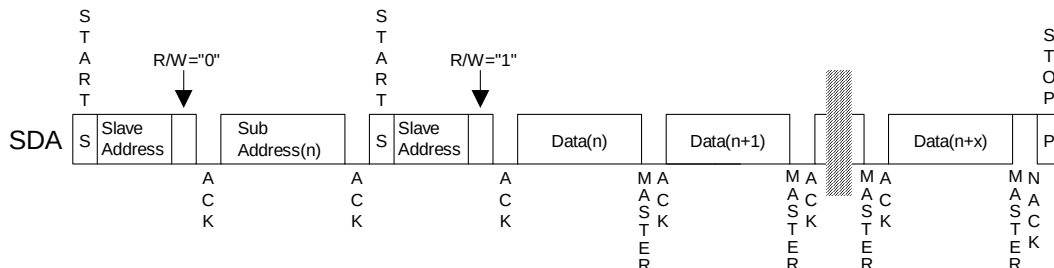


Figure 103. RANDOM ADDRESS READ (Except for 10bit SAR ADC Data)

When SAR ADC data is read, 5BH should be set as register address and 2 byte data should be read by RANDOM ADDRESS READ, then stop condition should be input. A/D readout format is MSB first, 2 byte width. Upper 10bits are valid on 2byte (16-bit), and lower 6bits are filled with zero.

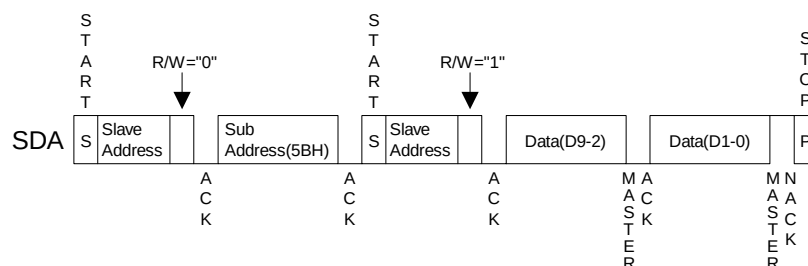


Figure 104. RANDOM ADDRESS READ (10bit SAR ADC Data)

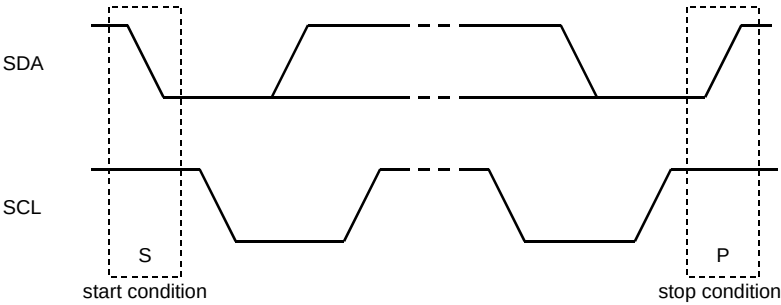


Figure 105. START and STOP Conditions

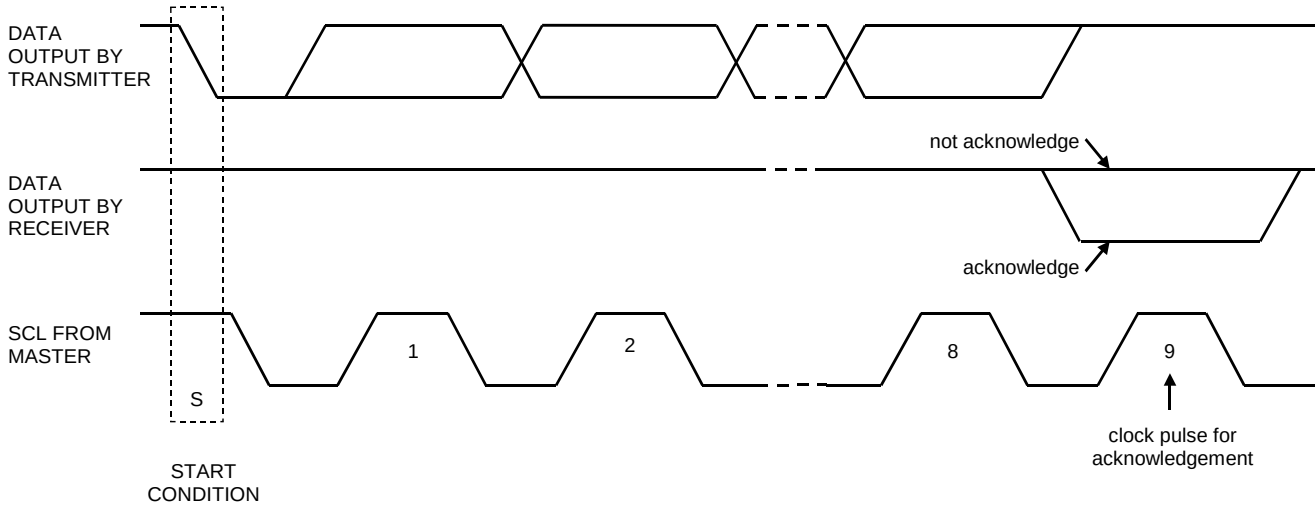


Figure 106. Acknowledge on the I²C-Bus

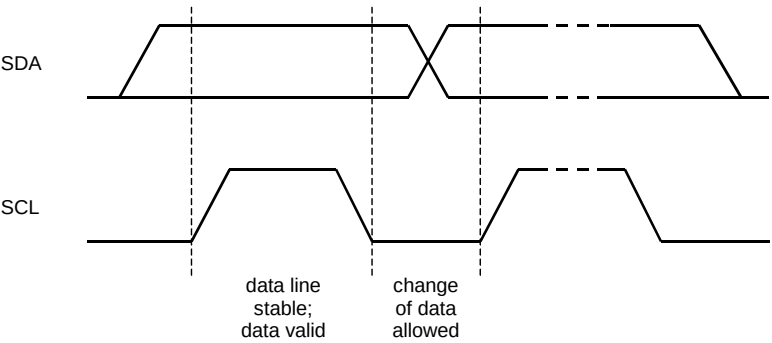


Figure 107. Bit Transfer on the I²C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	AD/DA Power Management	PMDAR	PMDAL	PMADR	PMADL	PMMICR	PMMICL	PMMP	PMVCM
01H	PLL Mode Select 0	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	PLL Mode Select 1	BTCLK	LP	BCKO	PS1	PS0	MCKO	M/S	PMPLL
03H	Format Select	0	0	0	SDOD	MSBS	BCKP	DIF1	DIF0
04H	MIC Signal Select	MDIF4	MDIF3	MDIF2	MDIF1	INR1	INR0	INL1	INL0
05H	MIC Amp Gain	MGNR3	MGNR2	MGNR1	MGNR0	MGNL3	MGNL2	MGNL1	MGNL0
06H	Mixing Power Management 0	0	0	0	0	0	DTMIC	PMLOOPR	PMLOOPL
07H	Mixing Power Management	PMMAINR4	PMMAINL4	PMMAINR3	PMMAINL3	PMMAINR2	PMMAINL2	PMMAINR1	PMMAINL1
08H	Output Volume Control	HPG3	HPG2	HPG1	HPG0	0	L1VL2	L1VL1	L1VL0
09H	LOUT1 Signal Select	L1G1	L1G0	LOOPL	LINL4	LINL3	LINL2	LINL1	DACL
0AH	ROUT1 Signal Select	L2G1	L2G0	LOOPR	RINR4	RINR3	RINR2	RINR1	DACR
0BH	LOUT2 Signal Select	L3G1	L3G0	LOOPL	LINH4	LINH3	LINH2	LINH1	DACHL
0CH	ROUT2 Signal Select	L4G1	L4G0	LOOPHR	RINH4	RINH3	RINH2	RINH1	DACHR
0DH	LOUT3 Signal Select	LPG1	LPG0	LOOPSL	LINS4	LINS3	LINS2	LINS1	DACSL
0EH	ROUT3 Signal Select	0	0	LOOPSR	RINS4	RINS3	RINS2	RINS1	DACSR
0FH	LOUT1 Power Management	0	0	RCV	LOOPM	LOM	LOPS1	PMRO1	PMLO1
10H	LOUT2 Power Management	0	PMRO2S	PMLO2S	LOOPM2	LOM2	MUTEN	PMRO2	PMLO2
11H	LOUT3 Power Management	L3VL1	L3VL0	LODIF	LOOPM3	LOM3	LOPS3	PMRO3	PMLO3
12H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
13H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
14H	ALC Reference Select	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
15H	Digital Mixing Control	SRMXR1	SRMXR0	SRMXL1	SRMXL0	PFMXR1	PFMXR0	PFMXL1	PFMXL0
16H	ALC Timer Select	0	RFST1	RFST0	WTM2	WTM1	WTM0	ZTM1	ZTM0
17H	ALC Mode Control	0	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
18H	Mode Control 1	DAM	MIXD	SDIM1	SDIM0	EQ	ADM	IVOLC	ALC
19H	Mode Control 2	SRA1	SRA0	BIV2	BIV1	BIV0	SMUTE	OVTM	OVOLC
1AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
1BH	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
1CH	Side Tone A Control	0	0	SVAR2	SVAR1	SVAR0	SVAL2	SVAL1	SVAL0
1DH	Digital Filter Select	GN1	GN0	LPF	HPF	EQ0	FIL3	0	PFSEL
1EH	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
1FH	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
20H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
21H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
22H	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
23H	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
24H	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
25H	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
26H	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
27H	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
28H	FIL1 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
29H	FIL1 Co-efficient 1	F1AS	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
2AH	FIL1 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
2BH	FIL1 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
2CH	FIL2 Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	FIL2 Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	FIL2 Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	FIL2 Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
50H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
51H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
52H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
53H	PCM I/F Control 0	GPOM2	GPOE2	PLLBT2	PLLBT1	PLLBT0	PMPCM	PMSRB	PMSRA
54H	PCM I/F Control 1	SDOAD	BCKO2	MSBSA	BCKPA	LAWA1	LAWA0	FMTA1	FMTA0
55H	PCM I/F Control 2	SDOBD	PLLBT3	MSBSB	BCKPB	LAWB1	LAWB0	FMTB1	FMTB0
56H	Digital Volume B Control	BVL7	BVL6	BVL5	BVL4	BVL3	BVL2	BVL1	BVL0
57H	Digital Volume C Control	CVL7	CVL6	CVL5	CVL4	CVL3	CVL2	CVL1	CVL0
58H	Side Tone Volume Control	0	0	0	0	SDOA	SVB2	SVB1	SVB0
59H	Digital Mixing Control	SDOR1	SDOR0	SDOL1	SDOL0	BVMX1	BVMX0	SBMX1	SBMX0
5AH	SAR ADC Control	0	0	0	GPOM1	GPOE1	A1	A0	PMSAD

Note 67. PDN pin = “L” resets the registers to their default values.

Note 68. The bits defined as 0 must contain a “0” value.

Note 69. Addresses 1EH to 2FH and 32H to 4FH cannot be read.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	AD/DA Power Management	PMDAR	PMDAL	PMADR	PMADL	PMMICR	PMMICL	PMMP	PMVCM
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	(default)	0	0	0	0	0	0	0	0

PMVCM: VCOM Power Management

0: Power down (default)

1: Power up

When any blocks are powered-up, the PMVCM bit must be set to “1”. PMVCM bit can be set to “0” only when all power management bits are “0”.

PMMP: MPWR pin Power Management

0: Power down: Hi-Z (default)

1: Power up

PMMICL: MIC-Amp Lch Power Management

0: Power down (default)

1: Power up

PMMICR: MIC-Amp Rch Power Management

0: Power down (default)

1: Power up

PMADL: ADC Lch Power Management

0: Power down (default)

1: Power up

When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle (1059/fs=24ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMADR: ADC Rch Power Management

0: Power down (default)

1: Power up

PMDAL: DAC Lch Power Management

0: Power down (default)

1: Power up

PMDAR: DAC Rch Power Management

0: Power down (default)

1: Power up

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDN pin is “L”, all blocks are powered-down regardless of setting of this address. In this case, register is initialized to the default value.

When all power management bits are “0”, all blocks are powered-down. The register values remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin should be “L”.

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Mode Select 0	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	0	1	1	0

PLL3-0: PLL Reference Clock Select ([Table 4](#))

Default: “0110”(MCKI pin, 12MHz)

FS3-0: Sampling Frequency Select ([Table 5](#) and [Table 6](#)) and MCKI Frequency Select ([Table 11](#))

FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	PLL Mode Select 1	BTCLK	LP	BCKO	PS1	PS0	MCKO	M/S	PMPLL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management

0: EXT Mode and Power Down (default)

1: PLL Mode and Power up

M/S: Master / Slave Mode Select

0: Slave Mode (default)

1: Master Mode

MCKO: Master Clock Output Enable

0: Disable: MCKO pin = “L” (default)

1: Enable: Output frequency is selected by PS1-0 bits.

PS1-0: MCKO Output Frequency Select ([Table 9](#))

default: “00”(256fs)

BCKO: BICK Output Frequency Select at Master Mode ([Table 10](#))

LP: Low Power Mode

0: Normal Mode (default)

1: Low Power Mode: available at fs=22.05kHz or less.

BTCLK: Clock Mode of Audio CODEC

0: Synchronized to Audio I/F (default)

1: Synchronized to PCM I/F

BTCLK bit is enabled at only PMPLL bit = “0”. When BTCLK bit is “1”, Audio CODEC and the digital block (shown in [Figure 57](#)) operate by the clock generated by PLLBT.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Format Select	0	0	0	SDOD	MSBS	BCKP	DIF1	DIF0
	R/W	RD	RD	RD	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format ([Table 16](#))

Default: “10” (Left justified)

BCKP: BICK Polarity at DSP Mode ([Table 17](#))

“0”: SDTO is output by the rising edge (“↑”) of BICK and SDTI is latched by the falling edge (“↓”). (default)

“1”: SDTO is output by the falling edge (“↓”) of BICK and SDTI is latched by the rising edge (“↑”).

MSBS: LRCK Phase at DSP Mode ([Table 17](#))

“0”: The rising edge (“↑”) of LRCK is half clock of BICK before the channel change. (default)

“1”: The rising edge (“↑”) of LRCK is one clock of BICK before the channel change.

SDOD: SDTO Disable ([Table 47](#))

“0”: Enable (default)

“1”: Disable (“L”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	MIC Signal Select	MDIF4	MDIF3	MDIF2	MDIF1	INR1	INR0	INL1	INL0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

INL1-0: MIC-Amp Lch Input Source Select ([Table 18](#))

Default: “00” (LIN1)

INR1-0: MIC-Amp Rch Input Source Select ([Table 18](#))

Default: “00” (RIN1)

MDIF1: Line1 Input Type Select

0: Single-ended input (LIN1/RIN1 pins: default)

1: Full-differential input (IN1+/IN1– pins)

MDIF2: Line2 Input Type Select

0: Single-ended input (LIN2/RIN2 pins: default)

1: Full-differential input (IN2+/IN2– pins)

MDIF3: Line3 Input Type Select

0: Single-ended input (LIN3/RIN3 pins: default)

1: Full-differential input (IN3+/IN3– pins)

MDIF4: Line4 Input Type Select

0: Single-ended input (LIN4/RIN4 pins: default)

1: Full-differential input (IN4+/IN4– pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	MIC Amp Gain	MGNR3	MGNR2	MGNR1	MGNR0	MGNL3	MGNL2	MGNL1	MGNL0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	1	0	1	0	1	0	1

MGNL3-0: MIC-Amp Lch Gain Control ([Table 19](#))

Default: “0101” (0dB)

MGNR3-0: MIC-Amp Rch Gain Control ([Table 19](#))

Default: “0101” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mixing Power Management 0	0	0	0	0	0	DTMIC	PMLOOPR	PMLOOPL
	R/W	RD	RD	RD	RD	RD	RD	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMLOOPL: MIC-Amp Lch Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMLOOPR: MIC-Amp Rch Mixing Circuit Power Management

0: Power down (default)

1: Power up

DTMIC: Microphone Detection Result (Read Only: [Table 21](#))

0: Microphone is not detected. (default)

1: Microphone is detected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mixing Power Management 1	PMAINR4	PMAINL4	PMAINR3	PMAINL3	PMAINR2	PMAINL2	PMAINR1	PMAINL1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMAINL1: LIN1 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR1: RIN1 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINL2: LIN2 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR2: RIN2 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINL3: LIN3 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR3: RIN3 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINL4: LIN4 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR4: RIN4 Mixing Circuit Power Management

0: Power down (default)

1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Output Volume Control	HPG3	HPG2	HPG1	HPG0	0	L1VL2	L1VL1	L1VL0
	R/W	R/W	R/W	R/W	R/W	RD	R/W	R/W	R/W
	Default	1	0	1	1	0	1	0	1

L1VL2-0: LOUT1/ROUT1 Output Volume Control ([Table 67](#))

Default: "5H" (0dB)

HPG3-0: LOUT2/ROUT2 Output Volume Control ([Table 70](#))

Default: "BH" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	LOUT1 Signal Select	L1G1	L1G0	LOOPL	LINL4	LINL3	LINL2	LINL1	DACL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACL: Switch Control from DAC Lch to LOUT1

0: OFF (default)

1: ON

When PMLO1 bit is “1”, DACL bit is enabled. When PMLO1 bit is “0”, the LOUT1 pin goes to VSS1.

LINL1: Switch Control from LIN1 to LOUT1

0: OFF (default)

1: ON

LINL2: Switch Control from LIN2 to LOUT1

0: OFF (default)

1: ON

LINL3: Switch Control from LIN3 to LOUT1

0: OFF (default)

1: ON

LINL4: Switch Control from LIN4 to LOUT1

0: OFF (default)

1: ON

LOOPL: Switch Control from MIC-Amp Lch to LOUT1

0: OFF (default)

1: ON

L1G1-0: LIN1/RIN1 Mixing Gain Control ([Table 60](#))

Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ROUT1 Signal Select	L2G1	L2G0	LOOPR	RINR4	RINR3	RINR2	RINR1	DACR
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACR: Switch Control from DAC Rch to ROUT1

0: OFF (default)

1: ON

When PMRO1 bit is “1”, DACR bit is enabled. When PMRO1 bit is “0”, the ROUT1 pin goes to VSS1.

RINR1: Switch Control from RIN1 to ROUT1

0: OFF (default)

1: ON

RINR2: Switch Control from RIN2 to ROUT1

0: OFF (default)

1: ON

RINR3: Switch Control from RIN3 to ROUT1

0: OFF (default)

1: ON

RINR4: Switch Control from RIN4 to ROUT1

0: OFF (default)

1: ON

LOOPR: Switch Control from MIC-Amp Rch to ROUT1

0: OFF (default)

1: ON

L2G1-0: LIN2/RIN2 Mixing Gain Control ([Table 61](#))

Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	LOUT2 Signal Select	L3G1	L3G0	LOOPHL	LINH4	LINH3	LINH2	LINH1	DACHL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACHL: Switch Control from DAC Lch to LOUT2

0: OFF (default)

1: ON

LINH1: Switch Control from LIN1 to LOUT2

0: OFF (default)

1: ON

LINH2: Switch Control from LIN2 to LOUT2

0: OFF (default)

1: ON

LINH3: Switch Control from LIN3 to LOUT2

0: OFF (default)

1: ON

LINH4: Switch Control from LIN4 to LOUT2

0: OFF (default)

1: ON

LOOPHL: Switch Control from MIC-Amp Lch to LOUT2

0: OFF (default)

1: ON

L3G1-0: LIN3/RIN3 Mixing Gain Control ([Table 62](#))

Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ROUT2 Signal Select	L4G1	L4G0	LOOPHR	RINH4	RINH3	RINH2	RINH1	DACHR
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACHR: Switch Control from DAC Rch to ROUT2

0: OFF (default)

1: ON

RINH1: Switch Control from RIN1 to ROUT2

0: OFF (default)

1: ON

RINH2: Switch Control from RIN2 to ROUT2

0: OFF (default)

1: ON

RINH3: Switch Control from RIN3 to ROUT2

0: OFF (default)

1: ON

RINH4: Switch Control from RIN4 to ROUT2

0: OFF (default)

1: ON

LOOPHR: Switch Control from MIC-Amp Rch to ROUT2

0: OFF (default)

1: ON

L4G1-0: LIN4/RIN4 Mixing Gain Control ([Table 63](#))

Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	LOUT3 Signal Select	LPG1	LPG0	LOOPSL	LINS4	LINS3	LINS2	LINS1	DACSL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACSL: Switch Control from DAC Lch to LOUT3

0: OFF (default)

1: ON

When PMLO3 bit is “1”, DACSL bit is enabled. When PMLO3 bit is “0”, the LOUT3 pin goes to VSS1.

LINS1: Switch Control from LIN1 to LOUT3

0: OFF (default)

1: ON

LINS2: Switch Control from LIN2 to LOUT3

0: OFF (default)

1: ON

LINS3: Switch Control from LIN3 to LOUT3

0: OFF (default)

1: ON

LINS4: Switch Control from LIN4 to LOUT3

0: OFF (default)

1: ON

LOOPSL: Switch Control from MIC-Amp Lch to LOUT3

0: OFF (default)

1: ON

LPG1-0: MIC-Amp Mixing Gain Control ([Table 64](#))

Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ROUT3 Signal Select	0	0	LOOPSR	RINS4	RINS3	RINS2	RINS1	DACSR
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DACSR: Switch Control from DAC Rch to ROUT3

0: OFF (default)

1: ON

When PMRO3 bit is “1”, DACR bit is enabled. When PMRO3 bit is “0”, the ROUT3 pin goes to VSS1.

RINS1: Switch Control from RIN1 to ROUT3

0: OFF (default)

1: ON

RINS2: Switch Control from RIN2 to ROUT3

0: OFF (default)

1: ON

RINS3: Switch Control from RIN3 to ROUT3

0: OFF (default)

1: ON

RINS4: Switch Control from RIN4 to ROUT3

0: OFF (default)

1: ON

LOOPSR: Switch Control from MIC-Amp Rch to ROUT3

0: OFF (default)

1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	LOUT1 Power Management	0	0	RCV	LOOPM	LOM	LOPS1	PMRO1	PMLO1
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMLO1: LOUT1 Power Management

0: Power down (default)

1: Power up

PMRO1: ROUT1 Power Management

0: Power down (default)

1: Power up

LOPS1: LOUT1/ROUT1 Power Save Mode

0: Normal Operation (default)

1: Power Save Mode

LOM: Mono Mixing from DAC to LOUT1/ROUT1

0: Stereo Mixing (default)

1: Mono Mixing

LOOPM: Mono Mixing from MIC-Amp to LOUT1/ROUT1

0: Stereo Mixing (default)

1: Mono Mixing

RCV: Receiver Select

0: Stereo Line Output (LOUT1/ROUT1 pins) (default)

1: Mono Receiver Output (RCP/RCN pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	LOUT2 Power Management	0	PMRO2S	PMLO2S	LOOPM2	LOM2	MUTEN	PMRO2	PMLO2
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMLO2: LOUT2 Power Management

0: Power down (default)

1: Power up

PMRO2: ROUT2 Power Management

0: Power down (default)

1: Power up

MUTEN: LOUT2/ROUT2 Mute Control

0: Mute (default)

1: Normal operation

LOM2: Mono Mixing from DAC to LOUT2/ROUT2

0: Stereo Mixing (default)

1: Mono Mixing

LOOPM2: Mono Mixing from MIC-Amp to LOUT2/ROUT2

0: Stereo Mixing (default)

1: Mono Mixing

PMLO2S: LOUT2 MIX-Amp Power Management

0: Power down (default)

1: Power up

PMRO2S: ROUT2 MIX-Amp Power Management

0: Power down (default)

1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	LOUT3 Power Management	L3VL1	L3VL0	LODIF	LOOPM3	LOM3	LOPS3	PMRO3	PMLO3
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	1	0	0	0	0	0	0	0

PMLO3: LOUT3 Power Management

0: Power down (default)

1: Power up

PMRO3: ROUT3 Power Management

0: Power down (default)

1: Power up

LOPS3: LOUT3/ROUT3 Power Save Mode

0: Normal Operation (default)

1: Power Save Mode

LOM3: Mono Mixing from DAC to LOUT3/ROUT3

0: Stereo Mixing (default)

1: Mono Mixing

LOOPM3: Mono Mixing from MIC-Amp to LOUT3/ROUT3

0: Stereo Mixing (default)

1: Mono Mixing

LODIF: Lineout Select

0: Single-ended Stereo Line Output (LOUT3/ROUT3 pins) (default)

1: Full-differential Mono Line Output (LOP/LON pins)

L3VL1-0: LOUT3/ROUT3 Output Gain Control ([Table 73](#))

Default: “10” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
13H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level ([Table 33](#))

Default: “91H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	ALC Reference Select	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation (Recording); 0.375dB step, 242 Level ([Table 29](#))

Default: “E1H” (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	Digital Mixing Control	SRMXR1	SRMXR0	SRMXL1	SRMXL0	PFMXR1	PFMXR0	PFMXL1	PFMXL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PFMXL1-0: 5-band EQ Lch Input Mixing 1 ([Table 49](#))

Default: “00” (SDTI)

PFMXR1-0: 5-band EQ Rch Input Mixing 1 ([Table 50](#))

Default: “00” (SDTI)

SRMXL1-0: 5-band EQ Lch Input Mixing 2 ([Table 51](#))

Default: “00” (SDTI)

SRMXR1-0: 5-band EQ Rch Input Mixing 2 ([Table 52](#))

Default: “00” (SDTI)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	ALC Timer Select	0	RFST1	RFST0	WTM2	WTM1	WTM0	ZTM1	ZTM0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period ([Table 26](#))

Default: “00” (128/fs)

WTM2-0: ALC Recovery Waiting Period ([Table 27](#))

Default: “000” (128/fs)

RFST1-0: ALC First recovery Speed ([Table 30](#))

Default: “00” (4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	ALC Mode Control	0	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level ([Table 24](#))

Default: “00”

RGAIN1-0: ALC Recovery GAIN Step ([Table 28](#))

Default: “00”

LMAT1-0: ALC Limiter ATT Step ([Table 25](#))

Default: “00”

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation

0: Enable (default)

1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Mode Control 1	DAM	MIXD	SDIM1	SDIM0	EQ	ADM	IVOLC	ALC
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	0

ALC: ALC Enable

0: ALC Disable (default)

1: ALC Enable

IVOLC: Input Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When IVOLC bit = “1”, IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = “0”, IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

ADM: Mono Recording ([Table 44](#))

0: Stereo (default)

1: Mono: (L+R)/2

EQ: Select 5-Band Equalizer

0: OFF (default)

1: ON

SDIM1-0: SDTI Input Signal Select ([Table 48](#))

Default: “00” (L=Lch, R=Rch)

MIXD: DAC and SRC-A Mono Mixing ([Table 53](#) and [Table 54](#))

0: L+R (default)

1: (L+R)/2

DAM: DAC Mono Mixing ([Table 53](#))

0: Stereo (default)

1: Mono: (L+R) or (L+R)/2 is selected by MIXD bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	Mode Control 2	SRA1	SRA0	BIV2	BIV1	BIV0	SMUTE	OVTM	OVOLC
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	1

OVOLC: Output Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When OVOLC bit = “1”, OVL7-0 bits control both Lch and Rch volume level, while register values of OVL7-0 bits are not written to OVR7-0 bits. When OVOLC bit = “0”, OVL7-0 bits control Lch level and OVR7-0 bits control Rch level, respectively.

OVTM: Digital Volume Transition Time Setting

0: 1061/fs (default)

1: 256/fs

This is the transition time between OVL/R7-0 bits = 00H and FFH.

SMUTE: Soft Mute Control

0: Normal Operation (default)

1: DAC outputs soft-muted

BIV2-0: SDTIB Input Volume Control ([Table 41](#))

Default: “0H” (0dB)

SRA1-0: SRC-A Input Signal Select ([Table 54](#))

Default: “00” (Lch)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
1BH	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	0

OVL7-0, OVR7-0: Output Digital Volume ([Table 36](#))

Default: “18H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Side Tone A Control	0	0	SVAR2	SVAR1	SVAR0	SVAL2	SVAL1	SVAL0
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

SVAL2-0, SVAR2-0: Side Tone Volume A (SVOLA) ([Table 34](#))

Default: “000” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Select	GN1	GN0	LPF	HPF	EQ0	FIL3	HPFAD	PFSEL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	1	0

PFSEL: Signal Select of Programmable Filter Block ([Table 43](#))

0: ADC Output Data (default)

1: SDTI Input Data

HPFAD: HPF Control of ADC

0: OFF

1: ON (default)

When HPFAD bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPFAD bit is “0”, HPFAD block is through (0dB).

GN1-0: Gain Select at GAIN block ([Table 23](#))

Default: “00” (0dB)

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When FIL3 bit is “1”, the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is “0”, FIL3 block is OFF (MUTE).

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ0 bit is “1”, the settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit is “0”, EQ0 block is through (0dB).

HPF: HPF Coefficient Setting Enable

0: Disable (default)

1: Enable

When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable

0: Disable (default)

1: Enable

When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, LPF block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
1FH	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
20H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
21H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
22H	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
23H	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
24H	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
25H	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
26H	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
27H	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)

Default: "0000H"

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select

0: HPF (default)

1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ0 (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)

Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	FIL1 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
29H	FIL1 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
2AH	FIL1 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
2BH	FIL1 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		W	W	W	W	W	W	W	W
Default		F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH"							

F1A13-0, F1B13-B0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)

Default: F1A13-0 bits = "1FA9H", F1B13-0 bits = "20ADH" (fc=150Hz@fs=44.1kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	FIL2 Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	FIL2 Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	FIL2 Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	FIL2 Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-B0: FIL2 (LPF) Coefficient (14bit x 2)

Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
	R/W	RD	RD	RD	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ1 bit is “1”, the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is “0”, EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ2 bit is “1”, the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is “0”, EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ3 bit is “1”, the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is “0”, EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ4 bit is “1”, the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is “0”, EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ5 bit is “1”, the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is “0”, EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: "0000H"

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: "0000H"

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: "0000H"

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: "0000H"

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	EQ Control 250Hz/100Hz	EQB3	EQB2	EQB1	EQB0	EQA3	EQA2	EQA1	EQA0
51H	EQ Control 3.5kHz/1kHz	EQD3	EQD2	EQD1	EQD0	EQC3	EQC2	EQC1	EQC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
52H	EQ Control 10kHz	0	0	0	0	EQE3	EQE2	EQE1	EQE0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

EQA3-0: Select the boost level of 100Hz

EQB3-0: Select the boost level of 250Hz

EQC3-0: Select the boost level of 1kHz

EQD3-0: Select the boost level of 3.5kHz

EQE3-0: Select the boost level of 10kHz

See [Table 35](#).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
53H	PCM I/F Control 0	GPOM2	GPOE2	PLLBT2	PLLBT1	PLLBT0	PMPCM	PMSRB	PMSRA
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMSRA: SRC-A Power Management

0: Power down (default)

1: Power up

PMSRB: SRC-B Power Management

0: Power down (default)

1: Power up

PMPCM: PCM I/F Power Management

0: Power down (default)

1: Power up

PLLBT2-0: PLLBT Reference Clock Select ([Table 76](#))

PLLBT3 bit is D6 of Addr=55H.

Default: "0000": SYNCA

GPOE2: General Purpose Output 2 Enable at GPOM2 bit = "1"

"0": GPO2 pin = "L" (default)

"1": GPO2 pin = "H"

GPOM2: General Purpose Output 2 Operation Mode ([Table 92](#))

"0": Controlled by GPOE2 bit (default)

"1": MIC Detection Interrupt

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
54H	PCM I/F Control 2	SDOAD	BCKO2	MSBSA	BCKPA	LAWA1	LAWA0	FMTA1	FMTA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

FMTA1-0: PCM I/F A Format ([Table 84](#))

Default: “00” (Mode 0)

LAWA1-0: PCM I/F A Mode ([Table 82](#))

Default: “00” (Mode 0)

BCKPA: BICKA Polarity of PCM I/F A ([Table 86](#))

“0”: SDTOA is output by the rising edge (“↑”) of BICKA and SDTIA is latched by the falling edge (“↓”). (default)

“1”: SDTOA is output by the falling edge (“↓”) of BICKA and SDTIA is latched by the rising edge (“↑”).

MSBSA: SYNCA Phase of PCM I/F A ([Table 86](#))

“0”: The rising edge (“↑”) of SYNCA is half clock of BICKA before the channel change. (default)

“1”: The rising edge (“↑”) of SYNCA is one clock of BICKA before the channel change.

BCKO2: BICKA/B Output Frequency Select at Master Mode ([Table 77](#))

0: 16fs2 (default)

1: 32fs2

SDOAD: SDTOA Disable ([Table 56](#))

“0”: Enable (default)

“1”: Disable (“L”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
55H	PCM I/F Control 3	SDOBD	PLLBT3	MSBSB	BCKPB	LAWB1	LAWB0	FMTB1	FMTB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

FMTB1-0: PCM I/F B Format ([Table 85](#))

Default: “00” (Mode 0)

LAWB1-0: PCM I/F B Mode ([Table 83](#))

Default: “00” (Mode 0)

BCKPB: BICKB Polarity of PCM I/F B ([Table 87](#))

“0”: SDTOB is output by the rising edge (“↑”) of BICKB and SDTIB is latched by the falling edge (“↓”). (default)

“1”: SDTOB is output by the falling edge (“↓”) of BICKB and SDTIB is latched by the rising edge (“↑”).

MSBSB: SYNCB Phase of PCM I/F B ([Table 87](#))

“0”: The rising edge (“↑”) of SYNCB is half clock of BICKB before the channel change. (default)

“1”: The rising edge (“↑”) of SYNCB is one clock of BICKB before the channel change.

PLLBT3: PLLBT Reference Clock Select ([Table 76](#))

PLLBT2-0 bits is D5-3 of Addr=53H.

Default: “0000”: SYNCA

SDOBD: SDTOB Disable ([Table 58](#))

“0”: Enable (default)

“1”: Disable (“L”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	Digital Volume B Control	BVL7	BVL6	BVL5	BVL4	BVL3	BVL2	BVL1	BVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

BVL7-0: Digital Volume B ([Table 38](#))

Default: “18H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
57H	Digital Volume C Control	CVL7	CVL6	CVL5	CVL4	CVL3	CVL2	CVL1	CVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

CVL7-0: Digital Volume C ([Table 39](#))

Default: “18H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
58H	Side Tone Volume Control	0	0	0	0	SDOA	SVB2	SVB1	SVB0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SVB2-0: Side Tone Volume ([Table 40](#))

Default: “0H” (0dB)

SDOA: SDTOA Output Signal Select ([Table 55](#))

“0”: SRC-A (default)

“1”: SDTI-B

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
59H	Digital Mixing Control	SDOR1	SDOR0	SDOL1	SDOL0	BVMX1	BVMX0	SBMX1	SBMX0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SBMX1-0: SDTOB Output Signal Select ([Table 57](#))

Default: “00” (SDTIA)

BVMX1-0: SRC-B Input Signal Select ([Table 59](#))

Default: “00” (SDTIA)

SDOL1-0: SDTO Lch Output Mixing ([Table 45](#))

Default: “00” (Lch Signal Selected by [Table 44](#))

SDOR1-0: SDTO Rch Output Mixing ([Table 46](#))

Default: “00” (Rch Signal Selected by [Table 44](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5AH	SAR ADC Control	0	0	0	GPOM1	GPOE1	A1	A0	PMSAD
	R/W	RD	RD	RD	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMSAD: 10bit ADC Power Management

“0”: Power down (default)

“1”: Power up

A1-0: SAR ADC Measurement Mode ([Table 94](#))

Default: “00” (AIN1)

GPOE1: General Purpose Output 1 Enable at GPOM1 bit = “1”

“0”: GPO pin = “L” (default)

“1”: GPO pin = “H”

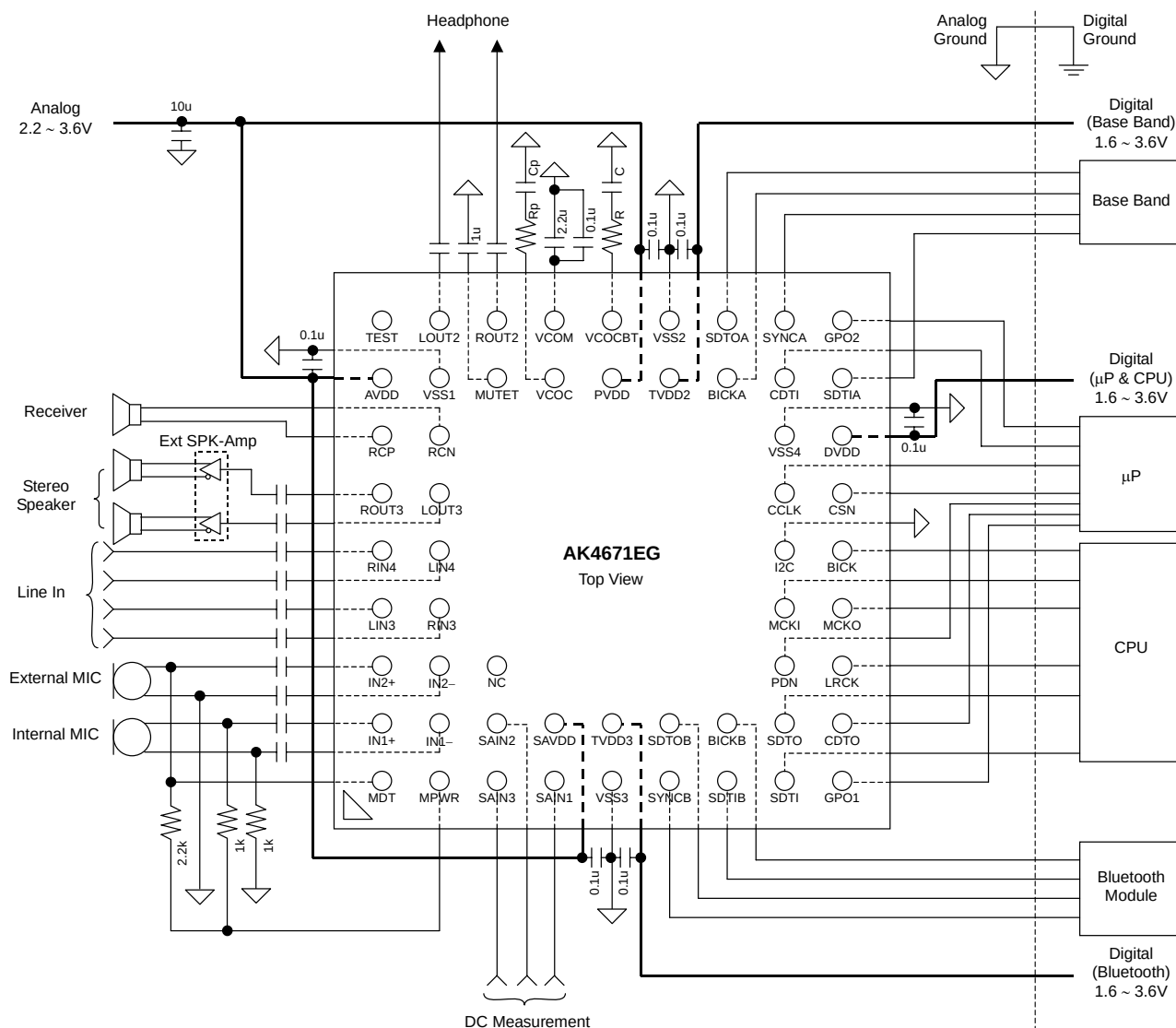
GPOM1: General Purpose Output 1 Operation Mode

“0”: Controlled by GPOE bit (default)

“1”: Controlled by A0 bit

SYSTEM DESIGN

Figure 108 shows the system connection diagram for the AK4671. The evaluation board [AKD4671] demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4671 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4671 is EXT mode (PMPLL bit = “0”), a resistor and capacitor of the VCOC pin is not needed.
- When the AK4671 is PLL mode (PMPLL bit = “1”), a resistor and capacitor of the VCOC pin is shown in [Table 4](#).
- When the AK4671 is used by master mode, LRCK and BICK pins are a Hi-Z state until M/S bit becomes “1”. LRCK and BICK pins of the AK4671 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.
- A resistor and capacitor of the VCOCBT pin is shown in [Table 76](#).
- After setting PDN pin = “H”, the PCM I/F clock pins of AK4671 are a Hi-Z state until PMPCM bit becomes “1”. The PCM I/F clock pins of master mode should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

Figure 108. Typical Connection Diagram
(Internal Full-differential Mic, External pseudo differential Mic, Receiver Output, 4-wire serial mode)

1. Grounding and Power Supply Decoupling

The AK4671 requires careful attention to power supply and grounding arrangements. AVDD, PVDD, SAVDD, DVDD, TVDD2 and TVDD3 are usually supplied from the system's analog supply. If AVDD, PVDD, SAVDD, DVDD, TVDD2 and TVDD3 are supplied separately, the power-up sequence is not critical. The PDN pin should be held to "L" when power-up. The PDN pin should be set to "H" after all power supplies are powered-up.

In case that the pop noise should be avoided at receiver output, headphone output and line output, the AK4671 should be operated by the following recommended power-up/down sequence.

1) Power-up

- The PDN pin should be held to "L" when power-up. The AK4671 should be reset by bringing the PDN pin "L" for 150ns or more.
- In case that the power supplies are separated in two or more groups, the power supply including DVDD should be powered ON at first.

2) Power-down

- Each power supplies should be powered OFF after the PDN pin is set to "L".
- In case that the power supplies are separated in two or more groups, the power supply including DVDD should be powered OFF at last.

VSS1, VSS2, VSS3 and VSS4 of the AK4671 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4671 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4671.

3. Analog Inputs

The Mic, Line and MIN inputs are single-ended. The input signal range scales with nominally at $0.6 \times \text{AVDD } V_{pp}$ (typ) at $\text{MGNL}=\text{MGNR}=0\text{dB}$ and single-ended input, centered around the internal common voltage ($0.5 \times \text{AVDD}$). The input signal should be AC coupled using a capacitor. The cut-off frequency is $f_c = 1/(2\pi RC)$. The AK4671 can accept input voltages from VSS1 to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit). VCOM voltage is $0.5 \times \text{AVDD}$ (typ).

When LOUT1, ROUT1, LOUT2, ROUT2, LOUT3/LOP and ROUT3/LON pins are single-ended output, these pins should be AC coupled using a capacitor. When RCP, RCN pins are full-differential output, these pins should be connected directly to a receiver. (RCP, RCN pins should be not AC coupled using a capacitor.)

CONTROL SEQUENCE (AUDIO)

■ Clock Set up

When ADC or DAC is powered-up, the clocks must be supplied.

1. PLL Master Mode.

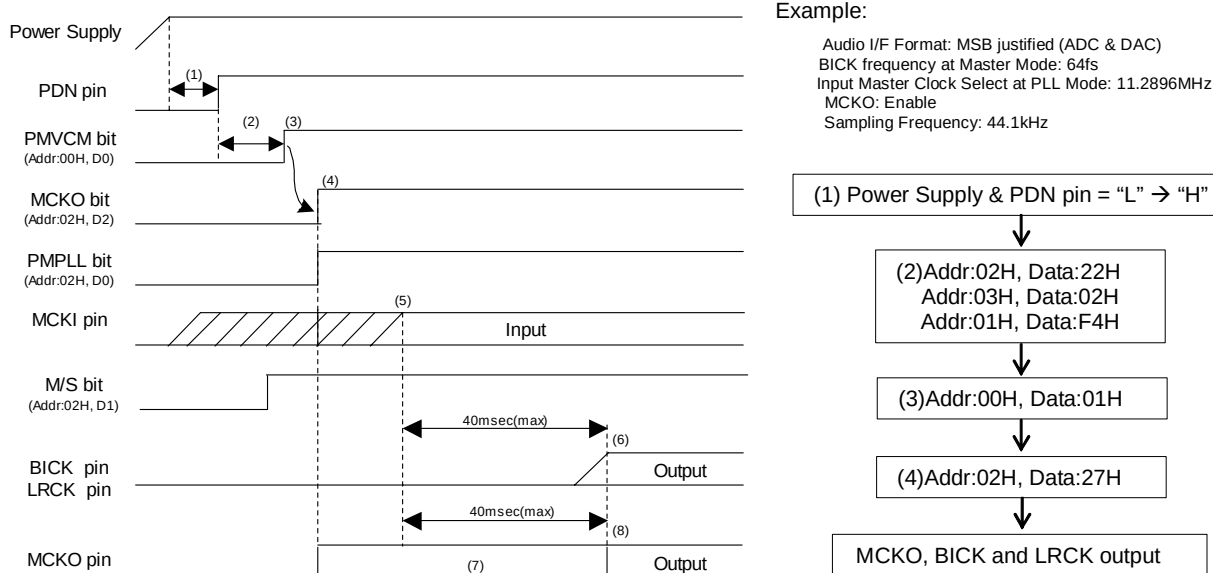


Figure 109. Clock Set Up Sequence (1)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671. The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.
- (4) In case of using MCKO output: MCKO bit = "1"
- (5) PLL lock time is 40ms(max.) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
- (6) The AK4671 starts to output the LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.
- (7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".
- (8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (MCKI pin)

Example:

Audio I/F Format: MSB justified (ADC & DAC)
 BICK frequency at Master Mode: 64fs
 Input Master Clock Select at PLL Mode: 11.2896MHz
 MCKO: Enable
 Sampling Frequency: 44.1kHz

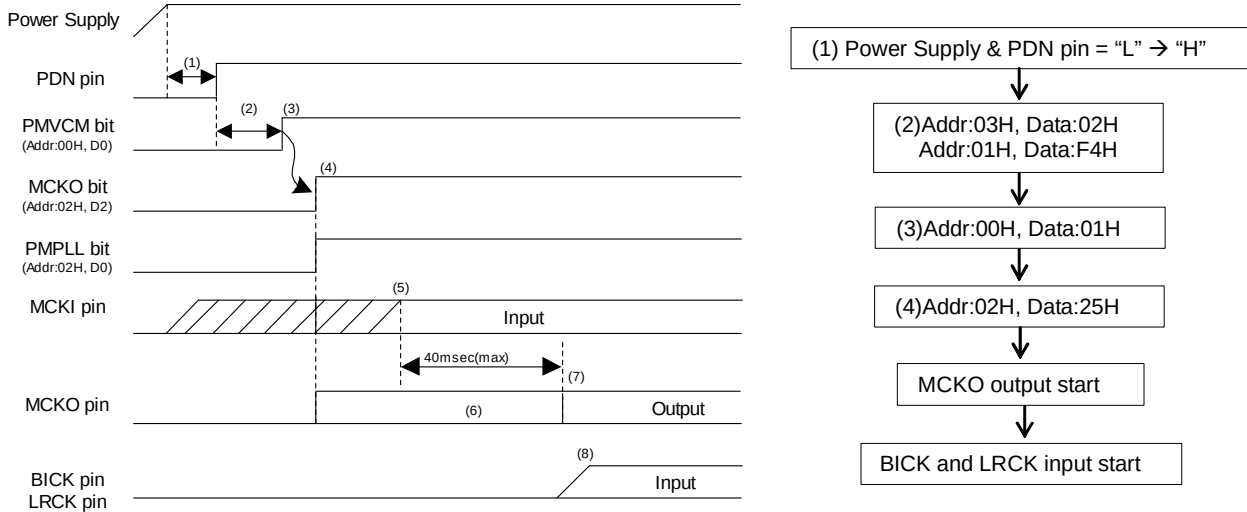


Figure 110. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671.
 The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) DIF1-0, PLL3-0 and FS3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) Enable MCKO output: MCKO bit = "1"
- (5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
 PLL lock time is 40ms(max.).
- (6) The normal clock is output from MCKO during this period.
- (7) The invalid frequency is output from MCKO after PLL is locked.
- (8) BICK and LRCK clocks should be synchronized with MCKO clock.

3. PLL Slave Mode (LRCK or BICK pin)

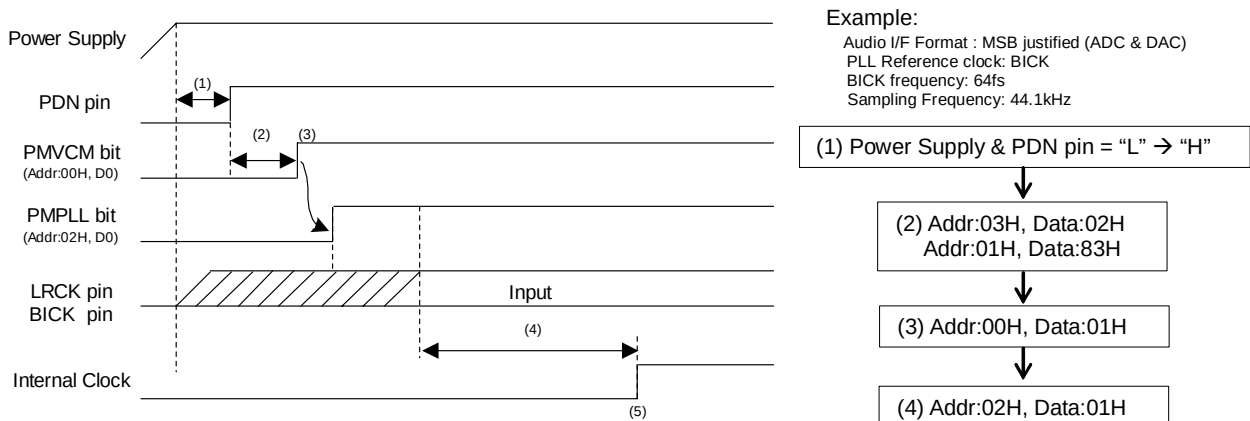


Figure 111. Clock Set Up Sequence (3)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671. The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) DIF1-0, FS3-2 and PLL3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms(max.) when LRCK is a PLL reference clock. And PLL lock time is 2ms(max.) when BICK is a PLL reference clock.
- (5) Normal operation starts after that the PLL is locked.

4. EXT Slave Mode

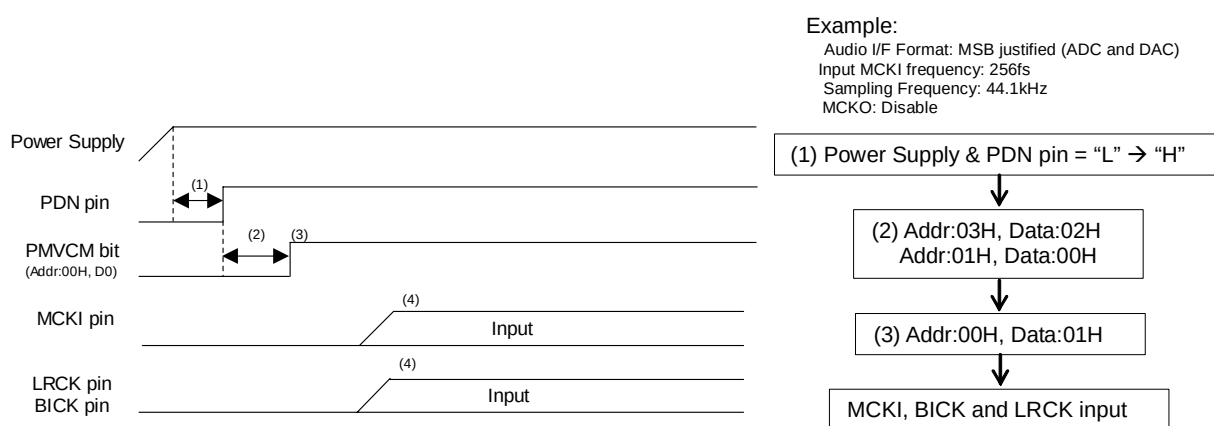


Figure 112. Clock Set Up Sequence (4)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671.
The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) DIF1-0 and FS1-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
- (4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

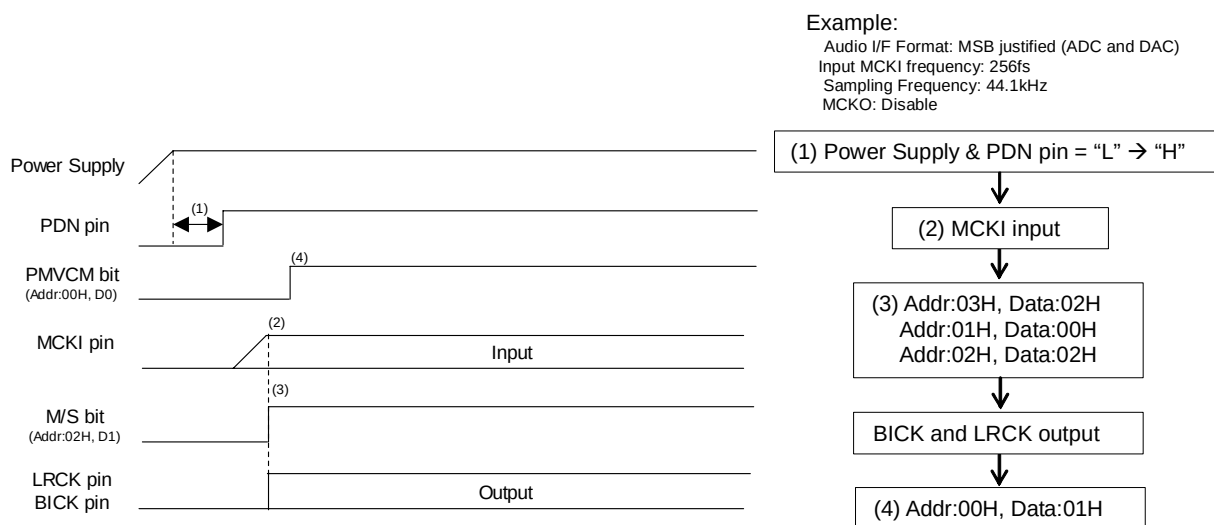


Figure 113. Clock Set Up Sequence (5)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671.
 The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) MCKI should be input.
- (3) After DIF1-0 and FS2-0 bits are set, M/S bit should be set to "1". Then LRCK and BICK are output.
- (4) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.

■ MIC Input Recording (Stereo)

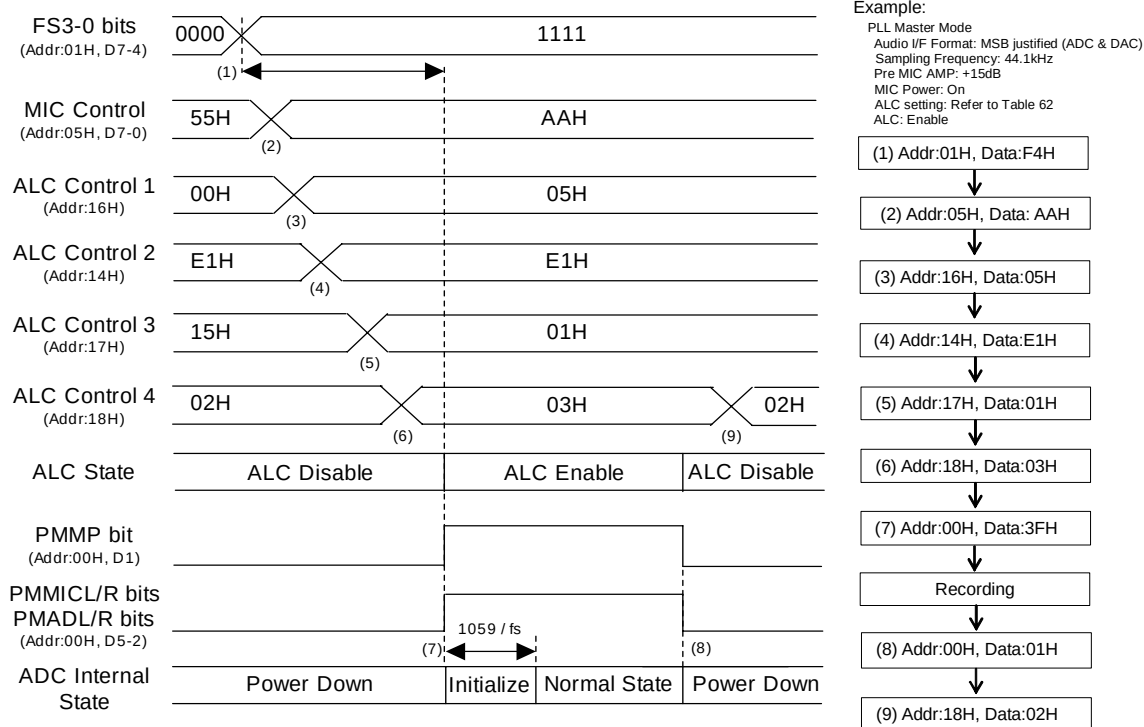


Figure 114. Stereo MIC Input Sequence
 (MIC Recording: LIN1/RIN1 → MICL/R → ADCL/R → ALC → Audio I/F → SDTO)

<Example>

This sequence is an example of ALC setting at $f_s=44.1\text{kHz}$. If the parameter of the ALC is changed, please refer to “Figure 62”.

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bits). When the AK4671 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up Gain for MIC-Amp (Addr: 05H)
- (3) Set up Timer Select for ALC (Addr: 16H)
- (4) Set up REF value for ALC (Addr: 14H)
- (5) Set up LMTH1-0, RGAIN1-0 and LMAT1-0 bits (Addr: 17H)
- (6) Set up ALC bit (Addr: 18H)
- (7) Power Up MIC and ADC: PMMP = PMMCL = PMMICR = PMADL = PMADR bits = “0” → “1”

The initialization cycle time of ADC is $1059/f_s=24\text{ms}@f_s=44.1\text{kHz}$.

After the ALC bit is set to “1” and ADC block is powered-up, the ALC operation starts from IVOL default value (0dB). The time of offset voltage going to “0” after the ADC initialization cycle depends on both the time of analog input pin going to the common voltage and the time constant of the offset cancel digital HPF. This time can be shorter by using the following sequence:

At first, PMVCM and PMMP bits should set to “1”. Then, the ADC should be powered-up. The wait time to power-up the ADC should be longer than 4 times of the time constant that is determined by the AC coupling capacitor at analog input pin and the internal input resistance.

- (8) Power Down MIC and ADC: PMMP = PMMCL = PMMICR = PMADL = PMADR bits = “1” → “0”
 When the registers for the ALC operation are not changed, ALC bit may be keeping “1”. The ALC operation is disabled because the ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK4671 goes to the manual mode (ALC bit = “0”) or ADC block is powered-down (PMADL = PMADR bits = “0”). IVOL gain is not reset when PMADL = PMADR bits = “0”, and then IVOL operation starts from the setting value when PMADL or PMADR bit is changed to “1”.
- (9) ALC Disable: ALC bit = “1” → “0”

Headphone-Amp Output

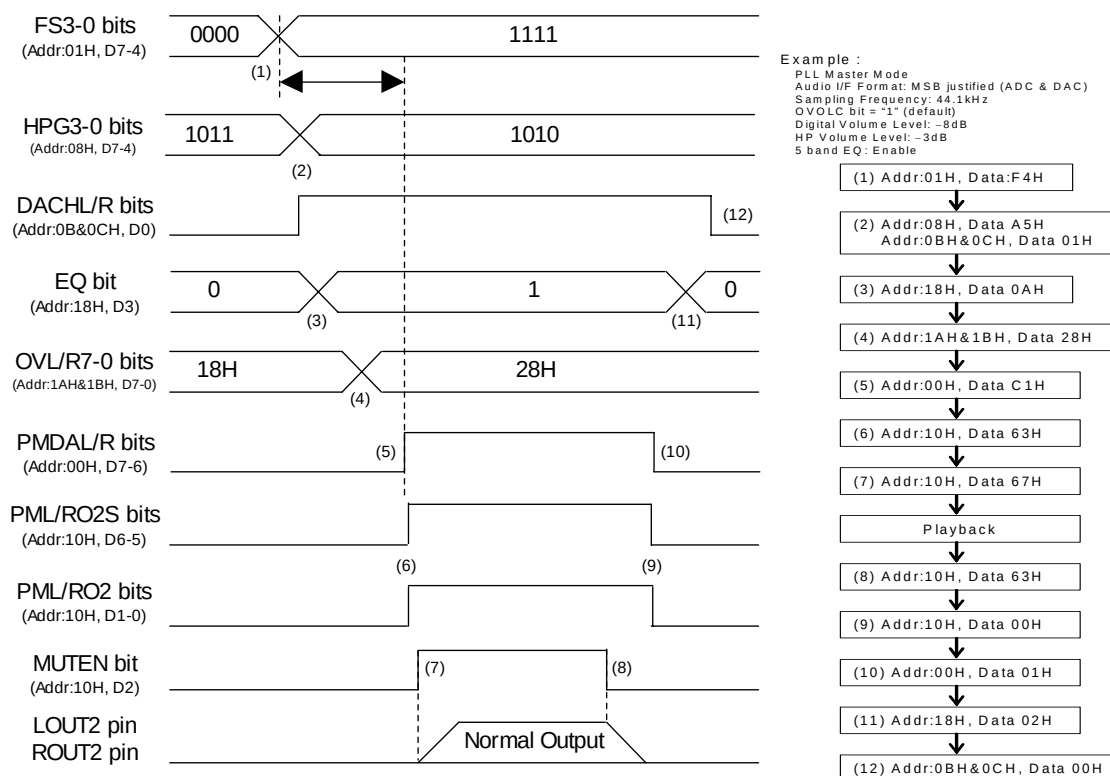


Figure 115. Headphone-Amp Output Sequence
(Headphone Playback: SDTI → Audio I/F → EQ → DATT → DACL/R → LOUT2/ROUT2)

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

- Set up a sampling frequency (FS3-0 bits). When the AK4671 is PLL mode, DAC and Headphone-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- Set up the path of "SDTI → DAC → HP-Amp": DACHL = DACHR bits = "0" → "1"
Set up analog volume for HP-Amp (Addr: 08H, HPG3-0 bits)
- Enable 5-band Equalizer: EQ bit = "0" → "1" (Boost amount is selected by Addr = 50H-52H.)
- Set up the output digital volume (Addr: 1AH and 1BH)
When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- Power up DAC: PMDAL = PMDAR bits = "0" → "1"
- Power up Headphone-Amp and MIX-Amp: PMLO2 = PMRO2 = PMLO2S = PMRO2S bits = "0" → "1"
Output voltages of Headphone-Amp are still VSS1.
- Rise up the common voltage of Headphone-Amp: MUTEN bit = "0" → "1"
The rise time depends on AVDD and the capacitor value connected with the MUTET pin. When AVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_f = 250\text{ms}(\text{max.})$.
- Fall down the common voltage of Headphone-Amp: MUTEN bit = "1" → "0"
The fall time depends on AVDD and the capacitor value connected with the MUTET pin. When AVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_f = 250\text{ms}(\text{max.})$.
If the power supply is powered-off or Headphone-Amp is powered-down before the common voltage goes to VSS2, the pop noise occurs. It takes twice of τ_f that the common voltage goes to VSS2.
- Power down Headphone-Amp and MIX-Amp: PMLO2 = PMRO2 = PMLO2S = PMRO2S bits = "1" → "0"
- Power down DAC: PMDAL = PMDAR bits = "1" → "0"
- Disable 5-band Equalizer: EQ bit = "1" → "0"
- Disable the path of "DAC → Headphone-Amp": DACHL = DACHR bits = "1" → "0"

■ Stereo Line Output

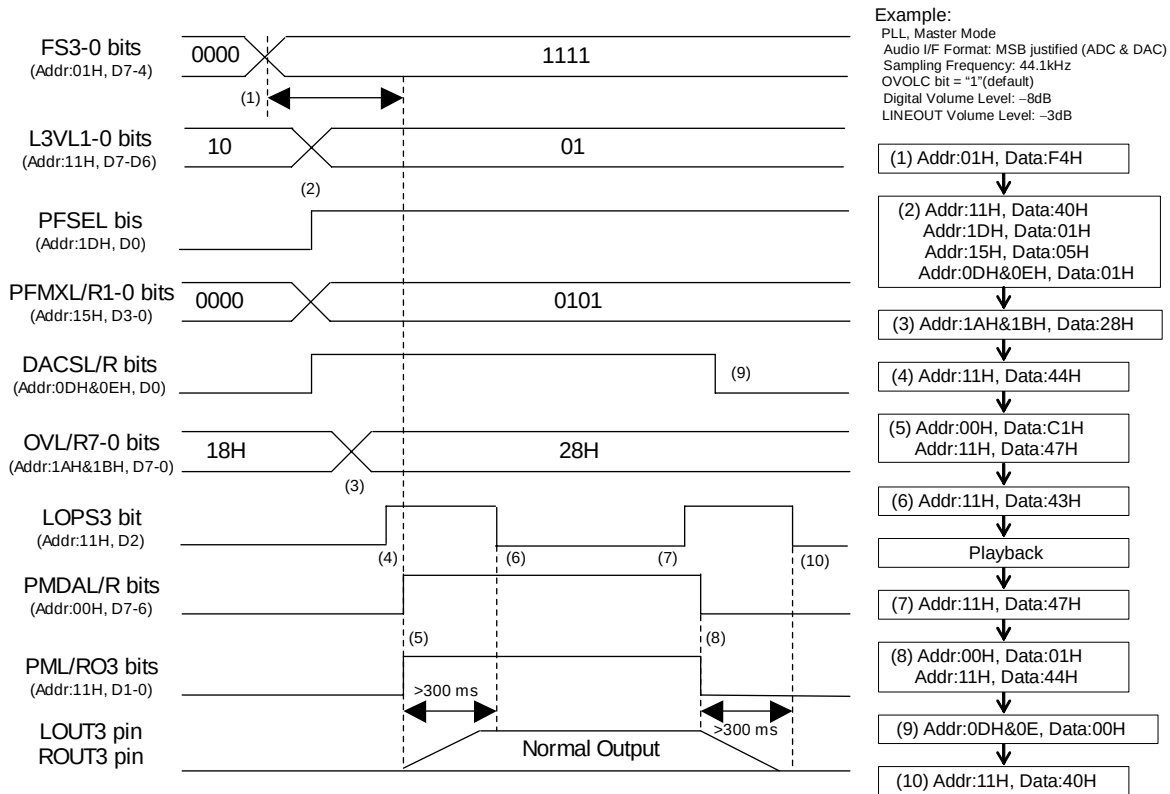


Figure 116. Stereo Lineout Sequence

(Speaker Playback: SDTI → Audio I/F → SVOLA → DATT → DACL/R → LOUT3/ROUT3 → External SPK-Amp)

<Example>

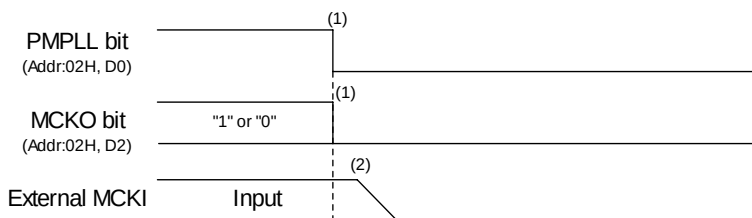
At first, clocks should be supplied according to "[Clock Set Up](#)" sequence.

- (1) Set up the sampling frequency (FS3-0 bits). When the AK4671 is PLL mode, DAC and Stereo Line-Amp should be powered-up in consideration of PLL lock time after the sampling frequency is changed.
- (2) Set up the path of "SDTI → DAC → Stereo Line-Amp": PFSEL = "0" → "1", PFMXL1-0 = PFMXR1-0 bits = "0000" → "0101", DACSL = DACSR bits = "0" → "1"
 Set up analog volume for Stereo Line-Amp (Addr: 11H, L3VL1-0 bits)
- (3) Set up the output digital volume (Addr: 1AH and 1BH)
 When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (4) Enter power-save mode of Stereo Line-Amp: LOPS3 bit = "0" → "1"
- (5) Power-up DAC and Stereo Line-Amp: PMDAL = PMDAR = PMLO3 = PMRO3 bits = "0" → "1"
 LOUT3 and ROUT3 pins rise up to VCOM voltage after PMLO3 and PMRO3 bits are changed to "1". Rise time is 300ms(max.) at C=1μF and AVDD=3.3V.
- (6) Exit power-save mode of Stereo Line-Amp: LOPS3 bit = "1" → "0"
 LOPS3 bit should be set to "0" after LOUT3 and ROUT3 pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS3 bit to "0".
- (7) Enter power-save mode of Stereo Line-Amp: LOPS3 bit: "0" → "1"
- (8) Power-down DAC and Stereo Line-Amp: PMDAL = PMDAR = PMLO3 = PMRO3 bits = "1" → "0"
 LOUT3 and ROUT3 pins fall down to VSS1. Fall time is 300ms(max.) at C=1μF and AVDD=3.3V.
- (9) Disable the path of "DAC → Stereo Line-Amp": DACSL = DACSR bits = "1" → "0"
- (10) Exit power-save mode of Stereo Line-Amp: LOPS3 bit = "1" → "0"
 LOPS3 bit should be set to "0" after LOUT3 and ROUT3 pins fall down.

■ Stop of Clock

Master clock can be stopped when ADC and DAC are not used.

1. PLL Master Mode



Example:

Audio I/F Format: MSB justified (ADC & DAC)
BICK frequency at Master Mode: 64fs
Input Master Clock Select at PLL Mode: 11.2896MHz
Sampling Frequency: 44.1kHz

(1) Addr:02H, Data:02H

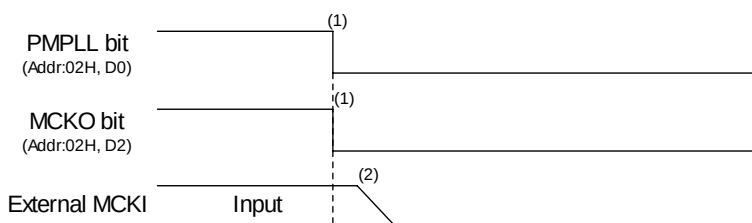
(2) Stop an external MCKI

Figure 117. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO clock: MCKO bit = "1" → "0"
- (2) Stop an external MCKI clock.

2. PLL Slave (MCKI pin)



Example

Audio I/F Format: MSB justified (ADC & DAC)
PLL Reference clock: MCKI
BICK frequency: 64fs
Sampling Frequency: 44.1kHz

(1) Addr:02H, Data:00H

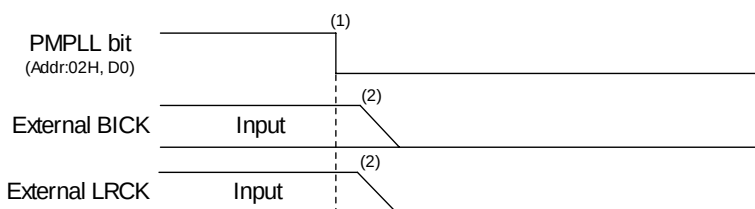
(2) Stop the external clocks

Figure 118. Clock Stopping Sequence (2)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
- (2) Stop the external master clock.

3. PLL Slave Mode (LRCK or BICK pin)



Example

Audio I/F Format: MSB justified (ADC & DAC)
PLL Reference clock: BICK
BICK frequency: 64fs
Sampling Frequency: 44.1kHz

(1) Addr:02H, Data:00H

(2) Stop the external clocks

Figure 119. Clock Stopping Sequence (3)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop the external BICK and LRCK clocks

4. EXT Slave Mode

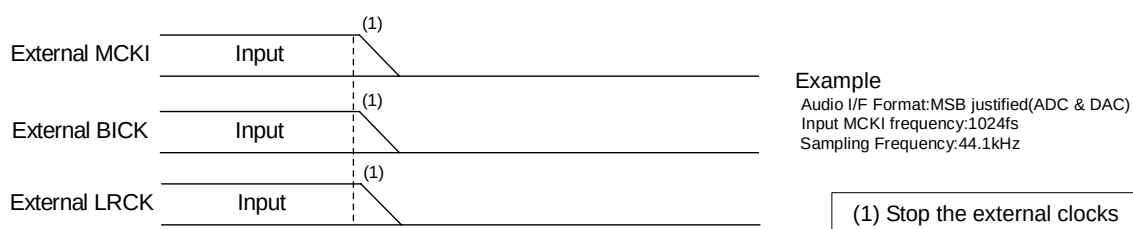


Figure 120. Clock Stopping Sequence (4)

<Example>

(1) Stop the external MCKI, BICK and LRCK clocks.

5. EXT Master Mode

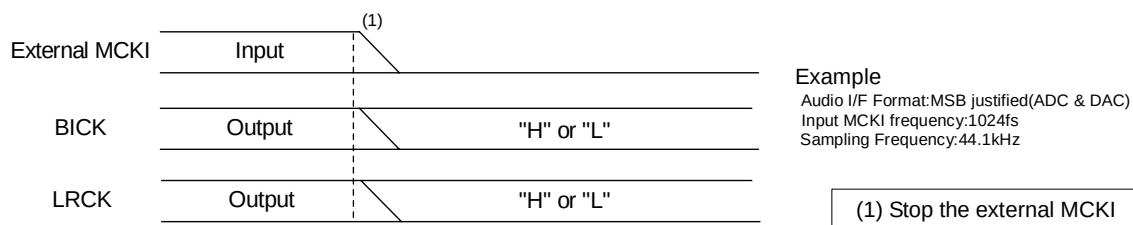


Figure 121. Clock Stopping Sequence (5)

<Example>

(1) Stop MCKI clock. BICK and LRCK are fixed to "H" or "L".

■ Power down

Power supply current can be shut down (typ. 20 μ A) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1 μ A) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", the registers are initialized.

CONTROL SEQUENCE (PCM)

■ Clock Set up

When ADC or DAC is powered-up, the clocks must be supplied.

1. PCM I/F A Slave Mode

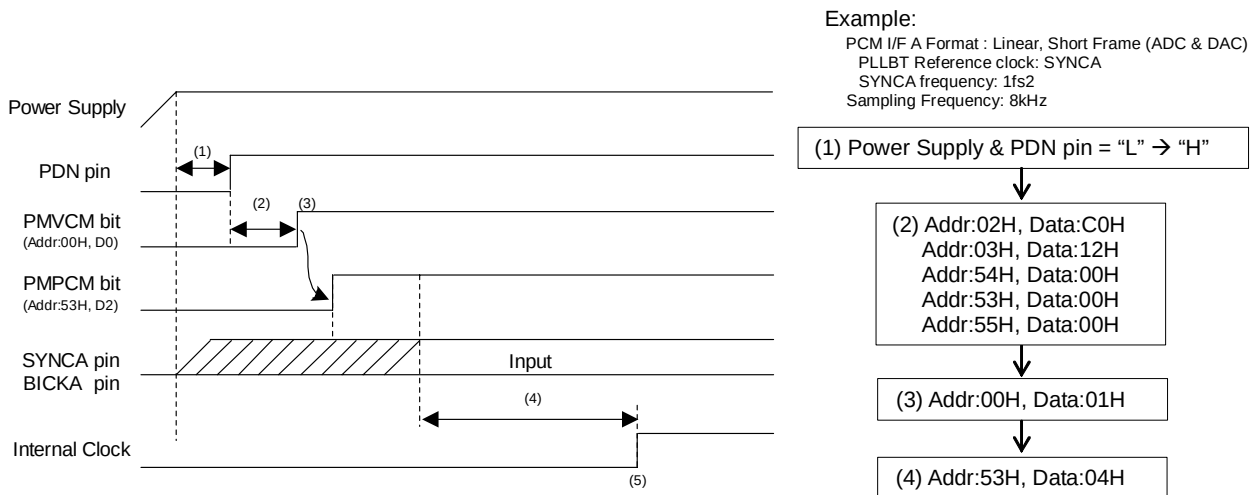


Figure 122. Clock Set Up Sequence (1)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671. The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) BTCLK, LP, SDOD, FMTA1-0, LAWA1-0, BCKPA, MSBSA, PLLBT3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) PLLBT starts after the PMPCM bit changes from "0" to "1" and PLLBT reference clock (SYNCA or BICKA pin) is supplied. PLLBT lock time is 260ms(max.) when SYNCA is a PLLBT reference clock. And PLLBT lock time is 40ms(max.) when BICKA is a PLLBT reference clock.
- (5) Normal operation starts after that the PLLBT is locked.

2. PCM I/F A Master Mode

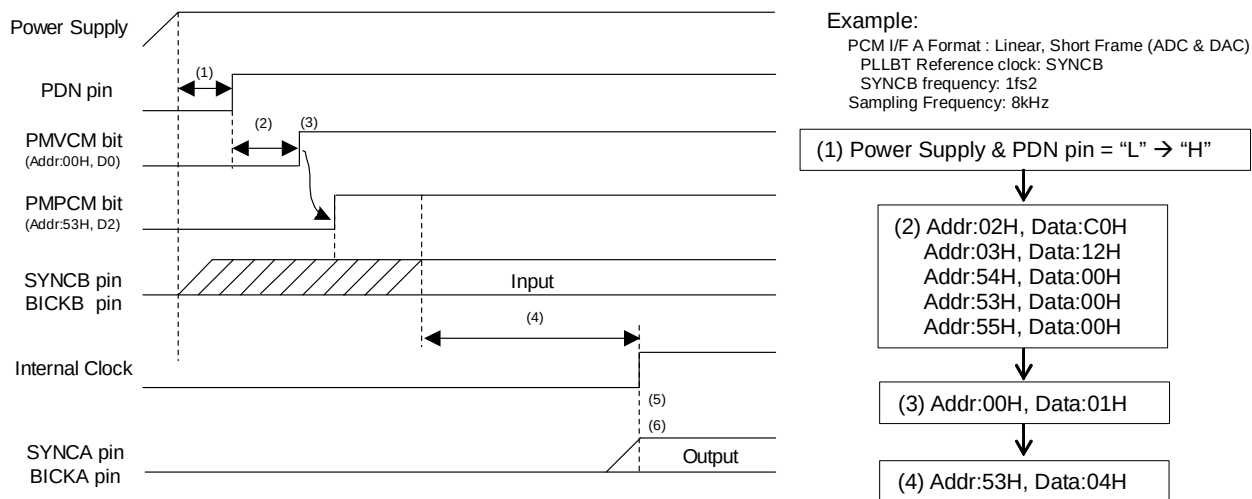


Figure 123. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4671. The AK4671 should be operated as the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at the receiver output, headphone output and lineout output.
- (2) BTCLK, LP, SDOD, FMTA1-0, LAWA1-0, BCKPA, MSBSA, PLLBT3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
- (4) PLLBT starts after the PMPCM bit changes from "0" to "1" and PLLBT reference clock (SYNCB or BICKB pin) is supplied. PLLBT lock time is 260ms(max.) when SYNCB is a PLLBT reference clock. And PLLBT lock time is 40ms(max.) when BICKB is a PLLBT reference clock.
- (5) Normal operation starts after that the PLLBT is locked.
- (6) The invalid frequency is output from SYNCA and BICKA after PLLBT is locked.

■ MIC Input Phone Call (Mono)

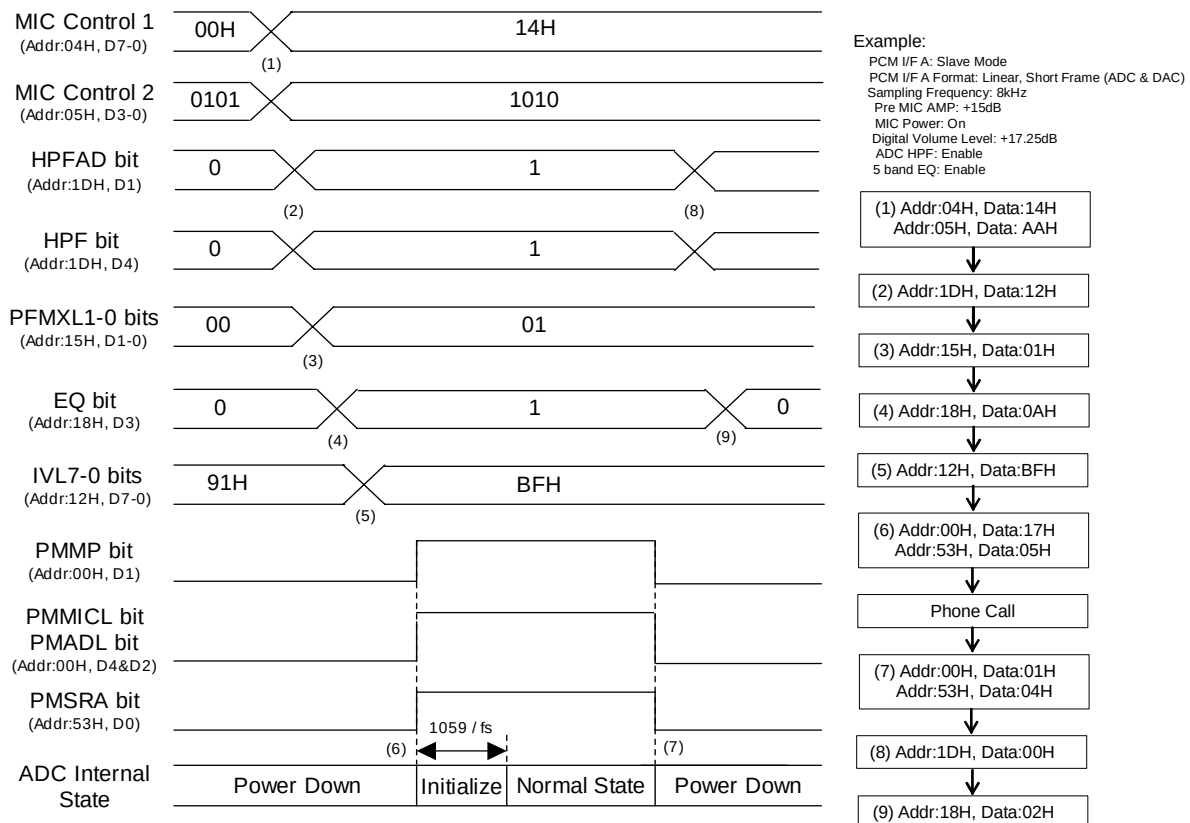


Figure 124. Mono MIC Input Sequence

(Phone Call Tx: IN1+/IN1- → MICL → ADCL → HPF → IVL → EQ → SRC-A → PCM I/F A → SDTOA)

<Example>

At first, clocks should be supplied according to “[Clock Set Up](#)” sequence. Also, MIC, ADC and SRC-A should be powered-up in consideration of PLLBT lock time.

(1) Set up Signal Select for MIC Input (Addr: 04H) and Gain for MIC-Amp (Addr: 05H)

(2) Enable ADC High Pass Filter: HPFAD bit = “0” → “1”

Enable the coefficient of High Pass Filter: HPF bit = “0” → “1” (Coefficient of wind-noise reduction filter is set by Addr = 28H- 2BH.)

This sequence is an example of HPF setting at $fs=8kHz$. The coefficient should be set when HPFAD = HPF bits = “0” or PMADL = PMADR = PMDAL = PMDAR bits = “0”.

(3) Set up the path of “ADC → 5-band EQ”: PFMXL1-0 bits = “00” → “01”

(4) Enable 5-band Equalizer: EQ bit = “0” → “1” (Boost amount is selected by Addr = 50H-52H.)

(5) Set up input volume (Addr: 12H)

When PMADL = PMADR bits = “0”, IVL7-0 and IVR7-0 bits should be set to “91H”(0dB).

(6) Power Up MIC, ADC and SRC-A: PMMP = PMMICL = PMADL = PMSRA bits = “0” → “1”

The initialization cycle time of ADC is $1059/fs=132ms@fs=8kHz$.

The time of offset voltage going to “0” after the ADC initialization cycle depends on both the time of analog input pin going to the common voltage and the time constant of the offset cancel digital HPF. This time can be shorter by using the following sequence:

At first, PMVCM and PMMP bits should set to “1”. Then, the ADC should be powered-up. The wait time to power-up the ADC should be longer than 4 times of the time constant that is determined by the AC coupling capacitor at analog input pin and the internal input resistance.

(7) Power Down MIC, ADC and SRC-A: PMMP = PMMICL = PMADL = PMSRA bits = “1” → “0”

IVOL gain is not reset when PMADL = PMADR bits = “0”, and then IVOL operation starts from the setting value when PMADL or PMADR bit is changed to “1”.

(8) Disable ADC High Pass Filter : HPFAD bit = “1” → “0”

Disable the coefficient of High Pass Filter: HPF bit = “1” → “0”

(9) Disable 5-band Equalizer: EQ bit = “1” → “0”

Receiver-Amp Output

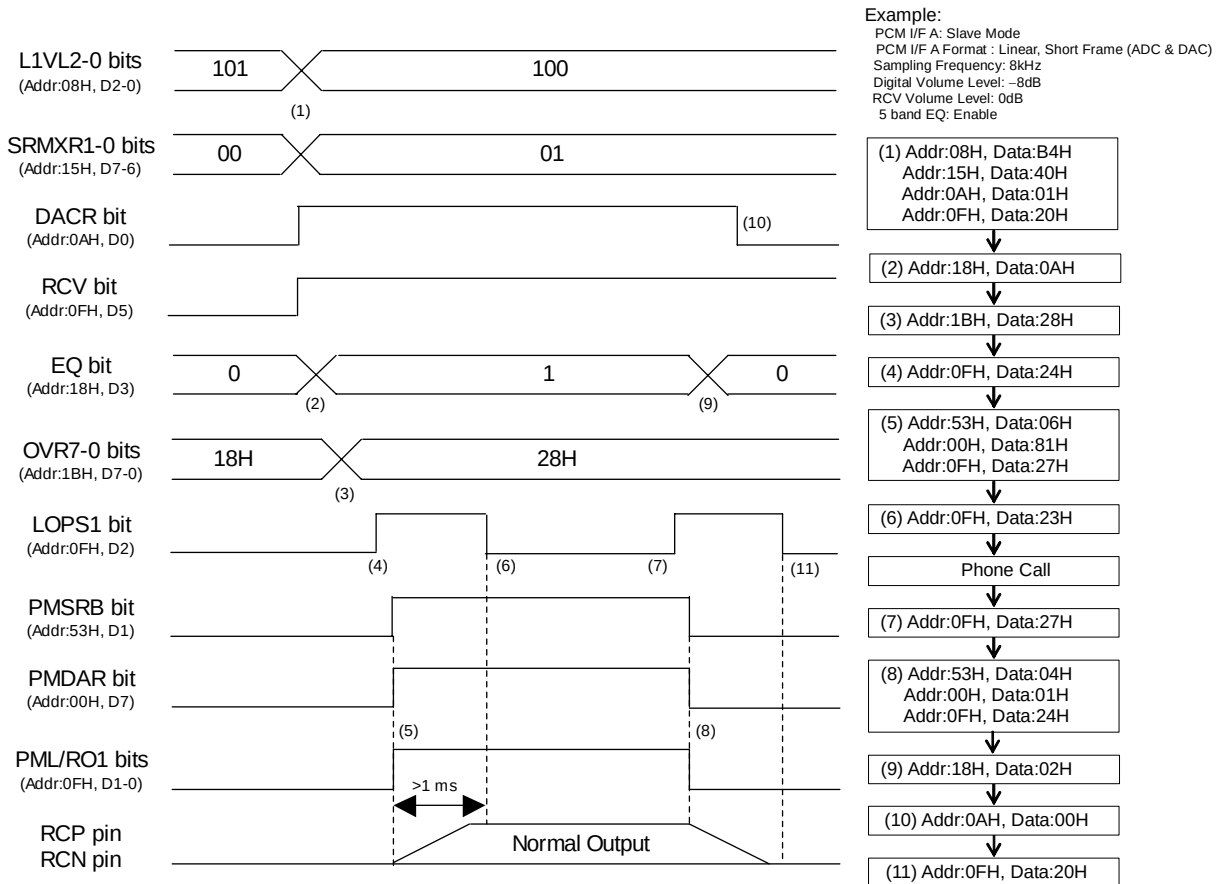


Figure 125. Receiver-Amp Output Sequence

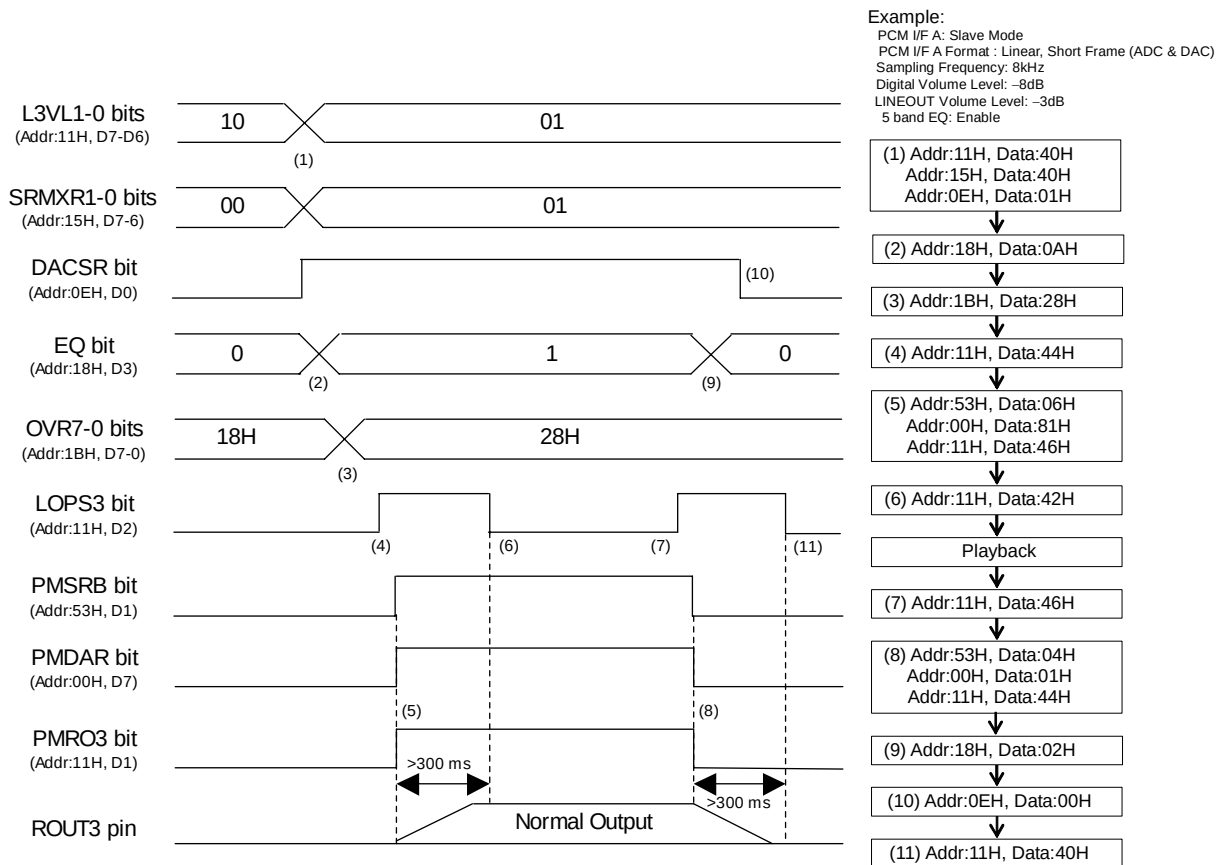
(Phone Call Rx: SDTIA → PCM I/F A → SRC-B → EQ → DATT → DACR → RCP/RCN)

<Example>

At first, clocks should be supplied according to “[Clock Set Up](#)” sequence. Also, SRC-B, DAC and Receiver-Amp should be powered-up in consideration of PLLBT lock time.

- (1) Set up the path of “SDTIA → DAC → Receiver-Amp”: SRMXR1-0 bits = “00” → “01”, DACR bit = “0” → “1”, RCV bit = “0” → “1”
 Set up analog volume for Receiver-Amp (Addr: 08H, L1VL2-0 bits)
- (2) Enable 5-band Equalizer: EQ bit = “0” → “1” (Boost amount is selected by Addr = 50H-52H.)
- (3) Set up the output digital volume (Addr: 1BH)
 When OVOLC bit is “1” (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (4) Enter power-save mode of Receiver-Amp: LOPS1 bit = “0” → “1”
- (5) Power-up SRC-B, DAC and Receiver-Amp: PMSRB bit = PMDAR = PMLO1 = PMRO1 bits = “0” → “1”
 RCN pin rise up to VCOM voltage after PMLO1 and PMRO1 bits are changed to “1”.
- (6) Exit power-save mode of Receiver-Amp: LOPS1 bit = “1” → “0”
 LOPS1 bit should be set to “0” after PCN pin rise up. Receiver-Amp goes to normal operation by setting LOPS1 bit to “0”.
- (7) Enter power-save mode of Receiver-Amp: LOPS1 bit: “0” → “1”
- (8) Power-down SRC-B, DAC and Receiver-Amp: PMSRB bit = PMDAR = PMLO1 = PMRO1 bits = “1” → “0”
 Receiver-Amp becomes to power-down mode.
- (9) Disable 5-band Equalizer: EQ bit = “1” → “0”
- (10) Disable the path of “DAC → Receiver-Amp”: DACR bit = “1” → “0”
- (11) Exit power-save mode of Receiver-Amp: LOPS1 bit = “1” → “0”
 LOPS1 bit should be set to “0” after Receiver-Amp power-down.

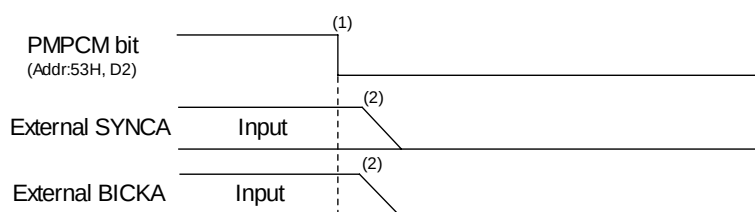
■ Mono Line Output



■ Stop of Clock

Master clock can be stopped when ADC and DAC are not used.

1. PCM I/F A Slave Mode



Example

PCM I/F A Format : Linear, Short Frame (ADC & DAC)
 PLLBT Reference clock: SYNCA
 SYNCA frequency: 1fs2
 Sampling Frequency: 8kHz

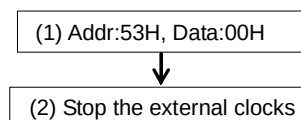
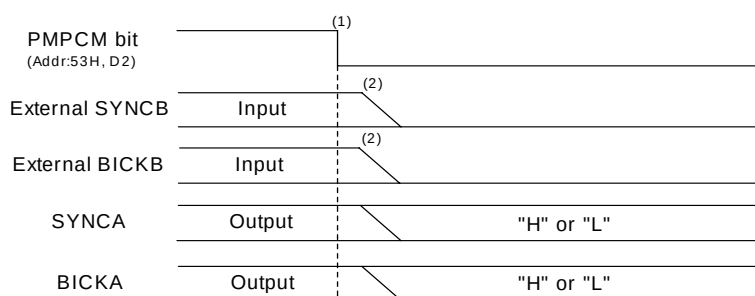


Figure 127. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLLBT: PMPCM bit = "1" → "0"
- (2) Stop the external SYNCA and BICKA clocks

2. PCM I/F A Master Mode



Example

PCM I/F A Format : Linear, Short Frame (ADC & DAC)
 PLLBT Reference clock: SYNCB
 SYNCB frequency: 1fs2
 Sampling Frequency: 8kHz

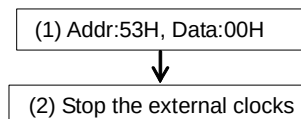


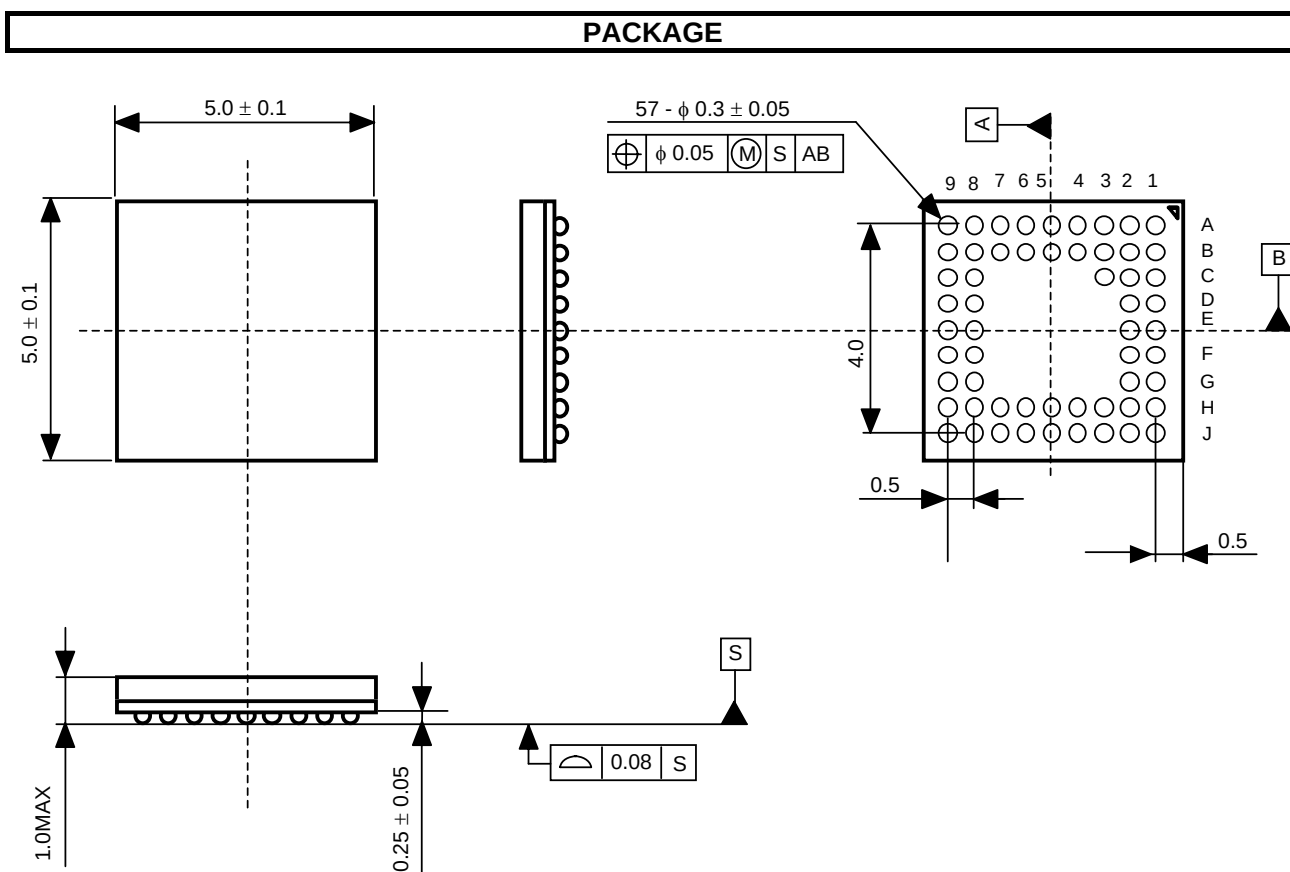
Figure 128. Clock Stopping Sequence (2)

< Example >

- (1) Power down PLLBT: PMPCM bit = "1" → "0"
- (2) Stop the external SYNCB and BICKB clocks. SYNCA and BICKA are fixed to "H" or "L".

■ Power down

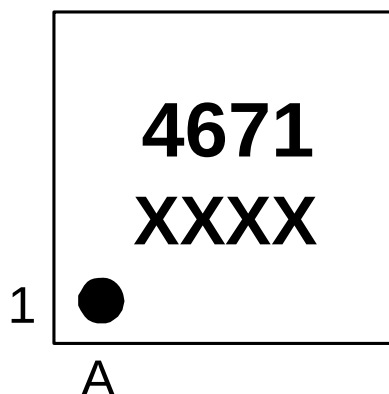
Power supply current can be shut down (typ. 20μA) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1μA) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", the registers are initialized.



■ Material & Lead finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Interposer material:	BT resin
Solder ball material:	SnAgCu

MARKING



XXXX: Date code (4 digit)
Pin #A1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/10/15	00	First Edition		
08/12/04	01	Specification Change	163	Package molding compound was changed.
10/06/04	02	Error Correct	6	Unused pin: BICKA, SYNCA, BICKB, SYNCB “Connect to VSS4” → “When all pins are unused, these pins should be connected to VSS4 and PMPCM bit must be always “0”. When either PCM I/F A(BICKA/ SYNCA) or PCM I/F B(BICKB/SYNCB) is used, unused pins are connected to pull-down/up resistor of about 100kΩ.”
			104	Table 86: MSBSA, BCKPA=“00” [MSB of SDTOA is output by the falling edge (“↓”) of SYNCA.] → [MSB of SDTOA is output by next rising edge (“↑”) of the falling edge (“↓”) of BICKA after the rising edge (“↑”) of SYNCA.] MSBSA, BCKPA=“01” [MSB of SDTOA is output by the falling edge (“↓”) of SYNCA.] → [MSB of SDTOA is output by next falling edge (“↓”) of the rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA.] MSBSA, BCKPA=“10” [MSB of SDTOA is output by the rising edge (“↑”) of the first BICKA after the rising edge (“↑”) of SYNCA.] → [MSB of SDTOA is output by the 2nd rising edge (“↑”) of BICKA after the rising edge (“↑”) of SYNCA.]

Date (YY/MM/DD)	Revision	Reason	Page	Contents
10/06/04	02	Error Correct	104	Table 86: MSBSA, BCKPA="11" [MSB of SDTOA is output by the falling edge ("↓") of the first BICKA after the rising edge ("↑") of SYNCA.] → [MSB of SDTOA is output by the 2nd falling edge ("↓") of BICKA after the rising edge ("↑") of SYNCA.]
			105 ~ 107	Table 87: MSBSB, BCKPB="00" [MSB of SDTOB is output by the falling edge ("↓") of SYNCB.] → [MSB of SDTOB is output by next rising edge ("↑") of the falling edge ("↓") of BICKB after the rising edge ("↑") of SYNCB.] MSBSB, BCKPB="01" [MSB of SDTOB is output by the falling edge ("↓") of SYNCB.] → [MSB of SDTOB is output by next falling edge ("↓") of the rising edge ("↑") of BICKB after the rising edge ("↑") of SYNCB.] MSBSB, BCKPB="10" [MSB of SDTOB is output by the rising edge ("↑") of the first BICKB after the rising edge ("↑") of SYNCB.] → [MSB of SDTOB is output by the 2nd rising edge ("↑") of BICKB after the rising edge ("↑") of SYNCB.] MSBSB, BCKPB="11" [MSB of SDTOB is output by the falling edge ("↓") of the first BICKB after the rising edge ("↑") of SYNCB.] → [MSB of SDTOB is output by the 2nd falling edge ("↓") of BICKB after the rising edge ("↑") of SYNCB.] Figure 84-91: Arrow of SYNCA and BICKA was added.

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