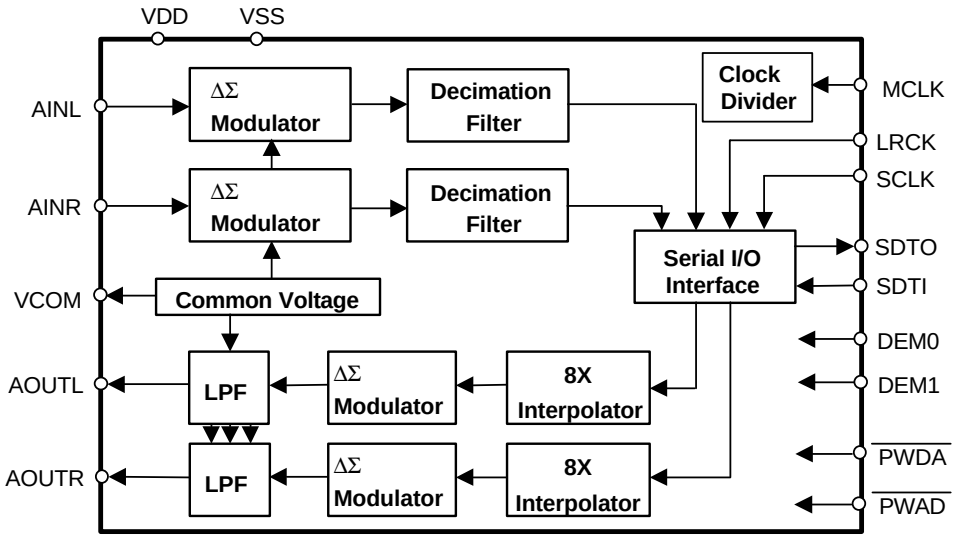
AK4550
Low Power & Small Package 16bit ΔΣ CODEC

GENERAL DESCRIPTION

The AK4550 is a low voltage 16bit A/D & D/A converter for portable digital audio system. In the AK4550, the loss of accuracy form clock jitter is also improved by using SCF techniques for on-chip post filter. Analog signal input/output of the AK4550 are single-ended, therefore, any external filters are not required. The AK4550 is suitable for portable digital audio system, as the AK4550 is lower power dissipation and a smaller package than AK4518.

FEATURES

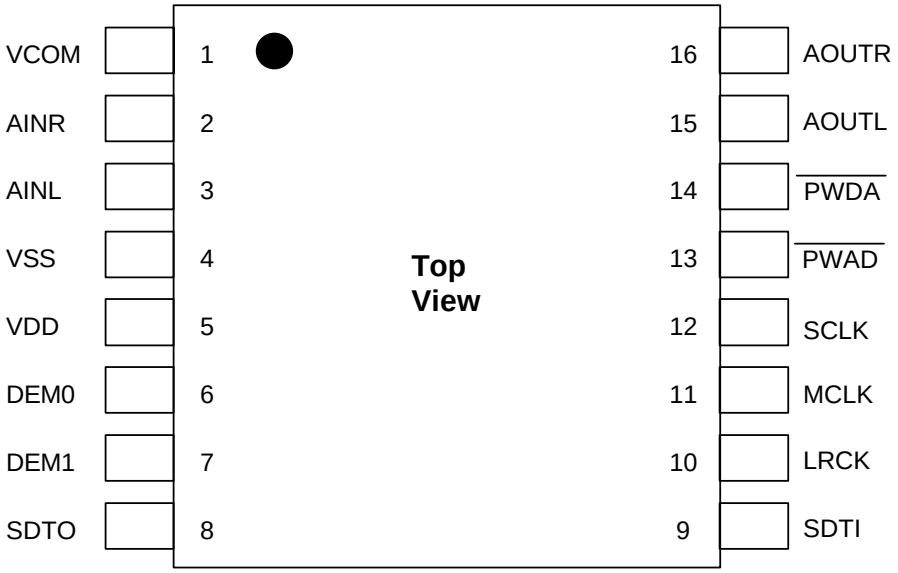
- ☐ **HPF for DC-offset cancel (fc=3.4Hz)**
- ☐ **Single-ended ADC**
  - **S/(N+D): 82dB@VDD=2.5V**
  - **Dynamic Range, S/N: 89dB@VDD=2.5V**
- ☐ **Single-ended DAC**
  - **Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
  - **S/(N+D): 85dB@VDD=2.5V**
  - **Dynamic Range, S/N: 92dB@VDD=2.5V**
- ☐ **Audio I/F format: MSB First, 2's Compliment (AK4518 compatible)**
  - **ADC: 16bit MSB justified**
  - **DAC: 16bit LSB justified**
- ☐ **Input/Output Voltage: 0.6 X VDD (=1.5Vpp@VDD=2.5V)**
- ☐ **High Jitter Tolerance**
- ☐ **Sampling Rate: 8kHz to 50kHz**
- ☐ **Master Clock: 256fs or 384fs or 512fs**
- ☐ **Power Supply: 2.3 to 3.6V**
- ☐ **Low Power Supply Current: 10mA**
- ☐ **Ta = -40 to 85°C**
- ☐ **Very Small Package: 16pin TSSOP**



■ Ordering Guide

AK4550VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4550	Evaluation Board for AK4550	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, 0.45 x VDD
2	AINR	I	Rch Analog Input Pin
3	AINL	I	Lch Analog Input Pin
4	VSS	-	Ground Pin
5	VDD	-	Power Supply Pin
6	DEM0	I	De-emphasis Control Pin
7	DEM1	I	De-emphasis Control Pin
8	SDTO	O	Audio Serial Data Output Pin
9	SDTI	I	Audio Serial Data Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	MCLK	I	Master Clock Input Pin
12	SCLK	I	Audio Serial Data Clock Pin
13	$\overline{\text{PWAD}}$	I	ADC Power-Down & Reset Mode Pin "L": Power down. ADC should always be reset upon power-up.
14	$\overline{\text{PWDA}}$	I	DAC Power-Down & Reset Mode Pin "L": Power down. DAC should always be reset upon power-up.
15	AOUTL	O	Lch Analog Output Pin
16	AOUTR	O	Rch Analog Output Pin

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	4.6	V
Input Current (Any Pin Except Supplies)	IIN	-	±10	mA
Input Voltage	VIN	-0.3	VDD+0.3	V
Ambient Temperature (power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note:1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	2.3	2.5	3.6	V

Note:1. All voltages with respect to ground.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=2.5V; fs=44.1kHz; Signal Frequency=1kHz; SCLK=64fs; Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics: Analog Source Impedance=470Ω (Note 2)					
Resolution				16	Bits
S/(N+D)	(-0.5dB Input)	72	82		dB
D-Range	(-60dB Input, A-weighted)	82	89		dB
S/N	(A-weighted)	82	89		dB
Interchannel Isolation		80	95		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Input Voltage	(Note 3)	1.35	1.50	1.65	Vpp
Input Resistance		50	100		kΩ
Power Supply Rejection	(Note 4)		35		dB
DAC Analog Output Characteristics: (Note 5)					
Resolution				16	Bits
S/(N+D)		75	85		dB
D-Range	(-60dB Output, A-weighted)	86	92		dB
S/N	(A-weighted)	86	92		dB
Interchannel Isolation		80	95		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Output Voltage	(Note 3)	1.35	1.50	1.65	Vpp
Load Resistance		10			kΩ
Load Capacitance				30	pF
Power Supply Rejection	(Note 4)		50		dB
Power Supplies					
Power Supply Current					
AD+DA	$\overline{PWAD}$ = "H", $\overline{PWDA}$ = "H"		10	15	mA
AD	$\overline{PWAD}$ = "H", $\overline{PWDA}$ = "L"		5.6	8.4	mA
DA	$\overline{PWAD}$ = "L", $\overline{PWDA}$ = "H"		5.6	8.4	mA
Power down (Note 6)	$\overline{PWAD}$ = "L", $\overline{PWDA}$ = "L"		10	50	uA
Power Consumption					
AD+DA	$\overline{PWAD}$ = "H", $\overline{PWDA}$ = "H"		25	37.5	mW
AD	$\overline{PWAD}$ = "H", $\overline{PWDA}$ = "L"		14	21	mW
DA	$\overline{PWAD}$ = "L", $\overline{PWDA}$ = "H"		14	21	mW
Power down (Note 6)	$\overline{PWAD}$ = "L", $\overline{PWDA}$ = "L"		25	125	uW

Notes: 2. The offset of ADC is removed by internal HPF.
3. Input /Output of ADC and DAC scales with VDD voltage. 0.6 X VDD(typ).
4. PSR is applied to VDD with 1kHz, 50mV.
5. Measured by AD725C (SHIBASOKU). RMS mode.
6. In case of power-down mode, all digital input including clocks pins (MCLK, SCLK, LRCK) are held VDD or VSS. But $\overline{PWAD}$ and $\overline{PWDA}$ pins are held VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD=2.3 ~ 3.6V; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 7)	±0.1dB	PB	0		17.4	kHz
	-1.0dB			20.0		kHz
	-3.0dB			21.1		kHz
Stopband		SB	27.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 8)		GD		17.0		1/fs
Group Delay Distortion		ΔGD			0	us
ADC Digital Filter (HPF):						
Frequency Response (Note 7)	-3dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz
DAC Digital Filter:						
Passband (Note 7)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 8)		GD		14.8		1/fs
DAC Digital Filter + Analog Filter						
Frequency Response	0 ~ 20.0kHz	FR		±0.5		dB

Notes: 7. The passband and stopband frequencies scale with fs (sampling frequency).
For examples, PB=20.0kHz(@ADC: -1.0dB, DAC: -0.1dB) are 0.454 x fs.

8. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 16bit data of both channels to the output register for ADC. For DAC, this time is from setting the 16bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VDD=2.3 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VDD	V
High-Level Output Voltage (Iout=-20uA)	VOH	VDD-0.1	-	-	V
Low-Level Output Voltage (Iout=20uA)	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	± 10	uA

SWITCHING CHARACTERISTICS

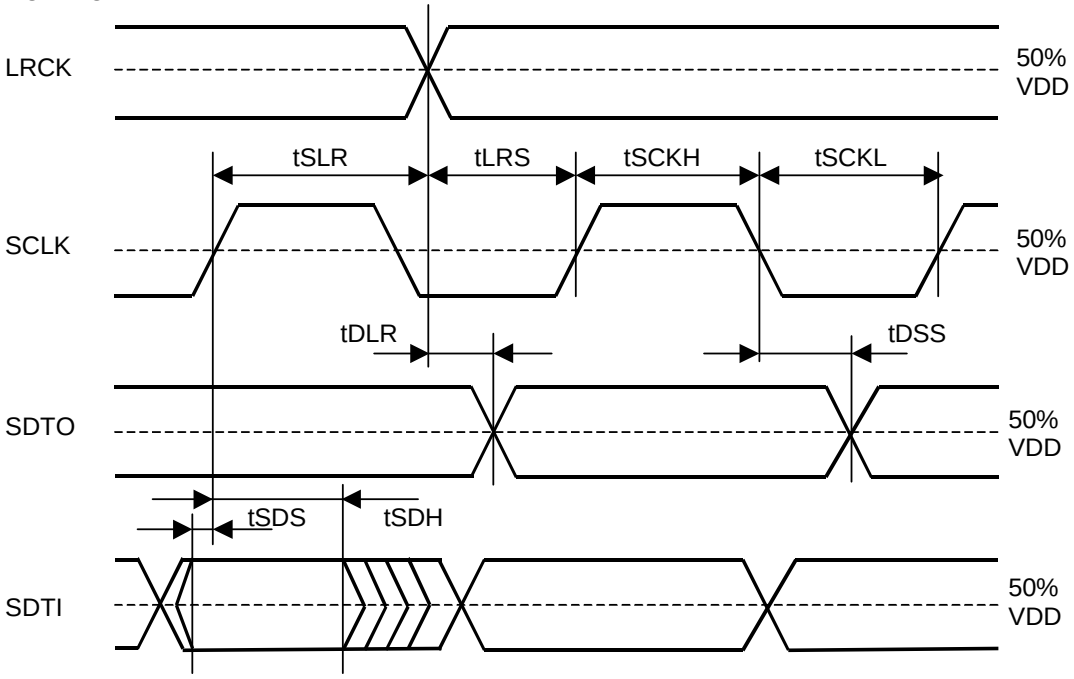
(Ta=25°C; VDD=2.3 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing	256fs:	fCLK	2.048	11.2896	12.8	MHz
	Pulse Width Low	tCLKL	28			ns
	Pulse Width High	tCLKH	28			ns
	384fs:	fCLK	3.072	16.9344	19.2	MHz
	Pulse Width Low	tCLKL	23			ns
	Pulse Width High	tCLKH	23			ns
	512fs:	fCLK	4.096	22.5792	25.6	MHz
	Pulse Width Low	tCLKL	16			ns
	Pulse Width High	tCLKH	16			ns
LRCK Frequency		fs	8	44.1	50	kHz
Duty Cycle			45		55	%
Serial Interface Timing						
SCLK Period		tSCK	312.5			ns
SCLK Pulse Width Low		tSCKL	130			ns
Pulse Width High		tSCKH	130			ns
LRCK Edge to SCLK "↑"	(Note 9)	tLRS	50			ns
SCLK "↑" to LRCK Edge	(Note 9)	tSLR	50			ns
LRCK Edge to SDTO (MSB)		tDLR			80	ns
SCLK "↓" to SDTO		tDSS			80	ns
SDTI Hold Time		tSDH	50			ns
SDTI Setup Time		tSDS	50			ns
Reset Timing						
$\overline{\text{PWAD}}$ or $\overline{\text{PWDA}}$ Pulse Width		tPW	150			ns
$\overline{\text{PWAD}}$ "↑" to SDTO Valid	(Note 10)	tPWV		2081		1/fs

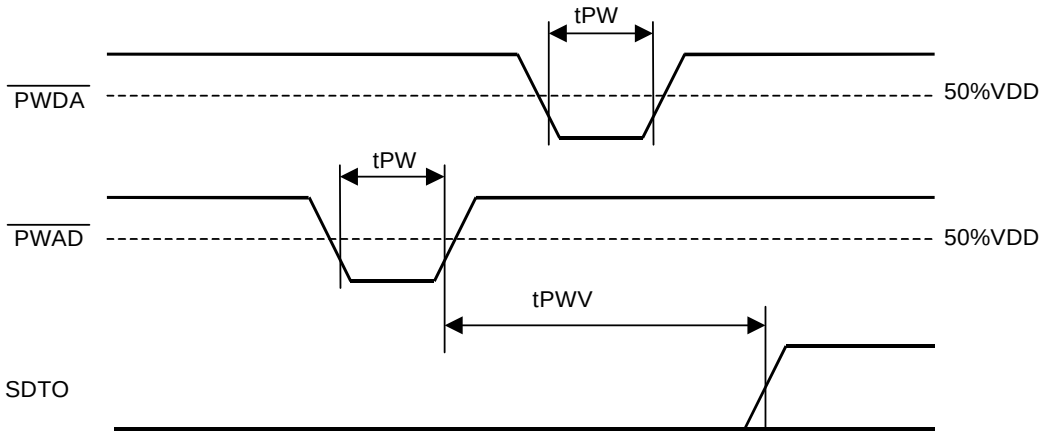
Notes: 9. SCLK rising edge must not occur at the same time as LRCK edge.

10. These cycles are the number of LRCK rising from $\overline{\text{PWAD}}$ rising.

■ **Timing Diagram**



Serial Interface Timing



Reset & Initialize Timing

OPERATION OVERVIEW

■ System Clock Input

The AK4550 can be input MCLK=256fs, 384fs or 512fs. The input clock applied to the MCLK as internal master clock is divided into 256fs automatically. The relationship between the external clock applied to the MCLK input and the desired sample rate is defined in Table 1. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. *fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4550 may occur click noise. In case of DAC, click noise is avoided by setting the inputs to “0”.

All external clocks(MCLK, SCLK, LRCK) must be present unless $\overline{\text{PWAD}}$ and $\overline{\text{PWDA}}$ = ”L”. If these clocks are not provided, the AK4550 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally.

fs	MCLK			SCLK	
	256fs	384fs	512fs	32fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	1.0240MHz	2.048MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	1.4112MHz	2.822MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	1.5360MHz	3.072MHz

Table 1. System Clock Example

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. The data is MSB first, 2’s compliment.

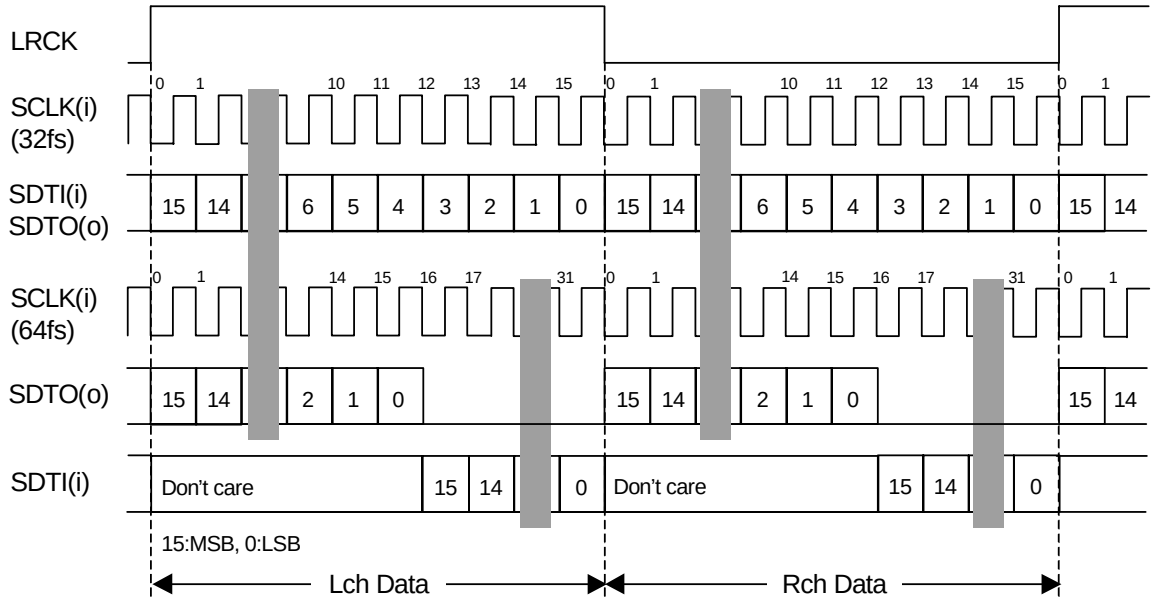


Figure 1. Audio Interface Timing

■ De-emphasis filter

The DAC of AK4550 includes the digital de-emphasis filter (tc=50/15us) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0=”1” and DEM1=”0”.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 2. De-emphasis filter control

■ Digital High Pass Filter

The AK4550 has a Digital High Pass Filter (HPF) for DC-offset cancel. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz and the frequency response at 20Hz is –0.12dB. It also scales with the sampling frequency (fs).

■ Power-down & Reset

The ADC and DAC of AK4550 are placed in the power-down mode by bringing each power down pin, $\overline{\text{PWAD}}$, $\overline{\text{PWDA}}$ = "L" independently and each digital filter is also reset at the same time. These resets should always be done after power-up. In case of the ADC, an anlog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 2081 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 2 shows the power-up sequence when the ADC is powered up before the DAC power-up.

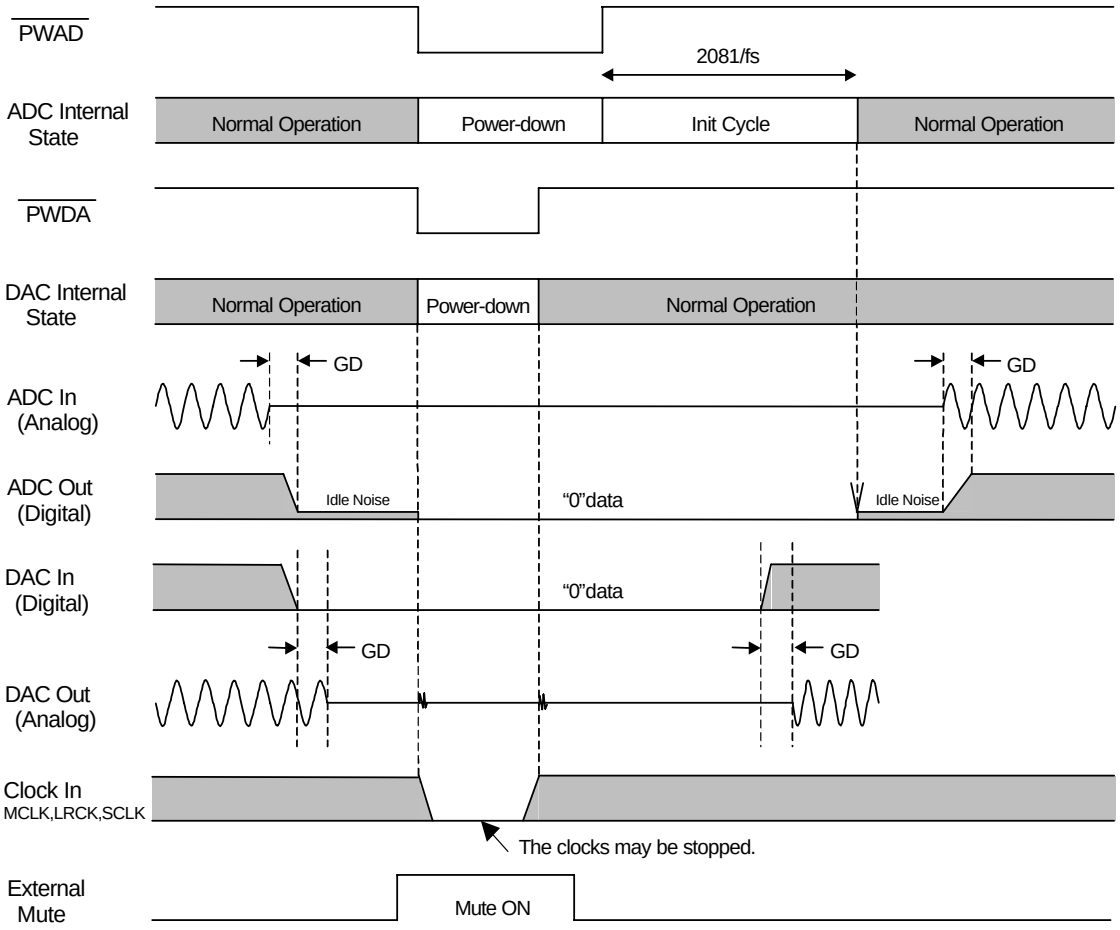


Figure 2. Power-up Sequence

SYSTEM DESIGN

Figure 3 shows the system connection diagram. An evaluation board[AKD4550] is available which demonstrates application circuit, optimum layout, power supply arrangements and measurement results.

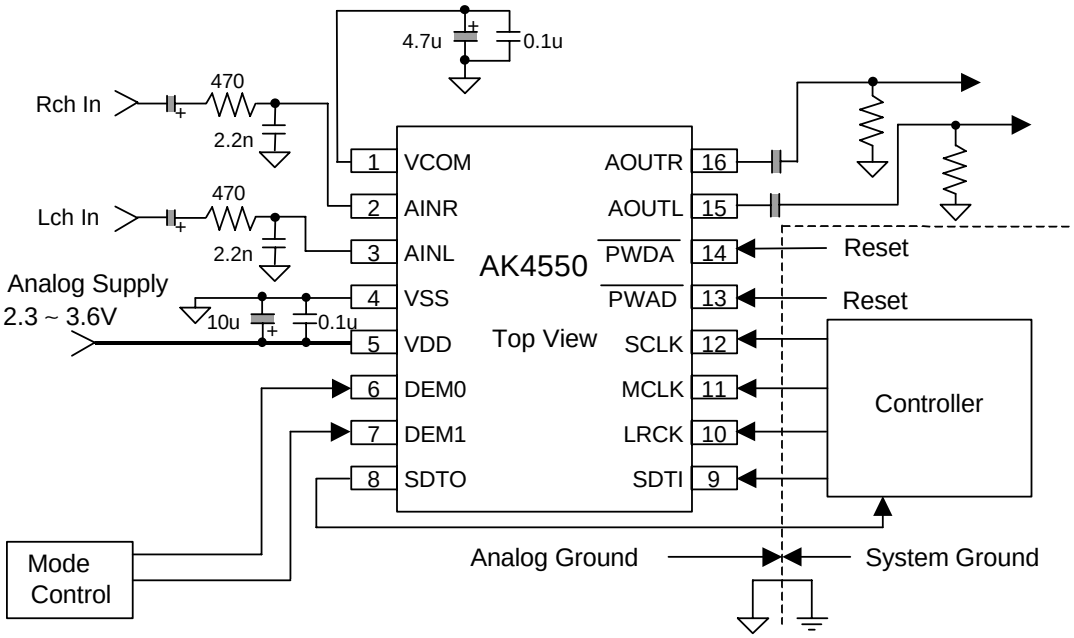


Figure 3. System Connection Diagram Example

Notes:

- LRCK=fs, 32fs ≤ SCLK ≤ 96fs, MCLK=256fs/384fs/512fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- Electrolytic capacitor value of VCOM depends on low frequency noise of supply voltage.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitors should be as near to the AK4550 as possible, with the small value ceramic capacitor being nearest.

2. Voltage Reference

The input to VDD voltage sets the analog input/output range. A 0.1uF ceramic capacitor and a 10uF electrolytic capacitor is connected to VDD and VSS pins, normally. VCOM is a signal ground of this chip. An electrolytic less than 4.7uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from the VDD, VCOM pins in order to avoid unwanted coupling into the AK4550.

3. Analog Inputs

ADC inputs are single-ended and internally biased to VCOM. The input signal range scales with the supply voltage and nominally 0.6xVDD Vpp(typ). The ADC output data format 2's compliment. The output code is 7FFFH(@16bit) for input above a positive full scale and 8000H(@16bit) for input below a negative full scale. The ideal code is 0000H(@16bit) with no input signal.

The AK4550 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter (fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6xVDD Vpp(typ). The DAC input data format is 2's compliment. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

■ Layout Pattern Example

AK4550 requires careful attention to power supply and grounding arrangements to optimize performance.
(Please refer to AKD4550 Evaluation Board layout pattern.)

1. VDD pin should be supplied from analog power supply on system, and VSS pin should be connected to analog ground on system. The AK4550 is placed on the analog ground plane, and near the analog ground and digital ground split. And analog and digital ground planes should be only connected at one point. The connection point should be near to the AK4550.

2. VDD pin should be distributed from the point with low impedance of regulator etc.

3. The series resistors are prevent on the clock lines to reduce overshoot and undershoot. To avoid digital noise coupling to analog circuit in the AK4550, a 10pF ceramic capacitor on MCLK pin is connected with digital ground.

4. 0.1uF ceramic capacitors of VDD-VSS pins and VCOM-VSS pins should be located as close to the AK4550 as possible. And these lines should be the shortest connection to pins.

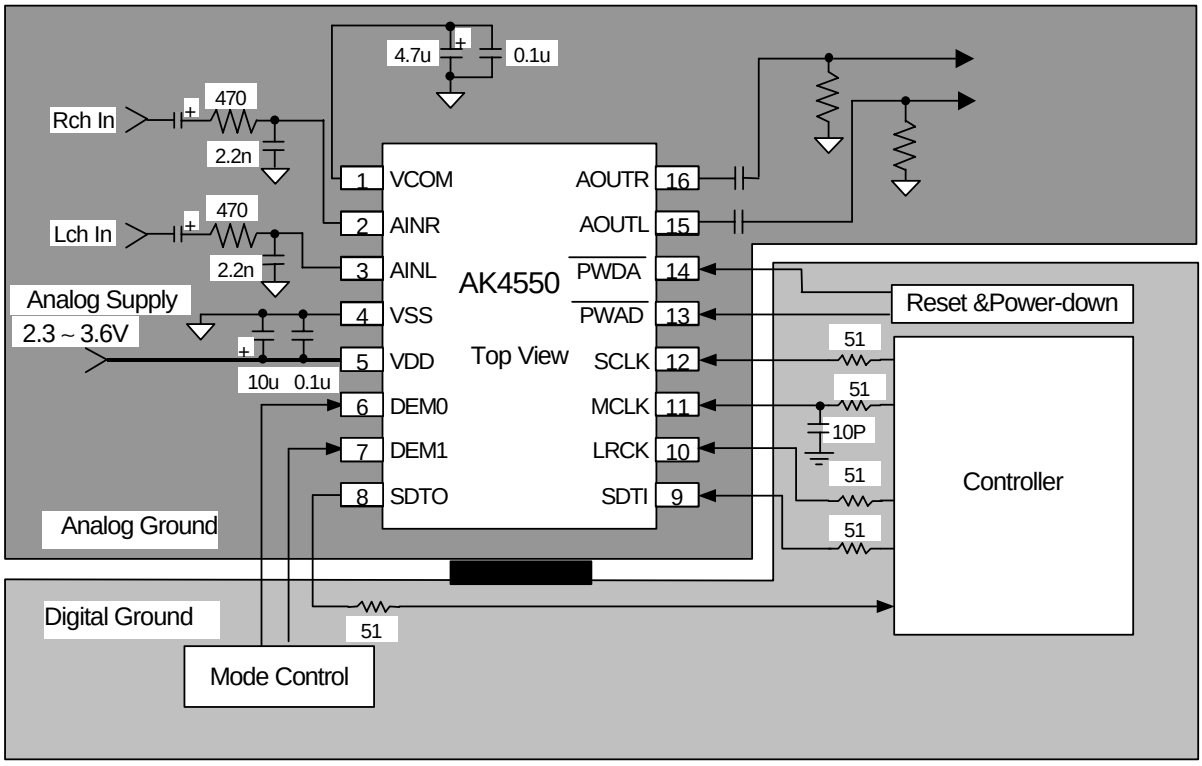
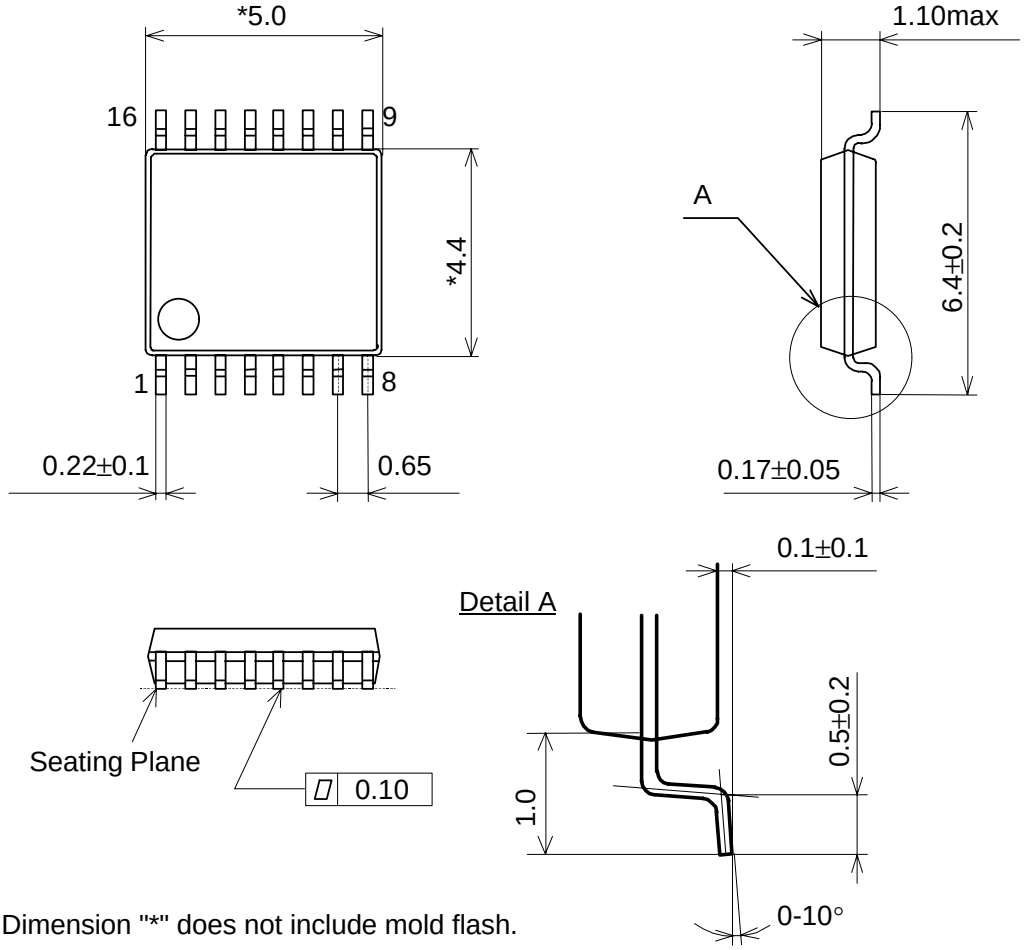


Figure 4. Layout Pattern Example

PACKAGE

16pin TSSOP (Unit: mm)

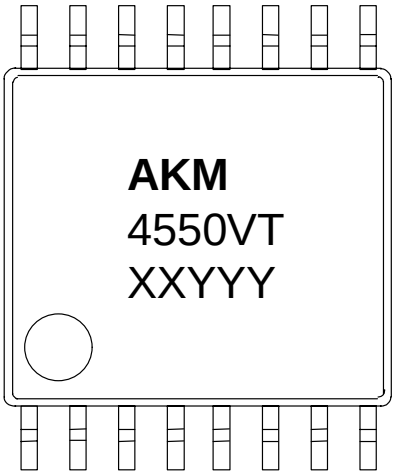


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: lot#
   YYY: Date Code
3) Marketing Code : 4550VT
4) Asahi Kasei Logo