AK4532

Internet/Network/General Purpose Multimedia Audio CODEC

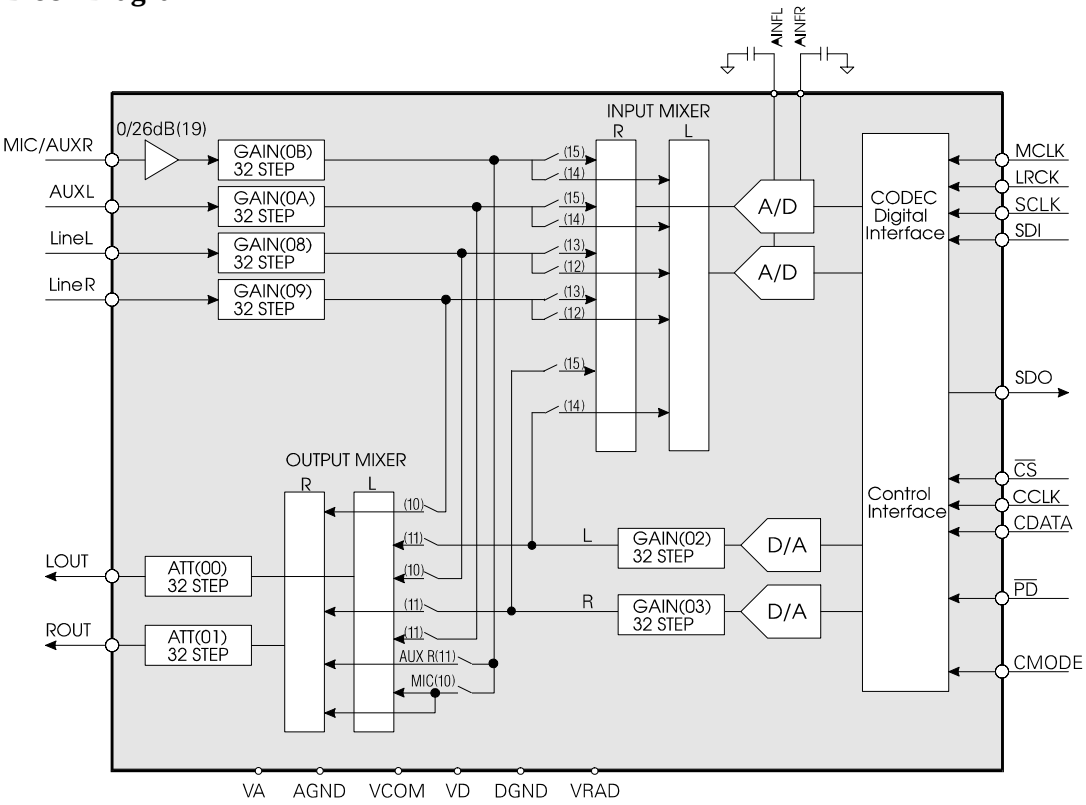
General Description

The AK4532 is a low-cost high-quality 16-Bit CODEC designed specifically for Internet Boxes, Network PCs, and to interface with audio/video controller ICs for standard PC applications. AKM's AK4532 serial interface mode simplifies the design process on existing and new audio projects. The converters can have a range of 4 to 50 kHz. For voice mail applications, an internal 26 dB microphone preamp has been added and because of the internal input mixer, music or other sounds can easily be mixed with voice.

Features

- 2ch Audio CODEC
- 2ch stereo including 1ch mono recording mixer with L/R, R/L, L/L and R/R switching
- 2ch stereo playback mixer
- Mic input with 26 dB optional gain
- High Jitter Tolerance
- Interface compatible with AKM's AK4531
- Sampling Rate: 4 kHz to 50 kHz
- 3-wire Serial Interface for Mixer Control
- 5 V operation, can connect to 3.3 V Digital Controller.
- Low power consumption - 150 mW
- Power down mode
- Small low profile package - 24 pin VSOP.

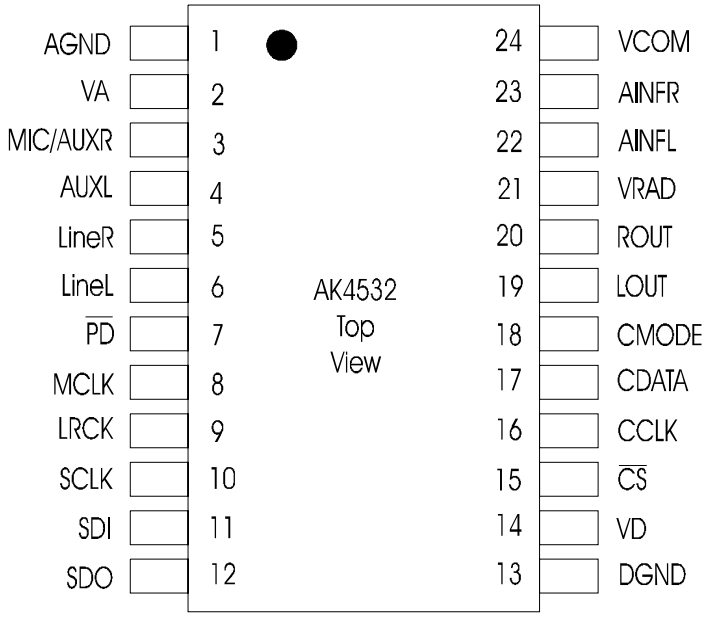
Block Diagram



Ordering Guide

AK4532	from -10°C to +70°C	24pin VSOP(0.65mm pitch)
AKD4532	Evaluation Board	

Pin Layout



Pin and Function

Pin	Pin Name	I/O	Function
1	AGND	-	Analog Ground
2	VA	-	Analog Power - 5V
3	MIC/AUXR	I	Mic or Right Aux Line Level Input
4	AUXL	I	Left Aux Line Level Input
5	LINER	I	Right Line Level Input
6	LINEL	I	Left Line Level Input
7	$\overline{PD}$	I	Power down and Reset
8	MCLK	I	Master Clock for CODEC
9	LRCK	I	Left Right Clock for CODEC
10	SCLK	I	Serial Clock for CODEC
11	SDI	I	Serial Data In
12	SDO	O	Serial Data Out
13	DGND	-	Digital Ground
14	VD	-	Digital Power - 5V
15	$\overline{CS}$	I	Chip Select
16	CCLK	I	Control Port Clock
17	CDATA	I	Control Port Data
18	CMODE	I	MCLK select (L:256fs, H:384fs)
19	LOUT	O	Left Analog Out
20	ROUT	O	Right Analog Out
21	VRAD	I	A/D Reference Connect to AGND with 0.1uF and 4.7uF capacitors
22	AINFL	-	L channel Antialias Filter Pin Connect to AGND with 1.0nF capacitor
23	AINFR	-	R channel Antialias Filter Pin Connect to AGND with 1.0nF capacitor
24	VCOM	-	Voltage Common Output Pin Connect to AGND with 0.1uF and 4.7uF capacitors.

Note: 1. No load current may be taken from the VCOM, VRAD pins for the external circuits.
2. All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

AGND, DGND = 0 V

Parameter		Symbol	min	max	Units
Power Supplies:	Analog Digital	VA VD	-0.3 -0.3	6.0 6.0 or VA+0.3	V V
Input Current, Any Pin except Supplies		IIN	-	+/- 10	mA
Analog Input Voltage Range		VINA	-0.3	6.0 or VA+0.3	V
Digital Input Voltage		VIND	-0.3	6.0 or VA+0.3	V
Ambient Temperature		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.
2. Max value is higher voltage of 6.0 or VA+0.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal Operating Specifications are not guarantee at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, Note 1)

Parameter		Symbol	min	typ	max	units
Power Supplies	Analog Digital	VA VD	4.5 4.5	5.0 5.0	5.5 VA	V V

Note 1: All voltages with respect to ground.

ANALOG CHARACTERISTICS

(Ta=25 °C; VA, VD = 5.0V; fs = 44.1kHz; Signal Frequency = 1 kHz; MCLK=256fs; BCLK = 64 fs; LRCK = fs, Gain, ATT and Mixer switches are defualt setting. Measurement frequency bandwidth is 10Hz to 20kHz, unless otherwise noted.)

Parameter		min	typ	max	units
A/D	measured via LineL and LineR				
Resolution				16	Bits
S/(N+D)	-0.5 dB Input	74	80		dB
S/N	A-weighted	84	90		dB
Dynamic Range	-60 dB Input, A-weighted	84	90		dB
Interchannel Isolation	(Note 1)	68	76		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			100		ppm/°C
Offset Error	(Note 2)		+/- 1		LSB
Input Voltage	(Note 4)	2.50	2.70	2.90	Vpp
Mixer Input Resistance		30	60	100	kΩ
D/A	measured via LOUT and ROUT				
Resolution				16	Bits
S/(N+D)		75	83		dB
S/N	A-weighted	83	87		dB
Dynamic Range	-60 dB Input, A-weighted	83	87		dB
Interchannel Isolation	(Note 1)	80	100		dB
Interchannel Gain Mismatch			0.2	0.7	dB
Gain Drift			100		ppm/°C
Output Voltage	(Note 4)	2.85	3.05	3.35	Vpp
Load Resistance		10			kΩ
Out-of-Band Noise	BW < 100 kHz		-81		dB
MIC Amp					
Gain		24	26	28	dB
Input Resistance	For 26dB setting	15	25	40	kΩ
Mixer Gain Control	32 Steps				
Step Size	(Note 3)	0	2		dB
Gain Control Range		-50		12	dB
Master Volume	32 Steps				
Step Size	(Note 3)	0	2		dB
Attenuation Control Range		-62		0	dB
Power Supplies					
Normal Operation	VA		27	40	mA
	VD		3	5	mA
	Power Dissipation		150	225	mW
Power-Down Mode	VA		10		uA
	VD		10		uA
	Power Dissipation		100	200	uW

Note: 1. Crosstalk between channels on the same A/D or D/A.
2. Internal HPF removes offset
3. Minimum spec applies to ≥ -40dB setting.
4. Input and Output voltage scale with VA.

FILTER CHARACTERISTICS

(Ta=25 °C; VA, VD = 5.0V ± 10%; fs = 44.1 kHz)

Parameter		Symbol	min	typ	max	Units
A/D Digital Filter (Decimation LPF)						
Passband (Note 1)	+/- 0.1 dB -0.5 dB -1.2 dB -6.7 dB	PB	0 0 0 0		16.5 19.0 20.0 22.05	kHz kHz kHz kHz
Stopband		SB	26.0			kHz
Passband Ripple		PR			+/- 0.1	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		Delta GD			0	uS
Group Delay (Note 2)		GD		16.1		1/fs
A/D Digital Filter (HPF)						
Frequency Response (Note 1)	-3 dB -0.5 dB -0.1 dB	FR		6.85 19.6 44.9		Hz Hz Hz
D/A Digital Filter						
Passband (Note 1)	+/- 0.1 dB -6.0 dB	PB	0 0		18.0 22.05	kHz kHz
Stopband		SB	26.1			kHz
Passband Ripple		PR			+/- 0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 2)		GD		14.4		1/fs
D/A Digital Filter + Analog Filter						
Frequency Response	0 to 20 kHz	FR		+/- 1.0		dB

Note: 1. The passband and stopband frequencies scale with fs.

2. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 16bit data of both channels to the output register of ADC. For DAC, this time is from setting 16bit data of both channels on input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25 °C; VA, VD = 5.0V±10%)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-80uA)	VOH	VD-0.4	-	-	V
Low-Level Output Voltage (Iout=80uA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	+/-10	uA

SWITCHING CHARACTERISTICS

(Ta=25 °C; VA, VD = 5.0V ± 10%, CL = 20pF)

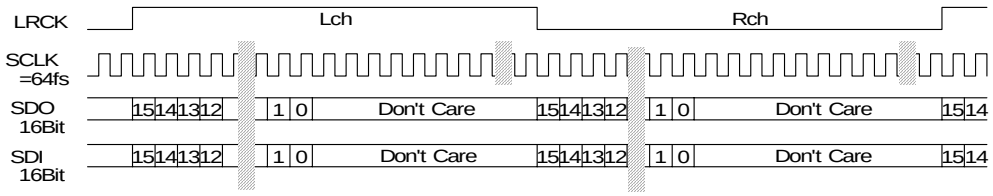
Parameter	Symbol	min	typ	max	Units
Master Clock Timing (CMODE=L)	fCLK	1.024	11.2896	12.800	MHz
(CMODE=H)	fCLK	1.536	16.9344	19.2	MHz
Pulse Width Low (CMODE=L)	fCLKL	31.25			ns
(CMODE=H)	fCLKL	23			ns
Pulse Width High (CMODE=L)	fCLKH	31.25			ns
(CMODE=H)	fCLKH	23			ns
LRCK Frequency (Note 1)	fs	4	44.1	50	kHz
Duty Cycle		45		55	%
Serial Interface Timing					
SCLK Period	tSCK	312.5			ns
SCLK Pulse Width Low	tSCKL	100			ns
SCLK Pulse Width High	tSCKH	100			ns
LRCK Edge to SCLK “rising edge” (Note 2)	tLRS	50			ns
SCLK “rising edge” to LRCK edge (Note 2)	tSLR	50			ns
SDI Hold Time	tSDH	50			ns
SDI Setup Time	tSDS	50			ns
LRCK to SDO(MSB)	tLRS			70	ns
SCLK “rising edge” to SDO	tSSD			70	ns
Control Interface Timing					
CCLK Period	tCCK	200 (Note 4)			ns
CCLK Pulse Width Low	tCCKL	80			ns
CCLK Pulse Width High	tCCKH	80			ns
CDATA Hold Time	tCDS	50			ns
CDATA Setup Time	tCDH	50			ns
$\overline{CS}$ High Level Time	tCSW	150 (Note 4)			ns
$\overline{CS}$ “falling edge” to CCLK “rising” time	tCSS	50 (Note 4)			ns
CCLK “rising time” to $\overline{CS}$ “rising” time	tCSH	50			ns
Reset Timing					
$\overline{PD}$ Pulse Width	tPD	150			ns
$\overline{PD}$ “rising edge” to SDO delay (Note 3)	tPDS		516		1/fs

Note: 1. If the duty of LRCK changes larger than 5% from 50%, the AK4532 is reset by the internal phase detecting circuit automatically.

2. SCLK rising edge must not occur at the same time as LRCK edge.
3. These cycles are the number of LRCK rising from $\overline{PD}$ rising.
4. fs ≥ 19.6kHz.
   In the case of fs <19.6kHz, these three parameters must meet a relationship of (tCSW + tCSS + 7 × tCCK) > 1/(32 × fs) in addition to these specifications.
   For example, when tCCK=200ns and tCSS=50ns at fs=8kHz, tCSW(min) is 2457ns.
   When tCSW=150ns and tCSS=50ns fs=8kHz, tCCK(min) is 530ns.

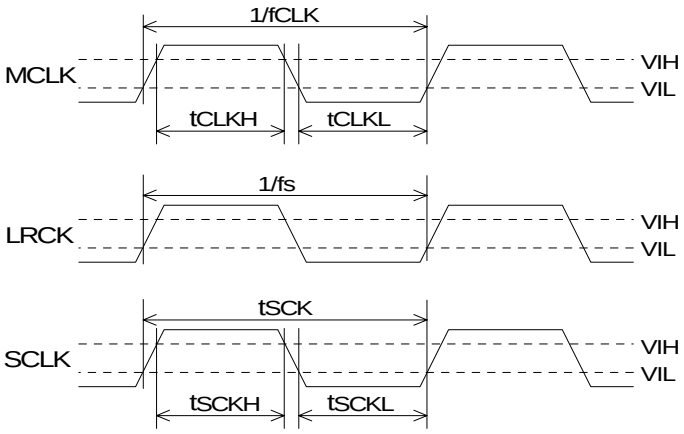
Audio Data Formats

The data format of ADC and DAC are MSB first & MSB justified with 16bit. The SCLK needs 32fs or more than 32fs in a LRCK cycle.

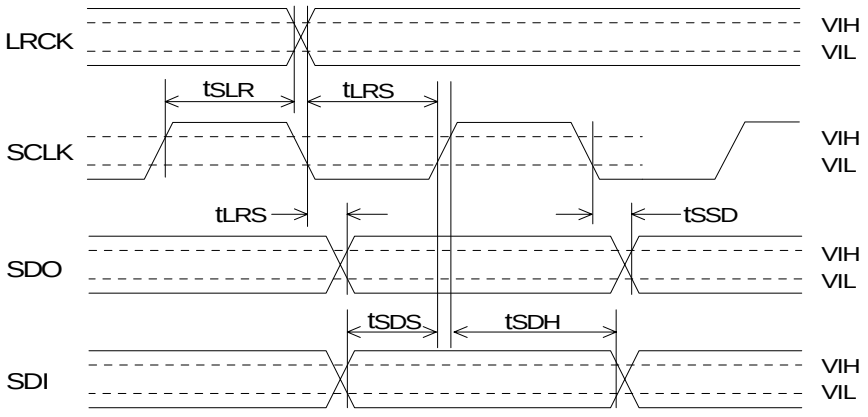


SDO,SDI - 15:MSB,0:LSB

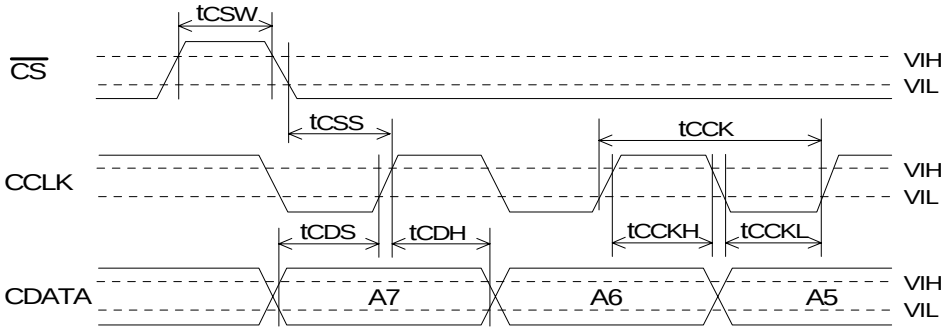
Timing Diagram



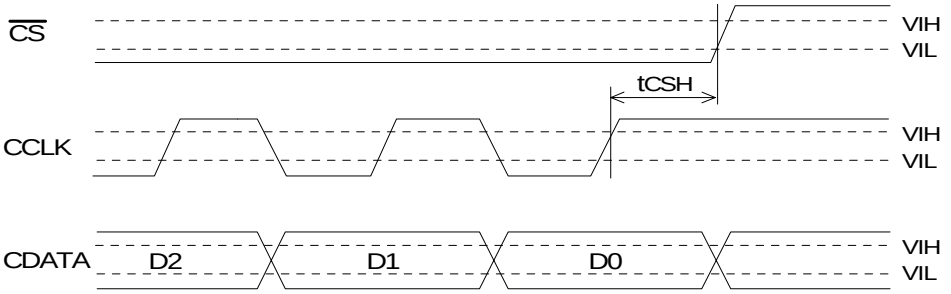
Clock Timing



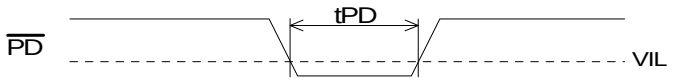
Serial Audio Interface Timing



Control Data Interface Timing 1



Control Data Interface Timing2



Power down and Reset Timing

OPERATION OVERVIW

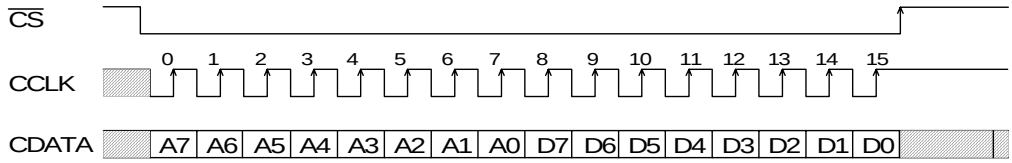
1. CONTROL REGISTER MAP

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00	Master Volume Lch	MUTE			ATT4	ATT3	ATT2	ATT1	ATT0
01	Master Volume Rch	MUTE			ATT4	ATT3	ATT2	ATT1	ATT0
02	Voice Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
03	Voice Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
08	Line Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
09	Line Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
0A	AUX Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
0B	AUX Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
10	Output Mixer SW 1				LineL	LineR			MIC
11	Output Mixer SW 2			AUXL	AUXR	VoiceL	VoiceR		
12	Lch Input Mixer SW 1				LineL	LineR			
13	Rch Input Mixer SW 1				LineL	LineR			
14	Lch Input Mixer SW 2				AUXL	AUXR	VoiceL		
15	Rch Input Mixer SW 2				AUXL	AUXR	VoiceR		
16	Reset and Power Down							$\overline{PD}$	$\overline{RST}$
19	MIC Amp Gain								MGAIN

Note: ATT* is data bits for the attenuation level.
GAI* is data bits for the gain level.

IMPORTANT: There is the compatibility between the AK4531 and AK4532. But the input mixer functions of those device has some different implication in the application, receptively.
And the other address of control register except those described in the above table and "1A" are "do not care". Address "1A" for testing shall be strictly prohibited to access.
Be ware that the three MSB address bits(A7, A6, A5) are ignored by AK4532. Writing to address "20" register will update the address "00" register for instance.

2. WRITE Timing of Control Register



A7-A0: Address
D7-D0: Control Data

3. Control Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00	Master Volume Lch	MUTE			ATT4	ATT3	ATT2	ATT1	ATT0
01	Master Volume Rch	MUTE			ATT4	ATT3	ATT2	ATT1	ATT0

MUTE 1: MUTE
0: No MUTE
ATT4:0 32 levels with 2 dB step
00000: 0dB
11111: -62 dB
Initial "0000 0000"(No MUTE & 0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02	Voice Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
03	Voice Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
08	Line Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
09	Line Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
0A	AUX Volume Lch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0
0B	AUX Volume Rch	MUTE			GAI4	GAI3	GAI2	GAI1	GAI0

MUTE 1: MUTE
0: No MUTE
ATT4:0 32 levels with 2 dB step
00000: 12dB
00110: 0 dB
11111: -50 dB
Initial "0000 0110"(No MUTE & 0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10	Output Mixer SW 1				LineL	LineR			MIC
11	Output Mixer SW 2			AUXL	AUXR	VoiceL	VoiceR		
12	Lch Input Mixer SW 1				LineL	LineR			
13	Rch Input Mixer SW 1				LineL	LineR			
14	Lch Input Mixer SW 2				AUXL	AUXR	VoiceL		
15	Rch Input Mixer SW 2				AUXL	AUXR	VoiceR		

ON/OFF of Mixer Switches
0: OFF
1: ON
Initial "000X XX00"
XXX=000: Addr=10,14,15 (All:OFF)
XXX=011: Addr=11(Output Mixer Voice R&L:ON)
XXX=100: Addr=12(Lch Input Mixer Line L :ON)
XXX=010: Addr=13(Rch Input Mixer Line R :ON)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16	Reset and Power Down							$\overline{PD}$	$\overline{RST}$
19	MIC Amp Gain								MGAIN

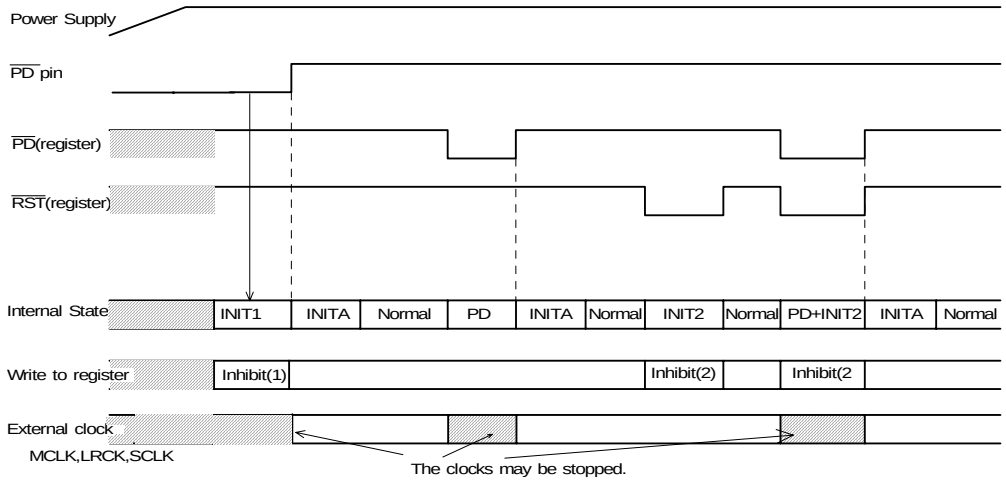
$\overline{RST}$ initializes the contents of all registers except $\overline{PD}$ and $\overline{RST}$ registers. When $\overline{PD}$ pin goes low, $\overline{RST}$ register becomes
"1".
1: Normal Operation
0: Initialize

$\overline{PD}$ register enables the power down. When $\overline{PD}$ pin goes low, $\overline{PD}$ register becomes "1".
1: Normal Operation
0: Power Down

MGAIN selects the gain of MIC amp. The initial state is "0".
0: Bypass (0dB)
1: 26 dB
Try to avoid pops and clicks when activating or inactivating this function.

4. Explanation of each sequence

4.1. Reset & Power down



- INIT1: Initializing all registers. The AK4532 exists in the power down state.
- INIT2: Initializing all registers except $\overline{PD}$, $\overline{RST}$ registers.
- INITA: Initializing the analog section. Initializing period is 516/fs.
- PD: Power down state. All analog outputs are floating.
  In case of $\overline{RST}$ register = "0", initializing all registers except $\overline{PD}$, $\overline{RST}$ registers.
- Inhibit(1): Inhibits writing to all registers.
- Inhibit(2): Inhibits writing to all registers except for $\overline{PD}$, $\overline{RST}$ registers.
- The AK4532 operates with the external clocks(MCLK, LRCK, SCLK) during initializing the analog section.

Figure 1. Reset & Power Down Sequence

4.2. $\overline{PD}$ pin operation

"H": Normal operation

"L": Initializing mode 1(INIT1 in Figure 1)

- Initializing all registers.
- Inhibits writing to all registers.
- The initialization of the analog section starts at rising edge of $\overline{PD}$ pin.
- SDO pin stays "L" during the initializing periods of 516/fs.
- Going into power down state.

4.3. $\overline{RST}$ register operation

"1": Normal operation

"0": Initializing mode 2(INIT2 in Figure 1)

- Initializing all registers except $\overline{PD}$, $\overline{RST}$ registers.
- Inhibits writing to all registers except $\overline{PD}$, $\overline{RST}$ registers.
- $\overline{RST}$ register goes "1" when $\overline{PD}$ pin goes "L".
- The analog section is not initialized.

4.4. $\overline{PD}$ register operation

"1": Normal operation

"0": Power down

- The contents of all registers are held.
- $\overline{PD}$ resister goes "1" when $\overline{PD}$ pin goes "L".
- All analog outputs(LOUT, ROUT) go floating.
- The initialization of the analog section starts at the rising edge of $\overline{PD}$ resister.
- SDO pin stays "L" during the initializing period of 516/fs.

4.5. SDO output pin operation

SDO output is the 16bit data of ADC and goes “L”(0000H) in the following cases.

- $\overline{PD}$ pin = “L”
- During initializing the analog section(516/fs).
- $\overline{RST}$ register = “0”
- $\overline{PD}$ register = “0”

4.6. Analog output pin(LOUT, ROUT) operation

These outputs are floating in the following case.

- $\overline{PD}$ pin = “L”
- $\overline{PD}$ register = “0”

5. System Clock

The external clocks which are required to operate the AK4532 are MCLK, LRCK and SCLK. MCLK should be synchronized with LRCK but the phase is free of care. As the AK4532 includes the phase detect circuit for LRCK, the AK4532 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not required except only upon power-up.

All external clocks should always be present whenever the AK4532 is in normal operation mode. If these clocks are not provided, the AK4532 may draw excessive current and do not possibly operate properly because the device utilizes the dynamic logic internally. If the external clocks are not present, the AK4532 should be in the power down mode.

5. Digital High Pass Filter

The ADC of the AK4532 has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 6.85Hz at fs=44.1kHz and the frequency response at 20Hz is -0.5dB. It also scales with sampling rate(fs).

System Design

Figure 2 shows the system connection diagram. An evaluation board is available which demonstrates the optimum layout, power supply arrangements and measurement results.

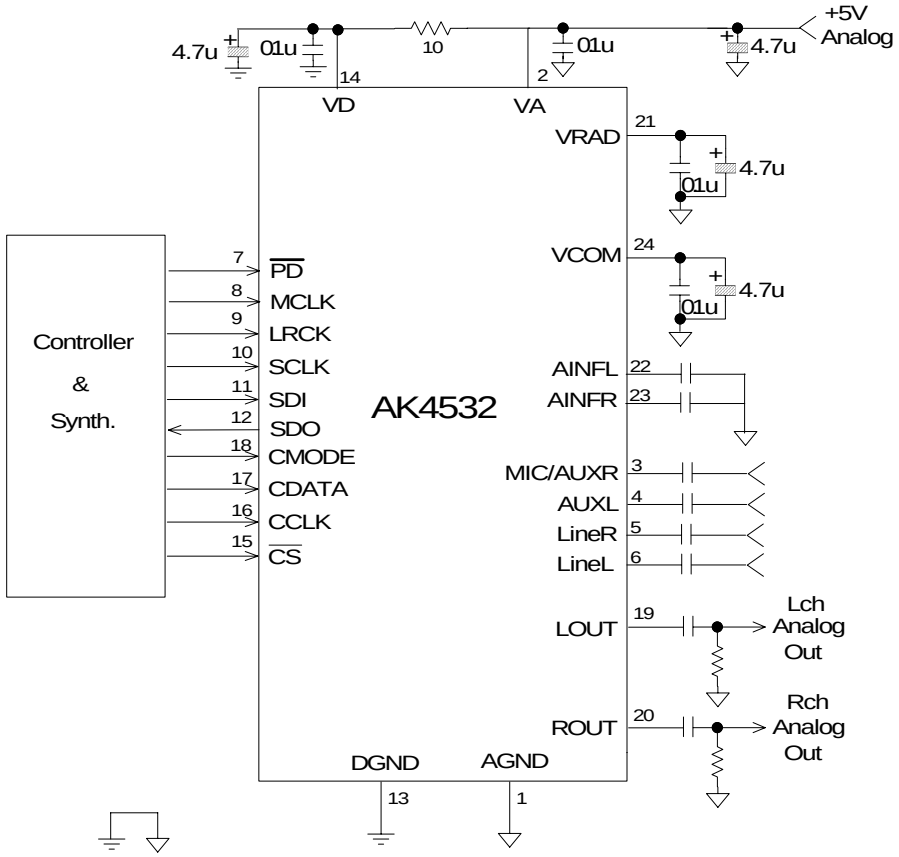


Figure 2. Typical Connection Diagram

1. Grounding and power supply decoupling

The AK4532 requires careful attention to power supply and grounding arrangements. VD should be supplied from analog power supply. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4532 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference

The on-chip voltage references are output on the VRAD and VCOM pins for decouping .

The VRAD is used as the reference of A/D conversion. The VCOM is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. Especially, the small value ceramic capacitors should be as near to the AK4532 as possible. No load current may be drawn from the VRAD and

VCOM pins. All signals, especially clocks, should be kept away from the VRAD and VCOM pins in order to avoid unwanted coupling into the chip.

3. Analog Inputs

The mixer input and the ADC inputs are single-ended and internally biased to the VCOM voltage with 60kΩ (typ) resistance. The input signal range is typically 2.83Vpp(1Vrms). Figure 3 is an example for 2Vrms line-level input circuit. The ADC output data format is 2's complement. The AK4532 accepts input voltages from AGND to VA. The output code is 7FFFH for input above a positive full scale and 8000H for input below a negative full scale. The ideal code is 0000H with no input signal. The DC offset is canceled by the internal HPF.

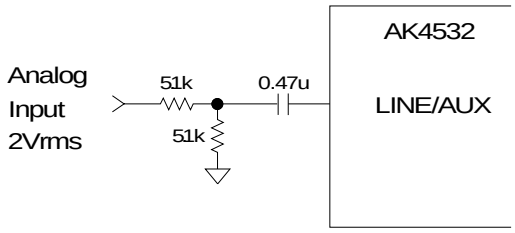


Figure 3. 2Vrms Line-level Input

The AK4532 samples the analog inputs at 64fs. The digital filter rejects all noise higher than the stop band. However, the filter will not reject frequencies right around 64fs(and multiples of 64fs). Most audio signals do not have significant energy at 64fs. As a result, two 1nF capacitors are necessary for AINFR and AINFL.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.83Vpp(1Vrms). The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFH and a negative full scale for 8000H. The ideal output is VCOM voltage for 0000H. The internal switched-capacitor filter and continuous-time filter almost remove the noise generated by the delta-sigma modulator of DAC beyond the audio passband, especially low sampling rate. The noise floor level is almost constant and the audible noise level is -83dB(typ) at 8kHz sampling.

5. Other information

5.1 Clock change

The clock change or LRCK phase shift should be done while muting the DAC output by the master volume or voice volume to avoid the click noise by out-of-synchronization.

ADC may output digital code at the clock change, or LRCK phase shift may produce incomplete or destroyed 16bit data. Then some attention is required carefully.

5.2 Offset on mixer inputs

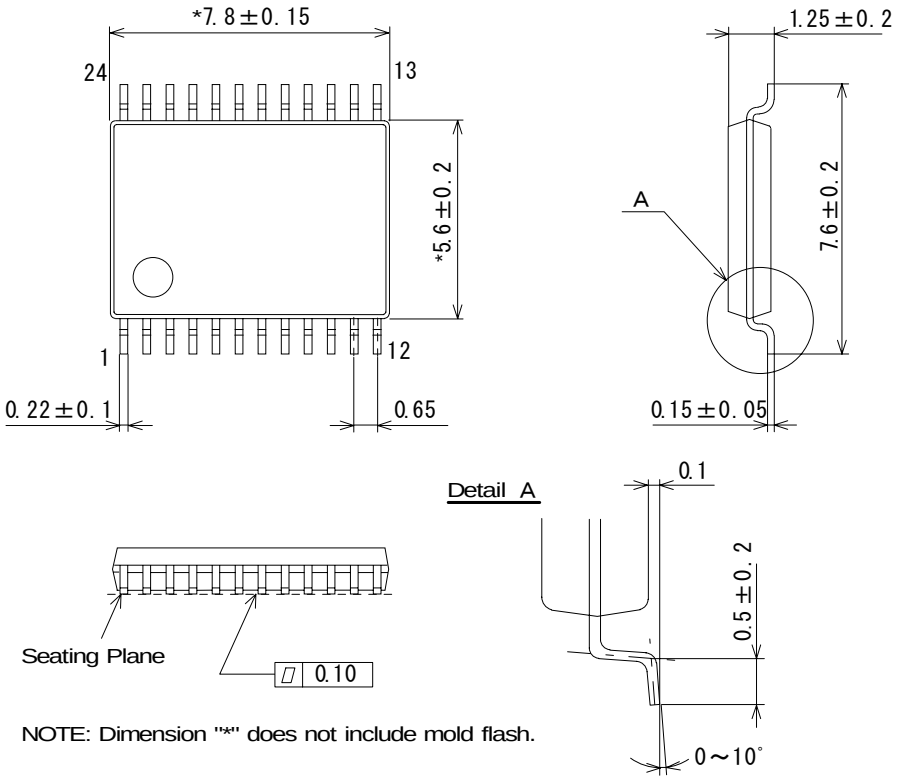
When the mixer gain is set to +12dB, the output has pretty large offset even if the inputs are no signal. Therefore, large click noise may occur when the gain level is changed quickly.

5.3 Click noise on the analog outputs

The click noise of about -50dB occurs from the analog outputs(LOUT, ROUT) at the power on/off or the transition of $\overline{PD}$ register. The analog outputs should be muted externally if the click noise influences systems application.

Package

● 24pin VSOP (Unit: mm)

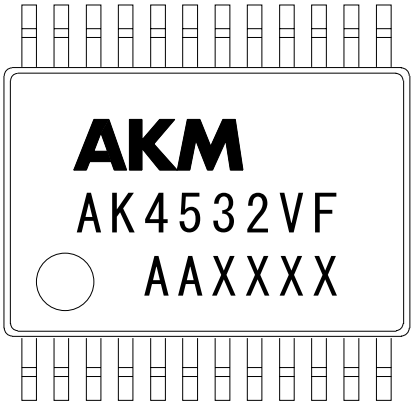


NOTE: Dimension "*" does not include mold flash.

■Package & Lead frame materiel

Package molding compound : Epoxy
Lead frame material :Cu
Lead frame surface treatment : Solder plate

Marking



1) Pin #1 indication
2) AA: LOT#
3) Date Code: XXXX(4 digits)
4) Marketing Code: AK4532-VF
5) Country of Origin
6) Asahi Kasei Logo

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